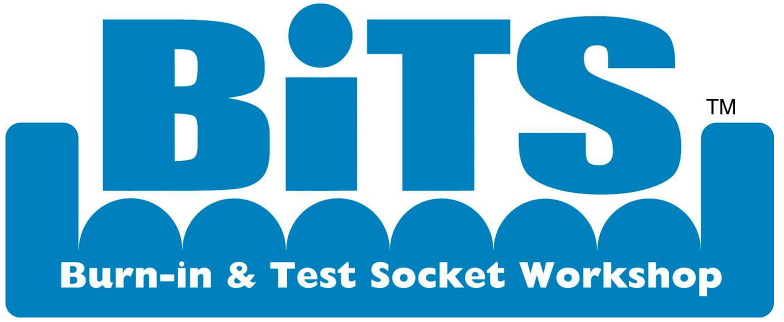

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Session 3

Electrical Analysis And Characterization

"Development Of Computational Model And Measurement Of Maximum Current Capability For Microprocessor Sockets"
David W. Song, Ashish Gupta, Chia-Pin Chiu — Intel Corporation

"Lumped And Distributed Equivalent Circuits For Test Sockets"
Gert Hohenwarter — GateWave Northern, Inc.

"Contactor Characterization Of RF Test/Burn In"
Ling Li Ong, Tim Swettlen — Intel Corporation

"Differential Impedance Characterization Of Test Sockets"
Eric Bogatin, Kevin DeFord, Meena Nagappan — Synergetix

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2006 Burn-In & Test Sockets Workshop
Development of Computational Model and Measurement of Maximum Current Capability for Microprocessor Sockets
David Song Ashish Gupta Chia-Pin Chiu
ATD Design Process Development
Intel Corporation, Chandler, AZ
Collaborators:
Suzana Prstic Yongmei Liu
Todd Young Seth Reynolds
Tom Paddock
intel
1

Agenda
Motivation
Introduction to Socket Thermal Analysis
Review of Previous Status
Improved Numerical Model for Contact Temperature Prediction
Improved Experimental Model Validation
Key Summary
Glossary
Sample LGA Socket
2

Motivation

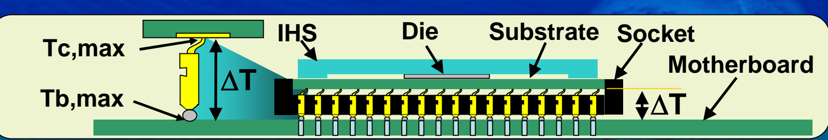
- Increasing need to quantify current per pin.
  → Higher local joule heating.
  → Higher socket contact temperature.
  → Accelerated increase in electrical contact resistance through product life.
- **Need to <u>more accurately evaluate</u> socket contact temperature at use-condition.**
  – Large uncertainty → Low confidence
  – Small uncertainty → High confidence → More margin
- **Intel is constantly driving <u>methodology improvements</u> for determining socket temperature.**

3

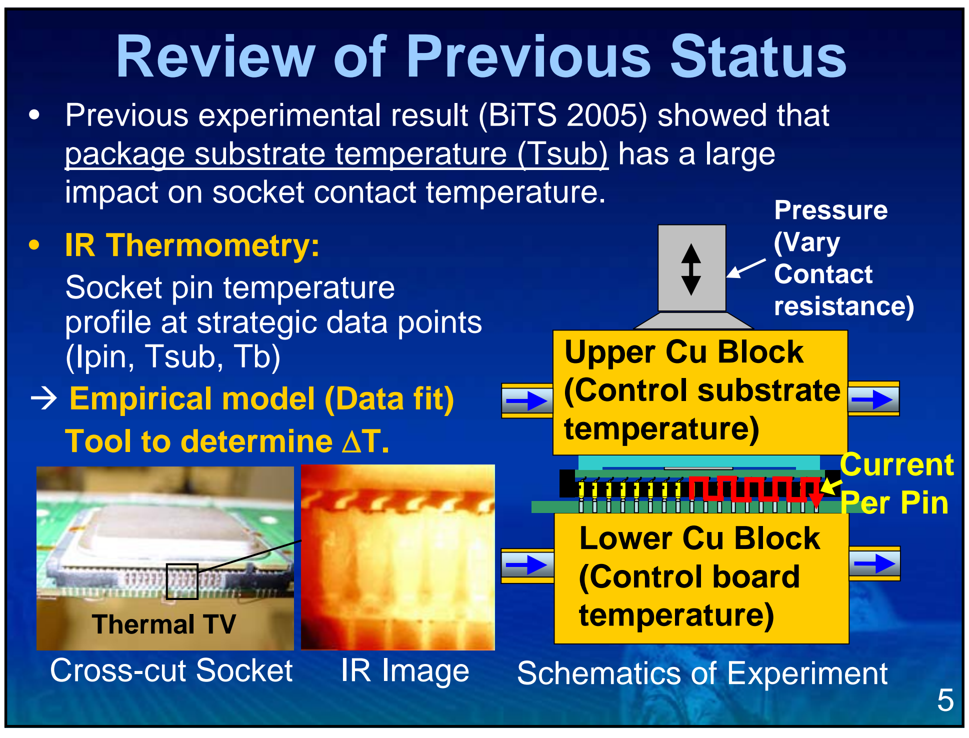
Socket Thermal Risk Assessment

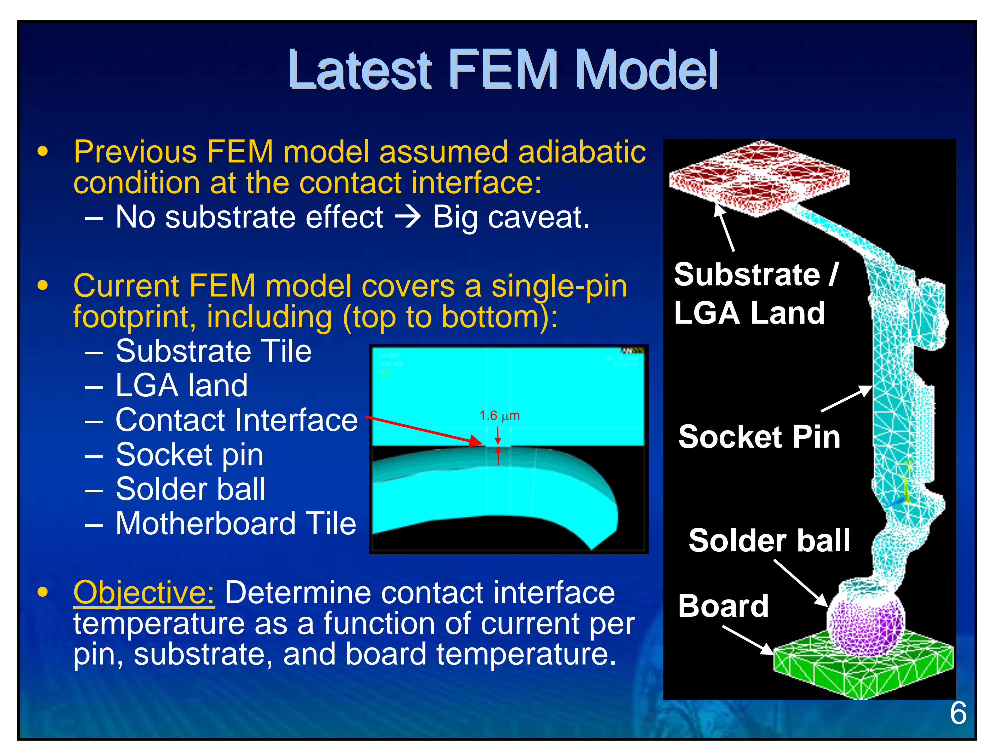
- **Socket Thermal Risk Assessment is governed by:**
  <u>Maximum allowed contact temperature</u> (Tc,max)
  <u>Need Risk assessment</u> against Tc,max at the product boundary conditions.
- Current Method for Socket Thermal Risk Assessment:
  –<u>Correlate</u> Tc,max to the maximum board temperature (Tboard,max) → Easier to measure & validate.

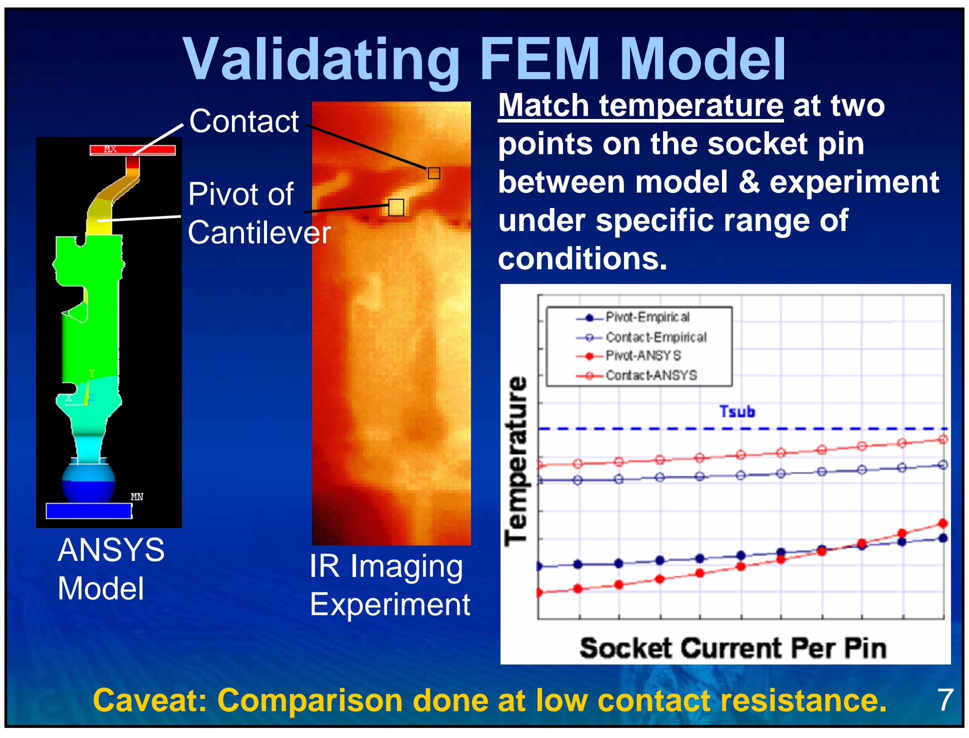
  Tb,max = Tc,max – ΔT (For given conditions)
- Tools:
  –Finite Element Model (FEM) Simulation (ie, ANSYS)
  –Infrared (IR) Experimental Characterization

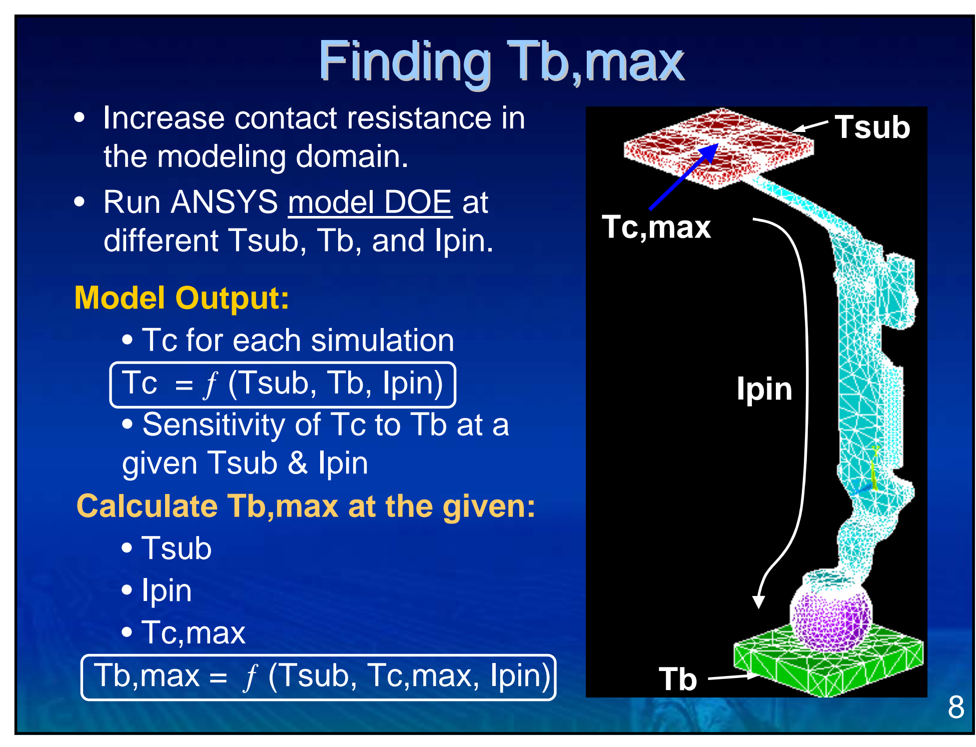


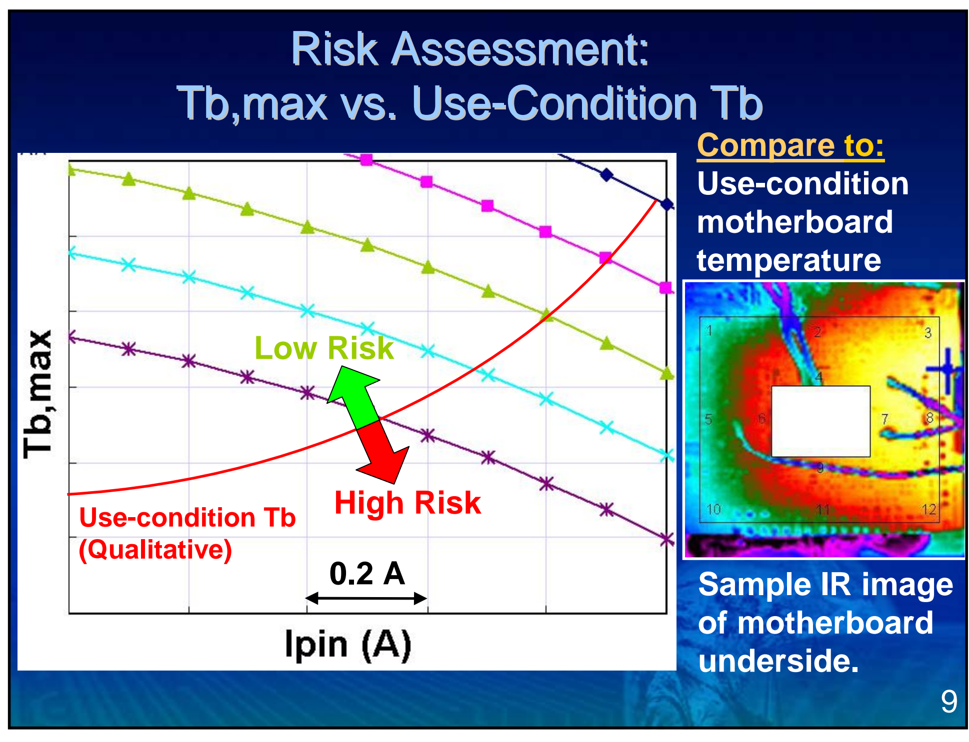
4

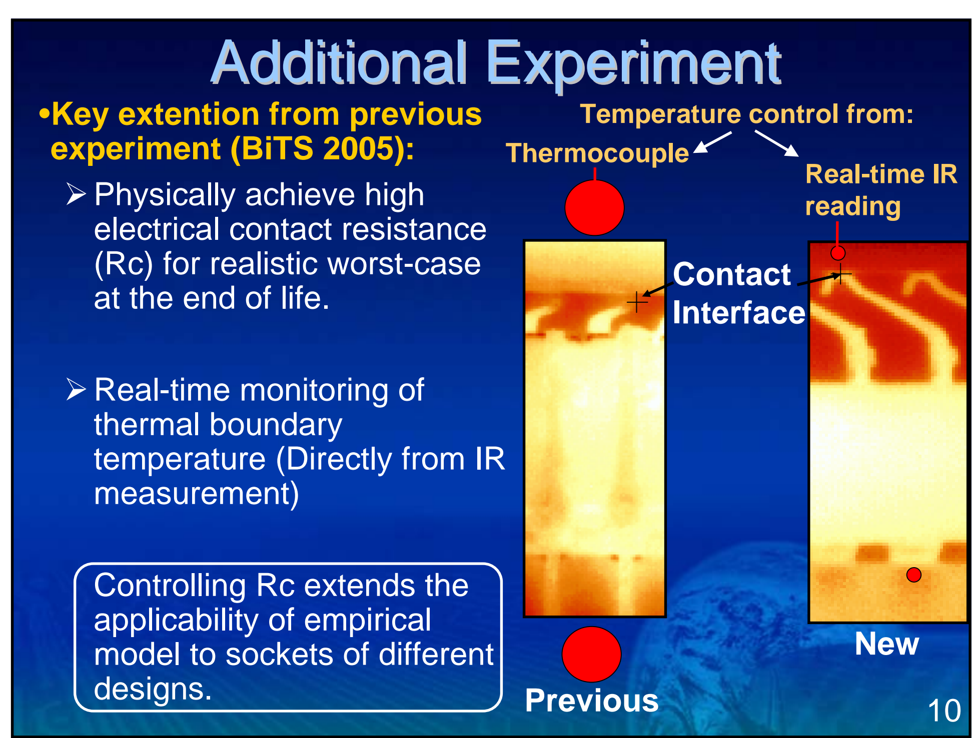

Review of Previous Status
Previous experimental result (BiTS 2005) showed that package substrate temperature (Tsub) has a large impact on socket contact temperature.
IR Thermometry:
Socket pin temperature profile at strategic data points (Ipin, Tsub, Tb)
→ Empirical model (Data fit)
Tool to determine ΔT.
Pressure (Vary Contact resistance)
Upper Cu Block (Control substrate temperature)
Current Per Pin
Lower Cu Block (Control board temperature)
Thermal TV
Cross-cut Socket
IR Image
Schematics of Experiment
5

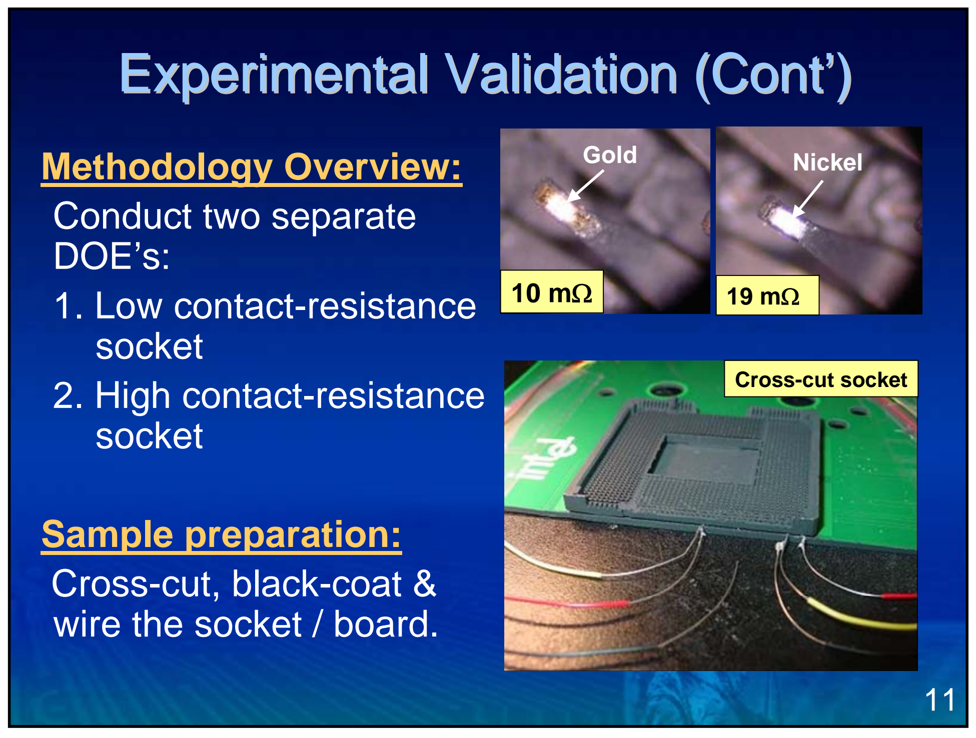

Latest FEM Model
Previous FEM model assumed adiabatic condition at the contact interface:
– No substrate effect → Big caveat.
Current FEM model covers a single-pin footprint, including (top to bottom):
– Substrate Tile
– LGA land
– Contact Interface
– Socket pin
– Solder ball
– Motherboard Tile
Objective: Determine contact interface temperature as a function of current per pin, substrate, and board temperature.
1.6 µm
Substrate / LGA Land
Socket Pin
Solder ball
Board
6

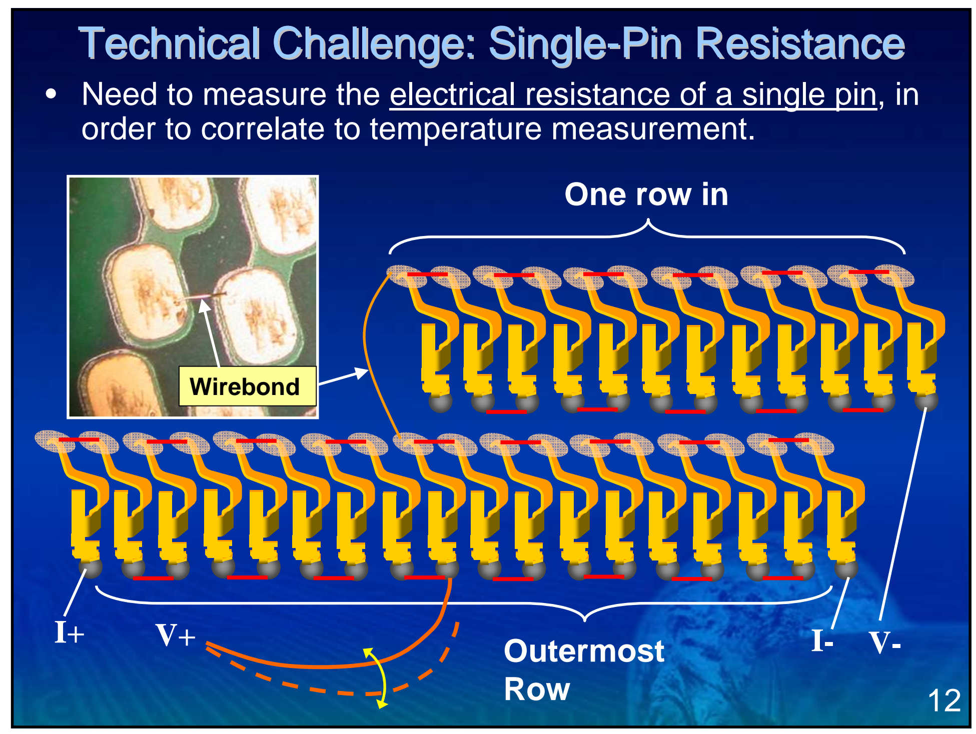

Validating FEM Model
Contact
Pivot of Cantilever
ANSYS Model
IR Imaging Experiment
Match temperature at two points on the socket pin between model & experiment under specific range of conditions.
Pivot-Empirical
Contact-Empirical
Pivot-ANSYS
Contact-ANSYS
Tsub
Temperature
Socket Current Per Pin
Caveat: Comparison done at low contact resistance.
7

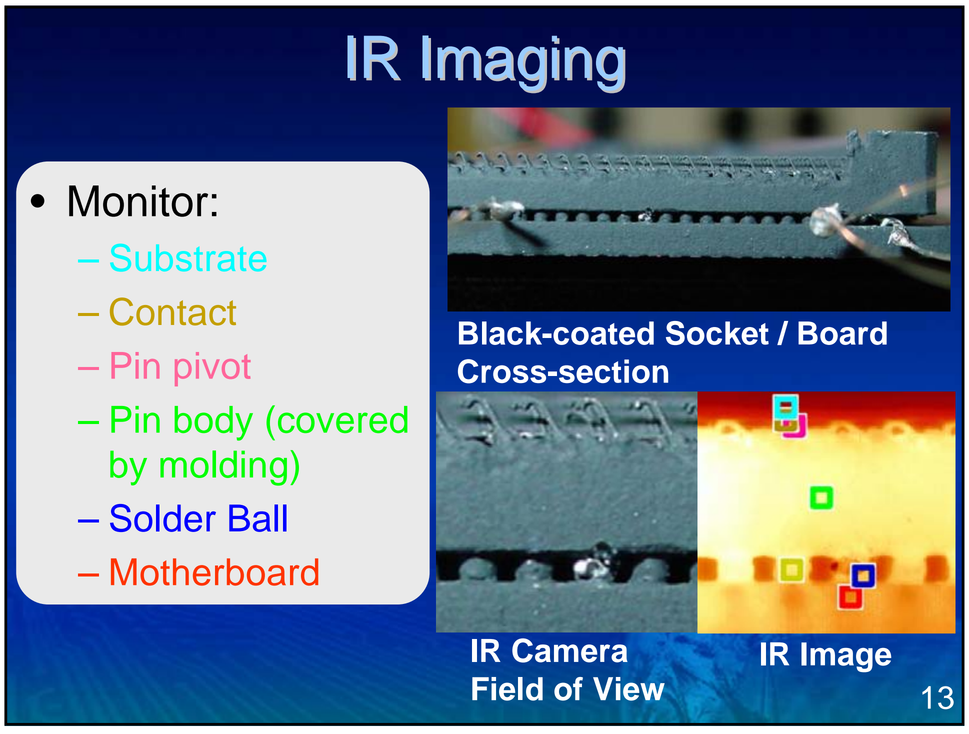

Finding Tb,max
• Increase contact resistance in the modeling domain.
• Run ANSYS model DOE at different Tsub, Tb, and Ipin.
Model Output:
• Tc for each simulation
Tc = f (Tsub, Tb, Ipin)
• Sensitivity of Tc to Tb at a given Tsub & Ipin
Calculate Tb,max at the given:
• Tsub
• Ipin
• Tc,max
Tb,max = f (Tsub, Tc,max, Ipin)
Tsub
Tc,max
Ipin
Tb
8

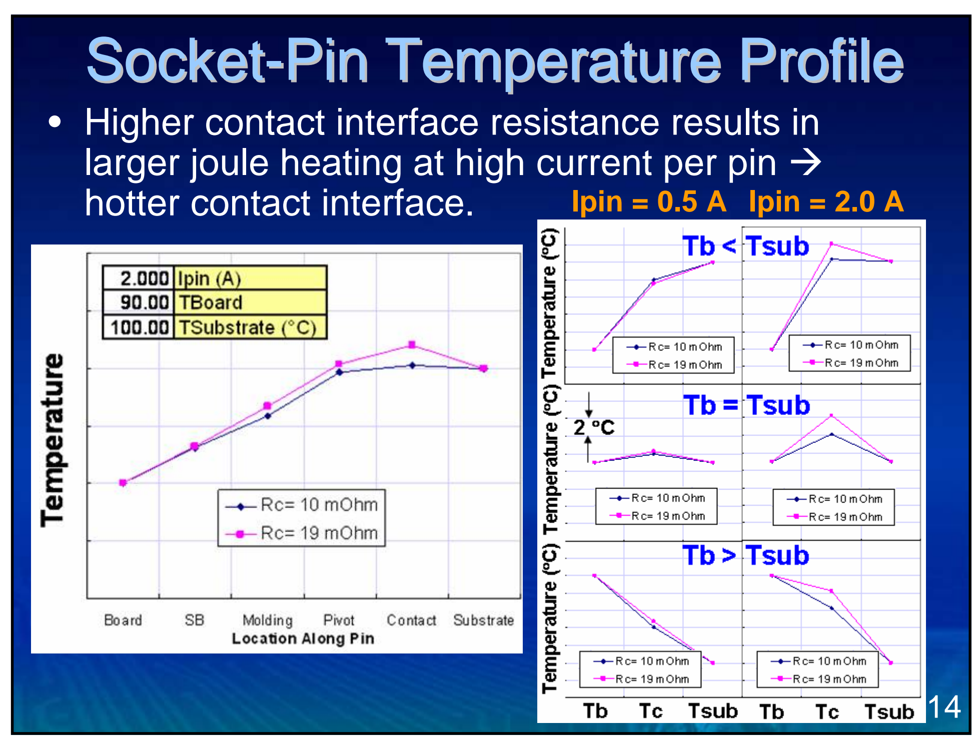

Risk Assessment:
Tb,max vs. Use-Condition Tb
Compare to:
Use-condition motherboard temperature
Tb,max
Low Risk
High Risk
Use-condition Tb (Qualitative)
0.2 A
Ipin (A)
Sample IR image of motherboard underside.
9


Additional Experiment
•Key extention from previous experiment (BiTS 2005):
➢ Physically achieve high electrical contact resistance (Rc) for realistic worst-case at the end of life.
➢ Real-time monitoring of thermal boundary temperature (Directly from IR measurement)
Controlling Rc extends the applicability of empirical model to sockets of different designs.
Temperature control from:
Thermocouple
Real-time IR reading
Contact Interface
Previous
New
10


Experimental Validation (Cont')
Methodology Overview:
Conduct two separate DOE's:
1. Low contact-resistance socket
2. High contact-resistance socket
Sample preparation:
Cross-cut, black-coat & wire the socket / board.
Gold
10 mΩ
Nickel
19 mΩ
Cross-cut socket
11

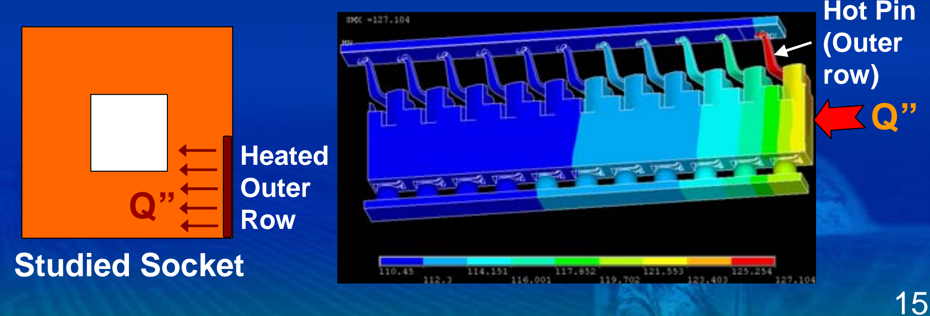

Technical Challenge: Single-Pin Resistance
• Need to measure the electrical resistance of a single pin, in order to correlate to temperature measurement.
Wirebond
One row in
I+
V+
Outermost Row
I-
V-
12


IR Imaging
• Monitor:
– Substrate
– Contact
– Pin pivot
– Pin body (covered by molding)
– Solder Ball
– Motherboard
Black-coated Socket / Board Cross-section
IR Camera Field of View
IR Image
13


Socket-Pin Temperature Profile
• Higher contact interface resistance results in larger joule heating at high current per pin → hotter contact interface.
Ipin = 0.5 A
Ipin = 2.0 A
2.000 Ipin (A)
90.00 TBoard
100.00 TSubstrate (°C)
Temperature
Rc= 10 mOhm
Rc= 19 mOhm
Board
SB
Molding
Pivot
Contact
Substrate
Location Along Pin
Tb < Tsub
Tb = Tsub
Tb > Tsub
2 °C
Temperature (°C)
Tb
Tc
Tsub
14

Ongoing Activity: Extend FEM Model to Multiple Contacts

- FEM must capture the experimental boundary conditions: pin-to-pin interaction and environmental effects (like system airflow).
- The model can be used to study the placement of high current contacts.
- The model can be further used for socket thermal solution design and optimization.



15

Key Summary

- Socket thermal analysis has been significantly improved in both numerical modeling and experimental methodology.
- For numerical model, the effect of substrate temperature (very important) has been added and matched to the previous empirical model.
- New infrared-imaging experimental methodology incorporates significant improvements over the previous one (BiTS 2005), most notably the physical achievement and measurement of high-resistance socket pin.
- Improvements in methodology will increase confidence in critical socket thermal risk assessment and ultimately provide an increased margin in socket current capacity.

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Glossary (Alphabetical Order)

BKM – Best known Method
DAC – Data acquisition and control
DOE – Design of experiment
FEM – Finite element analysis
IHS – Integrated heatsink
Ipin – Current per socket pin
IR – Infrared
ΔT – Temperature drop between the socket pin contact interface and the local motherboard temperature.
Tb – Motherboard temperature
Tb,max – Maximum allowed motherboard temperature
Tc – Contact interface temperature
Tc,max – Maximum allowed contact temperature
Tsub – Package substrate temperature
TV – Test vehicle,
i.e. a mock-up processor/ socket/board set.

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Lumped and Distributed Equivalent Circuits for Test Sockets

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

GateWave Northern, Inc.
Gert Hohenwarter
GateWave Northern, Inc.

Objectives

- Demonstrate uses and limits of different models
- Show performance potential and limits of
  - Loadboard with socket
  - Fast PCB
  - Loopback from a DUT onto a PCB
  - Straight thru
- Point out some pitfalls
- Place socket properties into application perspective

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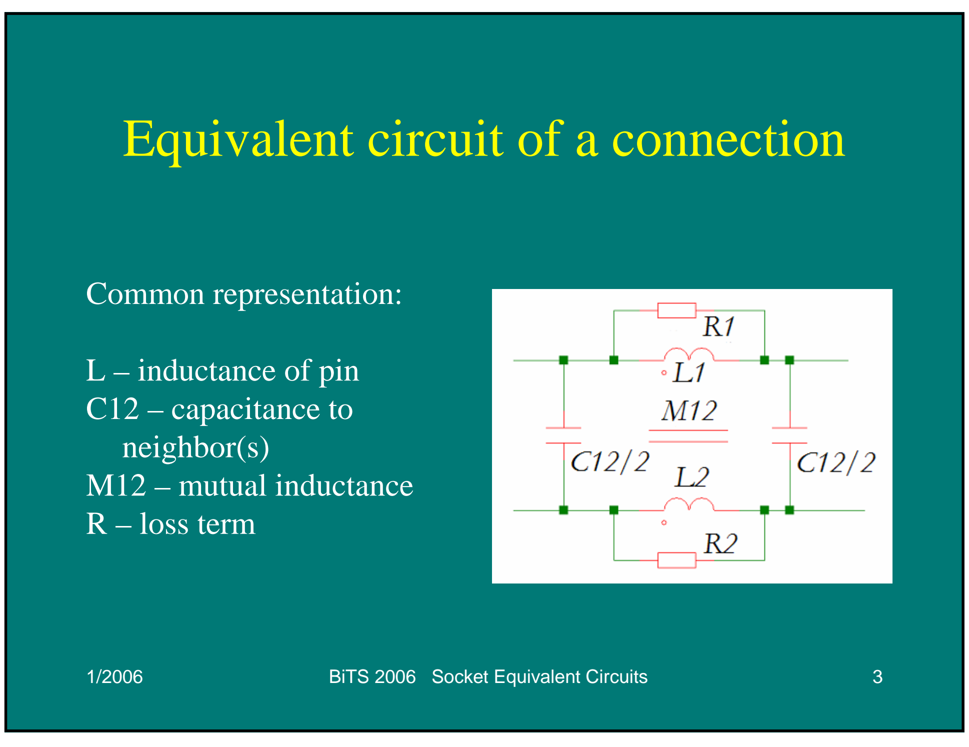
Equivalent circuit of a connection
Common representation:
L – inductance of pin
C12 – capacitance to neighbor(s)
M12 – mutual inductance
R – loss term
R1
L1
M12
C12/2
L2
C12/2
R2
1/2006
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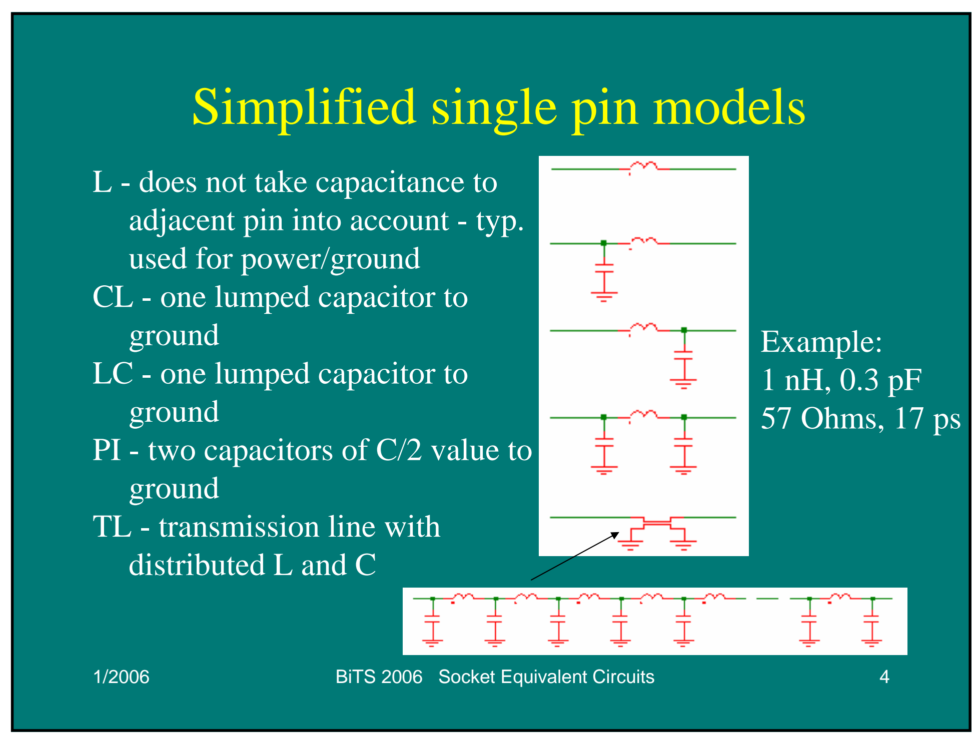
3


Simplified single pin models
L - does not take capacitance to adjacent pin into account - typ. used for power/ground
CL - one lumped capacitor to ground
LC - one lumped capacitor to ground
PI - two capacitors of C/2 value to ground
TL - transmission line with distributed L and C
Example:
1 nH, 0.3 pF
57 Ohms, 17 ps
1/2006
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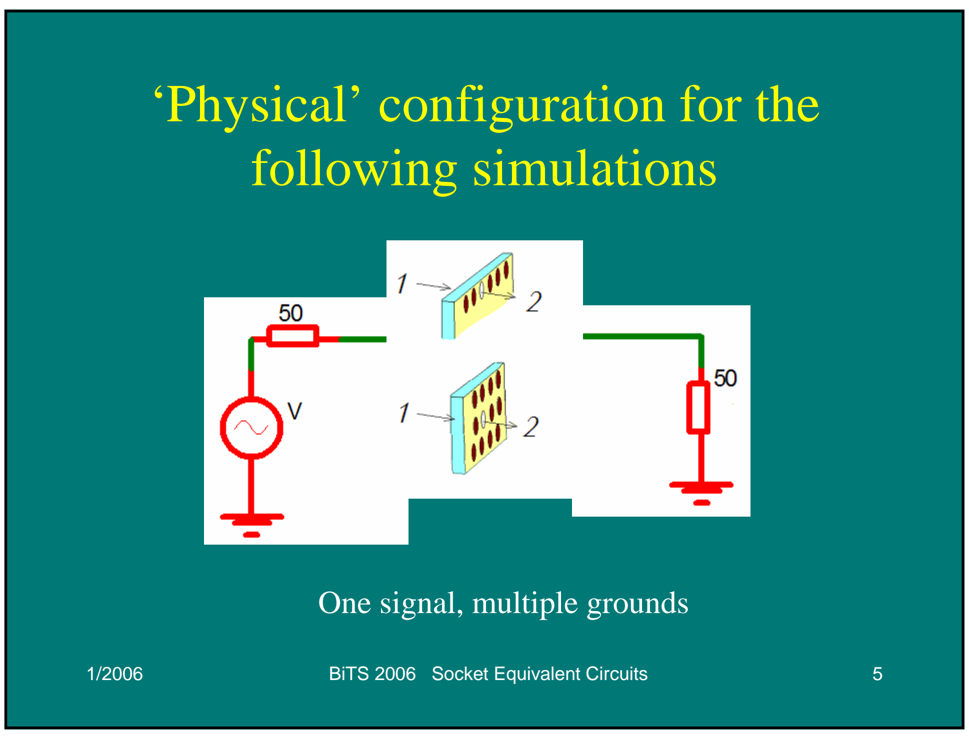
4


'Physical' configuration for the following simulations
50
V
1
2
1
2
50
One signal, multiple grounds
1/2006
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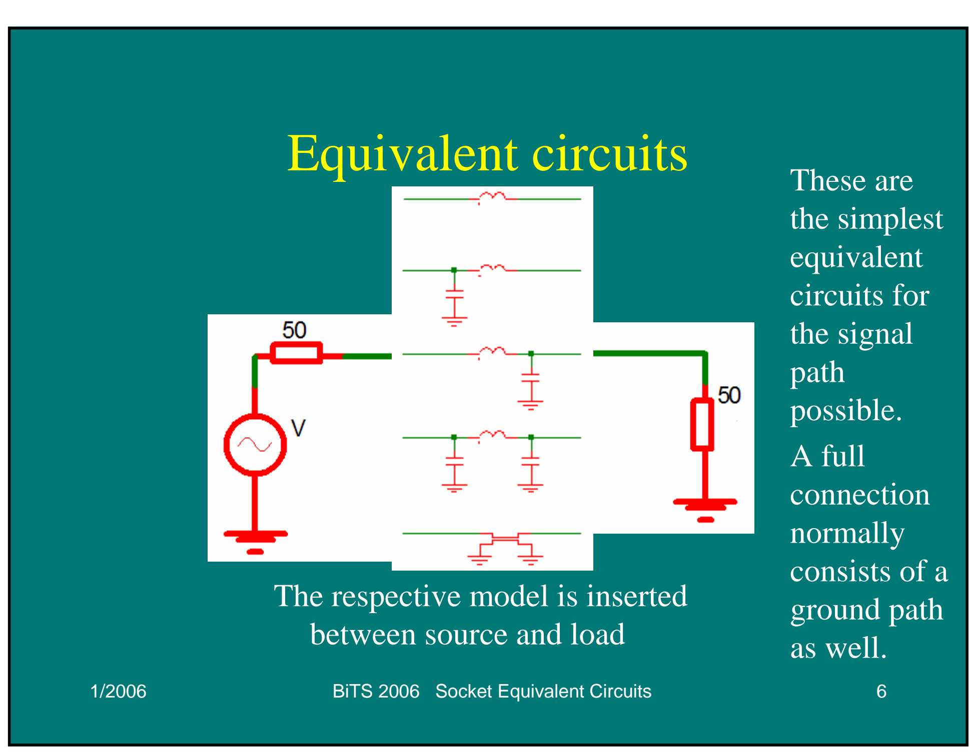
5


Equivalent circuits
50
V
50
These are the simplest equivalent circuits for the signal path possible.
A full connection normally consists of a ground path as well.
The respective model is inserted between source and load
1/2006
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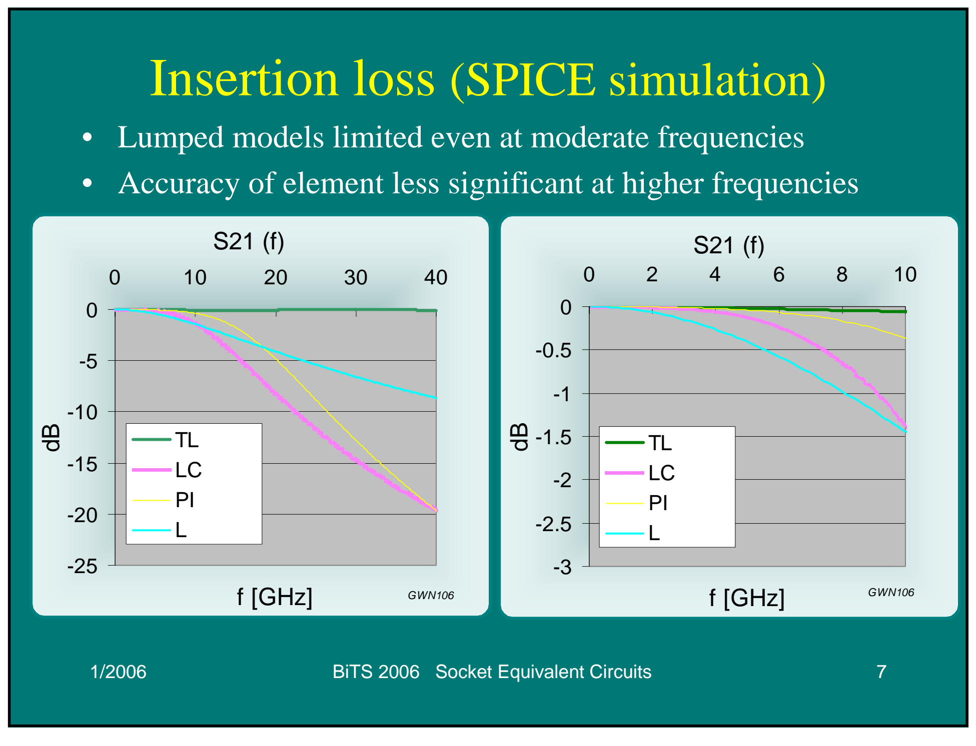
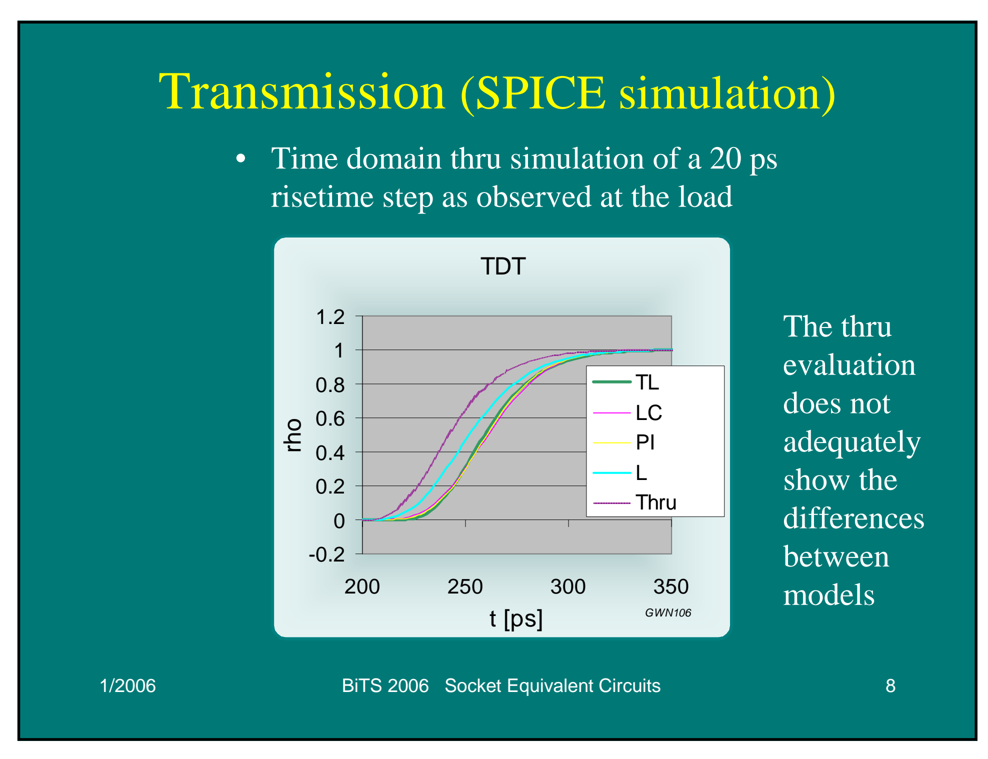

Insertion loss (SPICE simulation)
• Lumped models limited even at moderate frequencies
• Accuracy of element less significant at higher frequencies
S21 (f)
0
10
20
30
40
0
-5
-10
-15
-20
-25
dB
TL
LC
PI
L
f [GHz]
GWN106
S21 (f)
0
2
4
6
8
10
0
-0.5
-1
-1.5
-2
-2.5
-3
dB
TL
LC
PI
L
f [GHz]
GWN106
1/2006
BiTS 2006 Socket Equivalent Circuits
7


Transmission (SPICE simulation)
• Time domain thru simulation of a 20 ps risetime step as observed at the load
TDT
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
rho
TL
LC
PI
L
Thru
200
250
300
350
t [ps]
GWN106
The thru evaluation does not adequately show the differences between models
1/2006
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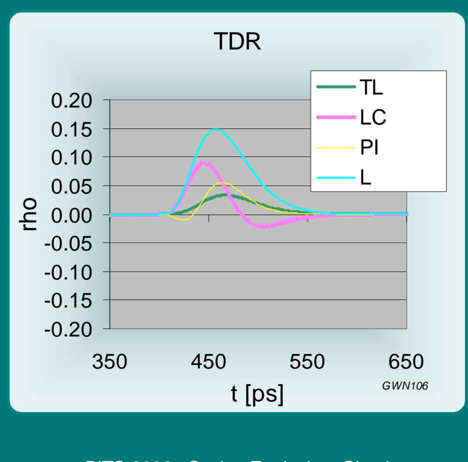
8

Lumped vs. distributed models

- TD reflection model (SPICE) shows significant differences



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Model applications

L - low frequencies - typ. used for power/ground

CL - low frequencies

LC - low frequencies

PI - moderate frequencies

TL - high frequencies, not suited for power and ground models

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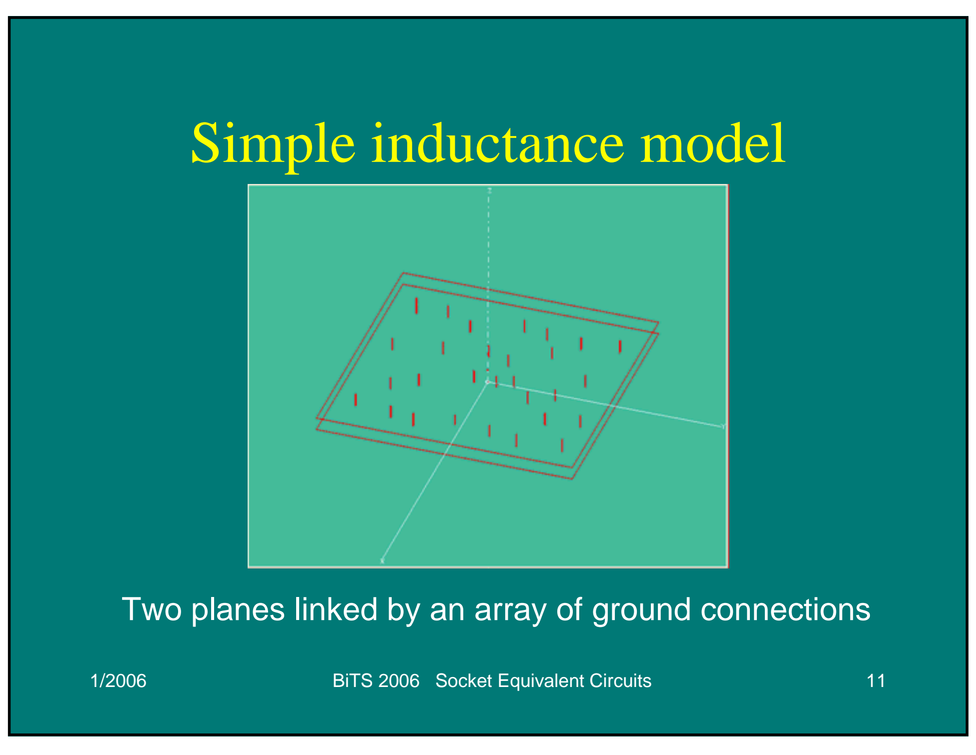
Simple inductance model
Two planes linked by an array of ground connections
1/2006
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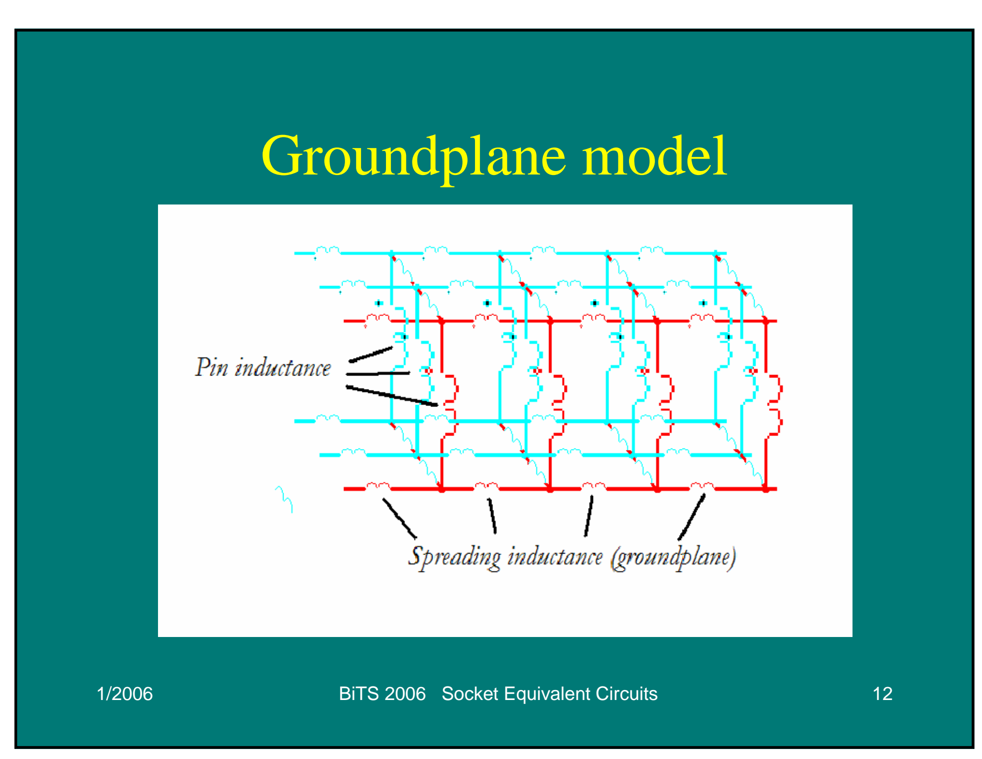
11


Groundplane model
Pin inductance
Spreading inductance (groundplane)
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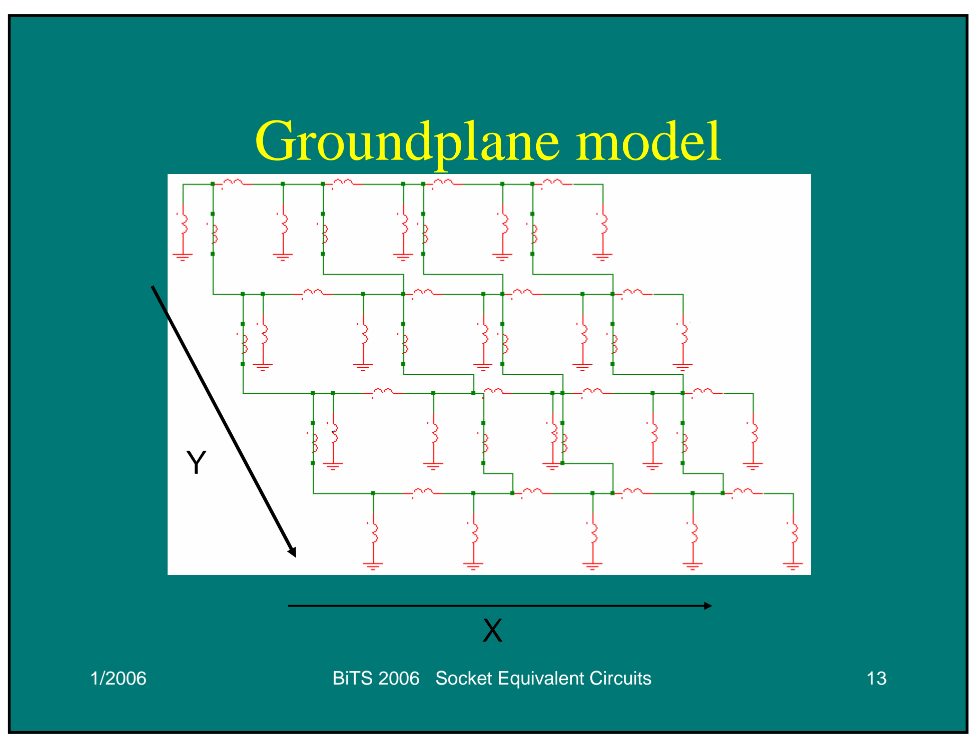
Groundplane model
Y
X
1/2006
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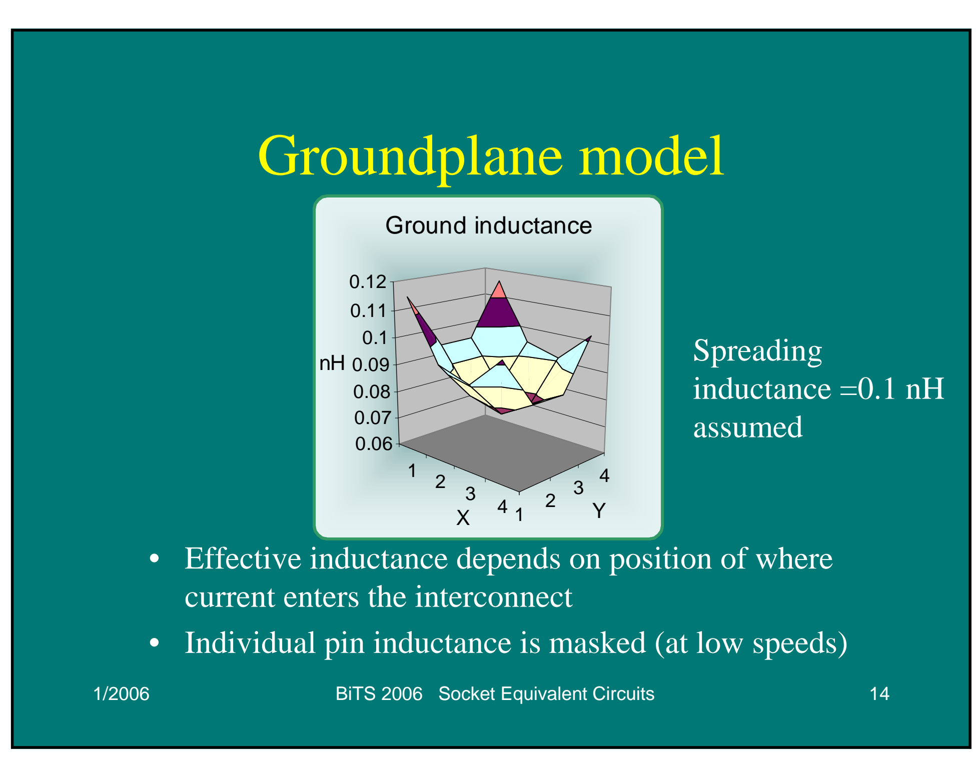
13


Groundplane model
Ground inductance
0.12
0.11
0.1
nH 0.09
0.08
0.07
0.06
1
2
3
4
X
1
2
3
4
Y
Spreading inductance =0.1 nH assumed
• Effective inductance depends on position of where current enters the interconnect
• Individual pin inductance is masked (at low speeds)
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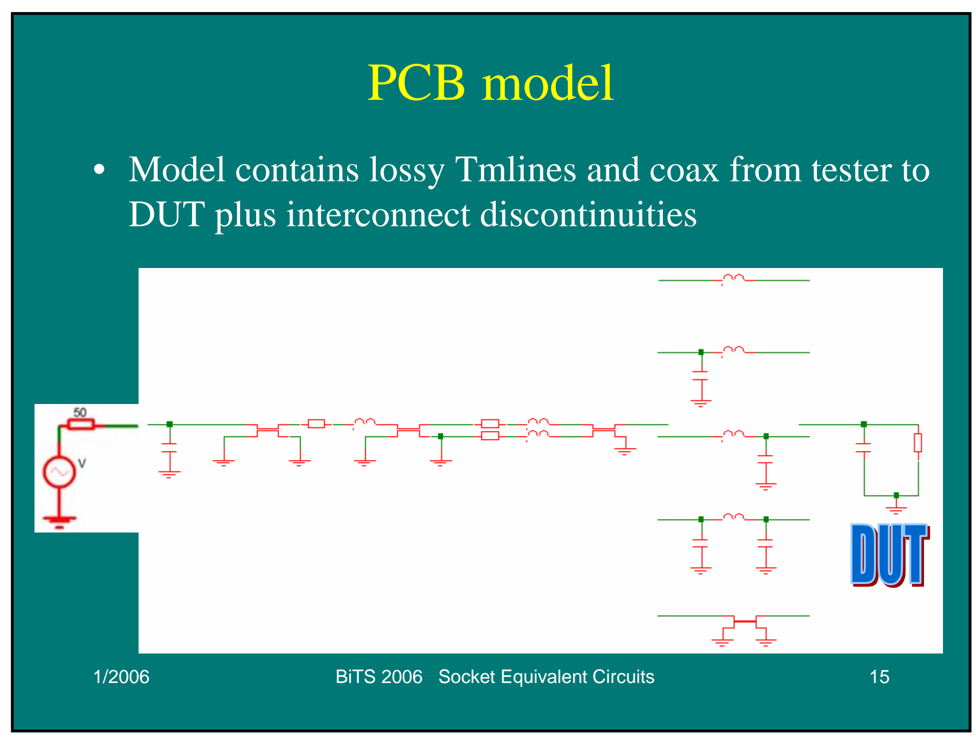
14


PCB model
• Model contains lossy Tmlines and coax from tester to DUT plus interconnect discontinuities
50
V
DUT
1/2006
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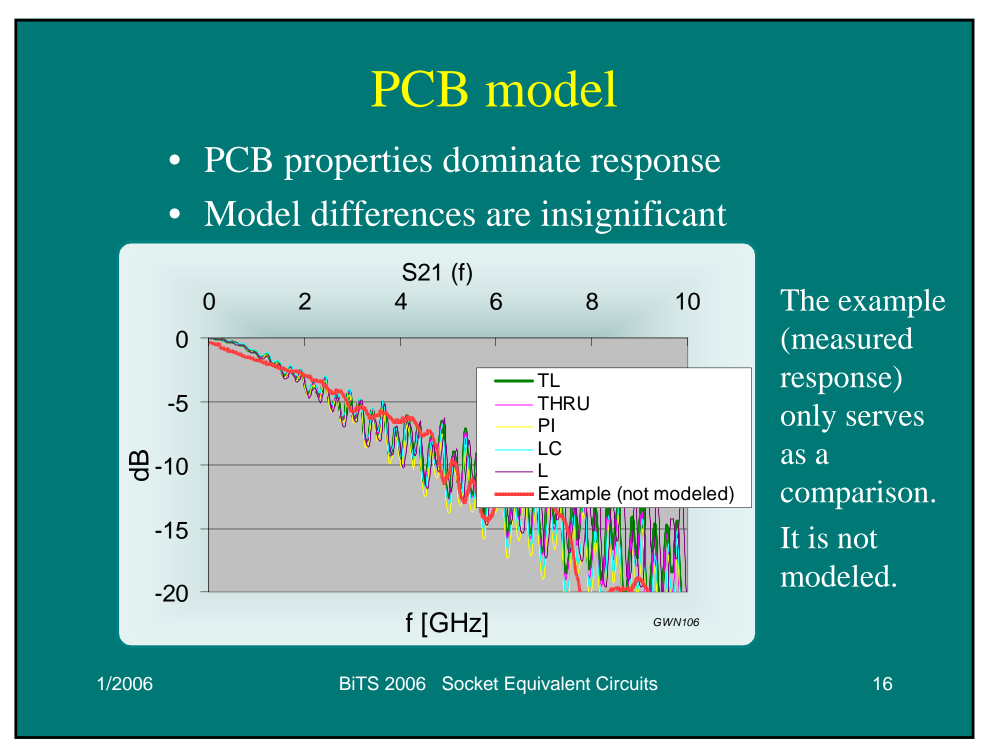
15


PCB model
• PCB properties dominate response
• Model differences are insignificant
S21 (f)
0
2
4
6
8
10
0
-5
-10
-15
-20
dB
TL
THRU
PI
LC
L
Example (not modeled)
f [GHz]
GWN106
The example (measured response) only serves as a comparison.
It is not modeled.
1/2006
BiTS 2006 Socket Equivalent Circuits
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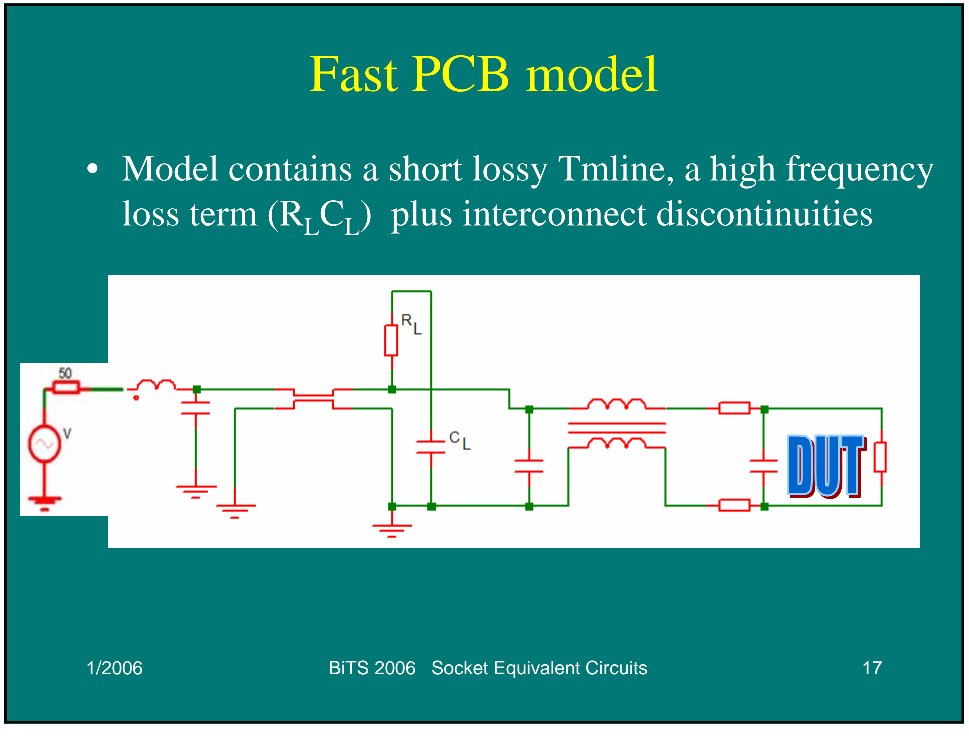
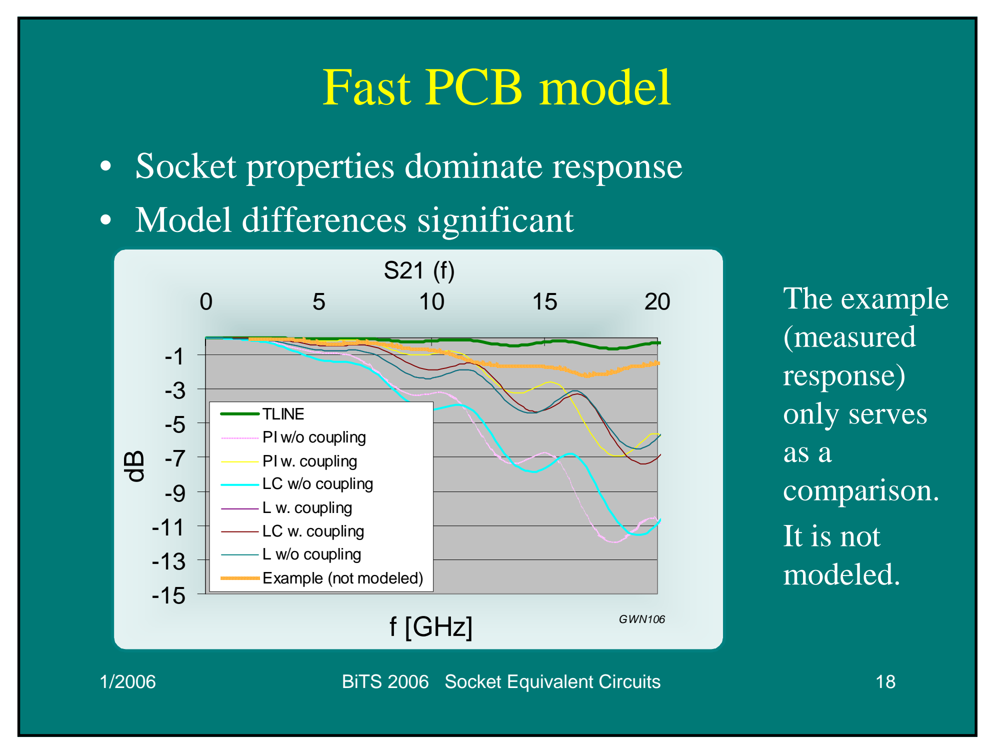

Fast PCB model
• Model contains a short lossy Tmline, a high frequency loss term (RLCL) plus interconnect discontinuities
50
V
RL
CL
DUT
1/2006
BiTS 2006 Socket Equivalent Circuits
17


Fast PCB model
• Socket properties dominate response
• Model differences significant
S21 (f)
0
5
10
15
20
-1
-3
-5
-7
-9
-11
-13
-15
dB
TLINE
PI w/o coupling
PI w. coupling
LC w/o coupling
L w. coupling
LC w. coupling
L w/o coupling
Example (not modeled)
f [GHz]
GWN106
The example (measured response) only serves as a comparison.
It is not modeled.
1/2006
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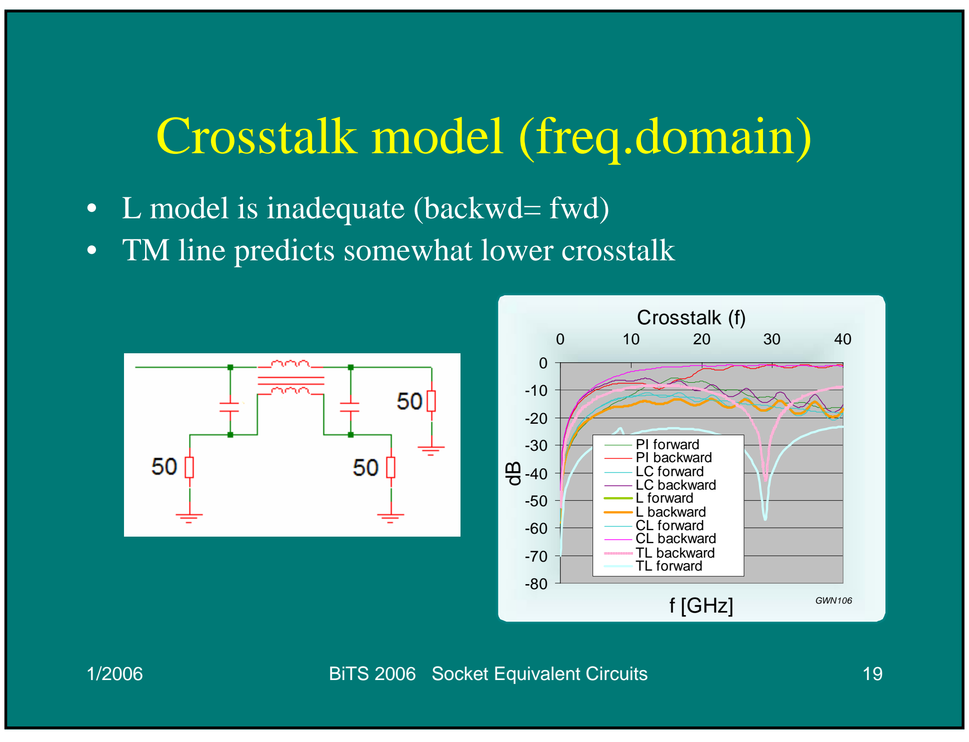
Crosstalk model (freq.domain)
• L model is inadequate (backwd= fwd)
• TM line predicts somewhat lower crosstalk
50
50
50
Crosstalk (f)
0
10
20
30
40
0
-10
-20
-30
-40
-50
-60
-70
-80
dB
PI forward
PI backward
LC forward
LC backward
L forward
L backward
CL forward
CL backward
TL backward
TL forward
f [GHz]
GWN106
1/2006
BiTS 2006 Socket Equivalent Circuits
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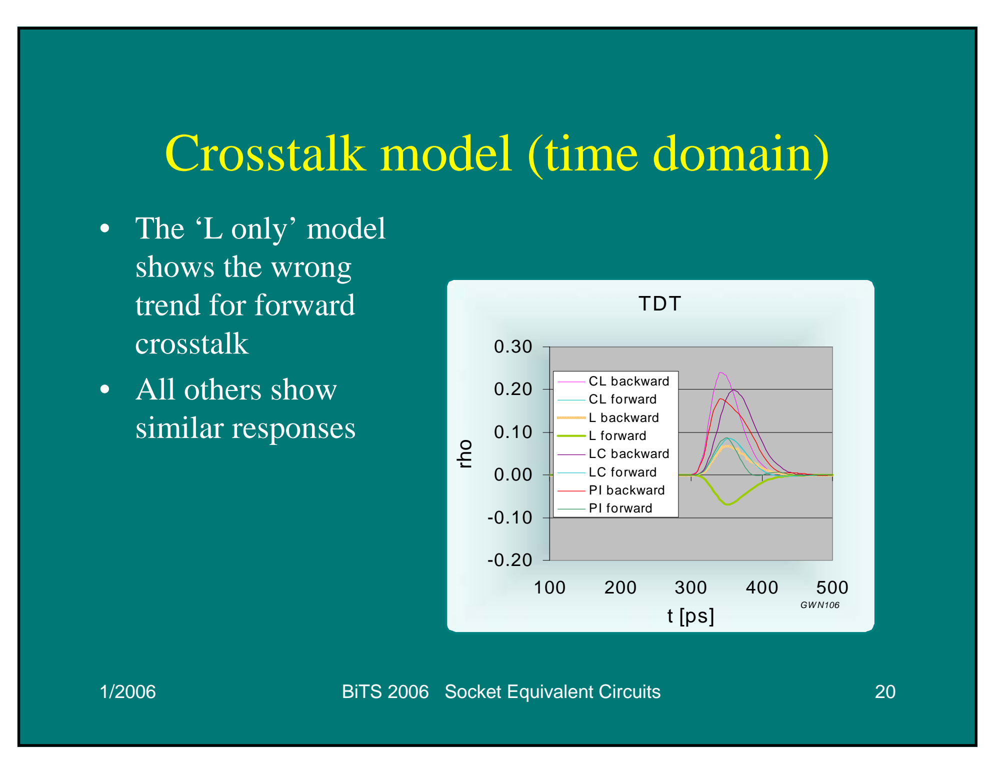
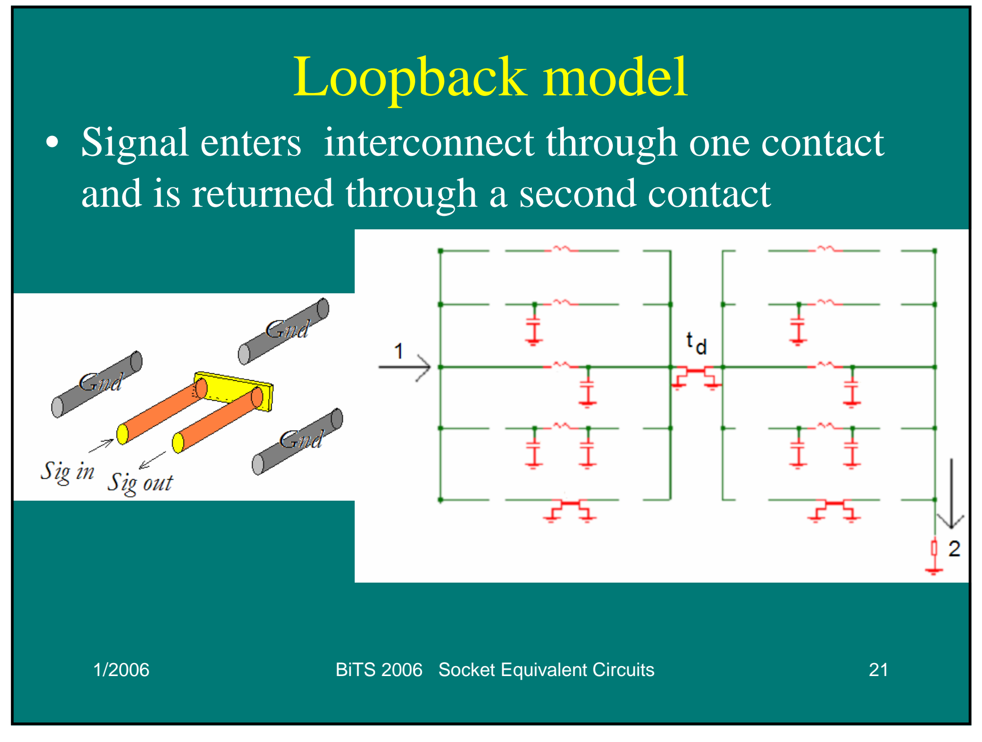

Crosstalk model (time domain)
• The 'L only' model shows the wrong trend for forward crosstalk
• All others show similar responses
TDT
0.30
0.20
0.10
0.00
-0.10
-0.20
rho
CL backward
CL forward
L backward
L forward
LC backward
LC forward
PI backward
PI forward
100
200
300
400
500
t [ps]
GWN106
1/2006
BiTS 2006 Socket Equivalent Circuits
20


Loopback model
• Signal enters interconnect through one contact and is returned through a second contact
Gnd
Gnd
Gnd
Sig in
Sig out
1
t_d
2
1/2006
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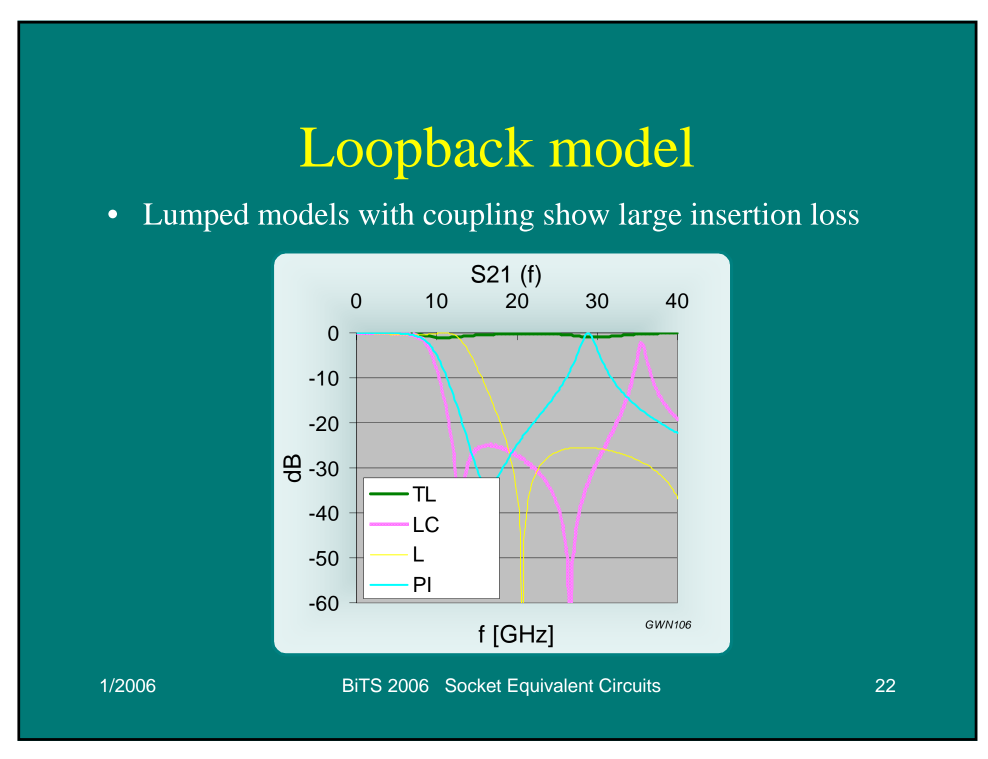
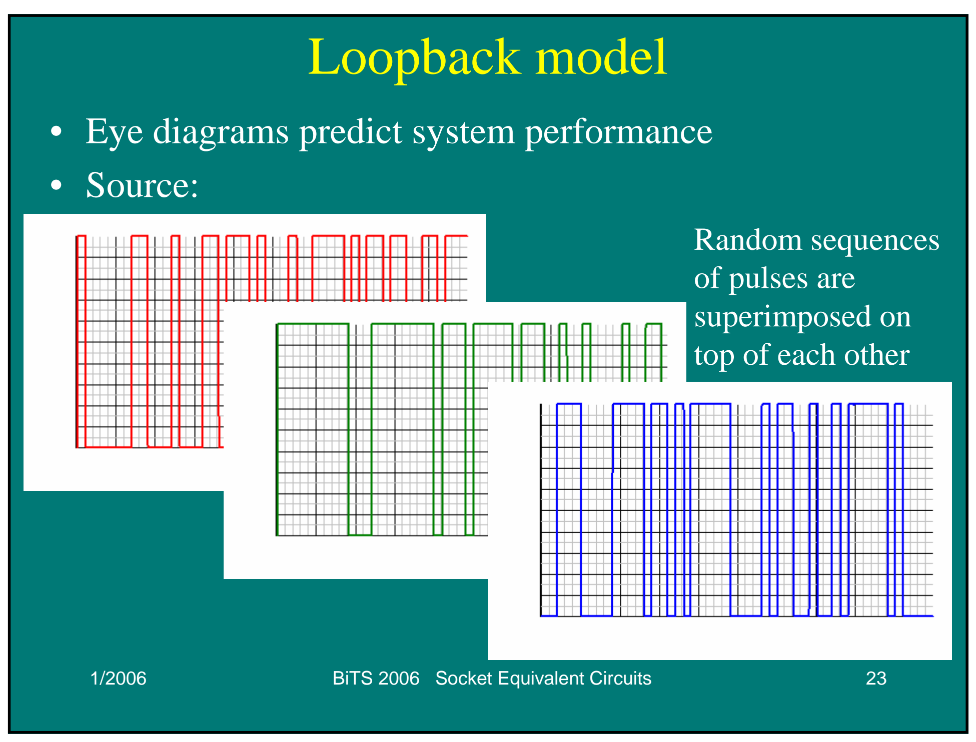

Loopback model
• Lumped models with coupling show large insertion loss
S21 (f)
0
10
20
30
40
0
-10
-20
-30
-40
-50
-60
dB
TL
LC
L
PI
f [GHz]
GWN106
1/2006
BiTS 2006 Socket Equivalent Circuits
22


Loopback model
• Eye diagrams predict system performance
• Source:
Random sequences of pulses are superimposed on top of each other
1/2006
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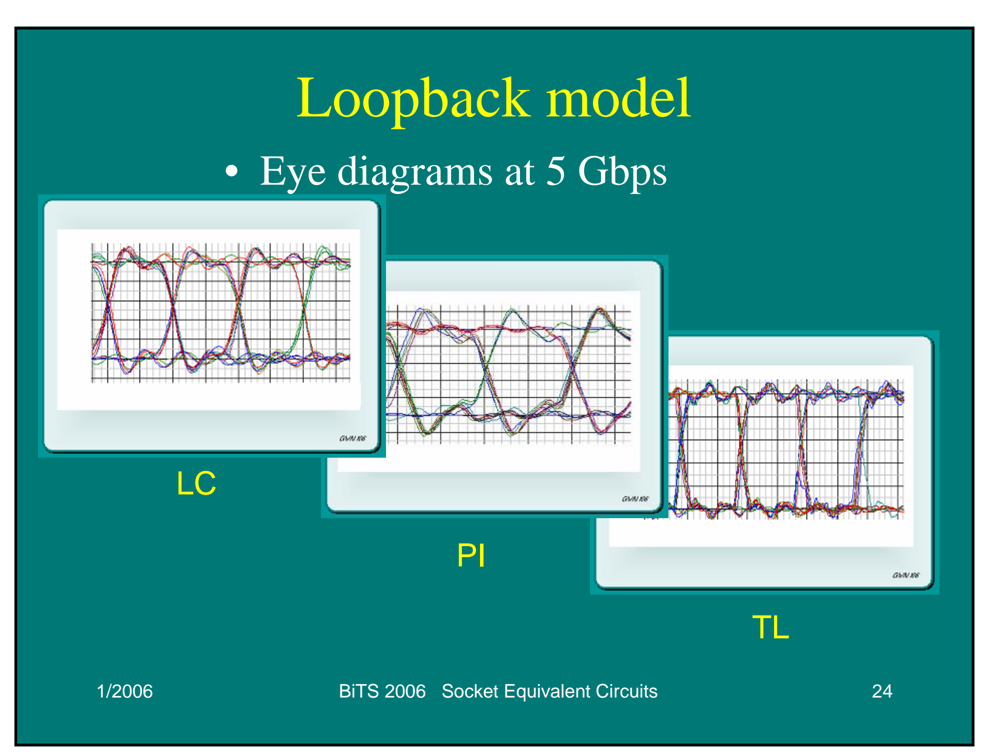
23


Loopback model
• Eye diagrams at 5 Gbps
LC
PI
TL
1/2006
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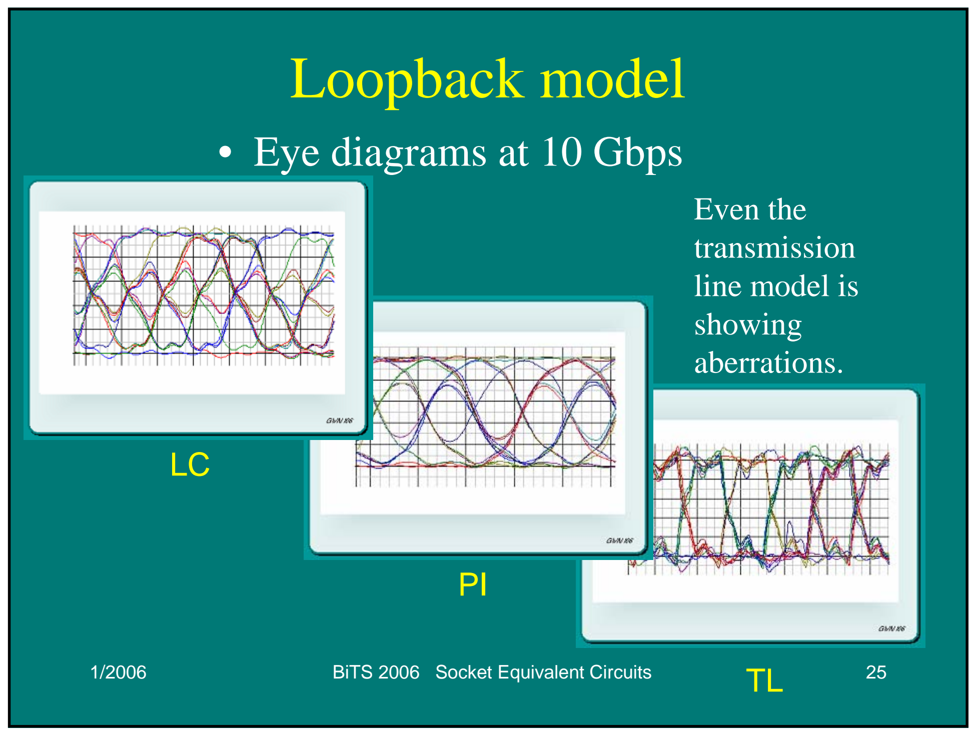
Loopback model
• Eye diagrams at 10 Gbps
Even the transmission line model is showing aberrations.
LC
PI
TL
1/2006
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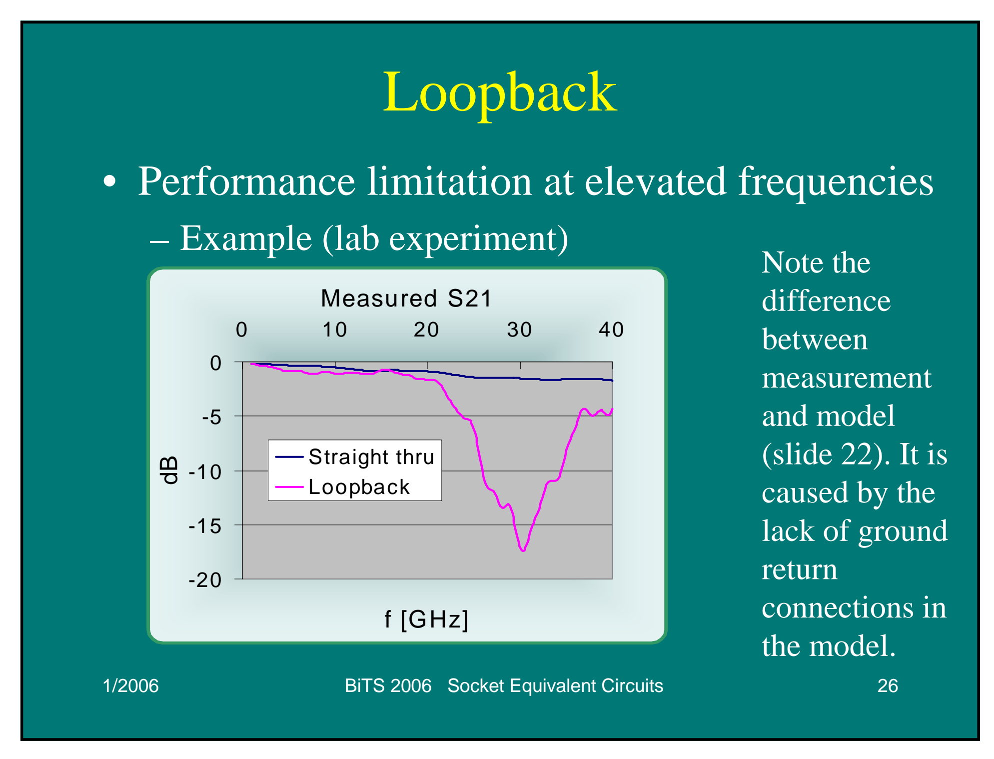
25


Loopback
• Performance limitation at elevated frequencies
– Example (lab experiment)
Measured S21
0
10
20
30
40
0
-5
-10
-15
-20
dB
Straight thru
Loopback
f [GHz]
Note the difference between measurement and model (slide 22). It is caused by the lack of ground return connections in the model.
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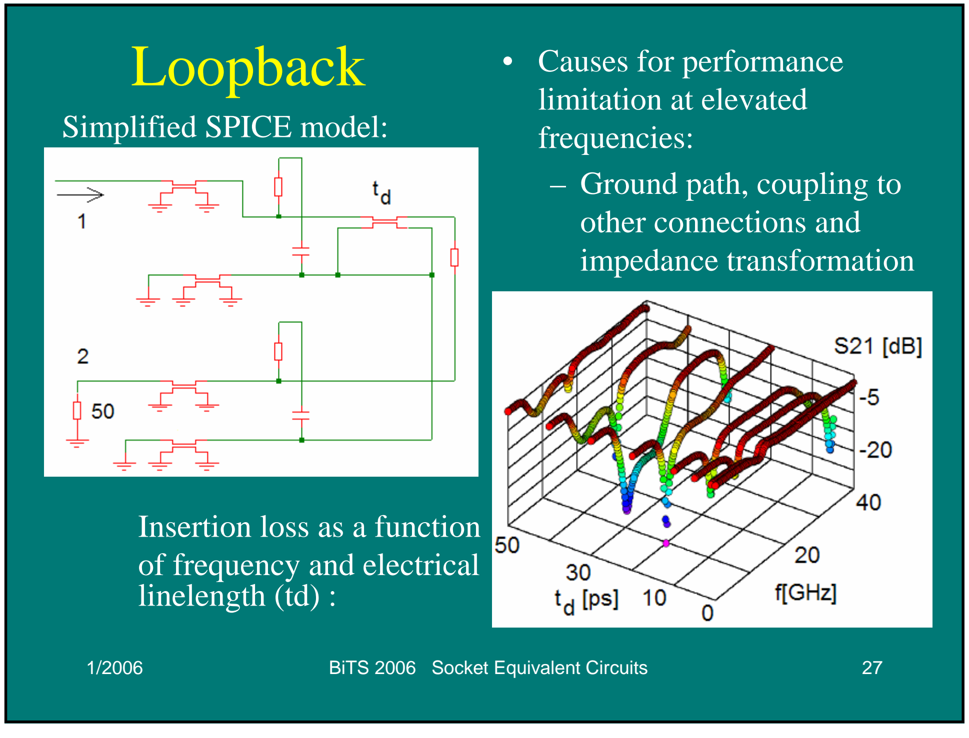
Loopback
Simplified SPICE model:
1
2
50
t_d
• Causes for performance limitation at elevated frequencies:
– Ground path, coupling to other connections and impedance transformation
S21 [dB]
-5
-20
40
50
30
t_d [ps]
10
0
20
f[GHz]
Insertion loss as a function of frequency and electrical linelength (td) :
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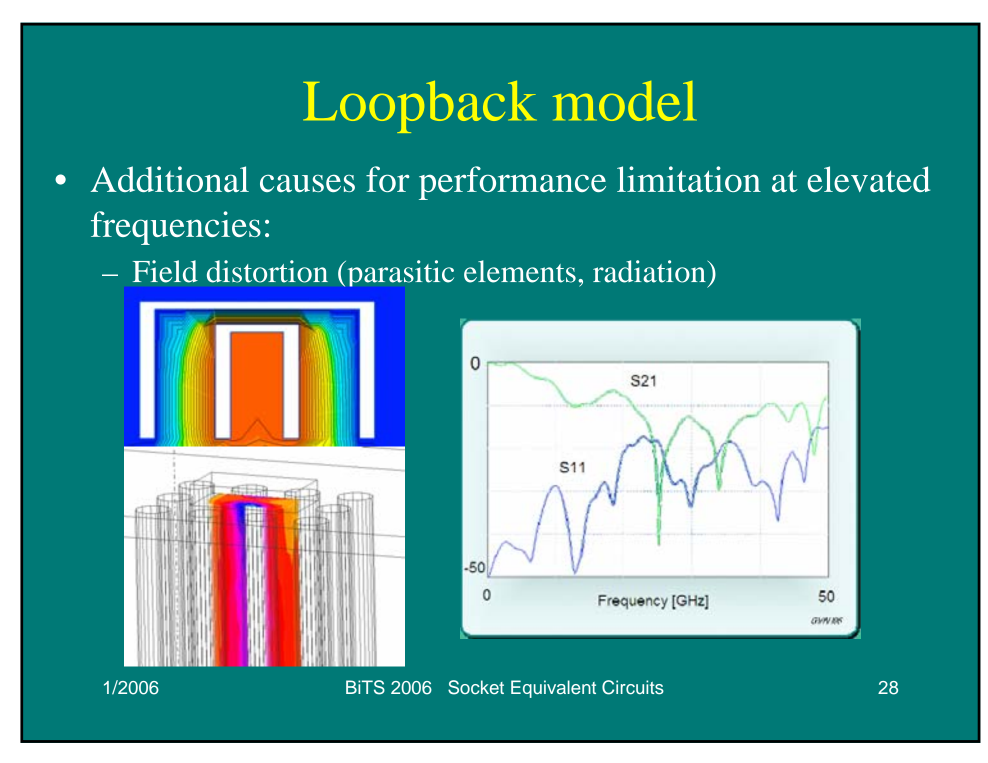
Loopback model
• Additional causes for performance limitation at elevated frequencies:
– Field distortion (parasitic elements, radiation)
0
S21
S11
-50
0
Frequency [GHz]
50
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Loopback model

- Performance limitation at elevated frequencies
  - Fields distorted
  - Multiple discontinuities
  - PCB loss/fringe/radiation contributions
  - Dependent on length of line between contacts
  - Ground return path disrupted

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Conclusion

- Interpretation (significance) of parameters and their variations depends on environment a socket is placed in
- At elevated frequencies, TMline representations become imperative
- Pin performance at elevated frequencies can only be assessed in configurations that allow these frequencies to be reached

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Objectives

- Introduction of Pin Inductance Characteristics
- Discuss techniques of measurement with fixture and without fixture.
- Summary

2

Why is this an issue for Intel?

- Wireless hardware leverages the cost/performance of QFN type package
  - Vss (return) pin population becomes an optimization
- IEEE 802.11 a/b/g/n products require stable power up to the band of operation:
  - 2.4 GHz & 5GHz
- Therefore, Stable path to power supply through the QFN; well into 5 GHz range without over designing the socket

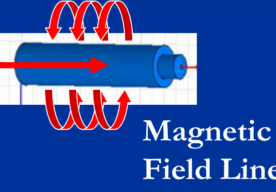
3

Introduction to Pin Inductance

Inductance can be explained with total number of magnetic field lines induced when current flows through conductor.

A) Partial self Inductance

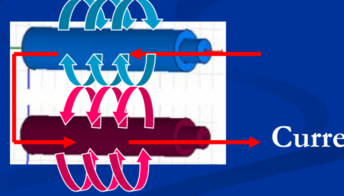
Inductance of a single pin



B) Mutual Inductance

Influence of one magnetic field to another magnetic field

Pitch ↓ , Mutual Inductance ↑



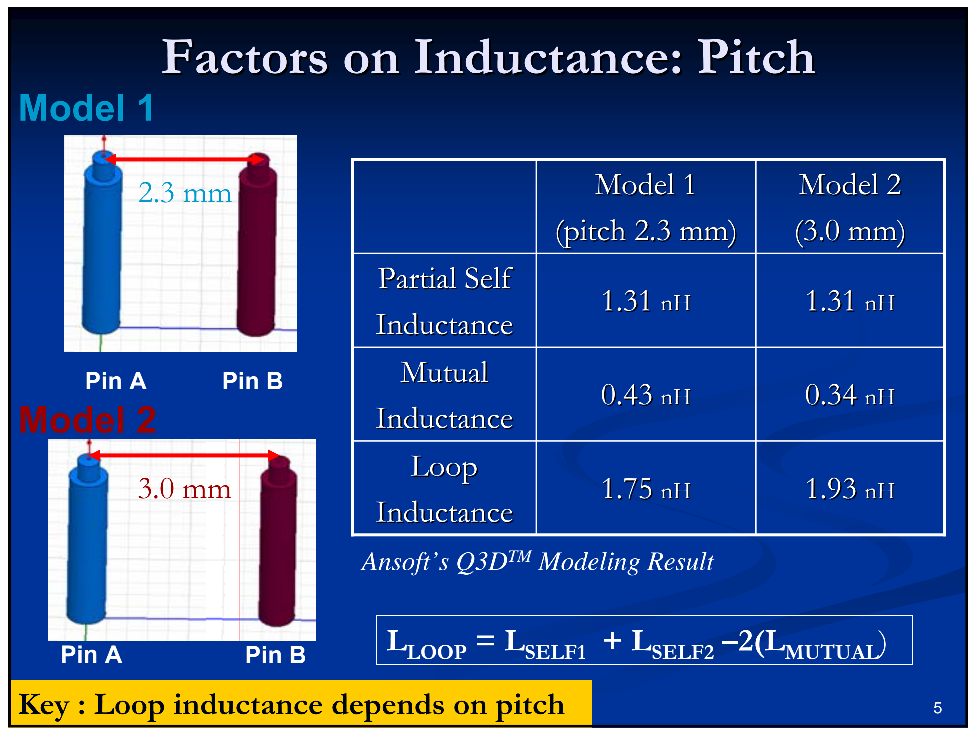
C) Loop Inductance

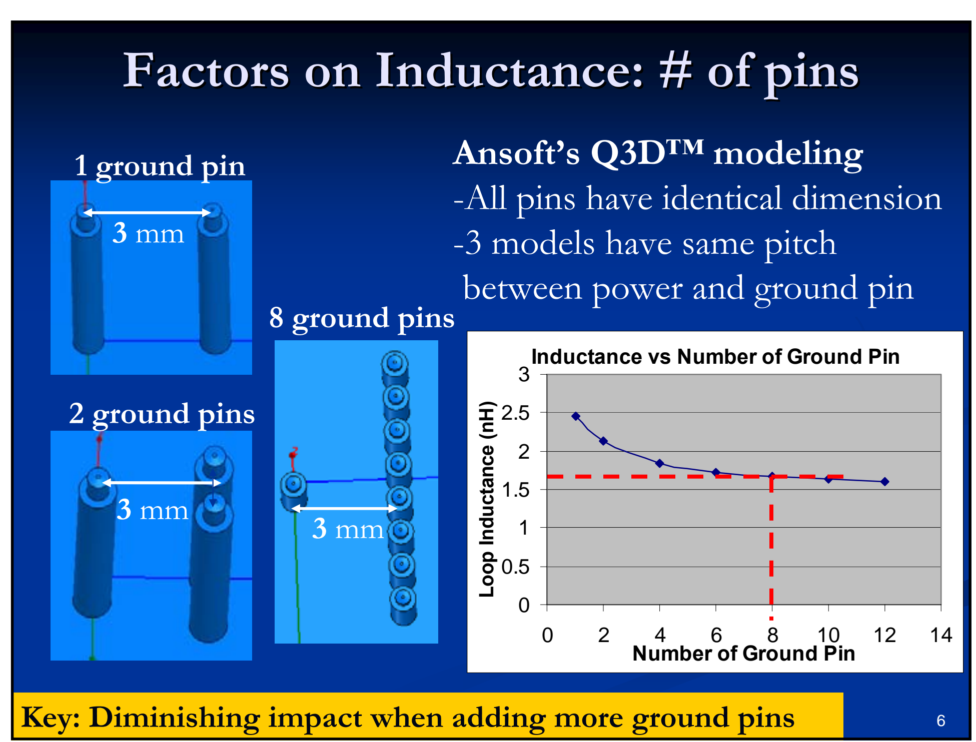
Total inductance induced when a complete loop of current path is formed.

$$L_{LOOP} = L_{SELF1} + L_{SELF2} - 2(L_{MUTUAL})$$

4

Paper #3


Factors on Inductance: Pitch
Model 1
2.3 mm
Pin A
Pin B
Model 2
3.0 mm
Pin A
Pin B
Model 1 (pitch 2.3 mm)
Model 2 (3.0 mm)
Partial Self Inductance
1.31 nH
1.31 nH
Mutual Inductance
0.43 nH
0.34 nH
Loop Inductance
1.75 nH
1.93 nH
Ansoft's Q3D™ Modeling Result
$L_{LOOP} = L_{SELF1} + L_{SELF2} - 2(L_{MUTUAL})$
Key : Loop inductance depends on pitch
5


Factors on Inductance: # of pins
1 ground pin
3 mm
2 ground pins
3 mm
8 ground pins
3 mm
Ansoft's Q3D™ modeling
-All pins have identical dimension
-3 models have same pitch
between power and ground pin
Inductance vs Number of Ground Pin
Loop Inductance (nH)
Number of Ground Pin
0
0.5
1
1.5
2
2.5
3
0
2
4
6
8
10
12
14
Key: Diminishing impact when adding more ground pins
6

Model usage

- 3D electrical modeling tools are good to quickly understand what happens when you change a given attribute

  … BUT …
- Time must be spent to validate key models with some form of measurement
- Complex models require finesse to utilize
  1) Simplify attributes when possible (cylinder for pin), or
  2) Model pieces of power path and stitch together
     - Even "small" QFN too complex for 3D elect. modeling

7

Model Stitching

- Like almost any modeling software, 3D electrical modeling can be broken into smaller pieces

Center Ground Pad

Power pin Ground pin

Steps:

1: Parse the package into 3D friendly size blocks
2: Model each block only focusing on power and ground pins
3: Produce a inductance per block and summate for total impact

8

Objectives

- Introduction of Pin Inductance Characteristics
- Discuss Inductance measurement techniques with and without fixture.
- Summary

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Measurement Flow

Decide pitch to be measured

↓

Setup measurement's equipment

↓

Post Process measured result to extract inductance

Equipment List:

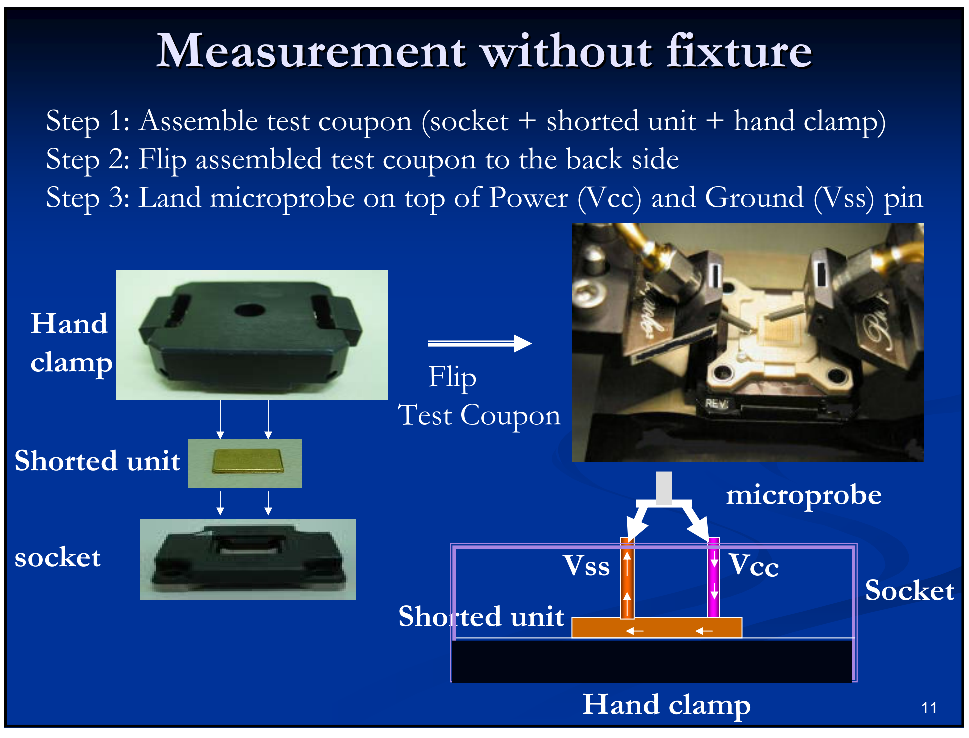
Network analyzer, Probe Station, Probe arm, Microprobe, Calibration Substrate.

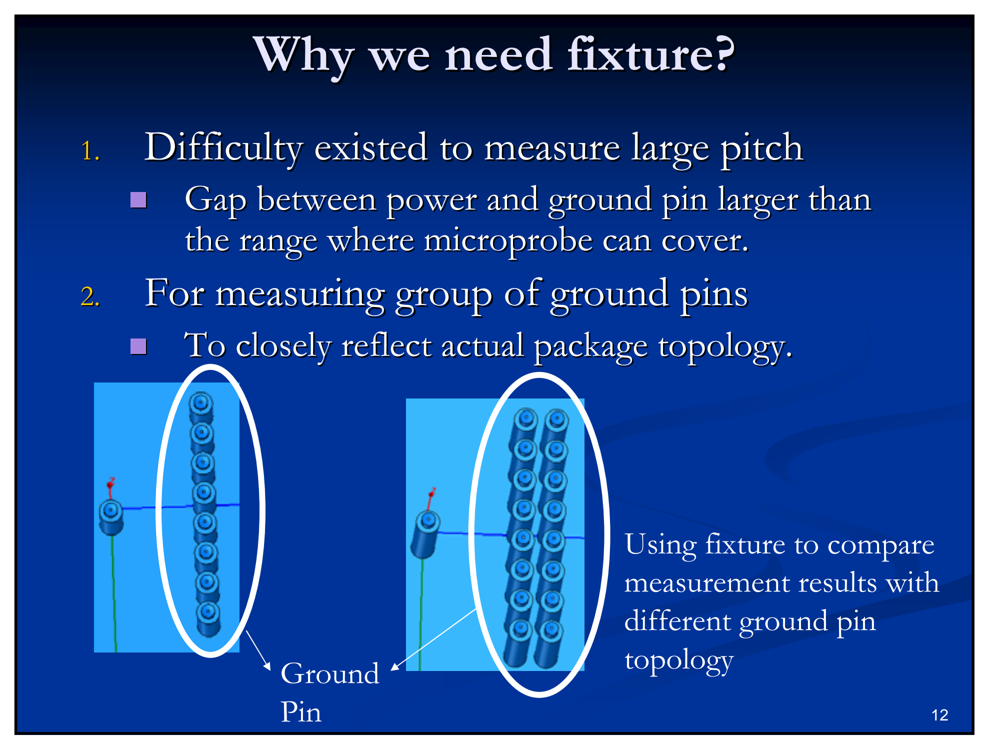
Measurement Steps:

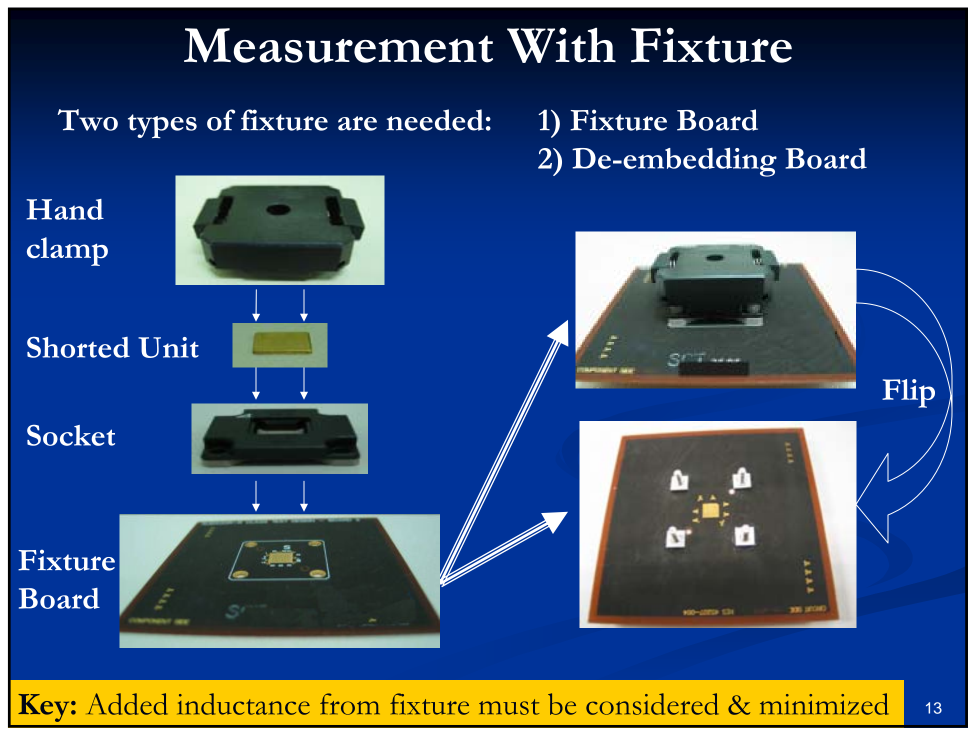
1. Attach appropriate microprobe to probe arm
2. Connect Network Analyzer to microprobe by coaxial cable
3. Calibrate microprobe with substrate.
4. Short Power and ground pin with shorted unit.
5. Start measurement on socket.

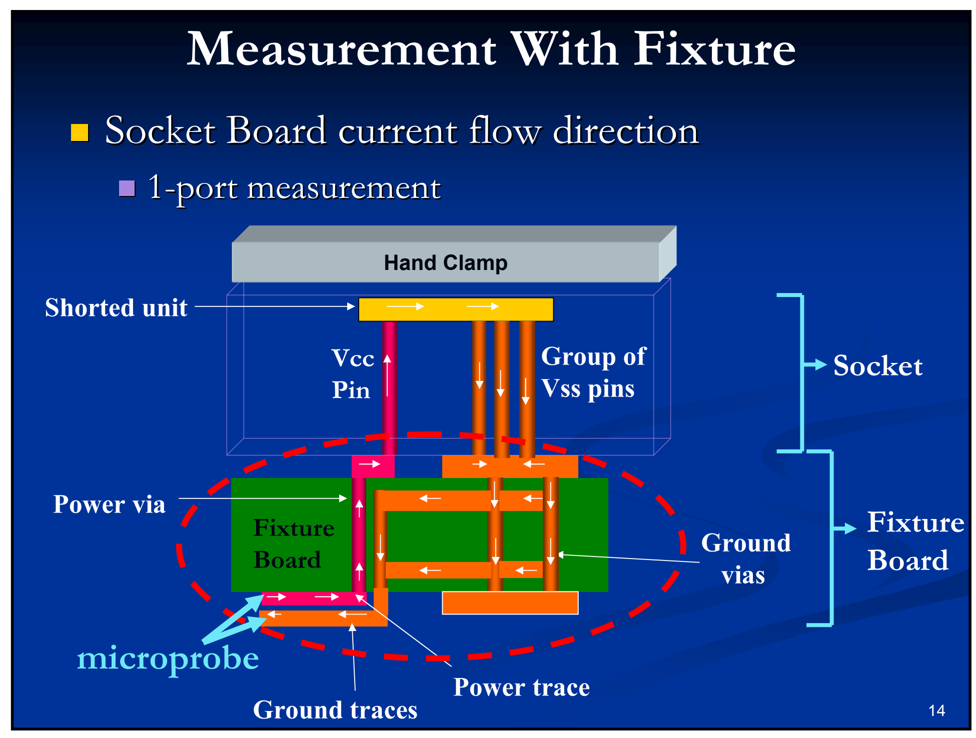
Note: Measurement repeatability was necessary to ensure result's consistency

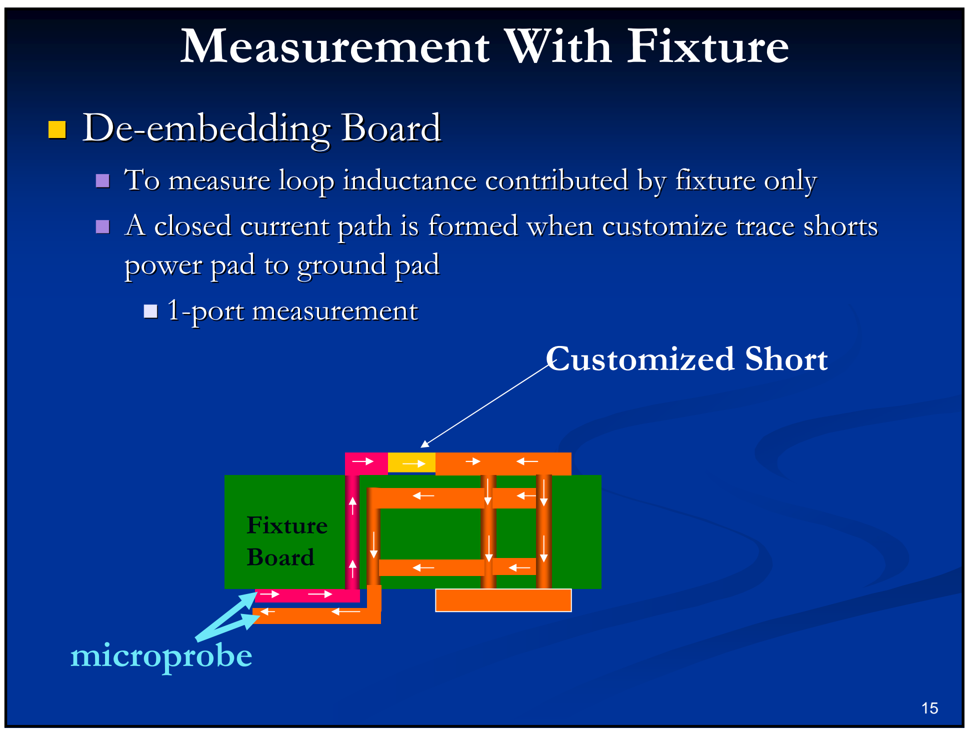
10

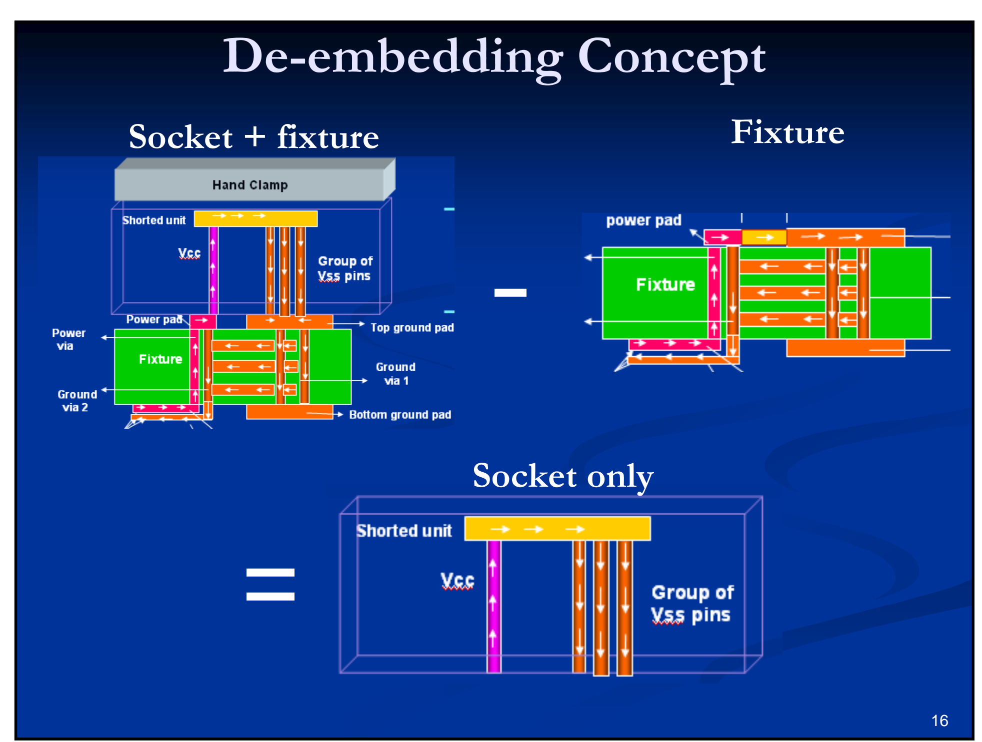

Measurement without fixture
Step 1: Assemble test coupon (socket + shorted unit + hand clamp)
Step 2: Flip assembled test coupon to the back side
Step 3: Land microprobe on top of Power (Vcc) and Ground (Vss) pin
Hand clamp
Shorted unit
socket
Flip
Test Coupon
microprobe
Vss
Vcc
Socket
Shorted unit
Hand clamp
11

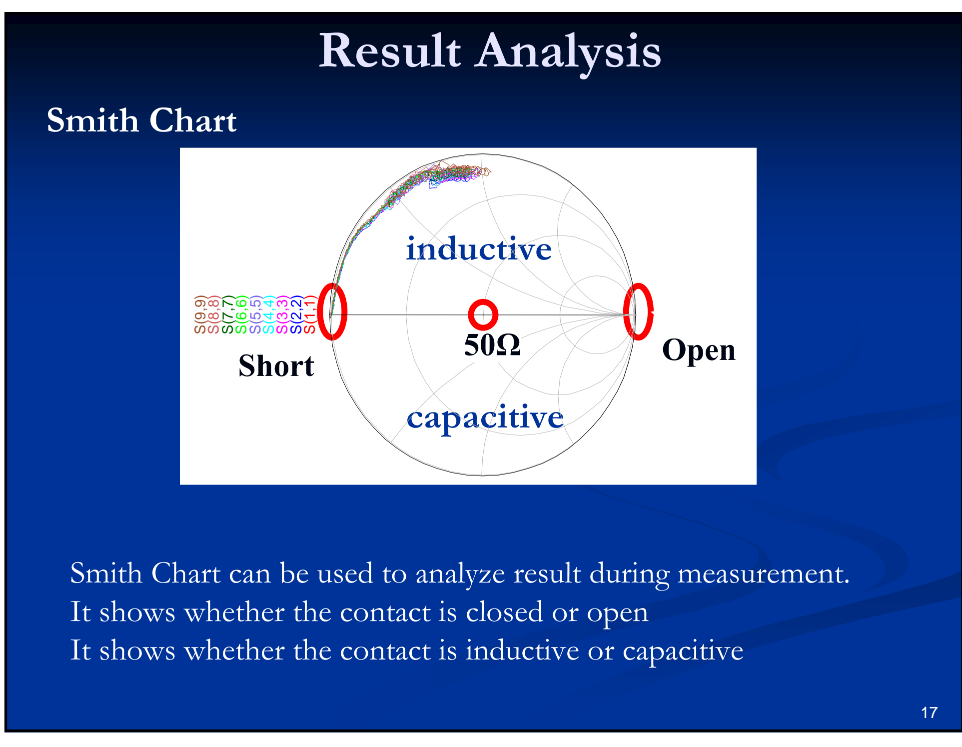

Why we need fixture?
1. Difficulty existed to measure large pitch
Gap between power and ground pin larger than the range where microprobe can cover.
2. For measuring group of ground pins
To closely reflect actual package topology.
Ground Pin
Using fixture to compare measurement results with different ground pin topology
12

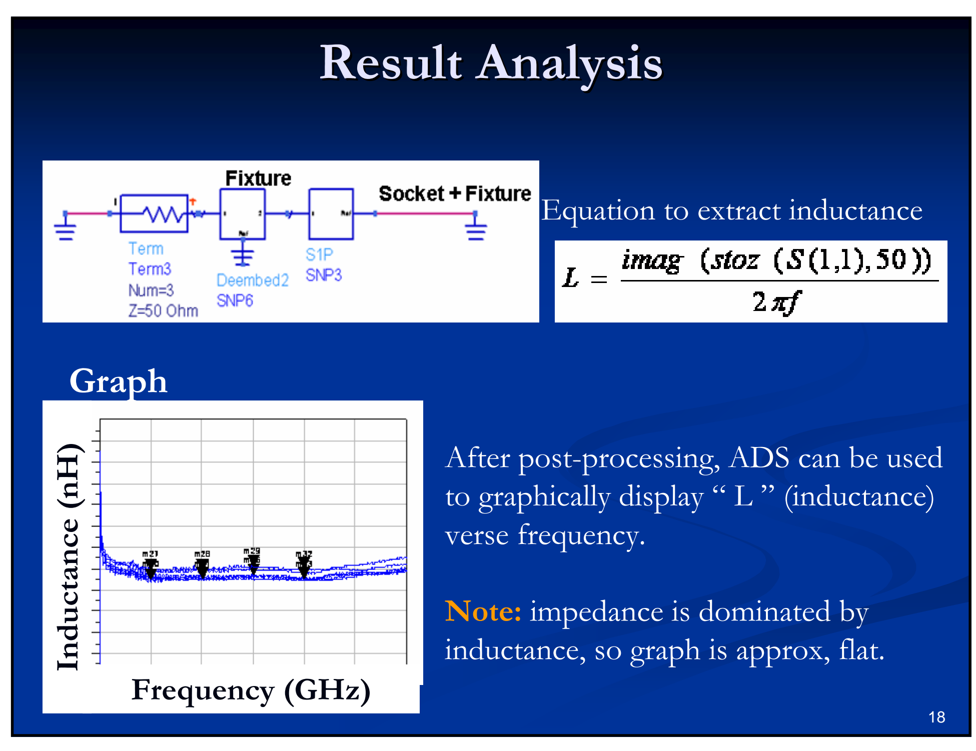

Measurement With Fixture
Two types of fixture are needed:
1) Fixture Board
2) De-embedding Board
Hand clamp
Shorted Unit
Socket
Fixture Board
Flip
Key: Added inductance from fixture must be considered & minimized
13


Measurement With Fixture
Socket Board current flow direction
1-port measurement
Hand Clamp
Shorted unit
Vcc Pin
Group of Vss pins
Socket
Power via
Fixture Board
Ground vias
Fixture Board
microprobe
Power trace
Ground traces
14


Measurement With Fixture
De-embedding Board
To measure loop inductance contributed by fixture only
A closed current path is formed when customize trace shorts power pad to ground pad
1-port measurement
Customized Short
Fixture Board
microprobe
15


De-embedding Concept
Socket + fixture
Fixture
Hand Clamp
Shorted unit
Vcc
Group of Vss pins
Power pad
Power via
Fixture
Top ground pad
Ground via 1
Ground via 2
Bottom ground pad
power pad
Fixture
-
Socket only
=
Shorted unit
Vcc
Group of Vss pins
16


Result Analysis
Smith Chart
inductive
S(9,9)
S(8,8)
S(7,7)
S(6,6)
S(5,5)
S(4,4)
S(3,3)
S(2,2)
S(1,1)
Short
50Ω
Open
capacitive
Smith Chart can be used to analyze result during measurement.
It shows whether the contact is closed or open
It shows whether the contact is inductive or capacitive
17


Result Analysis
Fixture
Socket + Fixture
Term
Term3
Num=3
Z=50 Ohm
Deembed2
SNP6
S1P
SNP3
Equation to extract inductance
$L = \frac{imag\ (stoz\ (S(1,1), 50))}{2\pi f}$
Graph
Inductance (nH)
Frequency (GHz)
After post-processing, ADS can be used to graphically display " L " (inductance) verse frequency.
Note: impedance is dominated by inductance, so graph is approx, flat.
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Summary

- **Important to optimize total loop inductance even in low power RF DUTs**
  - Balance total pins to meet needs, not exceed
- **When measuring, only loop inductance can be directly measured**
- **When modeling, validate results with measurements and expect to**
- **Fixture can be built to overcome measurement limitations of wide pitch and group pins topology**
  - Extra effort required to remove impacts of the added fixture

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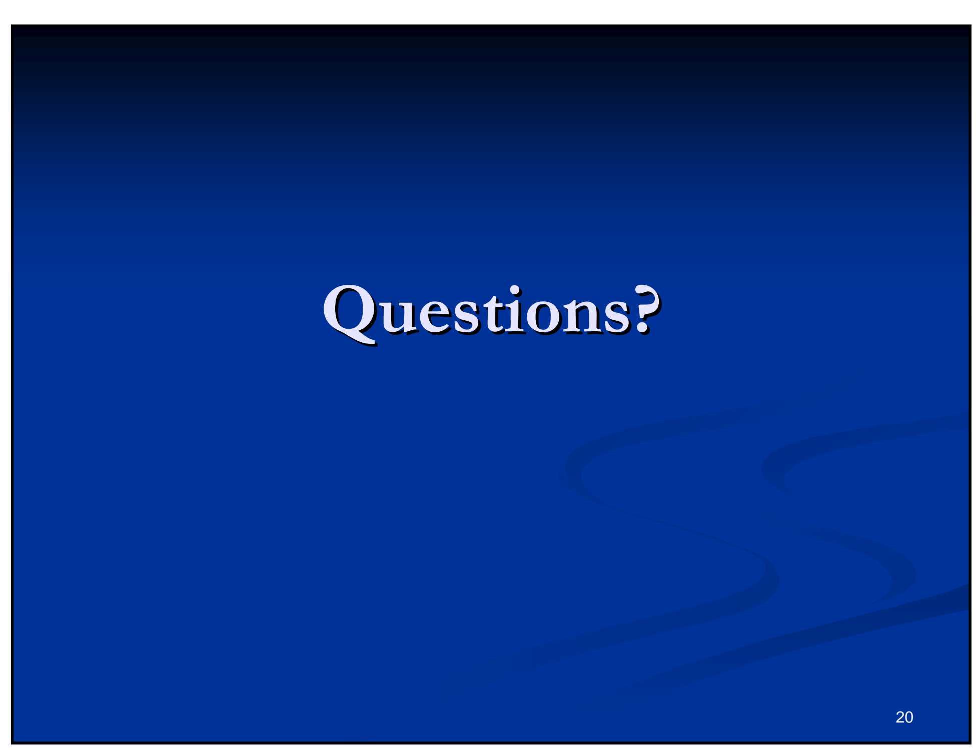

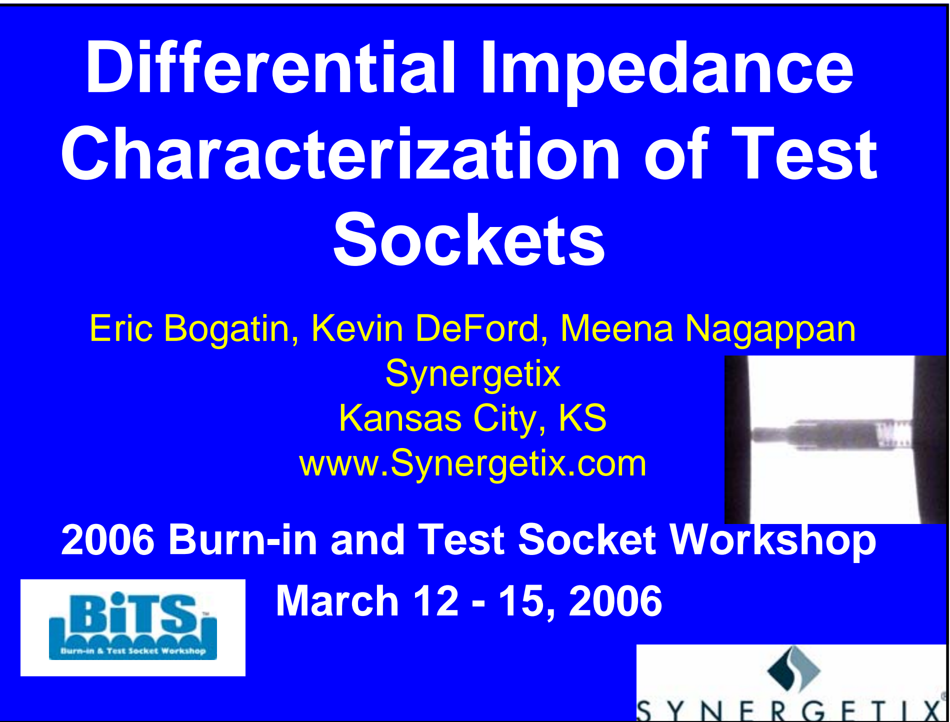

Agenda

- What's differential impedance
- What's characterization mean?
- The Synergetix Method
- Current results
- Future directions

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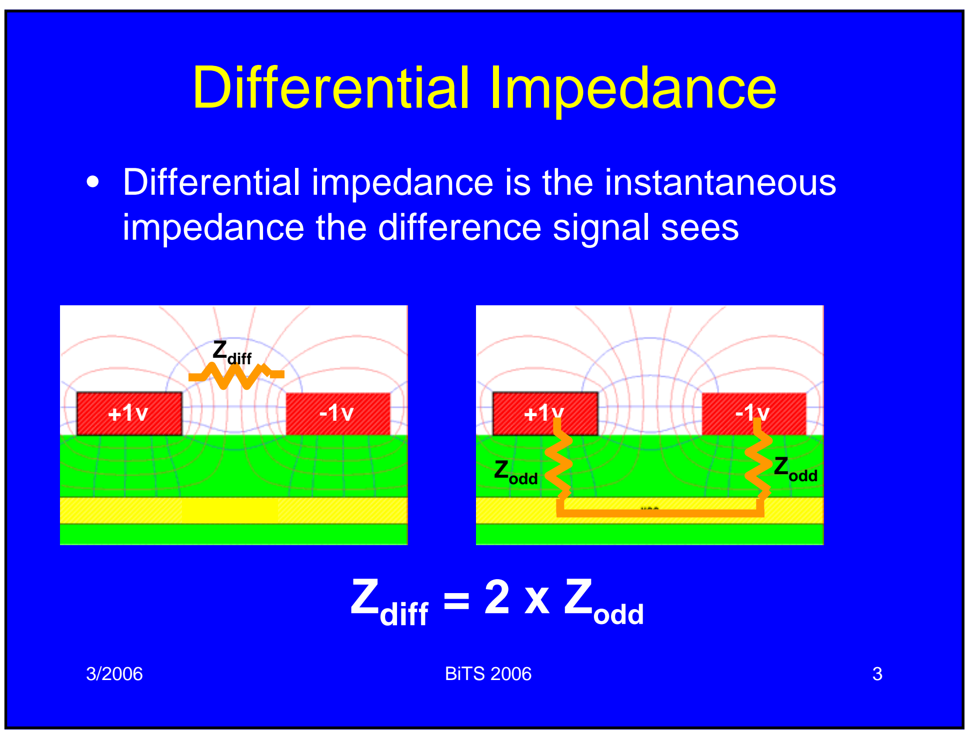
Differential Impedance
• Differential impedance is the instantaneous impedance the difference signal sees
Zdiff
+1v
-1v
+1v
-1v
Zodd
Zodd
Zdiff = 2 x Zodd
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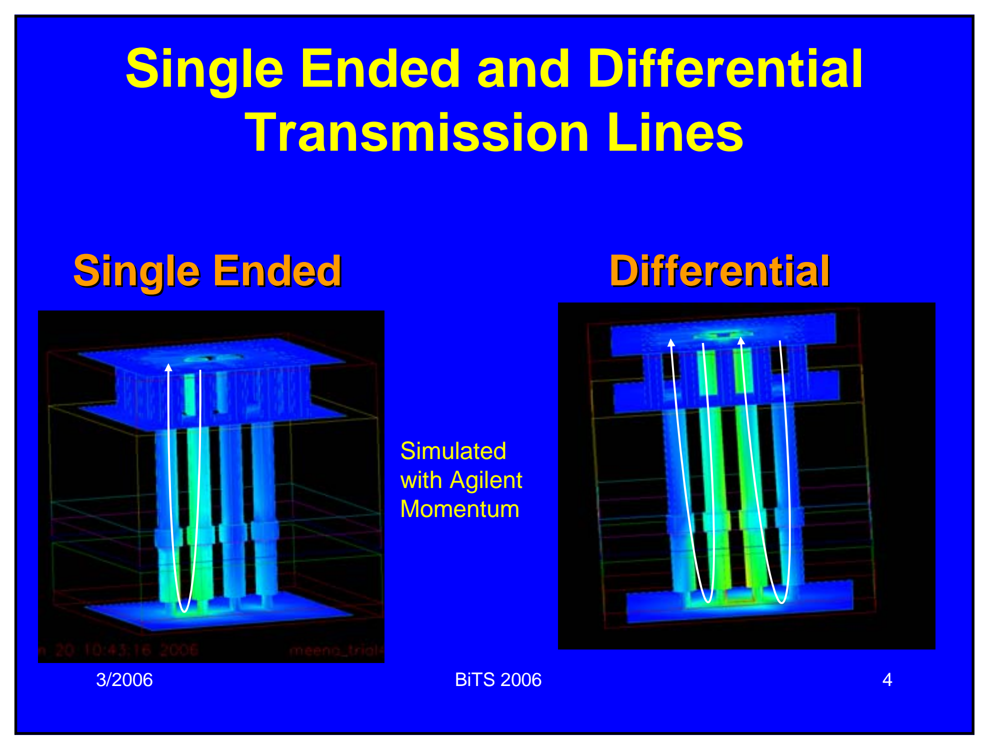
3


Single Ended and Differential Transmission Lines
Single Ended
Differential
Simulated with Agilent Momentum
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A Common Mis-Conception

"The return current of one line is carried by the other line."

When return currents overlap, second pin has the return current of the first pin	Signal to signal coupling >> signal to return coupling Return path not important	S S R
When return currents do not overlap, return current of each pin is in the return conductor	Signal to return coupling >> signal to signal coupling Return path critical	R S S R

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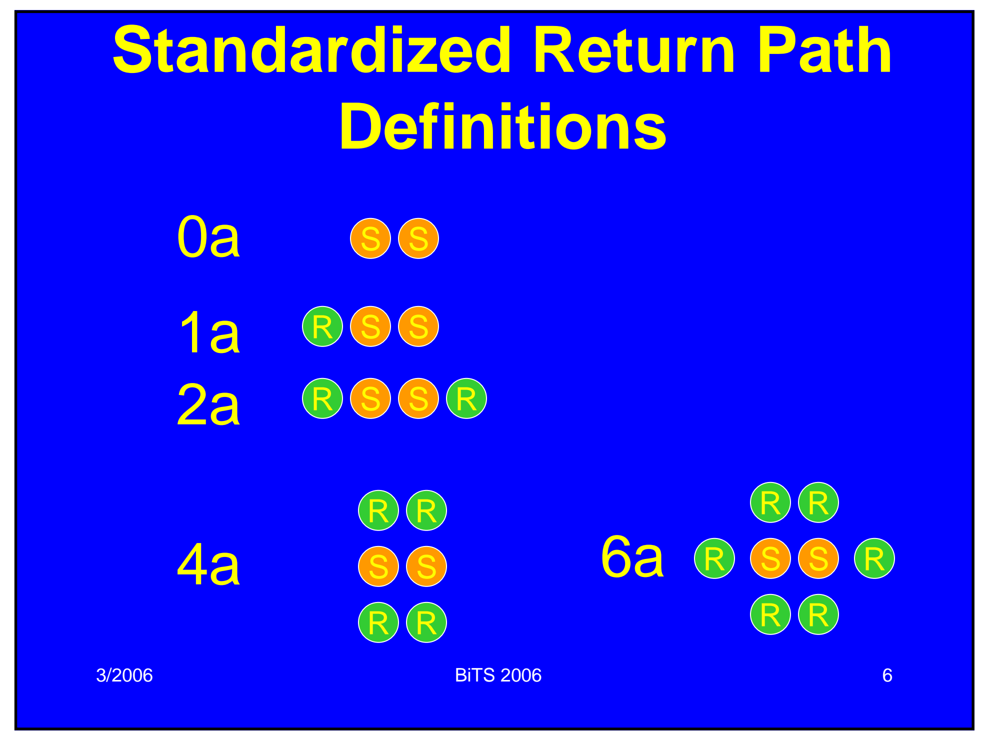
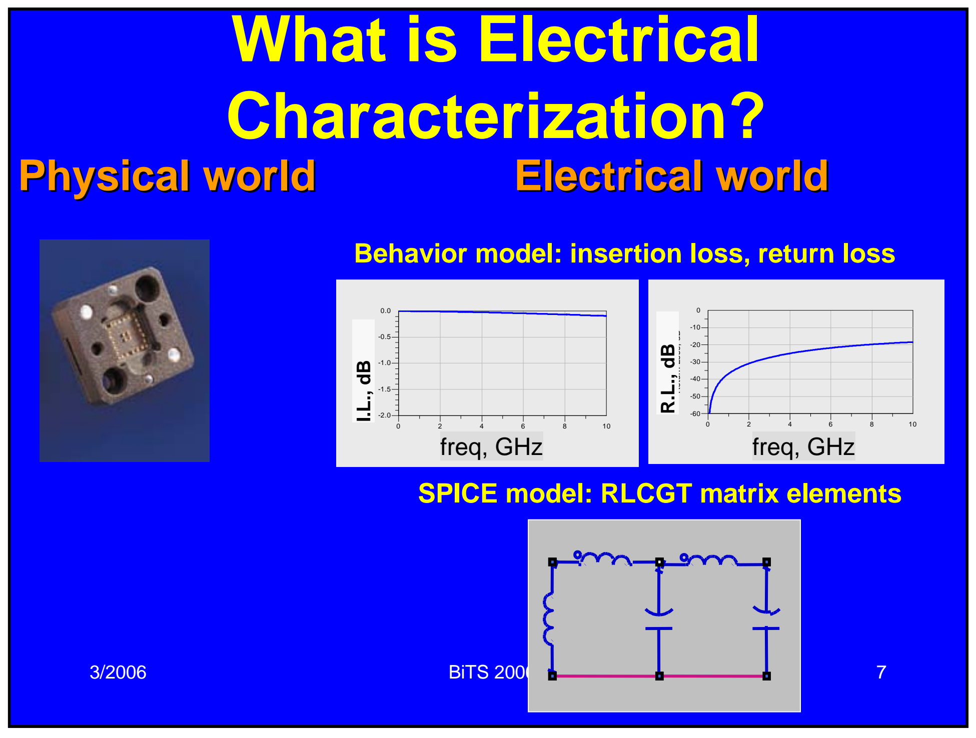
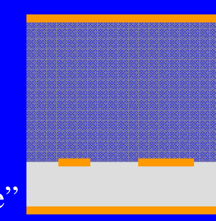




SPICE Topology Circuit Models for Ideal Differential Pairs

- Option 1: ideal, lossless differential pair
  - Zodd, Zeven, DKeven, DKodd, Length
- Option 2: ideal differential pair with skin depth limited conductor loss
- Option 3: ideal lossy model based on RLGC matrix elements
  - Includes dielectric loss, conductor loss, asymmetric impedance
  - Can be used to simulate all properties of a differential pair
  - Difficult to extract a “differential impedance”



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Synergetix Characterization Method Goals

- Simple, reproducible and generic for any probe configuration
- Unambiguously de-embed the fixturing
- Non-proprietary
- Circuit topology model with verified accuracy > 10 GHz
- Output a differential impedance that has meaning
- Provide differential insertion and return loss
- Use only 2 port VNA

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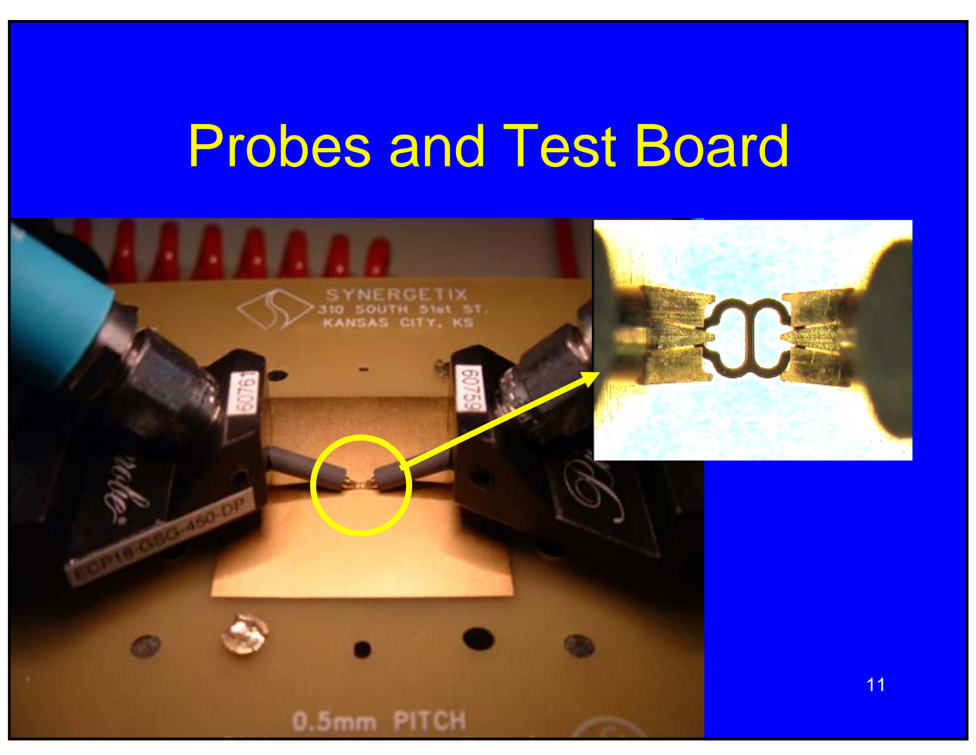
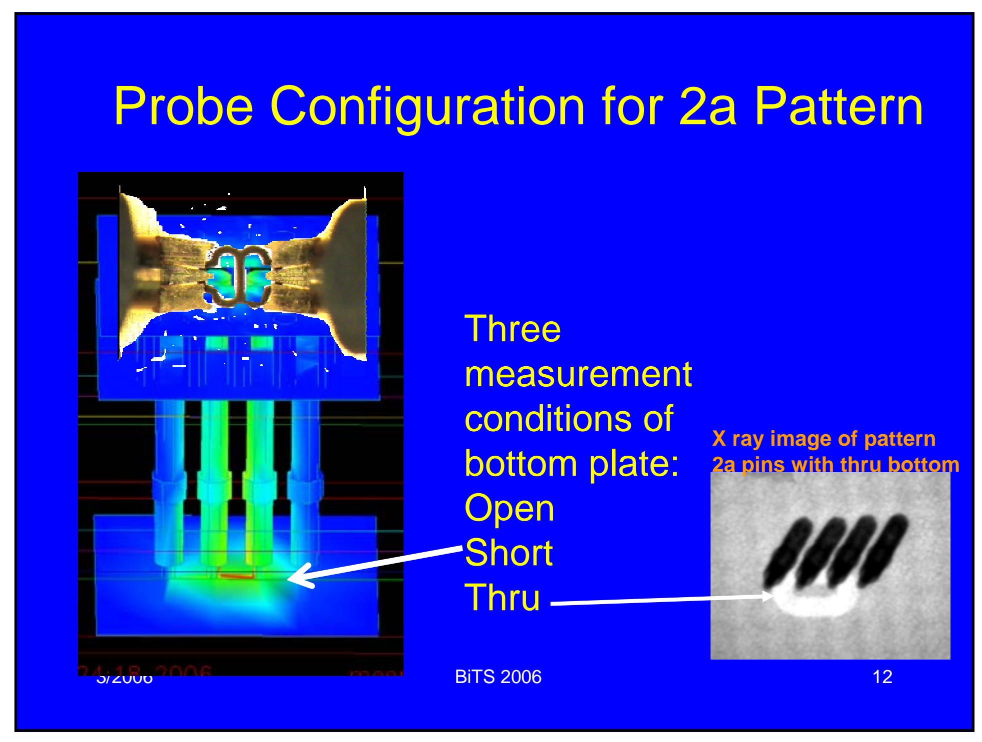
Synergetix System Configuration

- Agilent E8363B VNA
- Megaphase high bandwidth cables
- GGB industries pico probes
- Synergetix custom test board
- Synergetix custom rf test socket

10



Probes and Test Board
SYNERGETIX
310 SOUTH 51st ST.
KANSAS CITY, KS
60761
60759
0.5mm PITCH
11



Probe Configuration for 2a Pattern
Three measurement conditions of bottom plate:
Open
Short
Thru
X ray image of pattern 2a pins with thru bottom
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2 Port Differential Measurement Characterization Process

- Measure 2 port S parameters of
  - Fixture board: open, short, thru
  - Fixture + socket: open, short, thru
- Fit geophysical model terms to get agreement of simulated and measured 2 port S parameters
- Fit ideal differential pair model to geophysical model to get differential impedance
- Use model of socket (RLGC matrix values) to simulate differential insertion loss (Sdd21)

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ADS Geophysical Differential Model

fixture socket termination (thru)

Fit all parameters simultaneously for open, short, thru measurement

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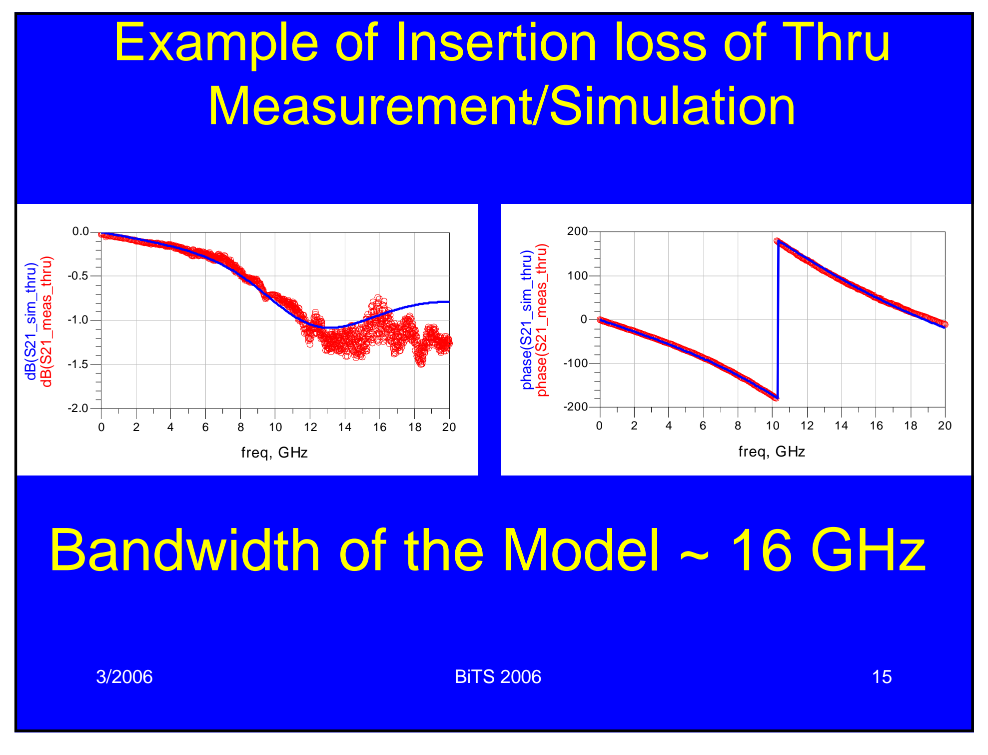
Example of Insertion loss of Thru Measurement/Simulation
dB(S21_sim_thru)
dB(S21_meas_thru)
freq, GHz
phase(S21_sim_thru)
phase(S21_meas_thru)
Bandwidth of the Model ~ 16 GHz
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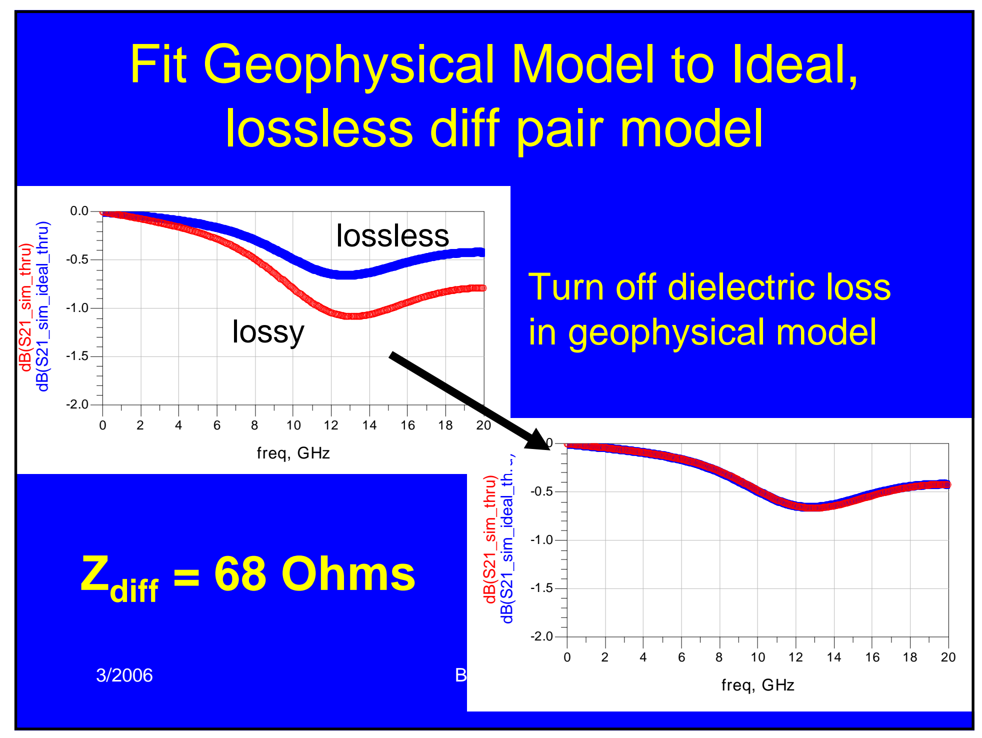
Fit Geophysical Model to Ideal, lossless diff pair model
lossless
lossy
dB(S21_sim_thru)
dB(S21_sim_ideal_thru)
freq, GHz
Turn off dielectric loss in geophysical model
Z_diff = 68 Ohms
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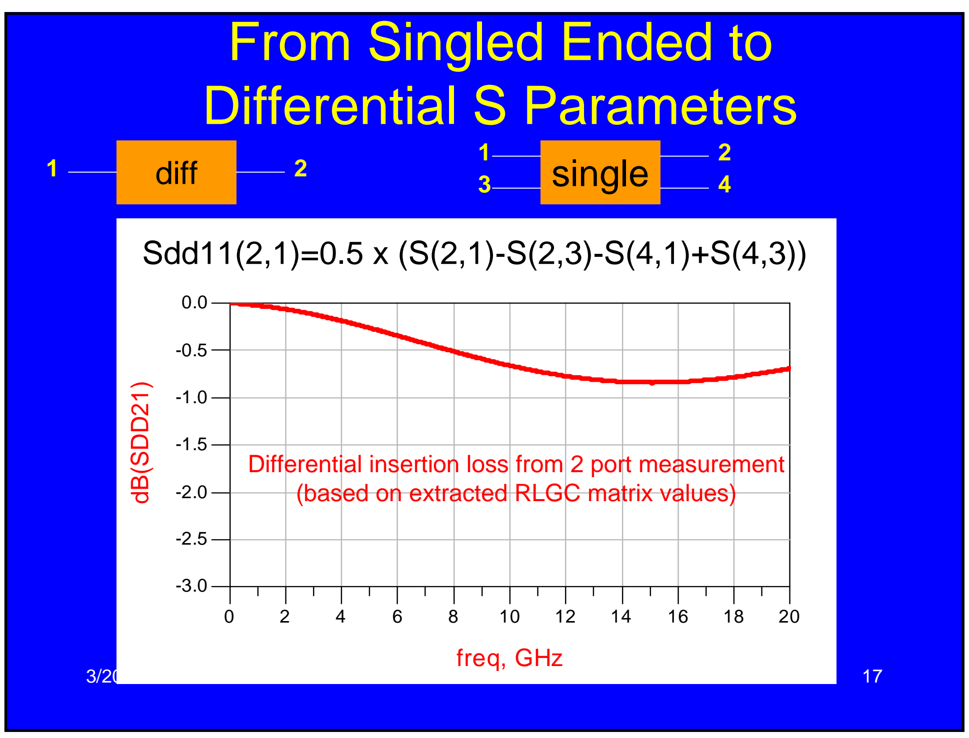

Conclusions

- Synergetix Characterization Method:
  - Simple, robust, reproducible
  - Non-proprietary
  - Accurate to > 10 GHz
  - Minimal and controllable artifacts
  - Output is SPICE compatible model
  - Direct measurement of model bandwidth
  - Accurate simulation of differential insertion loss
- Next step is match Agilent Momentum full wave simulation with measurement and use full wave simulation as analysis tool

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