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Keynote Address

"Test And Burn-in: The World Beyond Scaling"

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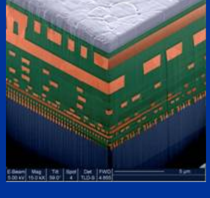

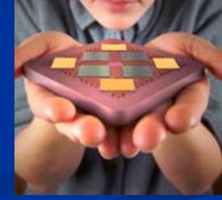

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Beyond Scaling….

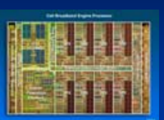
- Scaling has driven the industry for the past 40+ years
- Classical Scaling is dead….Now what?
- What does it mean to Test and Burn In ?

Beyond Scaling does not mean…

- Chips are not going to keep getting faster
- The performance of chips is no longer going to increase dramatically
- Reducing photolithography groundrules doesn’t matter
- Moore’s Law is dead !!

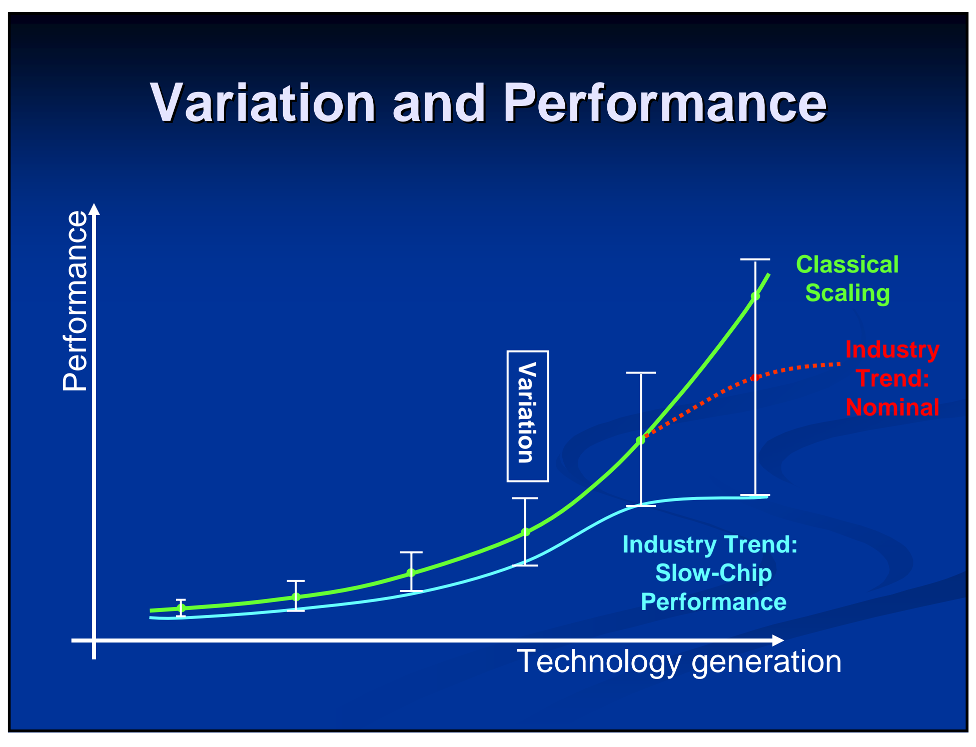
Beyond Scaling does mean….

- Architecture and system design will be the primary forces driving performance increases…not just clock frequency

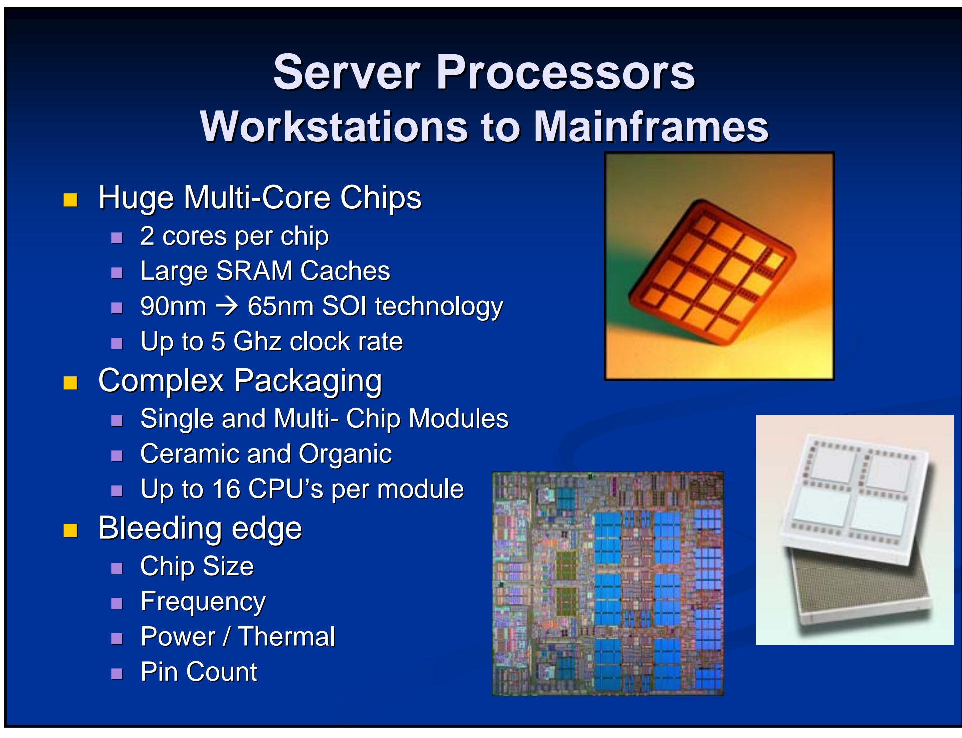


- New materials and processes will drive chip performance as much or more than photolithography groundrules

- Design and process interaction is increasing and increasingly hard to model and control
- Test and packaging complexity is increasing
- Economic challenges will be greater than ever


Variation and Performance
Performance
Classical Scaling
Industry Trend: Nominal
Variation
Industry Trend: Slow-Chip Performance
Technology generation

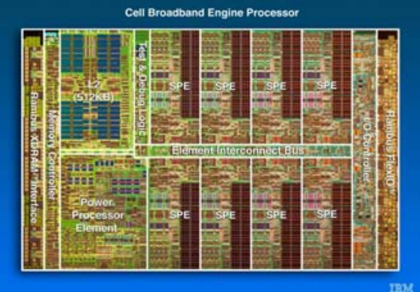
A Brief Glimpse into the World of IBM Technology
Server processors
Game Processors
ASIC / SOC
RF / Mixed Signal


Server Processors
Workstations to Mainframes
Huge Multi-Core Chips
2 cores per chip
Large SRAM Caches
90nm → 65nm SOI technology
Up to 5 Ghz clock rate
Complex Packaging
Single and Multi- Chip Modules
Ceramic and Organic
Up to 16 CPU's per module
Bleeding edge
Chip Size
Frequency
Power / Thermal
Pin Count

Game Processors
"A Supercomputer in your Living Room"
Not quite so Huge Multi-Core Chips
Up to 9 cores per chip
90nm → 65 nm SOI technology
Organic Packaging
Single Chip PBGA
Lidded and unlidded modules
Bleeding edge
Frequency
Power / Thermal
I/O
Consumer Market Cost Pressures
PlayStation
XBOX 360
Nintendo

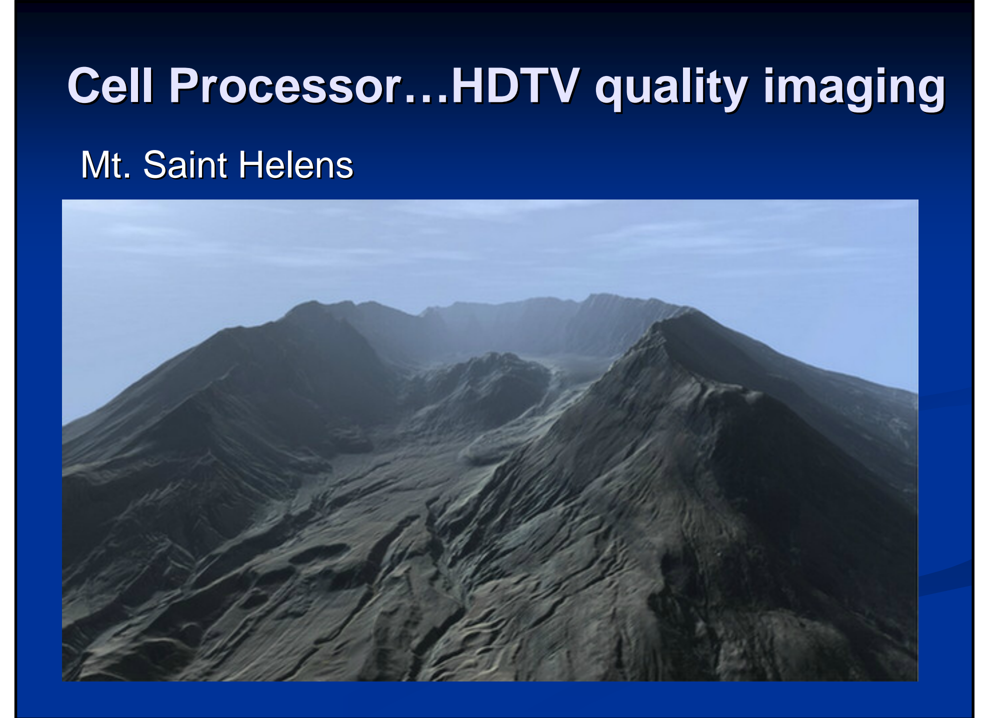
Cell Processor aka "Broadband Engine"

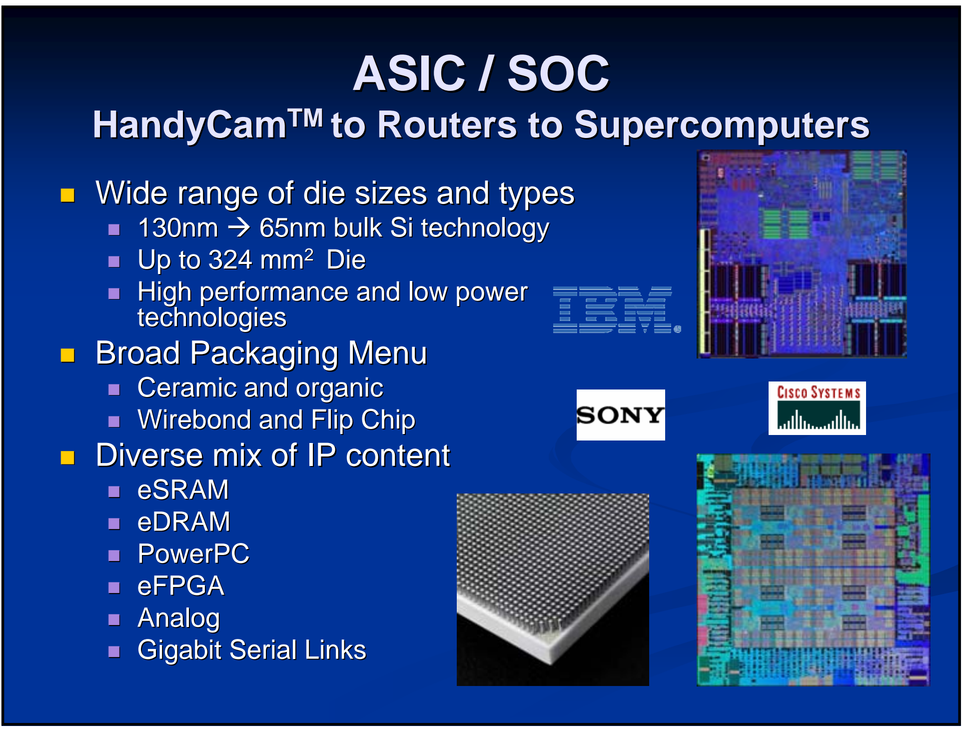
- Next Generation Power Processor for Gaming, Digital Home Entertainment, Defense, Medical Imaging and….
  - 64 bit Supercomputer on a Chip
  - 9 Processor Cores
  - 235 mm^2 chip
  - 42.5 mm Flip chip PBGA
  - >1200 pins / 486 IO
  - 3-4 Ghz Clock rate
  - 512KB L2 memory



Cell Processor…HDTV quality imaging

Mt. Saint Helens




ASIC / SOC
HandyCam™ to Routers to Supercomputers
Wide range of die sizes and types
130nm → 65nm bulk Si technology
Up to 324 mm² Die
High performance and low power technologies
Broad Packaging Menu
Ceramic and organic
Wirebond and Flip Chip
Diverse mix of IP content
eSRAM
eDRAM
PowerPC
eFPGA
Analog
Gigabit Serial Links
IBM
SONY
Cisco Systems

RF / Mixed Signal
"The World of Wireless"
Less aggressive groundrules…smaller die
0.5u to 90nm SiGe and RF CMOS
Die sizes starting at <1 mm²
Generally Low pin count
Mix of packaging technologies
KGD
Chip stack PBGA
QFN, TQFP, SOIC
Wirebond and Flip Chip
Primarily a foundry business
Wireless Handsets
Wireless Basestation
WLAN
GPS
Automotive (Navigation)
Power
IBM SILICON GERMANIUM

Meanwhile back in "Test World"…

- Test Leadership in the 21st century
  - What does it mean?
  - Does it matter ?
- What does "Beyond Scaling" mean to Test ?
- Some of the more "interesting" challenges

Test Leadership…what does it mean ?

- Not getting in the way
  - New technologies and products
  - Test Cost
  - Yield
  - Quality
- Providing value add differentiation
  - Time to Market
  - Yield Learning rate
  - Cost of Test
  - Quality and Reliability

Test Leadership…does it matter ?

- Can’t be a technology leader without it
- Key competitive weapon
  - Time to market
  - Quality and reliability
- Key profitability lever
  - Yield
  - Yield Learning rate
  - Test Cost

“Beyond Scaling”…some key Trends

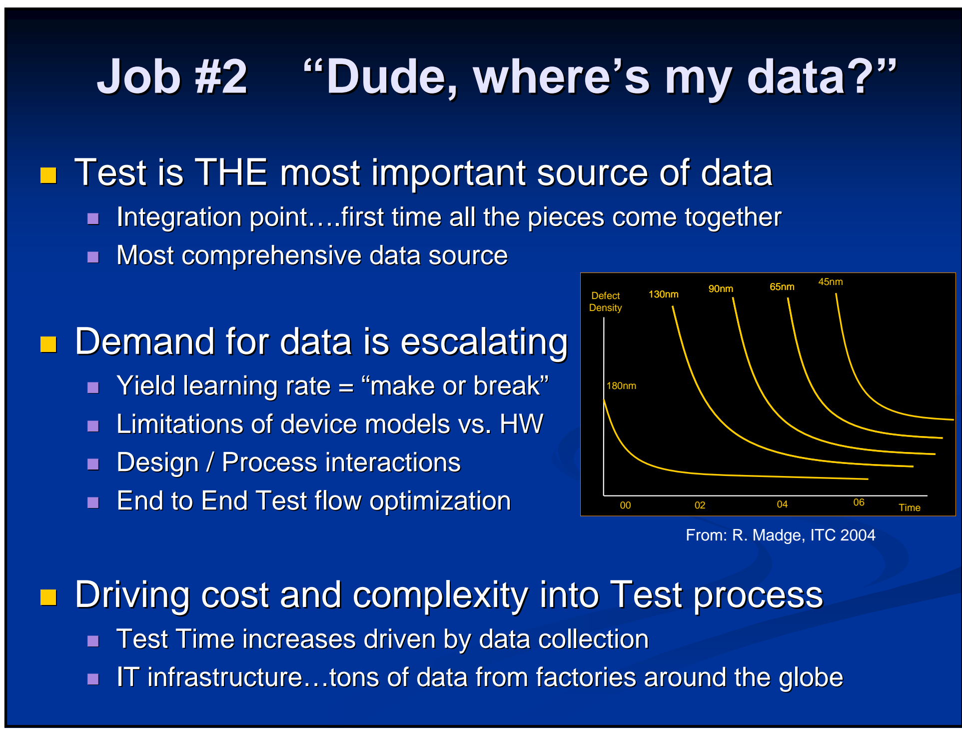
- **Yield Learning rate critical to business success**
- **Power / Thermal becoming a primary constraint**
- **Most of the Test function moving on die**
- **Design/process marginalities and systemic “defects” vs. random defects**
- **Many flavors of Good die…customization at Test**
- **SOC/SIP…integration of heterogeneous function**

What does all this mean to Test?

- The Role of Test is changing
- The business criticality of Test is increasing
- The leverage points are moving away from our historical "core" of equipment and Test programs
- The complexity of Test is increasing
  - Difficult to scale cost at the same rate as fab

The Changing Role of Test

- Job #1 = Sort Good from Bad
- Job #2 = Data Feedback to Design and Fab
- Job #3 = Value Added Product Transformation

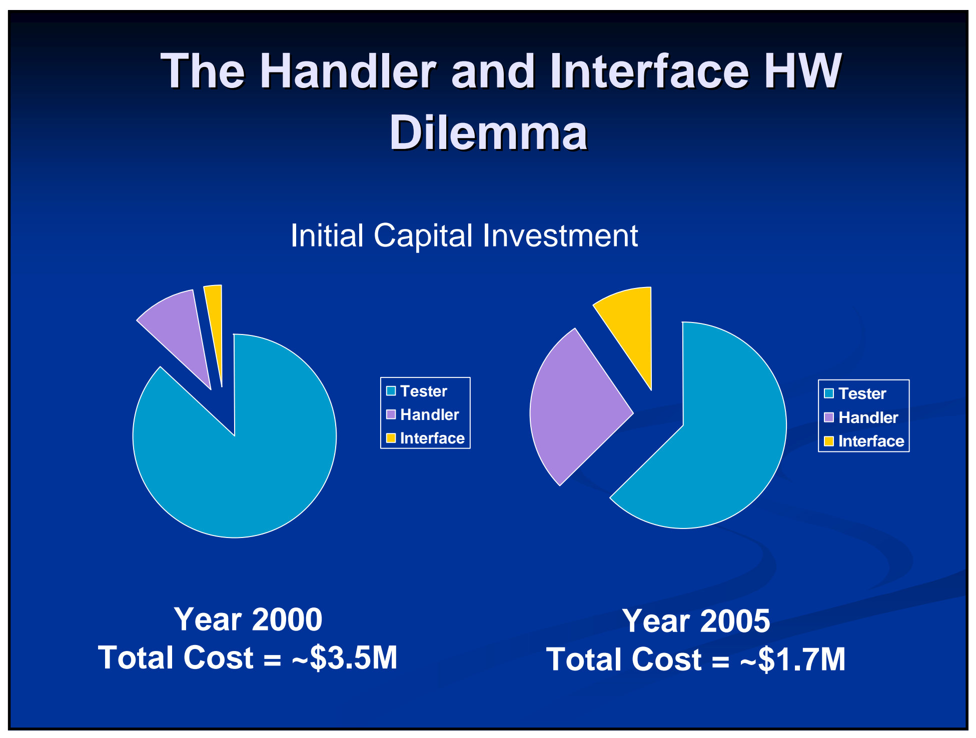


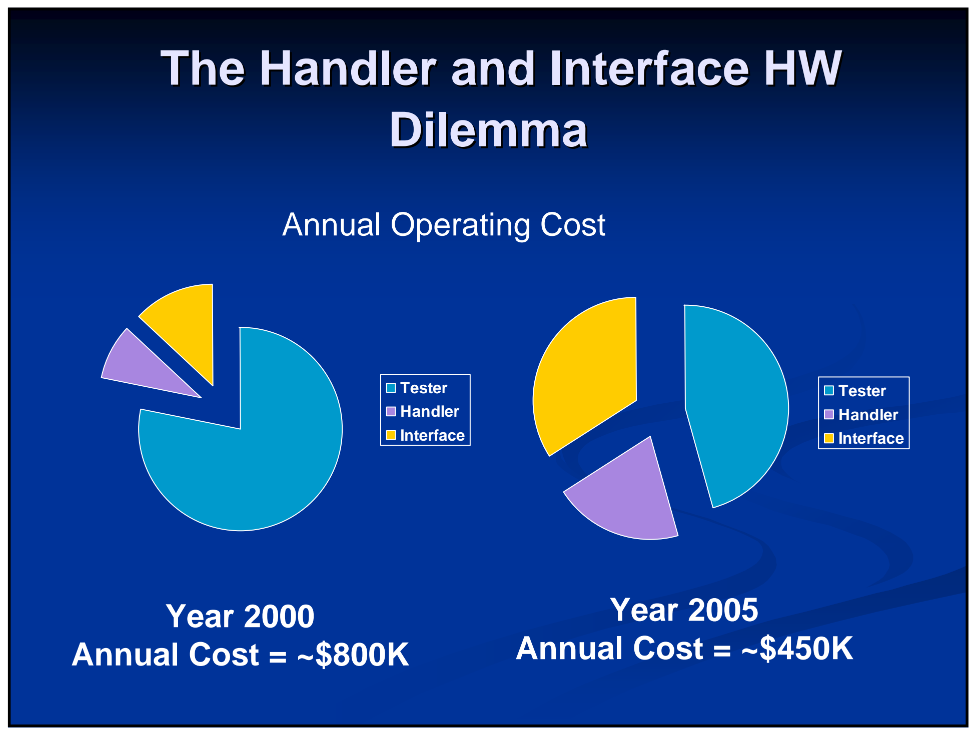
A few other "interesting" challenges

- "Collateral damage"…the silent killer
- "The SOC Fallacy"
- The Handler and Interface HW Dilemma
- The Power Problem

"Collateral Damage"

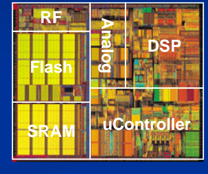
- Test process yield loss
  - Test equipment inaccuracies
    - Electrical, mechanical, thermal
  - Test process yield loss
- The quality vs. yield tradeoff
  - Overtesting to guarantee DPM levels
  - Overtesting at probe to protect package test yields
  - Difficulty in discriminating goods from bads
  - Differences between Test and Application conditions
  - Reliability screens and Burn in



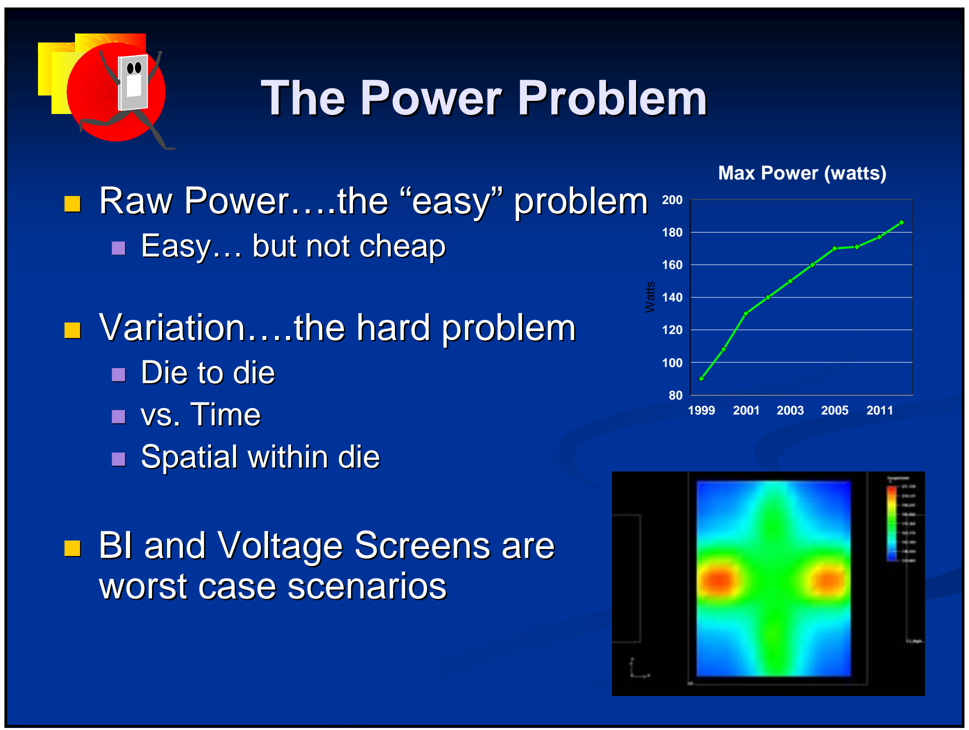


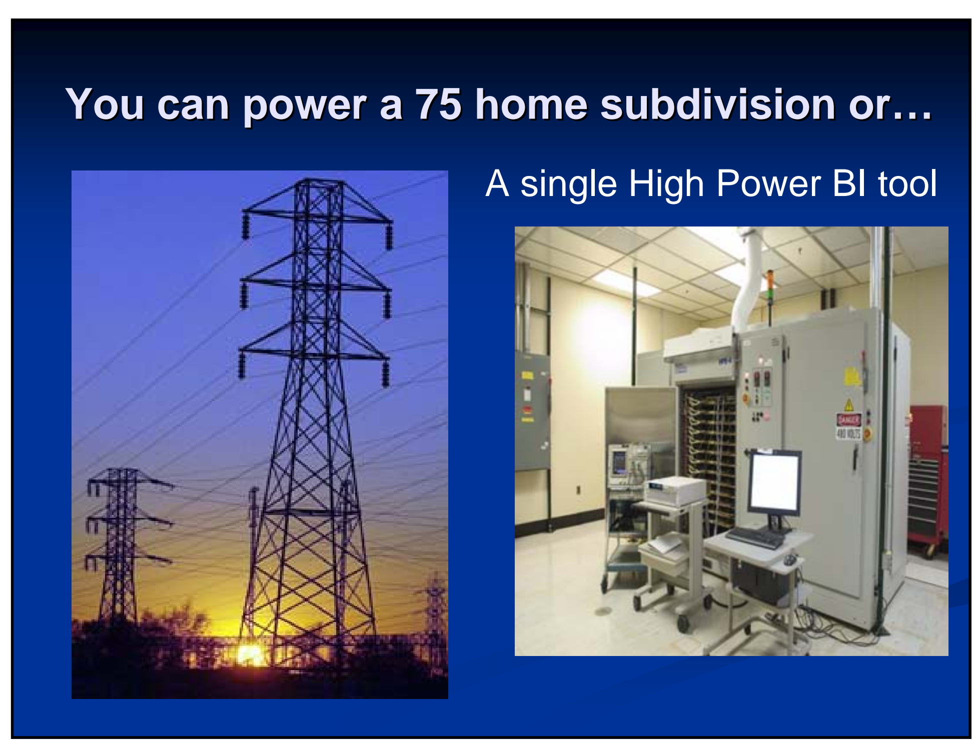
"The SOC Fallacy"

- Technically Feasible vs. Economically Rational
- The Challenge: Cost
  - Heterogeneous function in a single die or package
  - Divergent and often conflicting Test Methods



- SIP addresses the Die and Wafer Test cost problems
- SIP generally doesn't solve the package Test problem
  - "SOC Testers" often suffer from the same fallacy as SOC die
  - DFT and multiple insertions can mitigate the problem but don't solve it
  - "Concurrent Test" sounds great but is very hard to implement
  - KGD can help…but only if KGD and assembly are REALLY GOOD


The Power Problem
Raw Power….the "easy" problem
Easy… but not cheap
Variation….the hard problem
Die to die
vs. Time
Spatial within die
BI and Voltage Screens are worst case scenarios
Max Power (watts)
Watts
200
180
160
140
120
100
80
1999
2001
2003
2005
2011


You can power a 75 home subdivision or…
A single High Power BI tool

In closing…

- There is a bright future ahead in Test
  - There is life after Scaling…lots of it !!!
  - Plenty of interesting technical and economic challenges
- We've become a "value added" process !!!!
- We all have our work cut out for us

Thanks for listening