Burn-in & Test Socket Workshop

ARCHIVE 2006

Hot Topics Session

A Trio Of Trends And Challenges

"Test Handling Challenges Associated With Socket Designs"
John Pollock — Aetrium Incorporated

"Optimization Of Interconnects"
Ho Peng Ching — Micron Semiconductor Asia

"Thermal Considerations In Testing Very High Performance Devices"
Thomas Di Stefano — Centipede Systems

Test Handling Challenges Associated with Socket Designs

2006 Burn-in and Test Socket Workshop

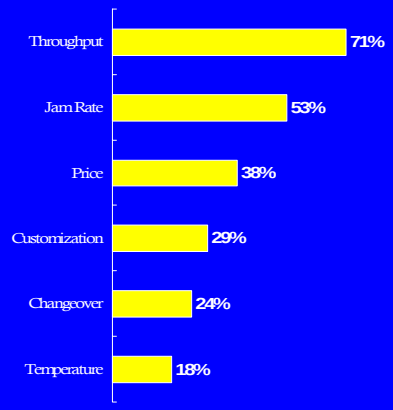
March 12 - 15, 2006

John Pollock
Vice President & General Manager
AETRIUM

Handler Purchase Criteria

End User Wants:

- Lowest Cost of Test
  - Dedicated High Volume
  - Flexible Small Lots
  - Quick Change Over
  - Tri-temperature

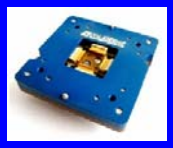


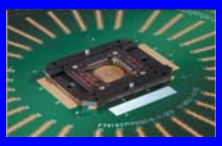
March 2006 Test Handling Challenges 2

Source: Booz Allen & Hamilton

Complete Solution

Semicon





BITS

ITC

March 2006 Test Handling Challenges 3

What's Driving the Socket Designs

- Increasing Device Performance
- Increasing Device Power (Thermal)
- Increasing Package Proliferation
- Increasing Package Assembly Methods
- Decreasing Geometries

March 2006 Test Handling Challenges 4

Device Performance Challenges

- Analog — Accuracy of Measurements
- Logic — Signal Speed & Thermal
- Mixed Signal — Speed & Accuracy
- Memory — Massively Parallel Contacts

March 2006 Test Handling Challenges 5

Handler Evolution

- Gravity
  - DIP, SOIC & QFN
- Pick & Place
  - QFP, PGA & BGA
- Turret
  - SOT
- Strip
  - SOIC & QFN
- Wafer
  - KGD

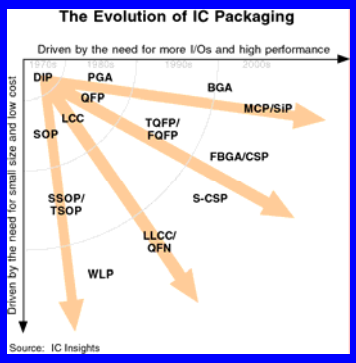




March 2006 Test Handling Challenges 6

Package Evolution

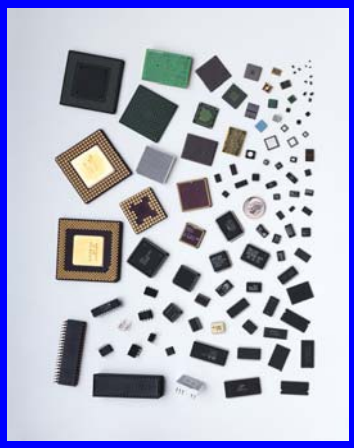
- Analog Devices
  - DIP, SOIC & QFN
- Logic, Memory & Mixed Signal
  - QFP, PGA & BGA
- Discrete
  - SOT



March 2006 Test Handling Challenges 7

Package Proliferation Challenges

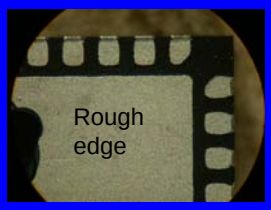
- Leaded
- Pads (Leadless)
- BGA
- Array
- Pitch
- Dimensional Tolerances

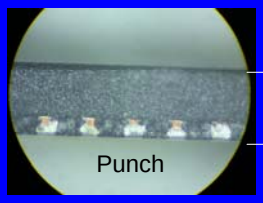


March 2006 Test Handling Challenges 8

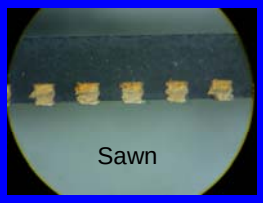
QFN Dimensional Tolerences

- Rough edges
  - Punch
  - Sawn
- Thickness





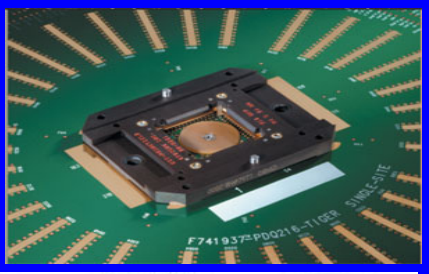
0.55, 0.75, 0.90 mm

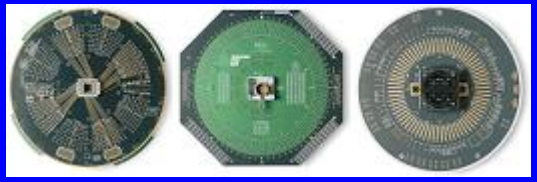


March 2006 Test Handling Challenges 9

Load Board Challenges

- Contactor Mounting
- Handler Alignment
- Multi Site
- Signal Conditioning

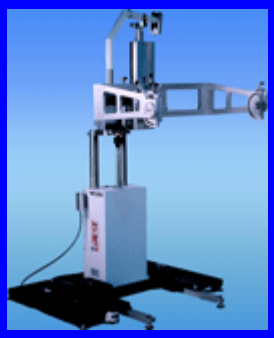




March 2006 Test Handling Challenges 10

Docking Challenges

- Direct Docking
- Cable Up Docking
- Dimensional Stack Ups
  - Socket
  - Load Board
  - Support Rings
  - Test Head Manipulators



March 2006 Test Handling Challenges 11

Tolerance Stack Ups

- X Direction
- Y Direction
- Z Direction
  - example

Tolerance Analysis - 5x5 MLF/QFN

COMPONENTS	Tolerance	Nominal	Feature
Plate:	0.0015	0.1975	
Leadbacker:	0.001	0.198	
Device:	0.0005	0.0341	Actual
	0.003	0.0354	Print
Socket	0.0008	0.039	Surface 1
	0.0008	0.031	Groove 1
	0.0002	0.027	Elastomer
	0.0005	0.017	Contact

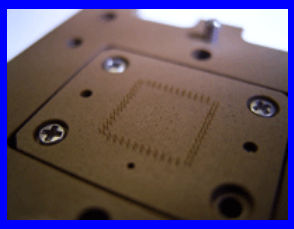
dimensions in inches

Nominal Tolerance:	Nominal Compression:	0.0086
Maximum Tolerance	Minimum Compression:	0.0033
Minimum Tolerance:	Maximum Compression:	0.0139

March 2006 Test Handling Challenges 12

Contacting Measurement Challenges

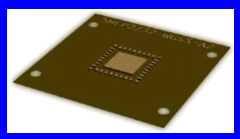
- Performance
- Lead Length
- Signal Conditioning
- Non Kelvin
- Kelvin

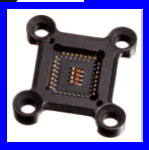


March 2006 Test Handling Challenges 13

Kelvin Contacting Challenges

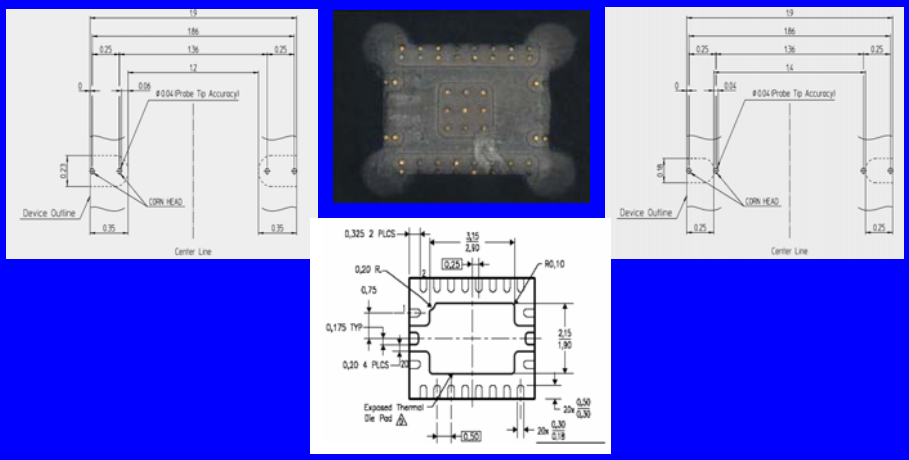
- Pogo Pins
  - Cleaning Issues
  - Shorter Life
- Wires (fingers)
  - Scrub
- Elastomers
  - Capacitance and Inductance





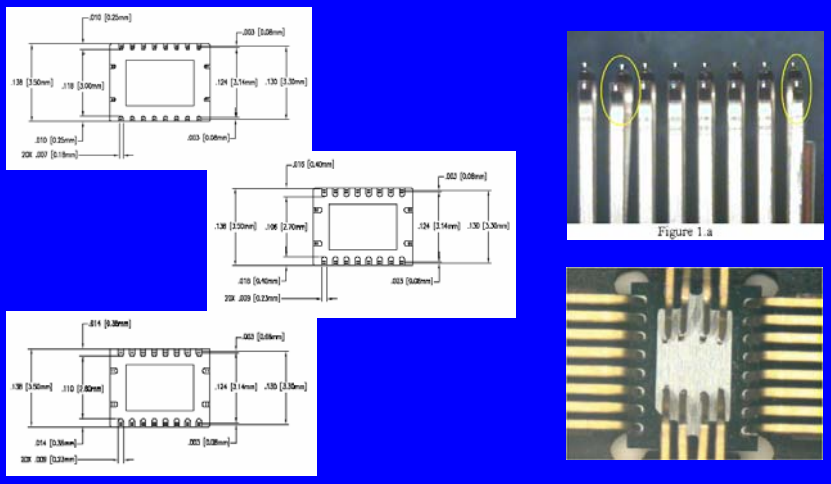
March 2006 Test Handling Challenges 14

Kelvin Pogo Pin Contacting



March 2006 Test Handling Challenges 15

Kelvin Wire Finger Contacting



March 2006 Test Handling Challenges 16

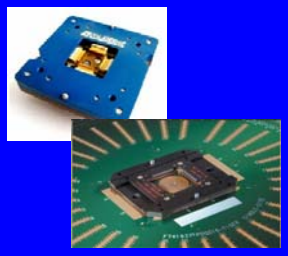
Thermal Challenges

- Temperature Range
  - +155°C to -55°C
- Convection vs Conduction
- Test Site Accuracy
  - ± 1°C or less
- Environmental Sealing
  - Frosting

March 2006 Test Handling Challenges 17

Going Forward

Can not lose sight of continuing to provide the most simple and cost effective total solution



Requires a joint effort

March 2006 Test Handling Challenges 18

Steps For Going Forward

- Propose Test Socket Committee
  - Define Best Practices
  - Members From
    - IDM
    - Handlers Manufacturers
    - Socket Manufacturers
    - Load Board Manufacturers
    - Tester Manufacturers

March 2006 Test Handling Challenges 19

Thank You

Questions?

Optimization of Interconnects

2006 Burn-in and Test Socket Workshop

March 12–15, 2006

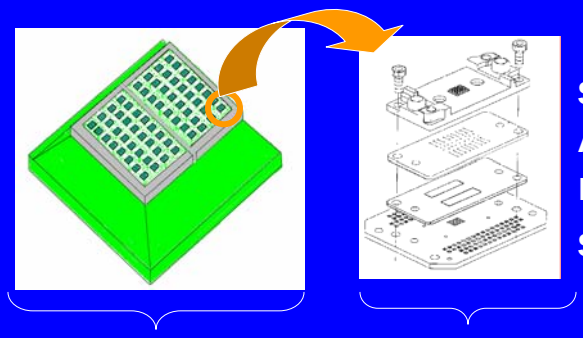
Ho Peng Ching
Micron Semiconductor Asia

Agenda

- Background
- Design Review
  - Board-to-Board Interposer Design
  - Signal-Gnd Via Structure
- System-Level Performance
- Conclusions
- References
- Acknowledgments

Background

- Recap of the Flexi-Interface Test Interface Fixture [1]



3/2006 3

Background

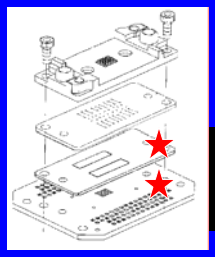
- Extracts from their conclusion
  - The concept was proven to be viable for device testing (for SDRAM). There is, however, still room for improvement on the interface between board-to-board.
  - The next challenge would be to prove the Flexi-interface concept for higher speed device testing (DDR2 and beyond).

3/2006 4

Background

What's next?

Extending the speed envelope of the current design by focusing on improving the electrical performance of the board-to-board interconnect.



Socket

Adaptor Board

Interconnect

Socket Board

3/2006 5

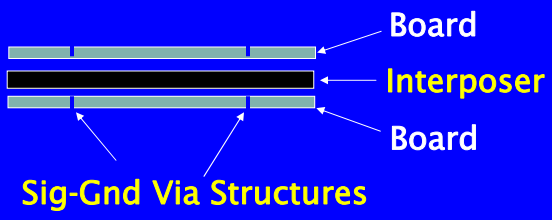
How ?

3/2006 6

Design Review

Area of Focus:

1. Board-to-Board Interposer
2. Signal-Gnd Via Structure



3/2006 7

Design Review

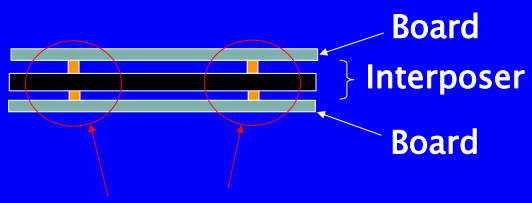
Let's begin with the

Board-to-Board Interposer

3/2006 8

Design Review
(Board-to-Board Interposer)

Current design shortfall:



Unshielded!

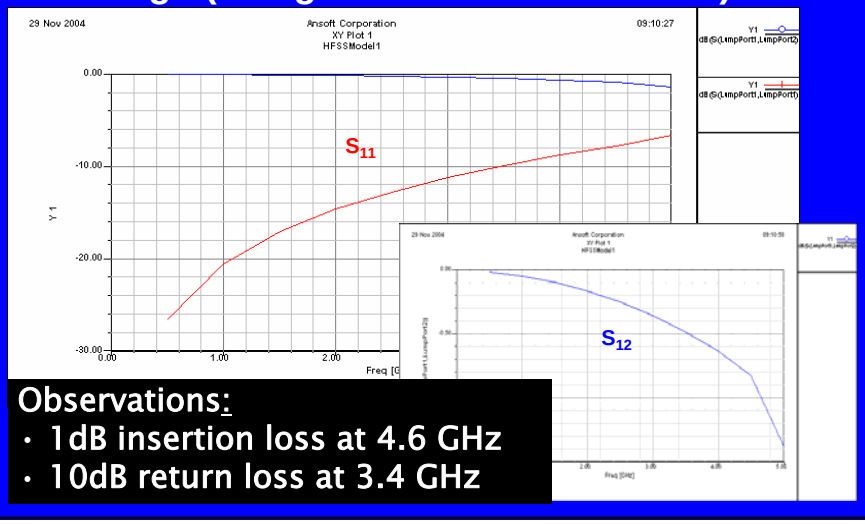
Proposed Design Change:

To minimize the unshielded signal path

3/2006 9

Design Review
(Board-to-Board Interposer)

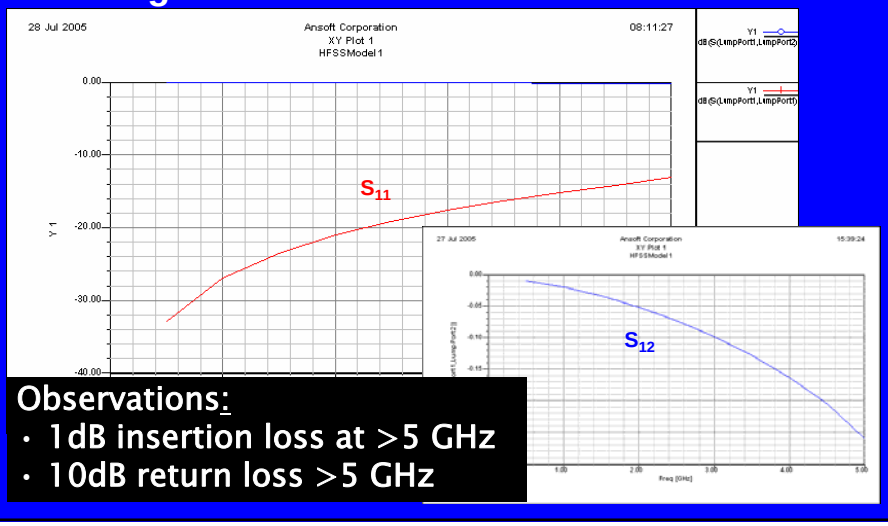
- Simulation results of original interposer design (using Ansoft HFSS software)



Observations:
- 1dB insertion loss at 4.6 GHz
- 10dB return loss at 3.4 GHz

Design Review
(Board-to-Board Interposer)

- Simulation results of optimized interposer design



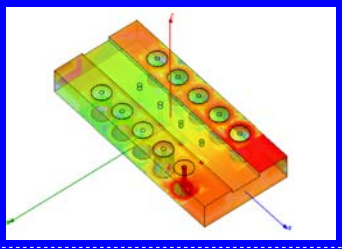
Observations:
- 1dB insertion loss at >5 GHz
- 10dB return loss >5 GHz

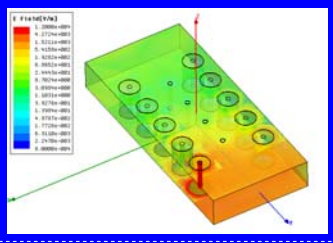
Design Review
(Board-to-Board Interposer)

- Field Plot

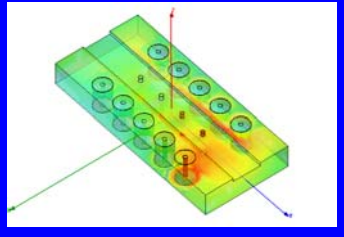
Original Design | Optimized Design

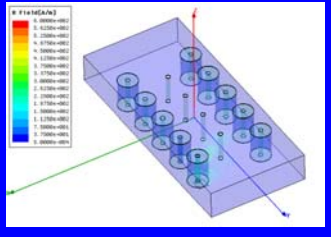
E-Field





H-Field





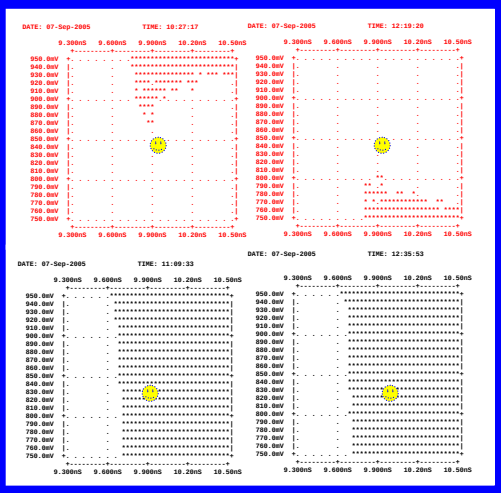
3/2006

Design Review
(Board-to-Board Interposer)

- Tester Shmoo Data:
  Original vs Optimized Interposer Design

Original Interposer

Optimized Interposer



☺ - DUT Passing Point

Observations:

Larger PASS region for the optimized interposer design

3/2006 13

Design Review
(Board-to-Board Interposer)

Summary

- From the simulation results, the optimized Board-to-board interposer has shown significant improvement over the original design in terms of Insertion Loss and Return Loss over a 5 GHz BW.

- The improvement seen from the simulation results was validated with Tester's shmoo data.

3/2006 14

Design Review
(Board-to-Board Interposer)

Summary

- This has helped to establish a good confidence level of using simulation for design assessment prior to actual prototype build.

3/2006 15

Design Review

Next let's look at

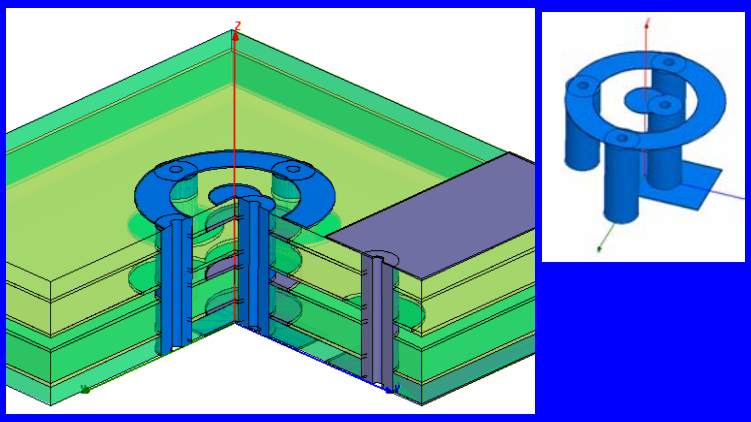
Signal-Gnd Via Structure

3/2006 16

Design Review
(Signal-Gnd Via Structure)

- **Original via structure**

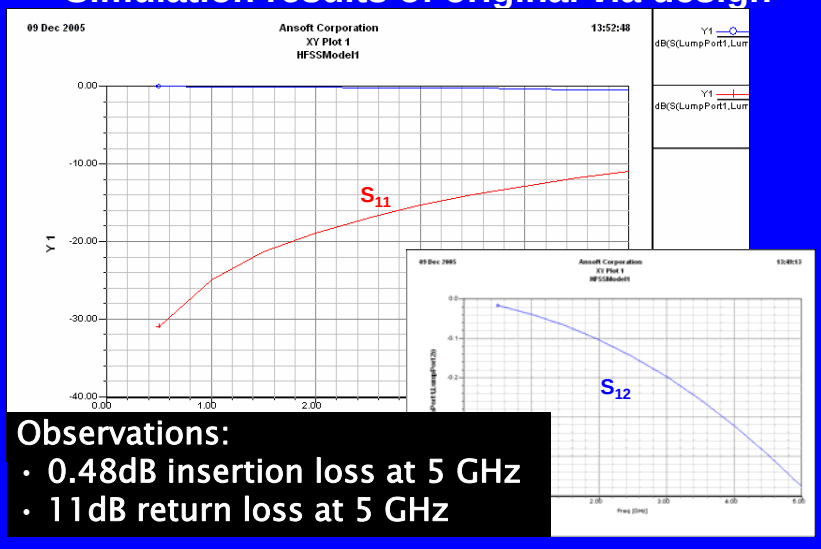
  - Offset signal via



3/2006 17

Design Review
(Signal-Gnd Via Structure)

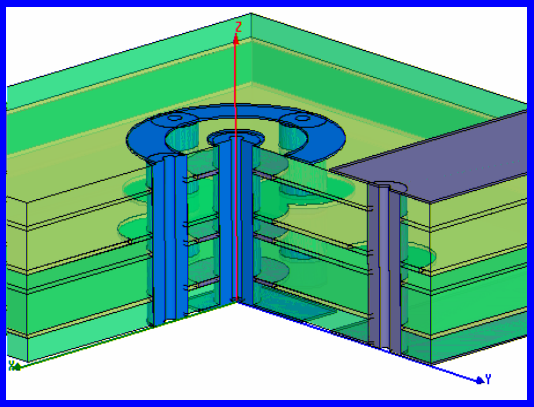
- **Simulation results of original via design**

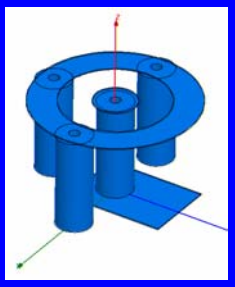


Observations:
- 0.48dB insertion loss at 5 GHz
- 11dB return loss at 5 GHz

Design Review
(Signal-Gnd Via Structure)

- **Optimized via structure**
  - Centered signal via

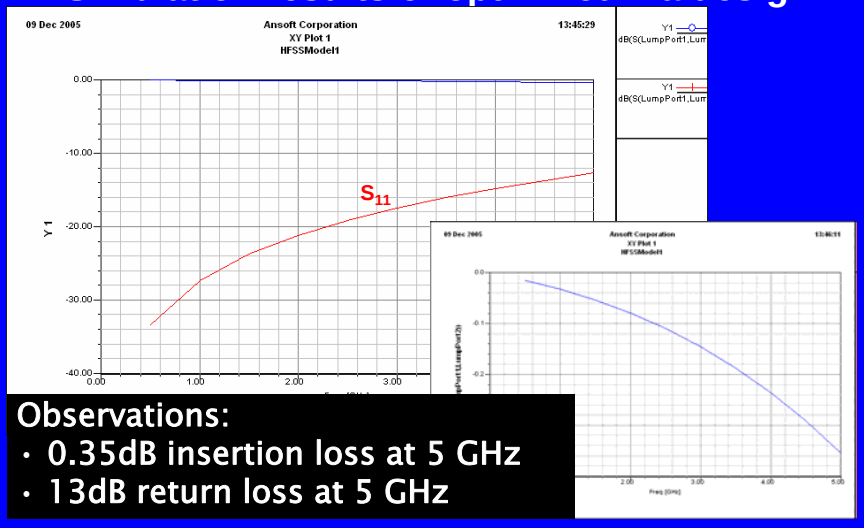




3/2006 19

Design Review
(Signal-Gnd Via Structure)

- **Simulation results of optimized via design**



Observations:
- 0.35dB insertion loss at 5 GHz
- 13dB return loss at 5 GHz

Design Review
(Signal-Gnd Via Structure)

Summary

- The simulation results show 27 percent improvement on insertion loss and 18 percent on return loss for the optimized signal-gnd via design as compared to original.
- However, this may need to be compromised with the mechanical requirement of having a larger signal pad, which the original design can provide. A larger landing pad is preferred for ease of contacting with the signal probes on the interposer.

3/2006 21

Design Review
(Signal-Gnd Via Structure)

Summary

- So does it justify a design change?
  Unless the impact of optimized via design can be quantified from a system-level perspective, no decision can be adequately made with respect to the final choice of design options. This will be dealt with in the next session on system-level performance.

3/2006 22

How to model

System-Level Performance

3/2006 23

System-Level Performance

- Objective:
  - Assessment of individual design gain from a system-level perspective
- Advantages:
  - Help to provide a matrix of merits on the various design combinations
  - Facilitate decision-making process on the selection of the most viable design combination with consideration to practicality and cost (expense versus performance index)

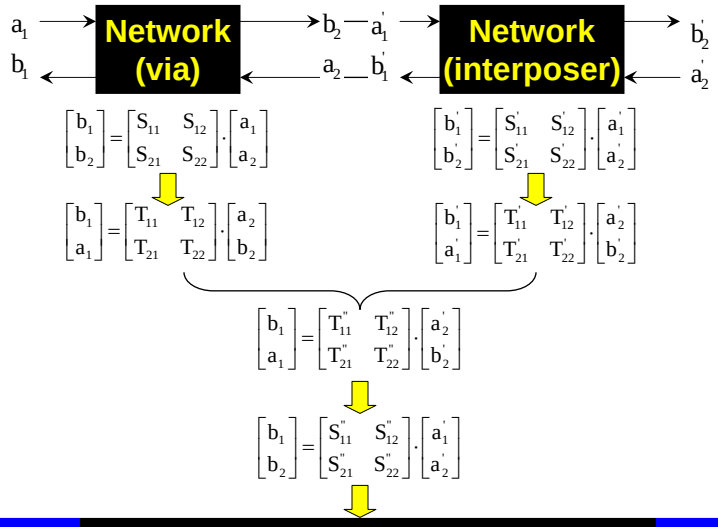
3/2006 24

System-Level Performance

- Explore a low-cost approach that can sufficiently provide the first order assessment. How?
  - Cascade the S-parameter matrices of individual network
  - Mathematically manipulate the matrices to obtain the system-level S-parameters [2]

3/2006 25

System-Level Performance



3/2006 26

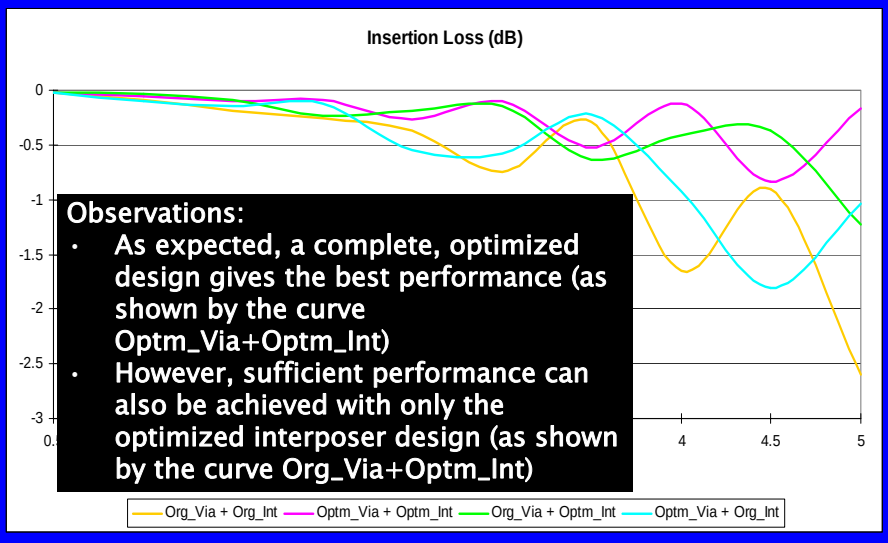
System-Level Performance

Design assessment matrix at system level

	Original Via Structure (Org_Via)	Optimize Via Structure (Optm_Via)
Original Interposer (Org_Int)	Worst case	??
Optimized Interposer (Optm_Int)	??	Best case

3/2006 27

System-Level Performance



Observations:
- As expected, a complete, optimized design gives the best performance (as shown by the curve Optm_Via+Optm_Int)
- However, sufficient performance can also be achieved with only the optimized interposer design (as shown by the curve Org_Via+Optm_Int)

3/2006 28

System-Level Performance

Summary:

- The system-level S-parameters can be obtained mathematically by manipulating the S-parameter matrices of individual networks (the interposer and via structure).
- As such, the system-level performance of various combinations of the interposer and via designs can be compared.

3/2006 29

System-Level Performance

Summary:

- The results show that the optimized interposer design has the biggest impact to the system-level performance.
- Thus, decision-making on the final choice of design combination is made much easier.

3/2006 30

In essence…

3/2006 31

Conclusions

- The simulation tool is used to assess the merits of design change during the design optimization cycle.
- The simulation result is validated using the tester's shmoo data. This has enhanced the confidence level of the simulation model.

3/2006 32

Conclusions

- Simulation data of individual network can be cascaded to provide an overall assessment of performance at a system level.
- The ability to obtain the system-level performance can be shown to aid decision making on the final choice of design combination.

3/2006 33

References

[1] Koh Tuan Meng and Lim Kok Lay, “A FLEXIBLE ELECTRICAL INTERFACE DESIGN FOR THE FIXTURE BETWEEN TESTER AND DUT TO ACHIEVE REDUCED COST AND LEADTIME IN ATE TOOLINGS”, BiTS 2003 Workshop.

[2] Agilent AN 154, S-Parameter Design, Application Note.

3/2006 34

Acknowledgments

Special thanks to the following people for their support on this project:

Seah Yee Choon, Koh Tuan Meng, Lim Kok Lay, Ong Boon Ngoh, Calvin Lim, Richard Teo and Yap Khai Tian from MSA Test Equipment R&D. Chia Yong Poo from MSA Assy Pkg R&D.

3/2006 35

Thermal Considerations in Testing Very High Performance Devices

Thomas Di Stefano
Centipede Systems
2110 Ringwood Avenue
San Jose, CA 95131
tom@centipedesystems.com

Centipede Systems

BiTS 2006

Thermal Considerations …

What's New ?

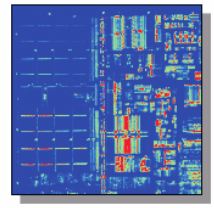
- More Thermal Gradients (Hot Spots)*
- Higher Power Densities
- Increased Testing of Bare Flip-Chips

* Dave Gardell, Thermal Characterization and Specification for Test and Burn-in, BiTS 2005

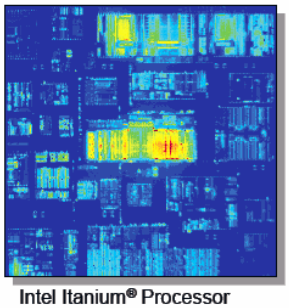
2

BiTS 2006

- Hot spots can be >300 W/cm2.



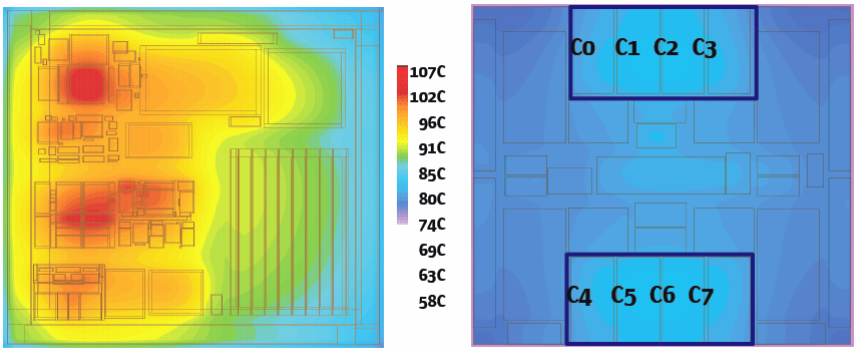
Intel Pentium® III Processor



Intel Itanium® Processor

Debendra Malek, Thermal Issues from ITRS Perspective, MEPTEC The Heat is On 2006

BiTS 2006



Bidyut Sen & Jim Jones, Thermal Challenges for Sparc Based Microprocessors, MEPTEC The Heat is On 2006

BiTS 2006

Thermal Considerations …

What's New ?

- More Thermal Gradients (Hot Spots)*
- Higher Power Densities
- Increased Testing of Bare Flip-Chips

* Dave Gardell, Thermal Characterization and Specification for Test and Burn-in, BiTS 2005

5 BiTS 2006

Thermal Considerations …

State of the Art

- **TIM Materials** — **$\Theta \sim 0.15\ ^{o}C\text{-}cm^2 / W$**
- **Temperature Control** — **$\pm 2\ ^{o}C$ average**

Emerging Problem – "Hot Spots"

- **Thermal Error Yield Loss**
- **Increased Re-test Rates**

6 BiTS 2006

Hot Spots → Reduced IC Performance → Thermal Error Yield Loss

Local Heating:

- Degrades Switching Time of Critical Nets,
- Reduces Performance ~ 0.5 % per ºC at 25 ºC
- Leads to Unnecessary Yield Loss

7 BiTS 2006

Yield Loss due to Hot Spots

"Every 15ºC increase locally causes a delay or skew to increase roughly 10 to 15%"

- Andrew Yang, TSMC EDN Sept /2005

Hot Spots Cause Performance Degradation

- Reduction of Surface Channel Mobility
  $\partial\mu / \partial T = - K\mu_0 / T$ K ~ 1.5 to 2.5
- Increased RC Delays
  $\partial RC / \partial T = 0.0038\ RC$

8 BiTS 2006

Thermal Error Yield Loss

Simplified Model Assumptions*

- Switching time is temperature dependent

$$\tau \sim 1.13 \times 10^{-4} \tau_0 T^{1.6} \quad (T \text{ in } ^oK)$$

- Worst case performance is determined by hot spot δT

$$\delta\tau / \delta T = 0.0055 \tau_0 \quad \text{Delay Time}$$

$$\delta f / \delta T = - 0.0055 f_0 \quad \text{Frequency}$$

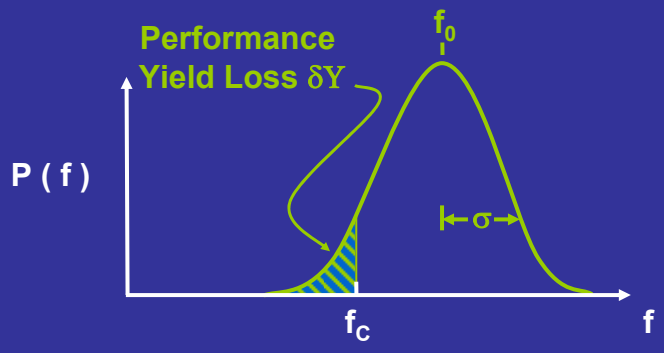
* Precise model depends upon specific details

9 BiTS 2006

Thermal Error Yield Loss

Simplified Model Assumptions*

- IC performance is a normal distribution around f_0



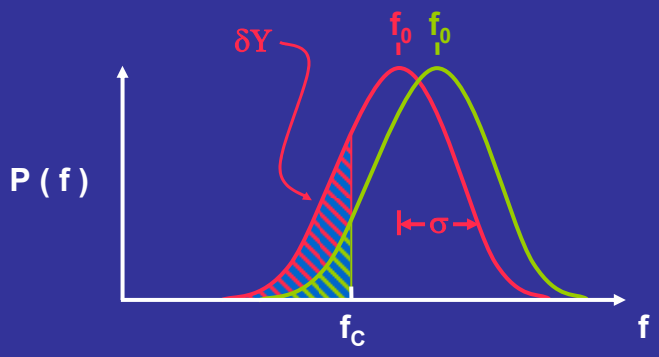
* Precise model depends upon specific details

10 BiTS 2006

Thermal Error Yield Loss

Simplified Model Assumptions*

- Performance yield curve is shifted by hot spot



* Precise model depends upon specific details

11

BiTS 2006

Thermal Error Yield Loss

Simplified Model*

- Performance yield curve is shifted by hot spot

$$Y = \tfrac{1}{2} + \tfrac{1}{2}\,\mathrm{erf}\left\{ (f_0(T) - f_C) / (\sigma\sqrt{2}) \right\}$$

- Yield loss due to hot spot

$$\delta Y/\delta T = -\,0.00242\,(f_0/\sigma)\left\{ 1 - 1.03\,(Y_0 - 0.5) - \ldots \right\}$$

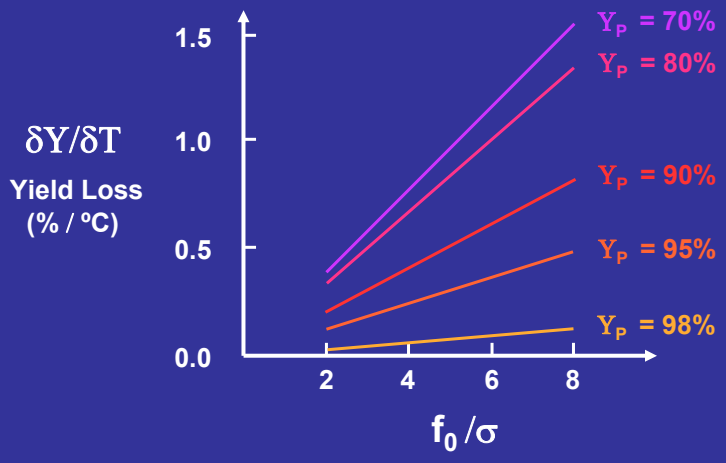
δT = **Hot Spot Temperature above** T_0

* Precise model depends upon specific details

12

BiTS 2006

Thermal Error Yield Loss

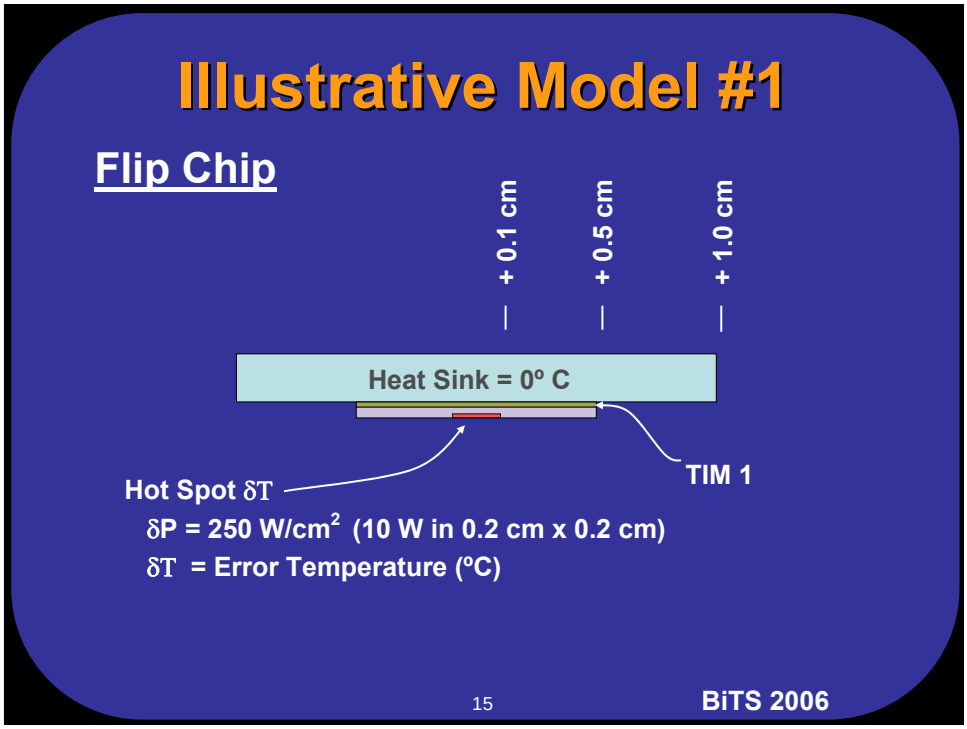


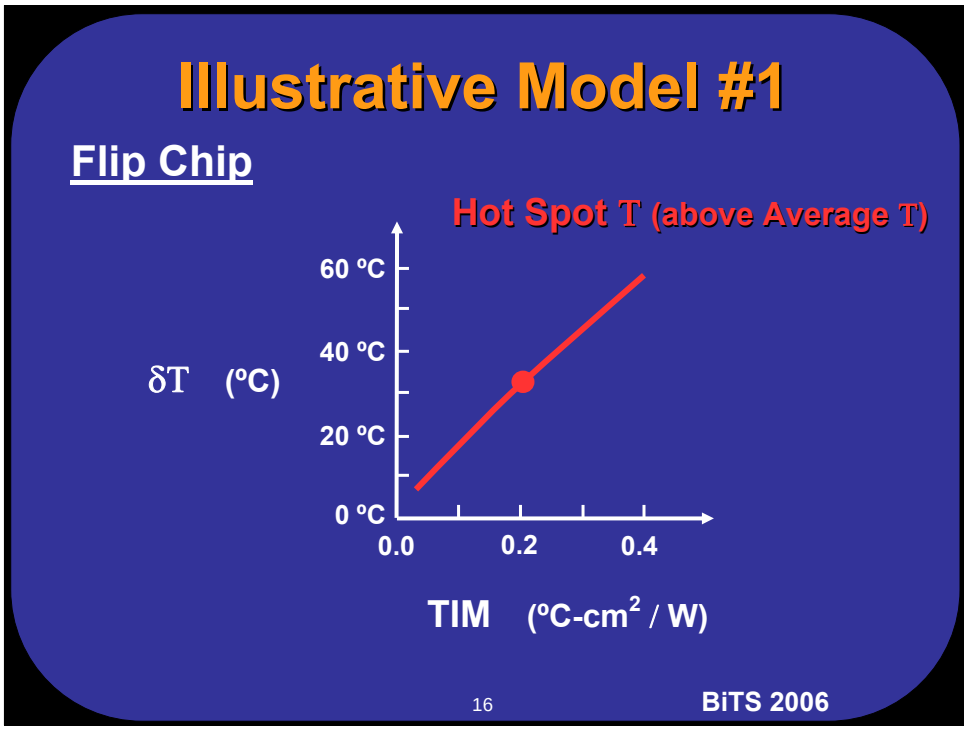
13 BiTS 2006

Test Methods can Introduce Thermal Errors :

- Insufficient Thermal Conductivity in TIM
- Errors due to Single Point Sensing
- Temperature Non-Uniformities on Heat Sink

14 BiTS 2006


Illustrative Model #1
Flip Chip
+ 0.1 cm
+ 0.5 cm
+ 1.0 cm
Heat Sink = 0º C
TIM 1
Hot Spot δT
δP = 250 W/cm2 (10 W in 0.2 cm x 0.2 cm)
δT = Error Temperature (ºC)
15
BiTS 2006


Illustrative Model #1
Flip Chip
Hot Spot T (above Average T)
δT (ºC)
60 ºC
40 ºC
20 ºC
0 ºC
0.0
0.2
0.4
TIM (ºC-cm2 / W)
16
BiTS 2006

Illustrative Model #1

Flip Chip Parameters

Hot Spot	10 W in 0.2 x 0.2 cm area
Performance Yield	Y_P = 95 %
Yield Distribution	$\sigma = 0.33\ f_0$
TIM Material	0.2 ºC-cm2 / W

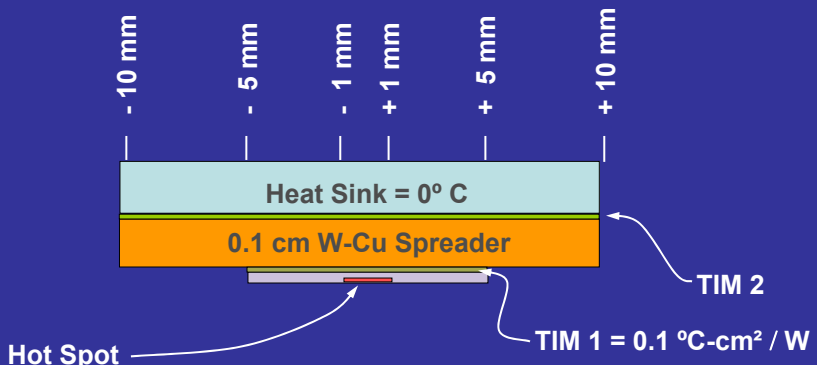
Temperature Error δT = 33ºC

Thermal Error Yield Loss = 5.9%

17 BiTS 2006

Illustrative Model #2

Thermal Spreader



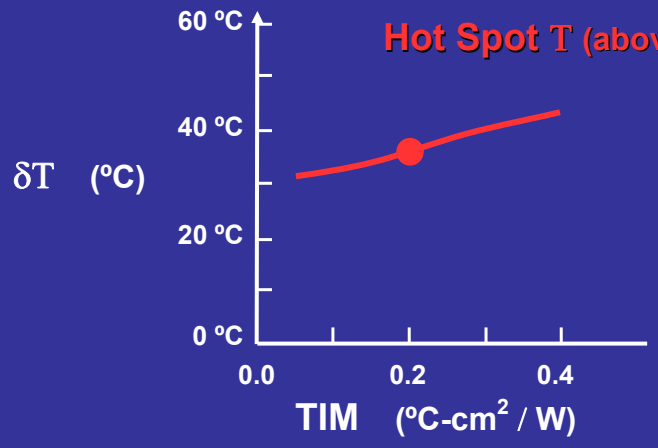
δP = 250 W/cm^2 (10 W in 0.2 cm x 0.2 cm)

δT = Error Temperature (ºC)

18 BiTS 2006

Illustrative Model #2

Thermal Spreader



19 BiTS 2006

Illustrative Model #2

Thermal Spreader Parameters

Hot Spot	10 W in 0.2 x 0.2 cm area
Performance Yield	Y_P = 95 %
Yield Distribution	$\sigma = 0.33\ f_0$
TIM Material	0.2 ºC-cm2 / W

Temperature Error δT = 36ºC

Thermal Error Yield Loss = 6.4 %

20 BiTS 2006

Caveat …

Thermal Error Yield Loss Model Must Take into Account the Actual:

- **Impact of Temperature on IC Performance**
- **Thermal Properties of Materials**
- **IC Performance Yield**

21 BiTS 2006

Thermal Considerations …

Local Heat Generation in IC

- Hot Spots Degrade Measured Chip Performance

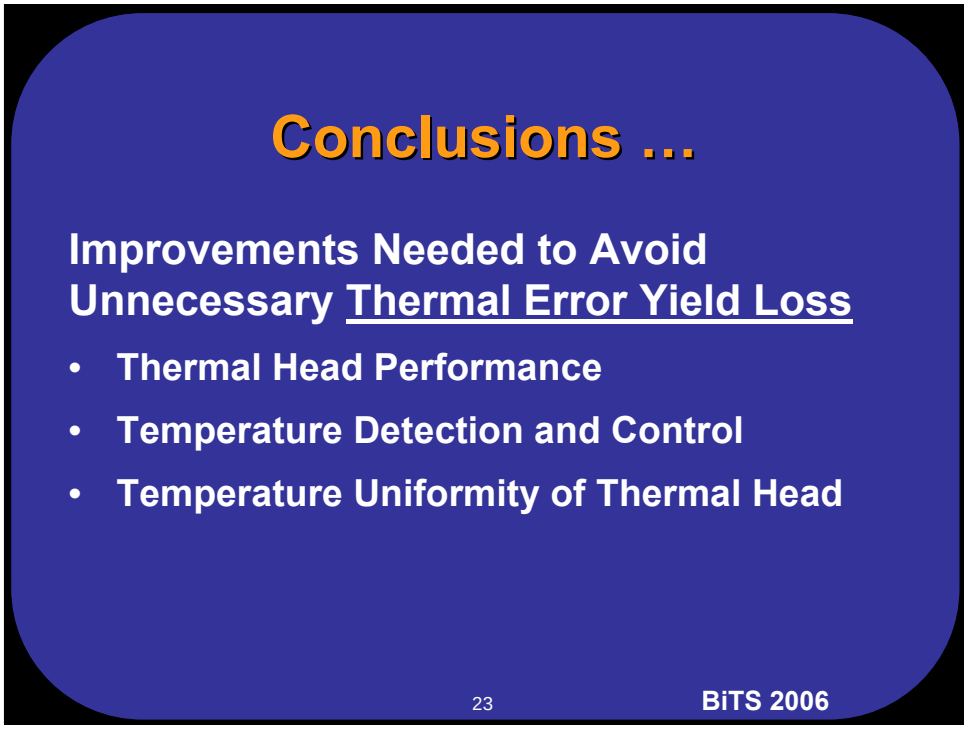
Single Point Temperature Measurement

- Local Variations Induce Errors in Control Temperature

Thermal Gradients on Heat Sink

- Degrade Measured Chip Performance

22 BiTS 2006


Conclusions …
Improvements Needed to Avoid Unnecessary Thermal Error Yield Loss
• Thermal Head Performance
• Temperature Detection and Control
• Temperature Uniformity of Thermal Head
23
BiTS 2006