Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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Burn-in & Test Socket Workshop

Technical Program

BiTS Tutorial
Sunday 3/06/05 1:00PM

“Signal Integrity of Sockets – Simplified!”

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Signal Integrity of Sockets- Simplified!

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2005 Burn-in and Test Socket Workshop
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BiTS
Burn-in & Test
Socket Workshop

SYNERGETIX

Outline

- ✓ Who cares?
- ✓ What's important: signal integrity, power integrity
- ✓ Common vocabulary
- ✓ Insertion loss: what is and is not important?
- ✓ Loop inductance: what is and is not important?

"It is better to uncover a little than to cover a lot"
- Francis Low

Electrical Performance in Perspective

- Performance
  - ✓ Compliance
  - ✓ Pitch
  - ✓ Cycle lifetime
  - ✓ Time between cleaning
  - ✓ Electrical
    - DC resistance
    - Hi Frequency
      - Signal Integrity
        - » Bandwidth
        - » Insertion loss
        - » Return loss
        - » SPICE models
      - Power integrity
        - » Loop inductance

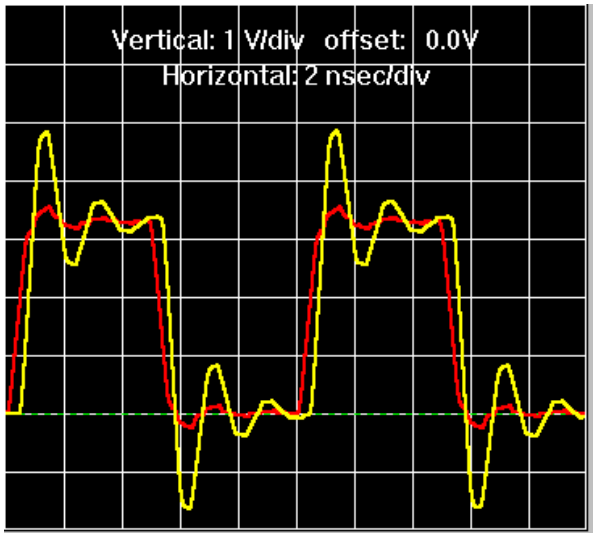
Constraints:
- **Vendors**
- **Corporate Culture**
- **Compatibility: Industry, Legacy**

Cost:
$$$, TCOO, Schedule, Risk

Partitioning:
- **Pin electronics**
- **Wiring/cabling**
- **Loadboards**
- **Sockets**

Signal Integrity and Interconnect Design

How the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips



Simulated with HyperLynx

Signal integrity problems occur when the interconnects are no longer electrically transparent

Signal Integrity Problems

TERMINATIONS
LINE DELAY
PARASITICS
CAPACITANCE
EMISSIONS
GROUND BOUNCE
EMI/EMC
LOADED LINES
ATTENUATION
POWER AND
NON-MONOTONIC EDGES
RETURN LOSS
GROUND DISTRIBUTION
GROUND BOUNCE
CRITICAL NET
SUSCEPTABILITY
SKIN DEPTH
SIGNAL INTEGRITY
LOOP INDUCTANCE
LOSSY LINES
IR DROP
INDUCTANCE
RINGING
RISE TIME DEGRADATION
CROSSTALK
INSERTION LOSS
STUB LENGTHS
MODE CONVERSION
RETURN CURRENT PATH
GAPS IN PLANES
IMPEDANCE DISCONTINUITIES
TRANSMISSION LINES
REFLECTIONS
DELTA I NOISE
RC DELAY
UNDERSHOOT, OVERSHOOT
DISPERSION

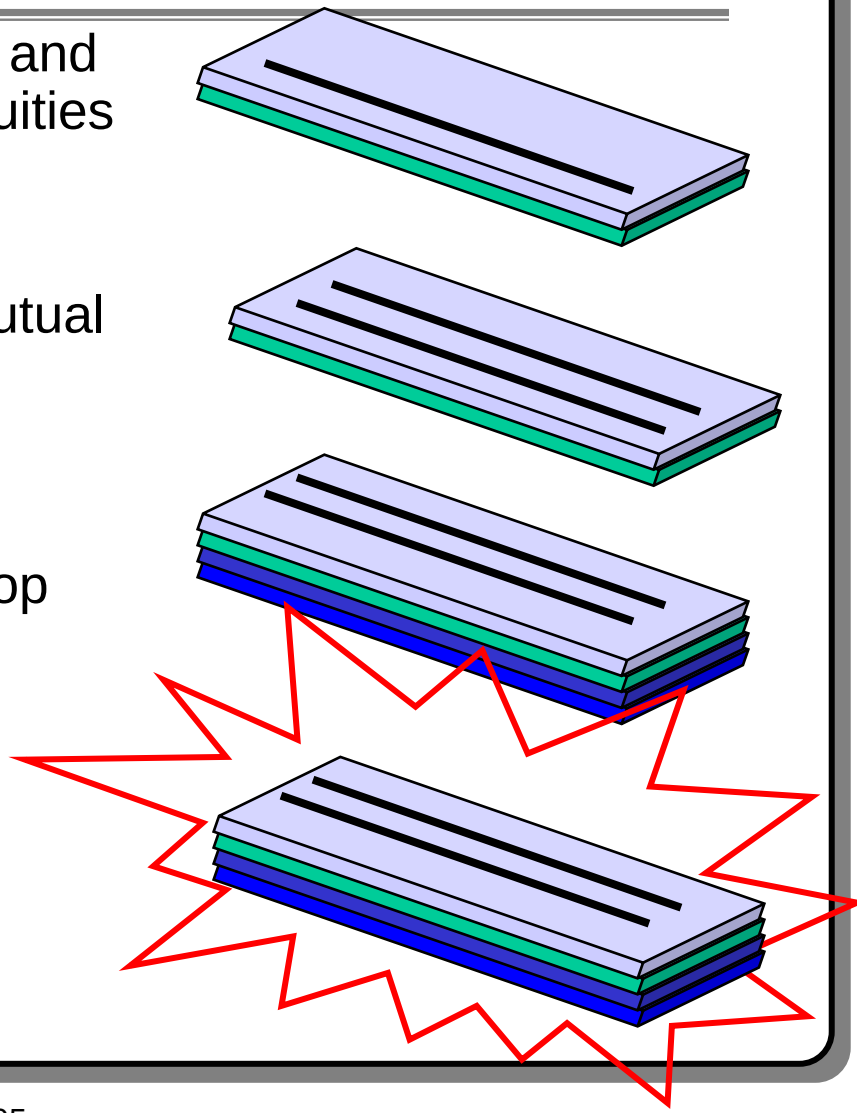
Four Families of Signal Integrity Problems

1. **Signal quality** of one net: reflections and distortions from impedance discontinuities in the signal or return path

2. **Cross talk** between multiple nets: mutual C and mutual L coupling

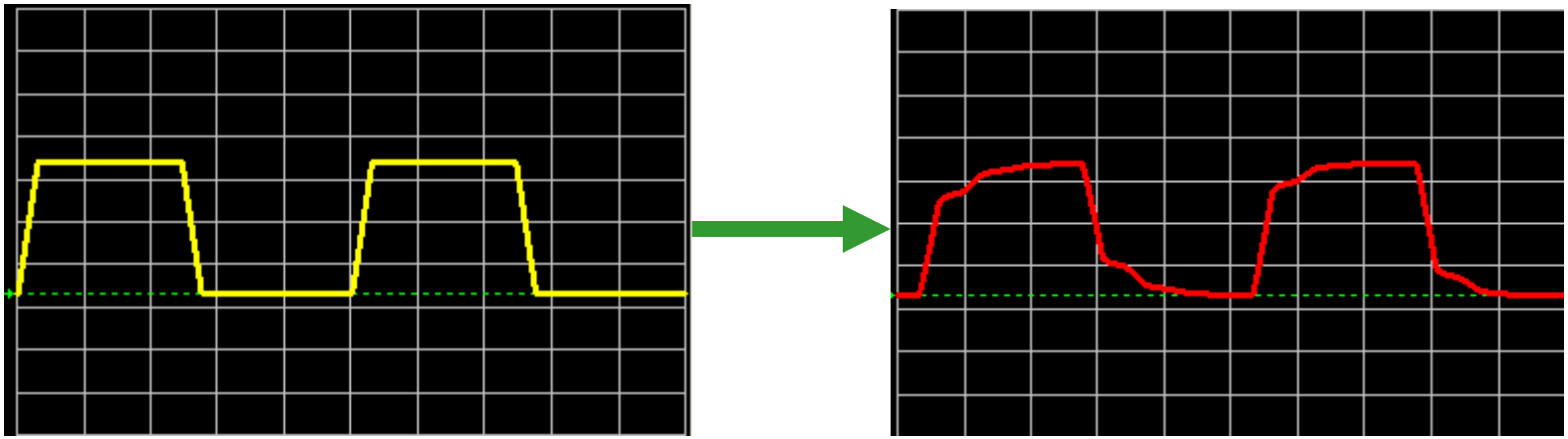
3. **Power integrity:** noise in the power distribution system (PDS): voltage drop across impedance in the pwr/gnd network

4. **EMI** from a component or the system



The Socket as a Component

- Purpose of an interconnect: “to transport a signal from one point to another with an acceptable level of distortion”



Simulated with HyperLynx

What’s important to know?

1. Will the system work?
2. Is the socket “good enough?”
3. How do you know before you build it and test it?

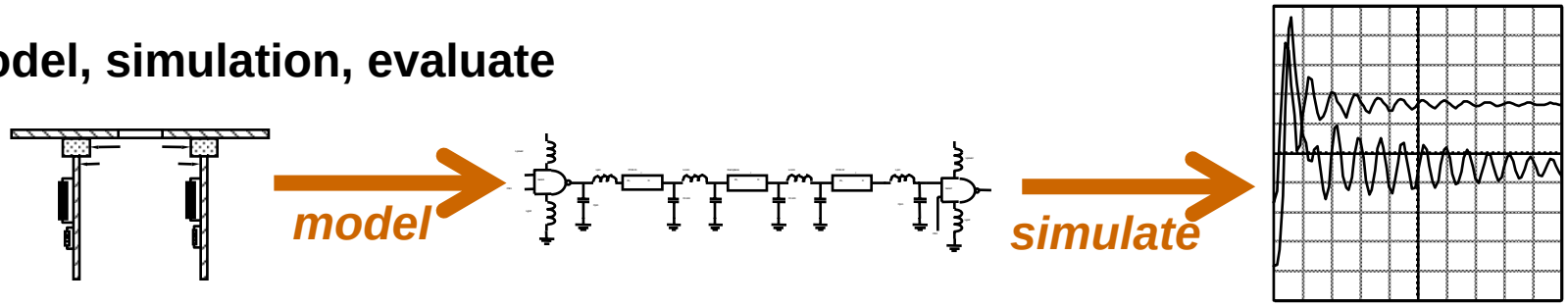
Build it and Test It

- Good news:
  - ✓ Always the final test
  - ✓ 100% certainty for that situation
- Bad news
  - ✓ What about the next socket?
  - ✓ What do you tell your supplier?
  - ✓ How does supplier evaluate quality?
  - ✓ If it doesn't work, where do you look to re-design?
  - ✓ Can you afford the time for multiple iterations?
- "Build it and test it" works when the interconnects are electrically transparent
  - ✓ Other specification methods are required for f > ~ 500 MHz
  - ✓ Everything except "build it and test it" is a compromise

2nd Best Solution

- The only way to know if the system will work before building and testing is system level simulation with accurate component models

Model, simulation, evaluate



- Needed: an accurate model of the socket which can be used in the SPICE level simulation:
  - ✓ SPICE model
  - ✓ Behavior model: S parameter model

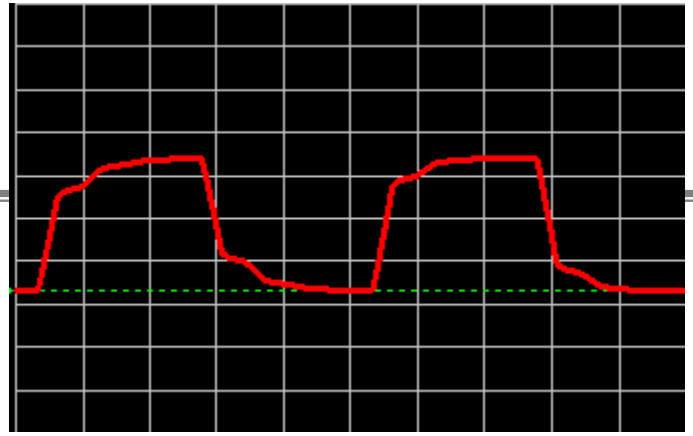
3rd Best Alternative

- Specify values of model parameters
  - ✓ Z_0
  - ✓ TD
  - ✓ L
  - ✓ C
  - ✓ Insertion loss
  - ✓ Return loss
- Specifications based on ***assumptions*** of the rest of the system
- Specifications are a pre-arranged compromise- sometimes based on:
  - ✓ System level simulation balancing cost-performance-constraints- (really hard!)
  - ✓ A guess
  - ✓ Because it worked in the last design
  - ✓ Enough margin for designer to sleep at night
  - ✓ Assuming performance is free
  - ✓ Incorrect assumptions
  - ✓ Information that was passed from engineer to engineer to engineer to engineer…(only one of whom might have an idea of what they want)

Universally used metric to define "goodness" of a socket:

-1 dB insertion loss bandwidth

- **Bandwidth**
- **Insertion loss**
- **dB**
- **Why -1 dB**
- **What design features influence this performance**



Is this acceptable?

Sometimes the frequency domain offers an easier path to the answer

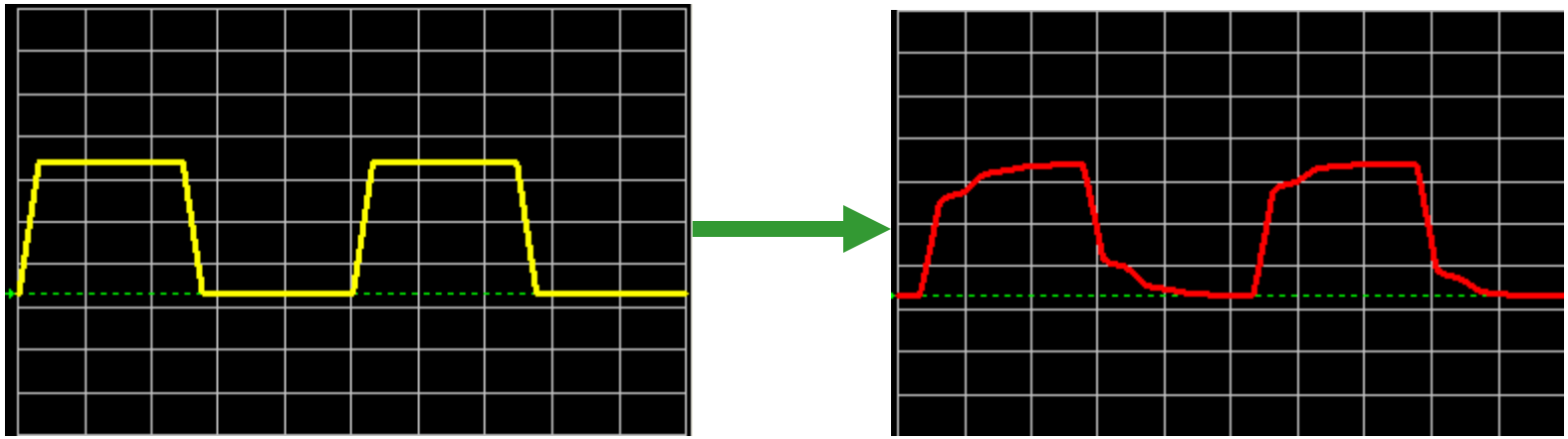
No new information in the frequency domain

The only reason we'd ever leave the time domain to go to the frequency domain:

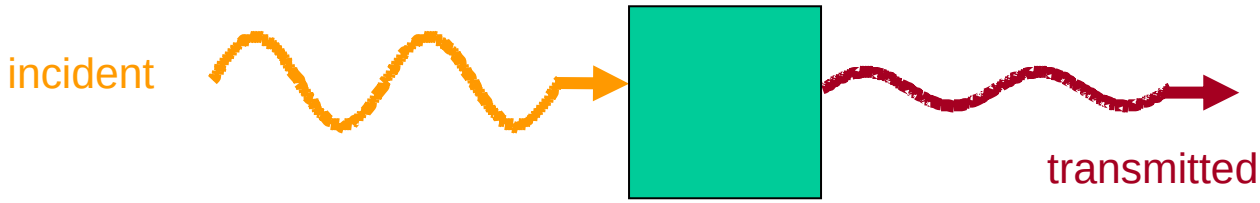
To get to the answer faster.

Two World Views

Time domain view



Frequency domain view



amplitude
phase

Up to the highest sine wave frequency that is significant

Bandwidth

Bandwidth: the highest sine wave frequency that is ***significant***

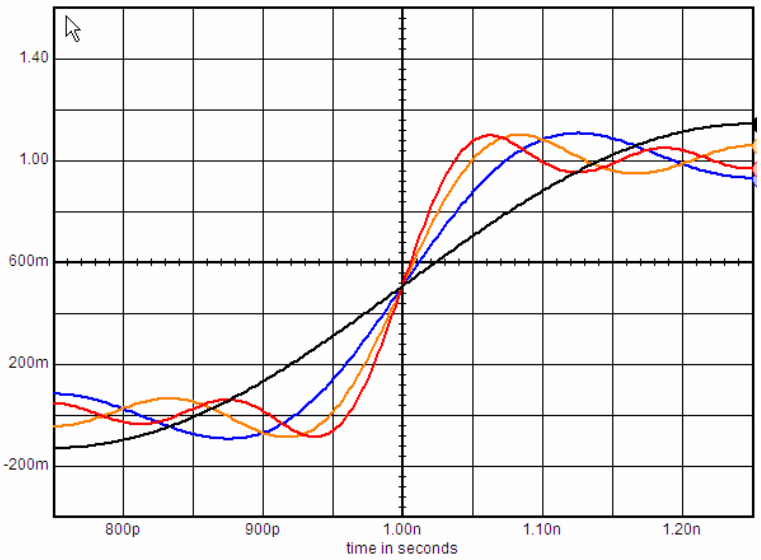
Bandwidth and the 10-90 Rise Time

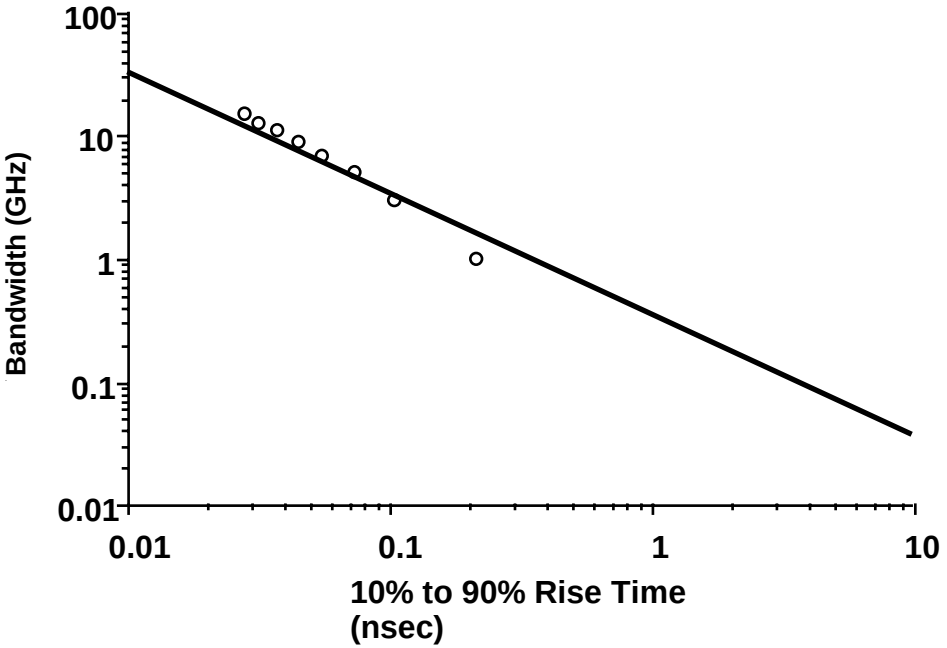
(see OLL-101 Bandwidth of Signals with SPICE)

The rule of thumb:

$$BW = \frac{0.35}{RT}$$

BW = bandwidth in GHz
RT = 10%→ 90% rise time in nsec





Clock Frequency and Bandwidth

$RT \approx 7\ \%\ T$ (a little aggressive, i.e., conservative estimate)

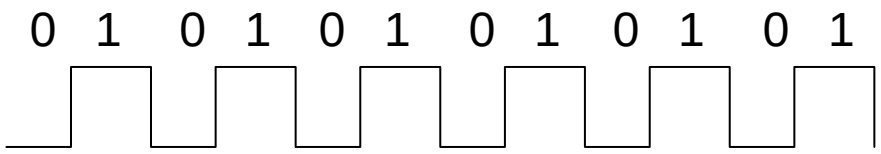
$$T_{period} = 15 \times RT \qquad RT = \frac{0.35}{BW}$$

$$T_{period} = 15\frac{0.35}{BW} \approx \frac{5}{BW} \qquad T_{period} = \frac{1}{F_{clock}}$$

If you don't know the rise time: $BW = 5 \times F_{clock}$

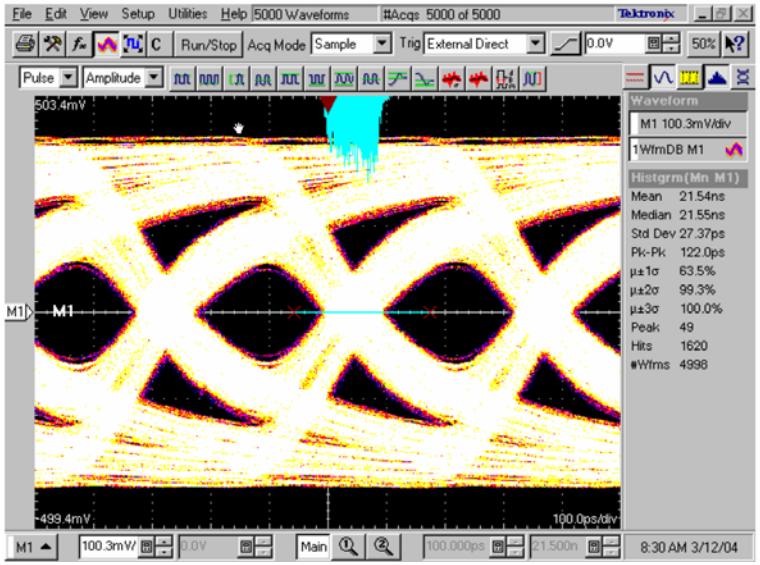
As a rough rule of thumb

Bandwidth and Bit Rate in high speed serial links (> 2 Gbps)



BR = bit rate
BW = bandwidth

For most high speed serial links:
Repeat frequency = ½ x BR
(for the 1010101010 pattern)



3,125 Gbps, Altera Stratix GX driver signal, after 42 inches on FR4 courtesy of Altera

- For the highest BR high speed serial links:
  - ✓ signal is almost a sine wave
  - ✓ BW ~ 1st harmonic of the repeat frequency
  - ✓ BW = ½ BR

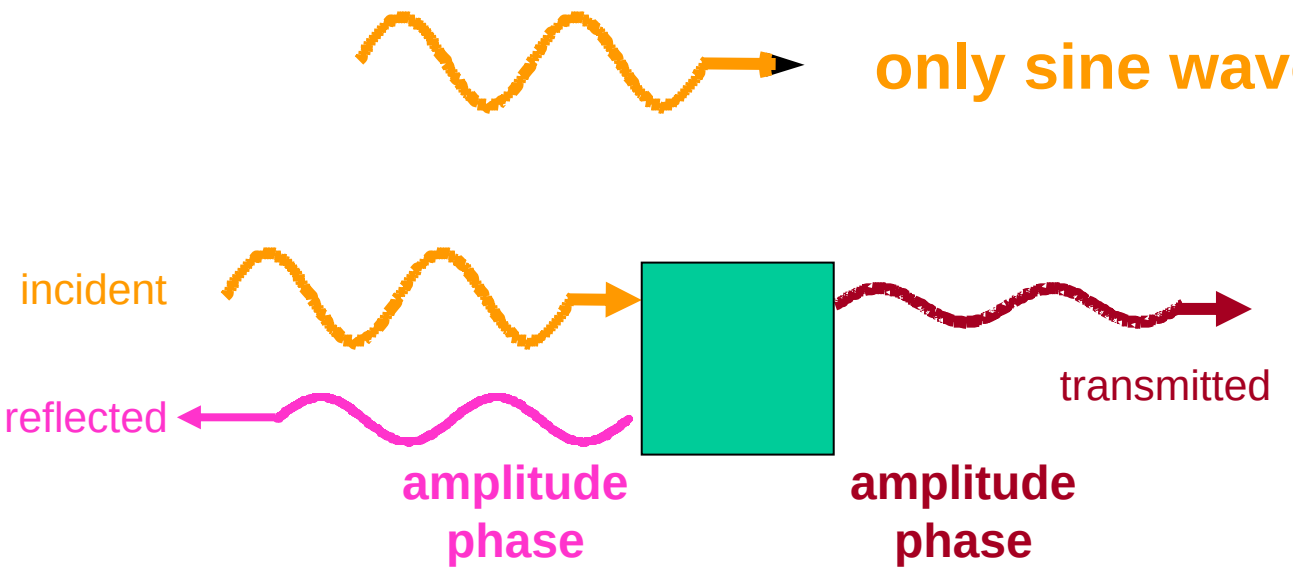
The rule of thumb: BW ~ ½ x BR

Key Assumptions

- Bandwidth is the highest sine wave frequency component that is significant
- Bandwidth is inherently only a rough approximate term- if an accurate frequency value is important, can't use the bandwidth
- If the socket meets performance spec for frequencies up to the bandwidth, it is "good enough"

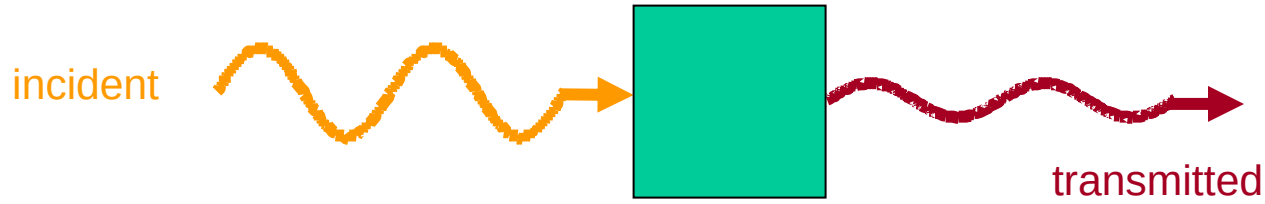
Transmitted Signals in the Frequency Domain

What are signals in the frequency domain?



Everything you ever wanted to know about the performance of a socket is contained in the reflected and transmitted signals

Terminology

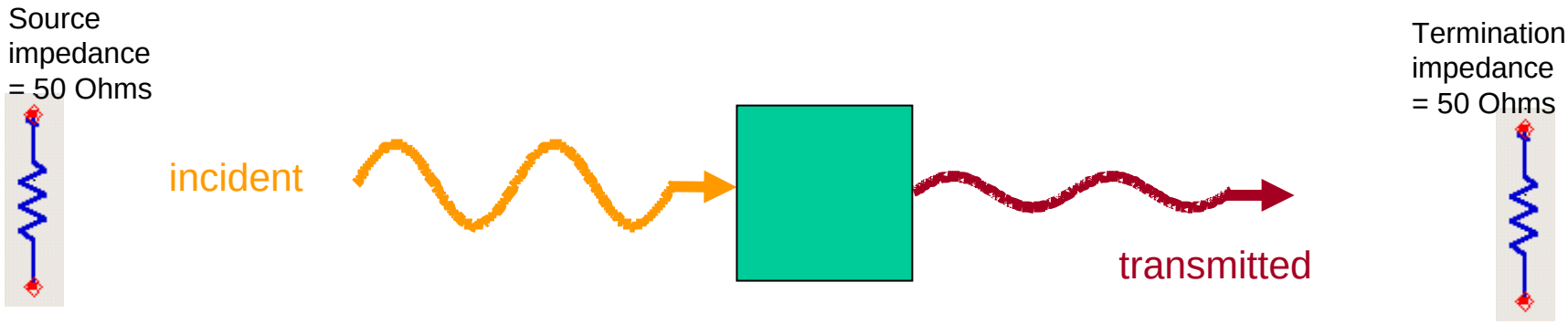


What's important: $\frac{V_{transmitted}}{V_{incident}}$ **at each frequency**

- Also called:
  - ✓ Insertion loss
  - ✓ S21
  - ✓ Transfer function

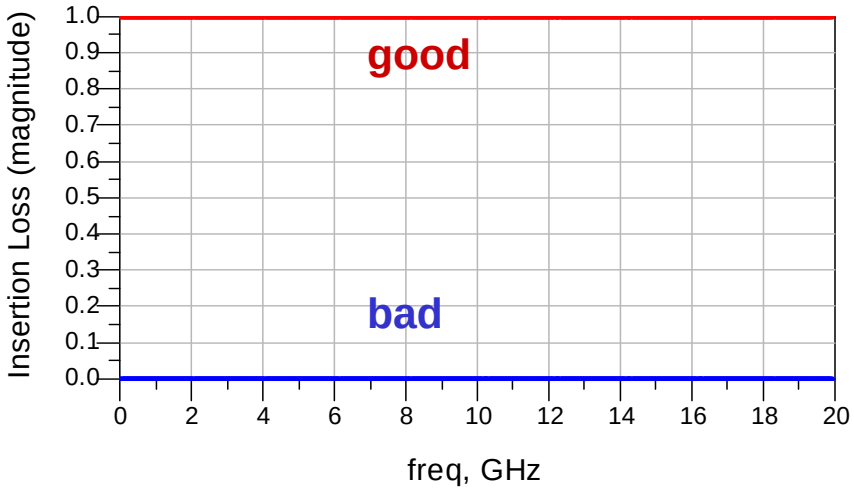
There is a magnitude and a phase at each frequency

Most Important Caveat



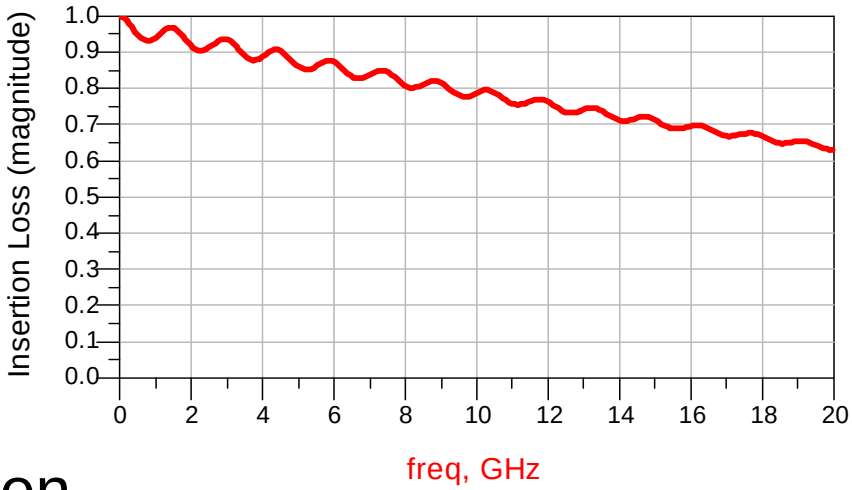
- The source impedance and the load impedance when defining S21 is always 50 Ohms.
- Insertion loss has significance if the end use environment is 50 Ohms

Good and Bad Insertion Loss



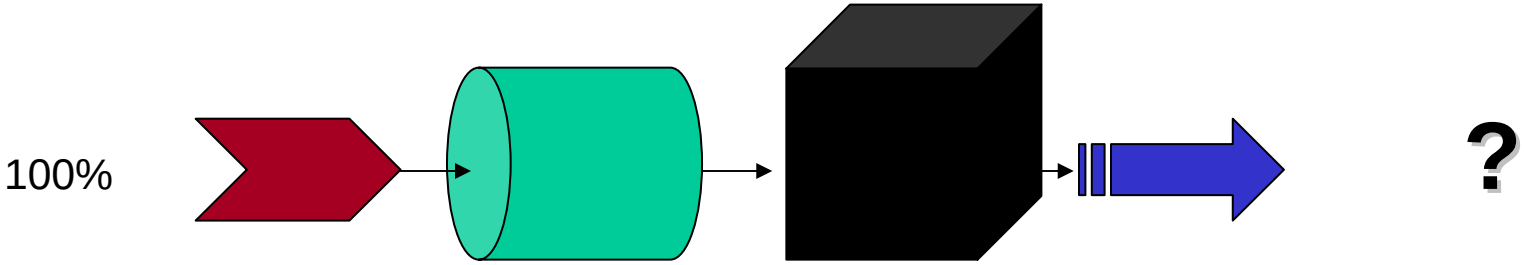
Simulated with Agilent ADS

Is this good?



- Is there a difference between
  - ✓ good
  - ✓ good enough
  - ✓ better ?

Insertion Loss of the System



Insertion losses:	**100%**	**x**	**100%**	**x**	**100%**	**x**	**50%**	**= 50%**
	100%	**x**	**90%**	**x**	**90%**	**x**	**50%**	**= 40%**
	91%	**x**	**95%**	**x**	**89%**	**x**	**95%**	**= 73%**

Using magnitudes, insertion losses multiply
If we used the log of the insertion loss, we could just add

The deciBel and Powers

Formalism: log of the ratio of two powers is in Bels

$$ratio[Bels] = \log\left(\frac{P_b}{P_a}\right)$$

10 deciBel = 1 Bels

$$ratio[dB] = 10\ x\ \log\left(\frac{P_b}{P_a}\right)$$

$$\frac{0.1watt}{1watt} = 10^{-1} = -10\ dB$$

$$\frac{0.001watt}{1watt} = 10^{-3} = -30\ dB$$

$$\frac{0.000001watt}{1watt} = 10^{-6} = -60\ dB$$

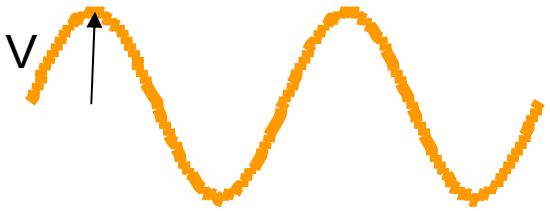
If we have the ratio of the **powers**, take the exponent of the power 10 and multiple by 10 to get the dB

If we have the number of dB, divide by 10 and put to the power of 10 and this is the ratio of the **powers**

-10 dB = 0.1 -20 dB = 0.01 -40 dB = 0.01%

The deciBel and Ratio of Voltages

When using dB to measure a ratio of ***amplitudes***, the dB ALWAYS refers to the ratio of the ***powers*** in the wave



$P \sim V^2$

$$ratio[dB] = 10\ x\ \log\left(\frac{P_b}{P_a}\right) = 10\ x\ \log\left(\frac{V_b^2}{V_a^2}\right) = 10\ x\ 2\ x\ \log\left(\frac{V_b}{V_a}\right) = 20\ x\ \log\left(\frac{V_b}{V_a}\right)$$

$$ratio[dB] = 20\ x\ \log\left(\frac{V_b}{V_a}\right)$$

When measuring the ratio of voltages, we use a 20
When measuring the ratio of powers, we use a 10

Insertion loss is the ratio of ***amplitudes***

From deciBel to Insertion Loss magnitude

If we have the number of dB,

1. divide by 20
2. put to the power of 10
3. this is the ratio of the **amplitudes**

$$\left(\frac{V_{out}}{V_{in}}\right) = 10^{\frac{ratio[dB]}{20}}$$

-20 dB = 0.1

-40 dB = 0.01

-60 dB = 0.001

-80 dB = 0.0001

0 dB = 1

-10 dB = 0.3

-25 dB = 0.05

-0.5 dB = 0.95

-1 dB = 0.90

-2 dB = 0.80

-3 dB = 0.70

When dB is small, Magnitude ~1 + dB/10

From magnitude to dB

If we have the ratio of the amplitudes,

$$ratio[dB] = 20\ x\ \log\left(\frac{V_{out}}{V_{in}}\right)$$

1. Write it to the power of 10
2. Take the exponent (or take the log of the number)
3. Multiply by 20
4. This is the dB

$$\frac{0.1 volt}{1 volt} = 10^{-1} = -20\ dB$$

$$\frac{0.01 volt}{1 volt} = 10^{-2} = -40\ dB$$

10% = -20 dB

1% = -40 dB

0.001 = -60 dB

90% = -1 dB

80% = -2 dB

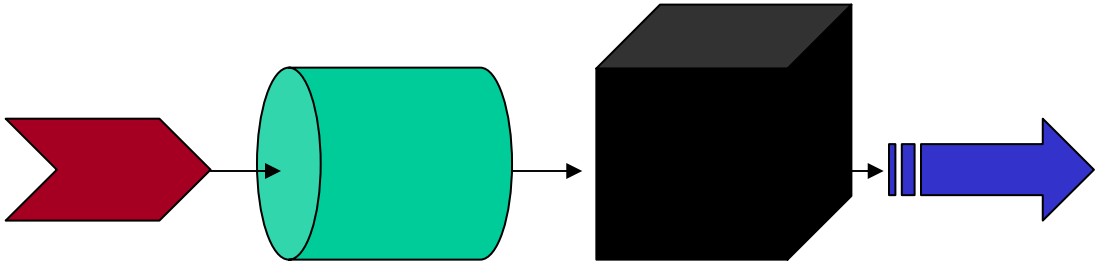
98% = -0.2 dB

When magnitude is close to 1, dB ~ (mag – 1) x 10

dB and Extreme Insertion Loss

- All the signal transmits: $S_{21} = 1 = 10^0 = 0$ dB
  - ✓ S_{21} = 0 dB everything is transmitted
  - ✓ Transparent interconnect
- Very little signal transmits: $S_{21} = 0.0001 = 10^{-4} = -80$ dB
  - ✓ S_{21} = really big, negative number, no signal at the far end
  - ✓ Really poor interconnect

Insertion Loss (dB) of the System



Insertion losses:	**0 dB**	**+**	**0 dB**	**+**	**0 dB**	**+**	**-6 dB**	**= -6 dB**
	0 dB	**+**	**-1 dB**	**+**	**-1 dB**	**+**	**-6 dB**	**= -8 dB**
	-1 dB	**+**	**-0.5 dB**	**+**	**-1.2 dB**	**+**	**-0.5 dB**	**= -3.2 dB**

If we use the log of the insertion loss (dB), we just add

What's a good value of Insertion Loss?

- Ideal total system insertion loss budget
  - ✓ At least 70% the amplitude of the signal at 2x the signal bandwidth
  - ✓ -3 dB at 2 x BW
  - ✓ If 100 MHz clock, BW ~ 500 MHz, 2x BW = 1 GHz: -3 dB @ 1 GHz
  - ✓ If 500 MHz clock, BW ~ 2.5 GHz, 2x BW = 5 GHz: -3 dB @ 5 GHz
- Practical total system insertion loss budget
  - ✓ -3 dB at signal BW
- Typical allocation of insertion loss to the socket
  - ✓ ~ -1 dB for socket
  - ✓ ~ -1 dB for load board
  - ✓ ~ -1 dB for tower pins and cables
- In rf applications, stability of insertion loss is critical
  - ✓ ~ -1 dB for socket, at carrier frequency is also a good metric
- If insertion loss < -1 dB at the application bandwidth, is this a guarantee system will work?

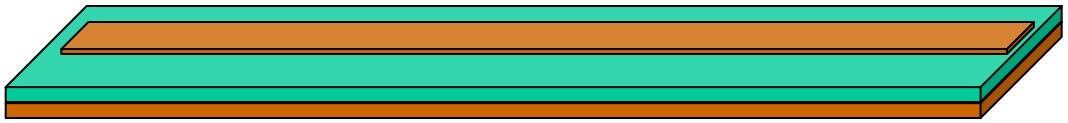
Value of -1 dB Insertion Loss Bandwidth as a Metric

- Relative comparison
- First pass screening
- Rough, rule of thumb for usable operating frequency
- Should not be used to sign off on a design
  - ✓ too approximate
  - ✓ too much margin? Too little?
  - ✓ Too many assumptions
- Multiple approximations:
  - ✓ Bandwidth of the signal
  - ✓ Is the system a 50 Ohm system?
  - ✓ Total system budget
  - ✓ Allocation to the socket
- A better approach (and much more expensive):
  - ✓ Model and simulate

What Affects Insertion Loss of a Socket?

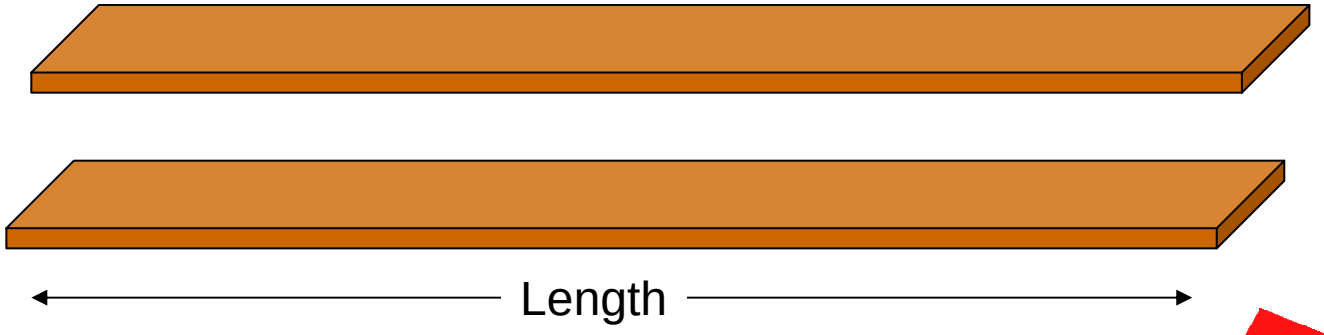
1. Matched Impedance
2. Controlled impedance
3. Discontinuities of load board
4. Length
5. Dielectric loss
6. Conductor loss
7. DC contact resistance

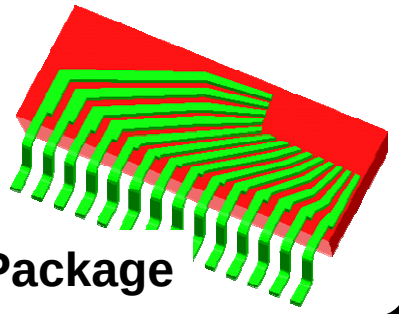
The Simplest Model of a Transmission Line



Microstrip

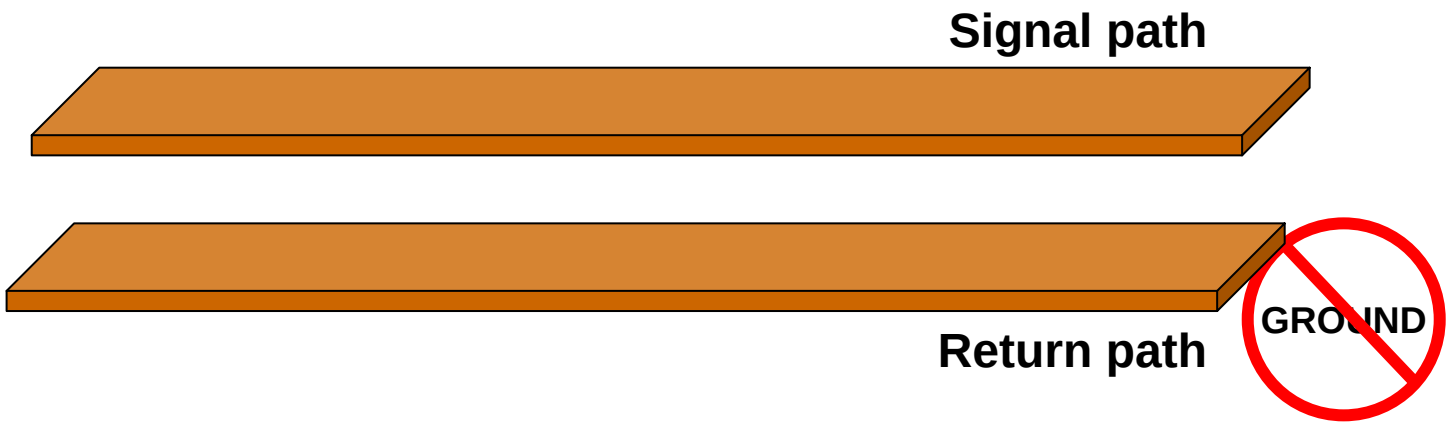
A "-1" order model:
Any two conductors with length



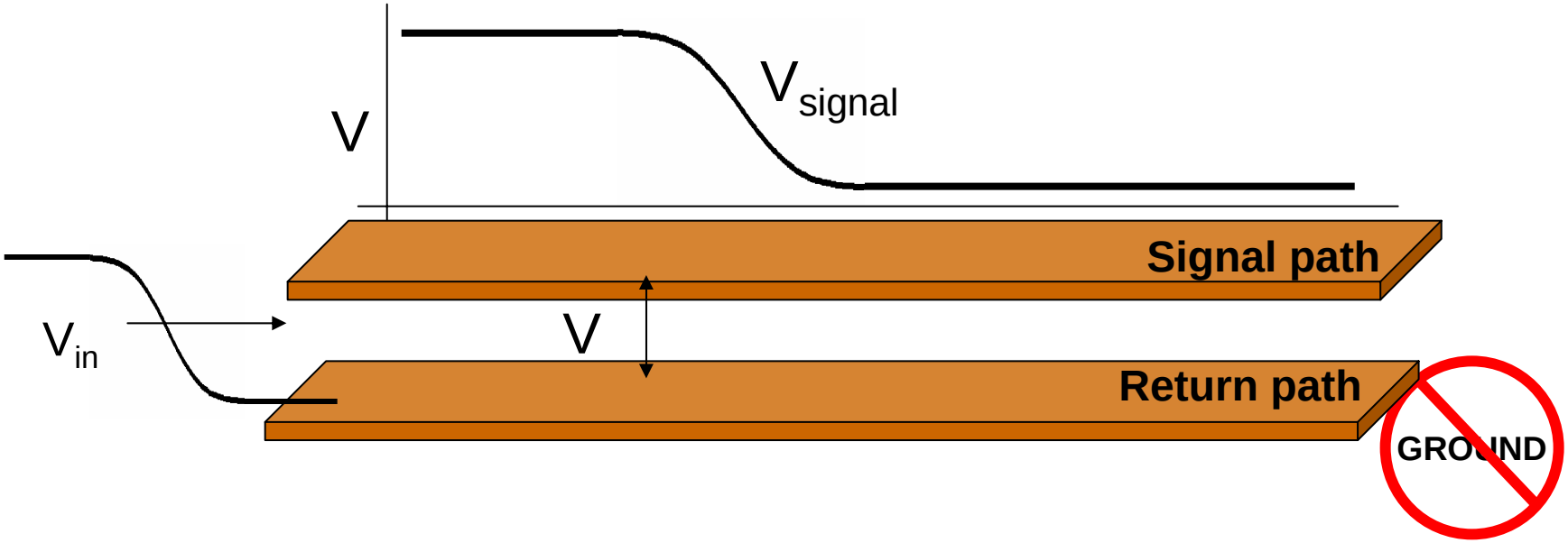


Lead frame of an IC Package

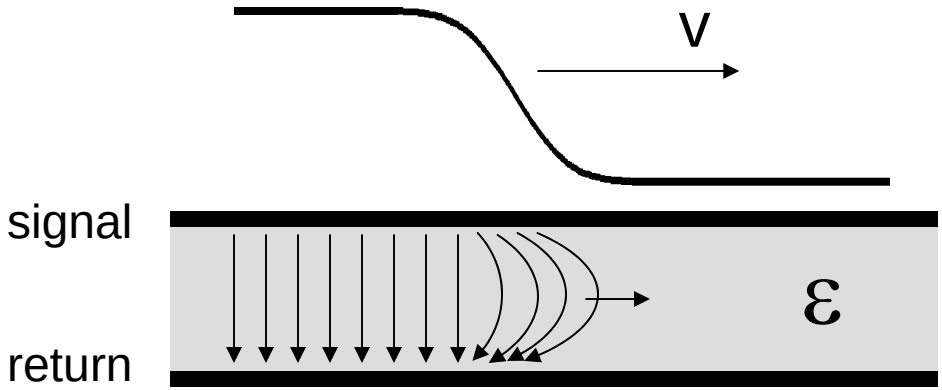
Labeling the Conductors



The Signal



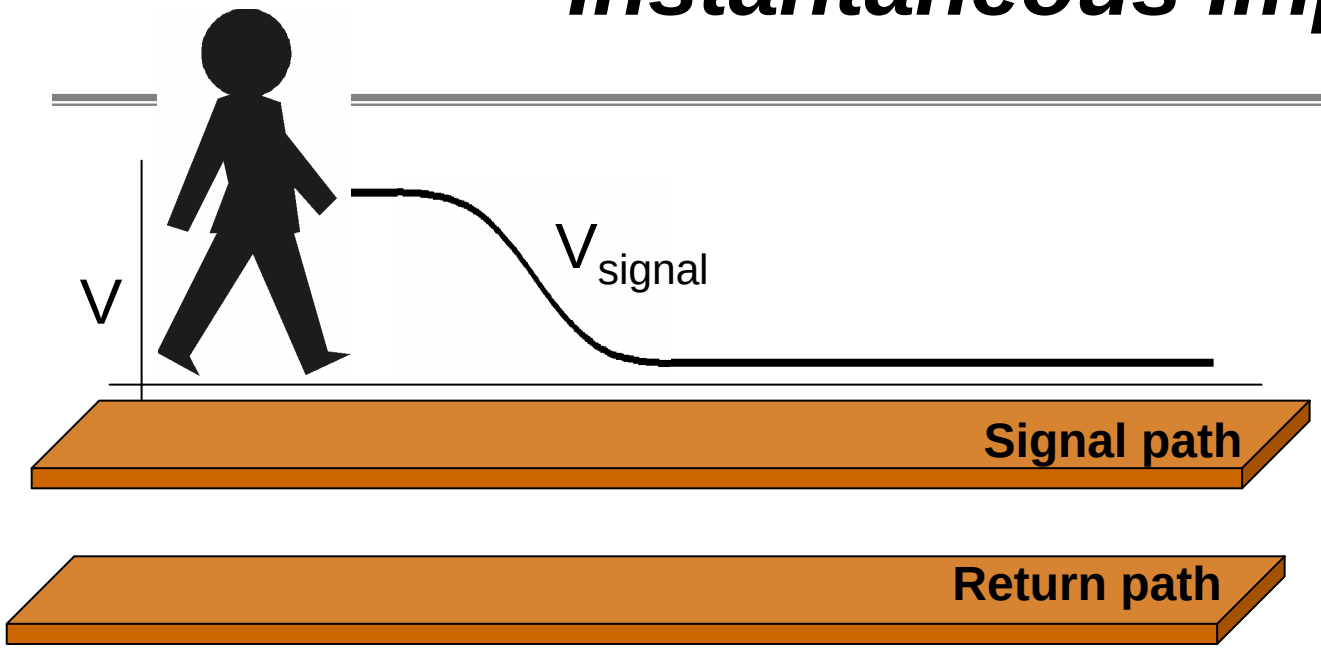
How fast does a signal move down a line?



in air: v = 186,000 miles per sec v = 12 inches/nsec

$$v = \frac{12\ \frac{inches}{n\,\mathrm{sec}}}{\sqrt{4}} = \frac{12\ \frac{inches}{n\,\mathrm{sec}}}{2} = 6\ \frac{inches}{n\,\mathrm{sec}}$$

Instantaneous Impedance



- Signal sees an “instantaneous impedance” each step along the path
- Instantaneous impedance depends on the geometry of signal and return path
- A controlled impedance when instantaneous impedance is constant
- One impedance that characterizes the interconnect:

- Characteristic impedance

Characteristic Impedance and Capacitance per Length

capacitance per length decreases, the characteristic impedance increases

50 Ohm PCB cross section

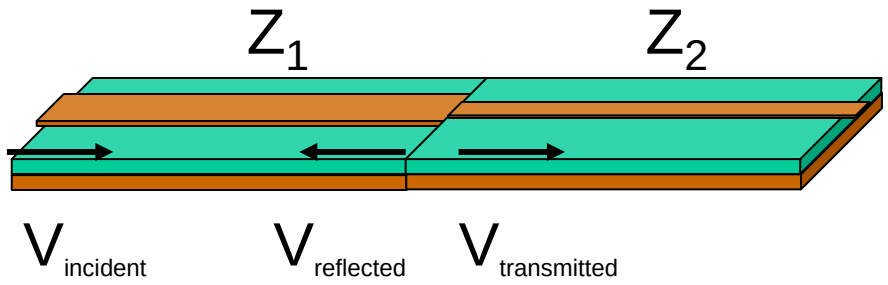
the capacitance per length increases, characteristic impedance decreases

$$Z_0 \sim \frac{1}{C_L}$$

Most Important Features of Characteristic Impedance

- Characteristic impedance is not about the signal path
- Characteristic impedance is not about the return path
- Characteristic impedance will depend both signal and return path, inseparably
- There is no such thing as the characteristic impedance of a single pin
- Change the return path configuration, you change the characteristic impedance
- ***(Obviously, the same goes for insertion loss!)***

Fundamental Property of Signals on Transmission Lines: Reflections

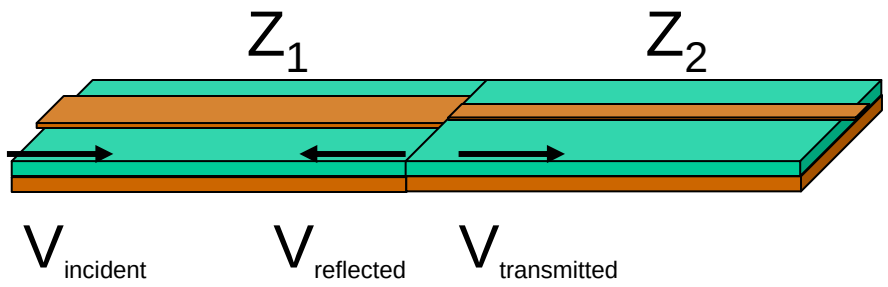


Z is instantaneous impedance

$$S_{11} = \frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1} \qquad S_{11} = \frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - 50\Omega}{Z_2 + 50\Omega}$$

1. Reflections from an open?
2. Reflections from a short?
3. Reflections from a "matched" load?

Fundamental Property of Signals on Transmission Lines: Transmission

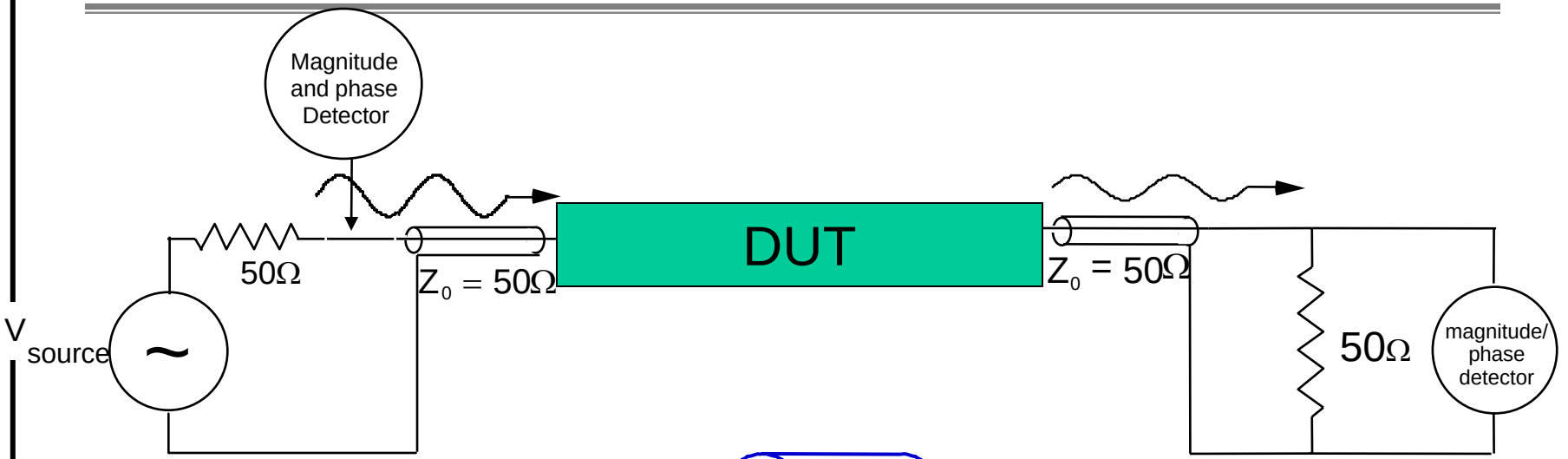


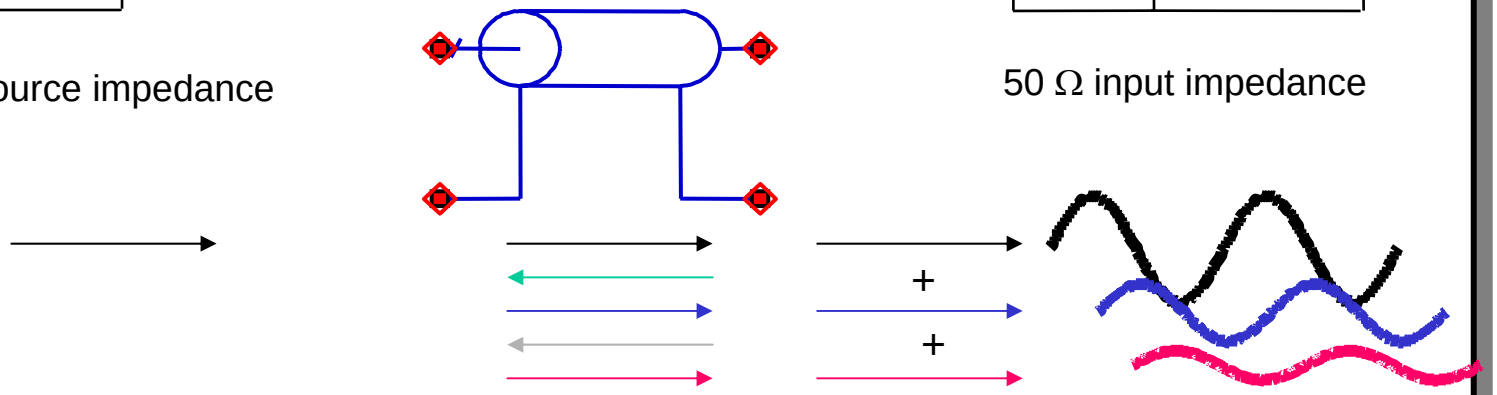
$$S_{21} = \frac{V_{transmitted}}{V_{incident}} = \frac{2\ x\ Z_2}{Z_2 + Z_1}$$

$$S_{21} = \frac{V_{transmitted}}{V_{incident}} = \frac{2\ x\ Z_2}{Z_2 + 50\Omega}$$

S_{21} for 50 Ohms?
S_{21} for 40 Ohms?

Insertion Loss





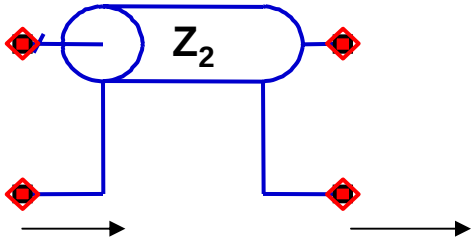
$S_{21} \sim Z_0 \sinh(\gamma \times len)$

Insertion Loss and Transmission Lines

- Depends on:
  - ✓ Change in characteristic impedance from 50 Ohms
  - ✓ Time Delay
  - ✓ Highest frequency

$$S_{21} = \frac{V_{transmitted}}{V_{incident}} = \frac{2\ x\ Z_2}{Z_2 + Z_1}$$

1st order approximation:



IL_1 $\qquad$ IL_2

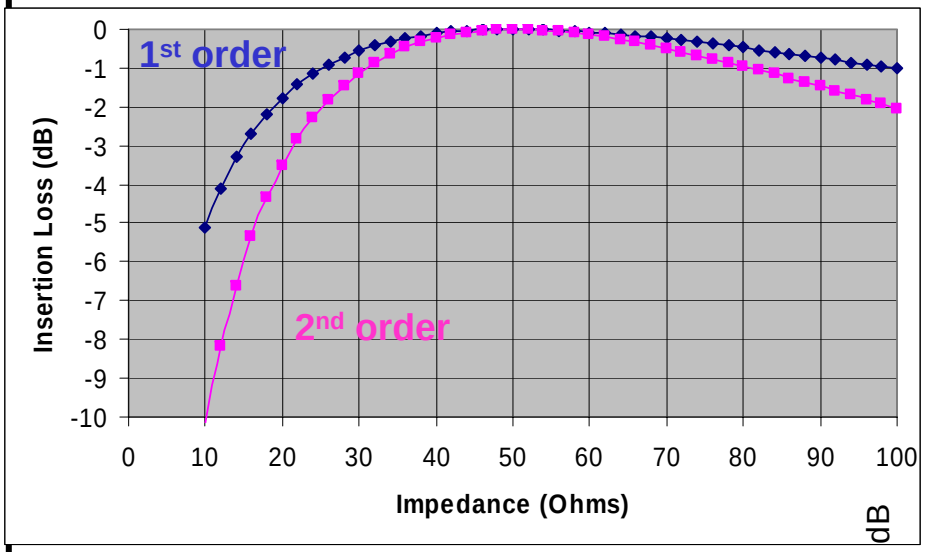
$$IL_1 = \frac{2\ x\ Z_2}{Z_2 + 50} \qquad IL_2 = \frac{2\ x\ 50}{50 + Z_2}$$

1st order:

$$IL = \frac{2\ x\ Z_2}{50 + Z_2}\ x\ \frac{2\ x\ 50}{50 + Z_2} = \frac{200\ x\ Z_2}{(50 + Z_2)^2}$$

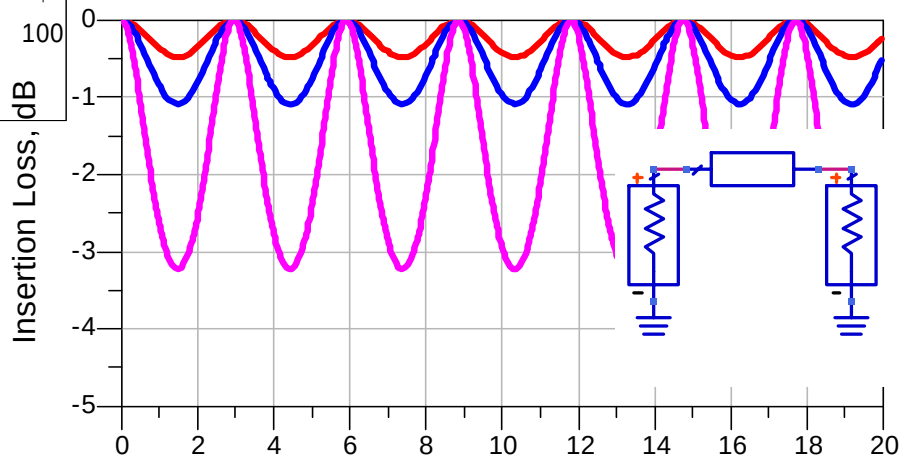
2st order: x 2 to account for the second reflection

Rough Estimates



2nd order Estimates

Z_0	Insertion Loss
70 Ohms	-0.5 dB
30 Ohms	-1 dB
20 Ohms	-3.2 dB

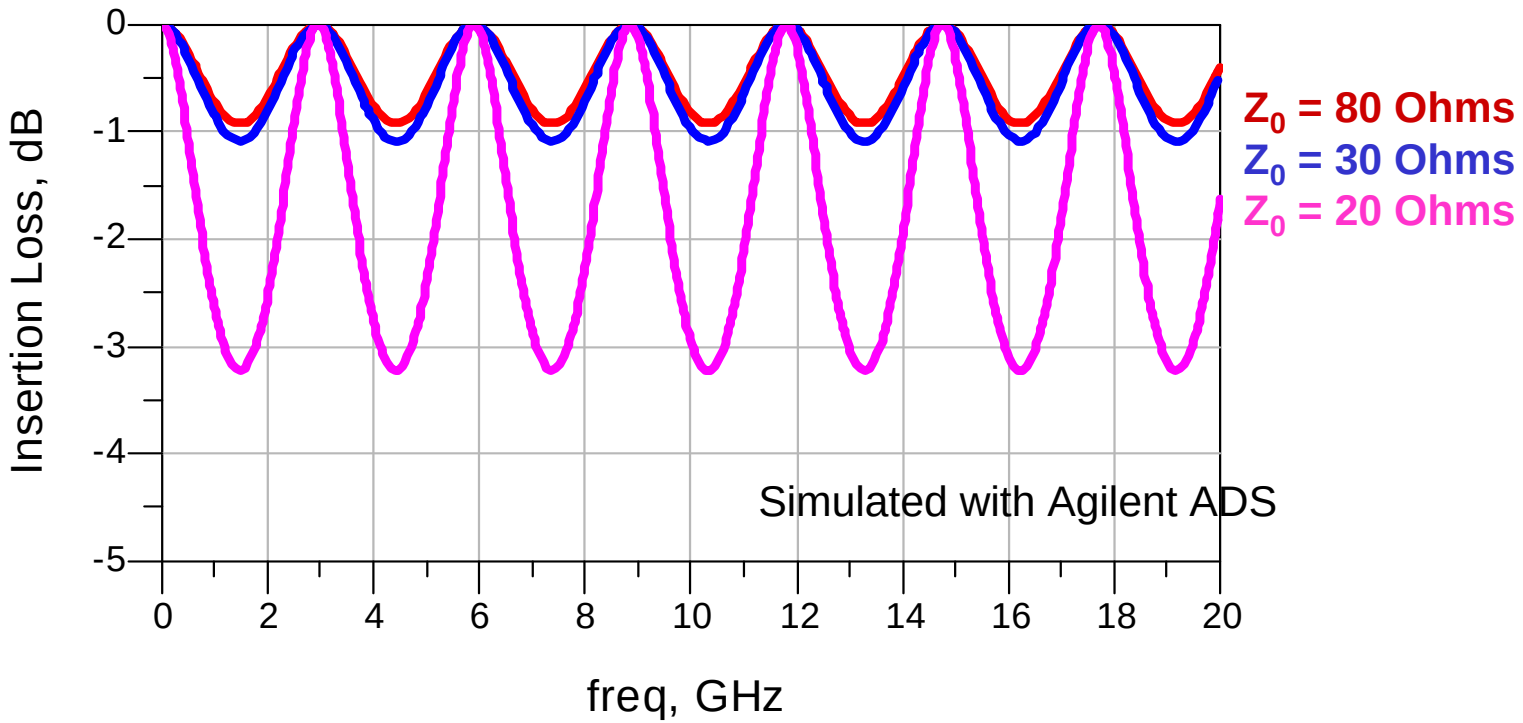


2nd order estimate: for > -1 dB insertion loss, keep 30 Ohms < Z_0 < 80 Ohms

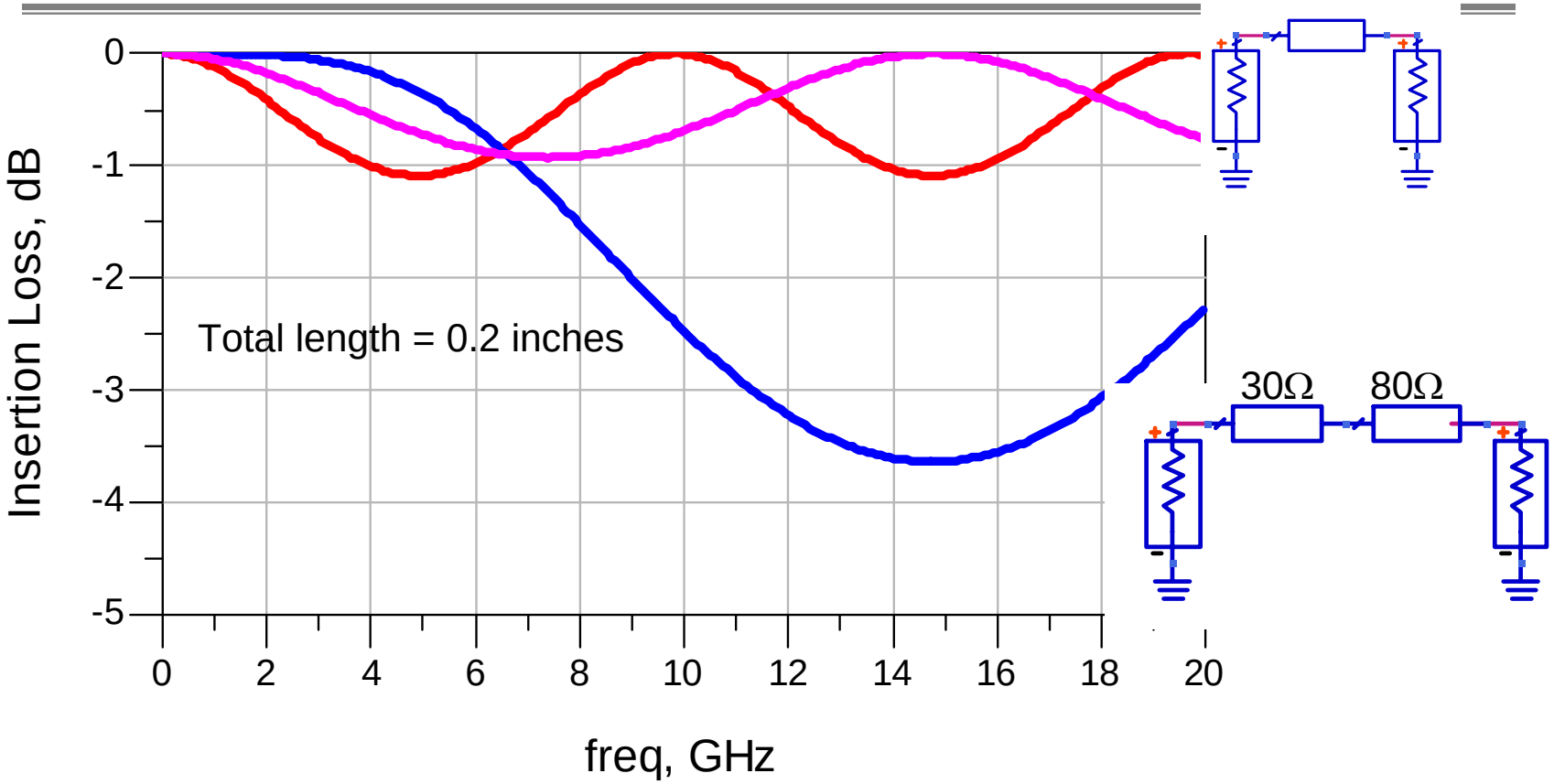
Simulated with Agilent ADS

Minimizing Insertion Loss Principle #1: Match Impedance to 50 Ohms

1. Uniform impedance interconnect
2. Match socket to 50 Ohms
3. Keep: 30 Ohms < Z_0 < 80 Ohms and insertion loss will never be greater than -1 dB

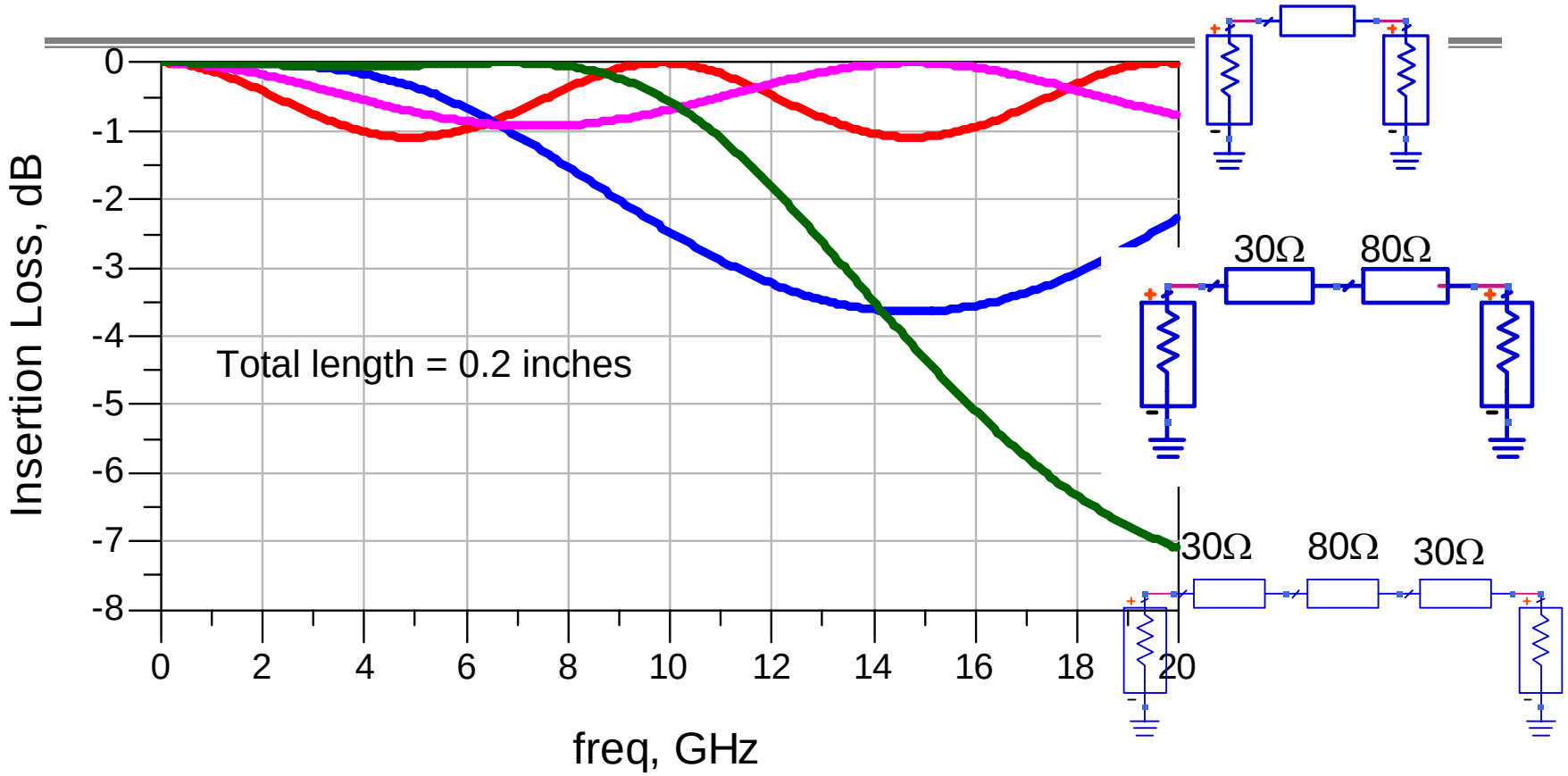


What if the Impedance is not Controlled?



- Low frequency behavior is related to ~ average impedance- can be better than either one
- Highest insertion loss can be much worse than either discontinuity (> 3x)

Three Impedance Discontinuities

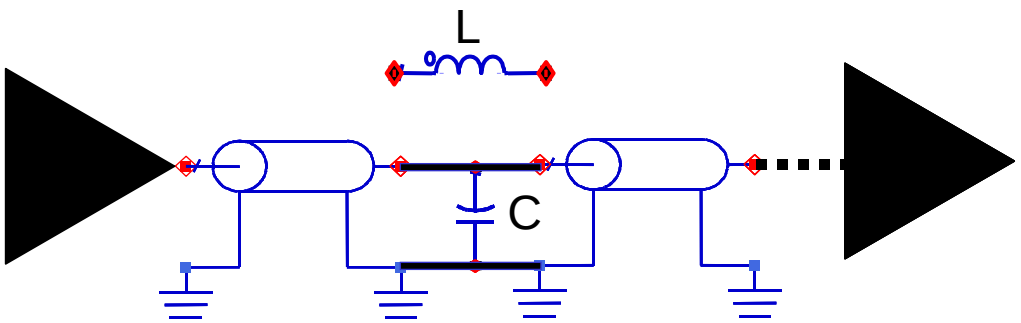


- Low frequency behavior is related to ~ average impedance- can be better than either one
- Highest insertion loss can be much worse than either discontinuity (> 7x)

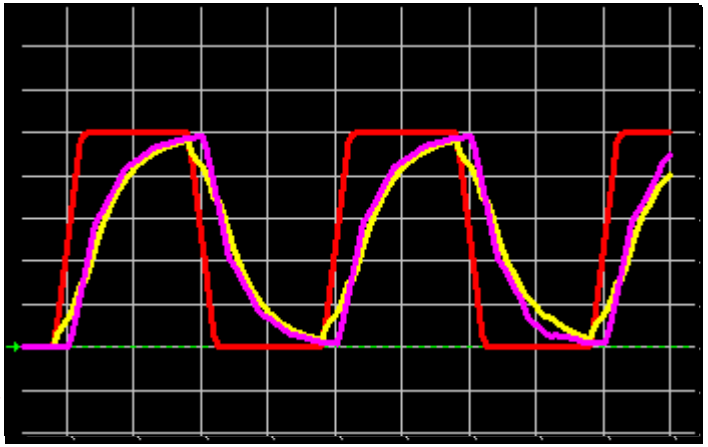
Minimizing Insertion Loss Principle #2: Use a controlled impedance interconnect

- Match average impedance to 50 Ohms
- Design for controlled impedance- uniform cross section

Time Domain Impact from C, L Discontinuities



50 psec/div



20 psec RT, no discontinuity

1 pF C discontinuity

Simulated with Hyperlynx

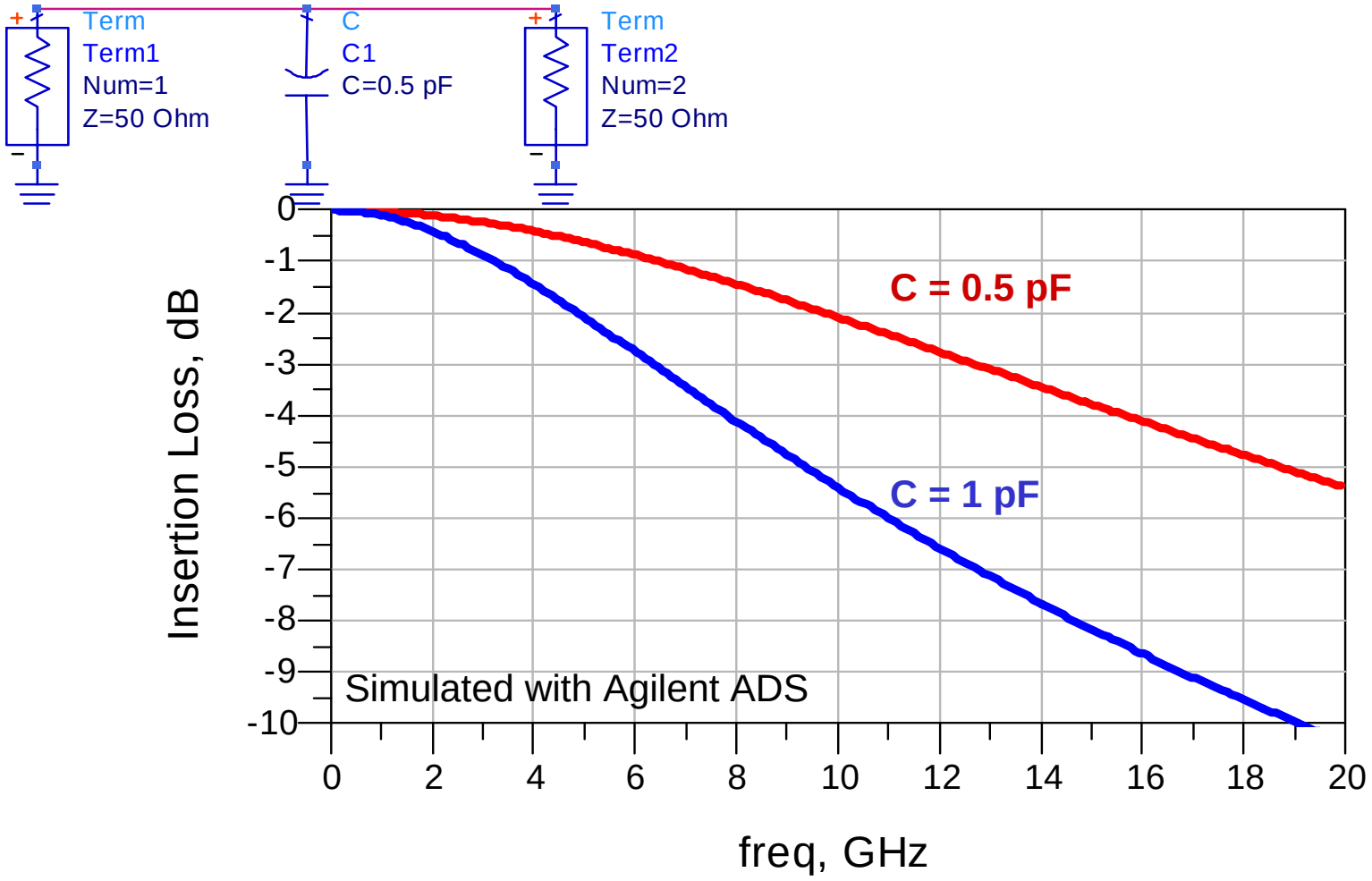
2.5 nH L discontinuity

Rise Time Degradation

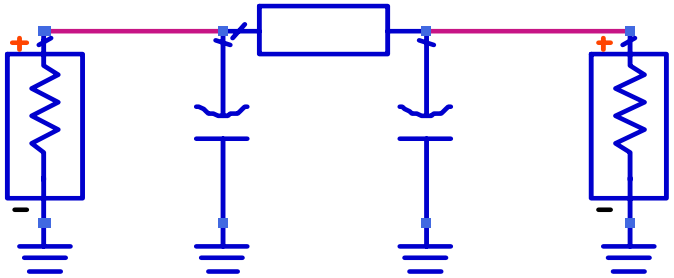
10%-90% RT = 2.2 x RC = 2.2 x ½ x Z_0 x C ~ Z_0 x C = 50 x 1 pF ~ 50 psec

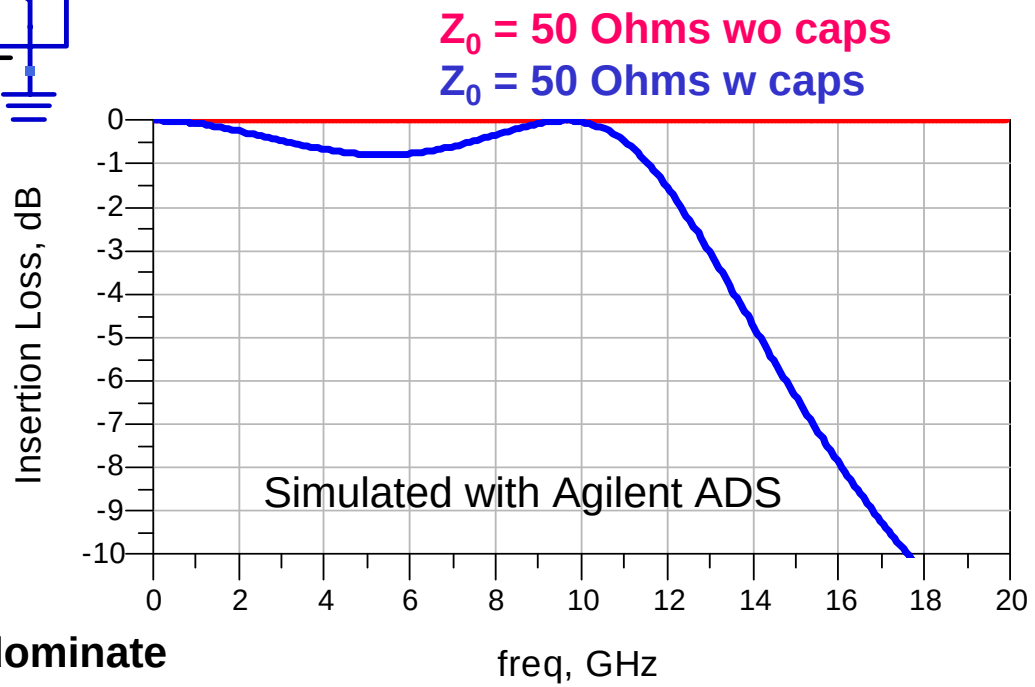
10%-90% RT = 2.2 x L/R = 2.2 x L/(2 x Z_0) ~ L/Z_0 = 2.5 nH/50 ~ 50 psec

Insertion Loss from Pad Capacitance



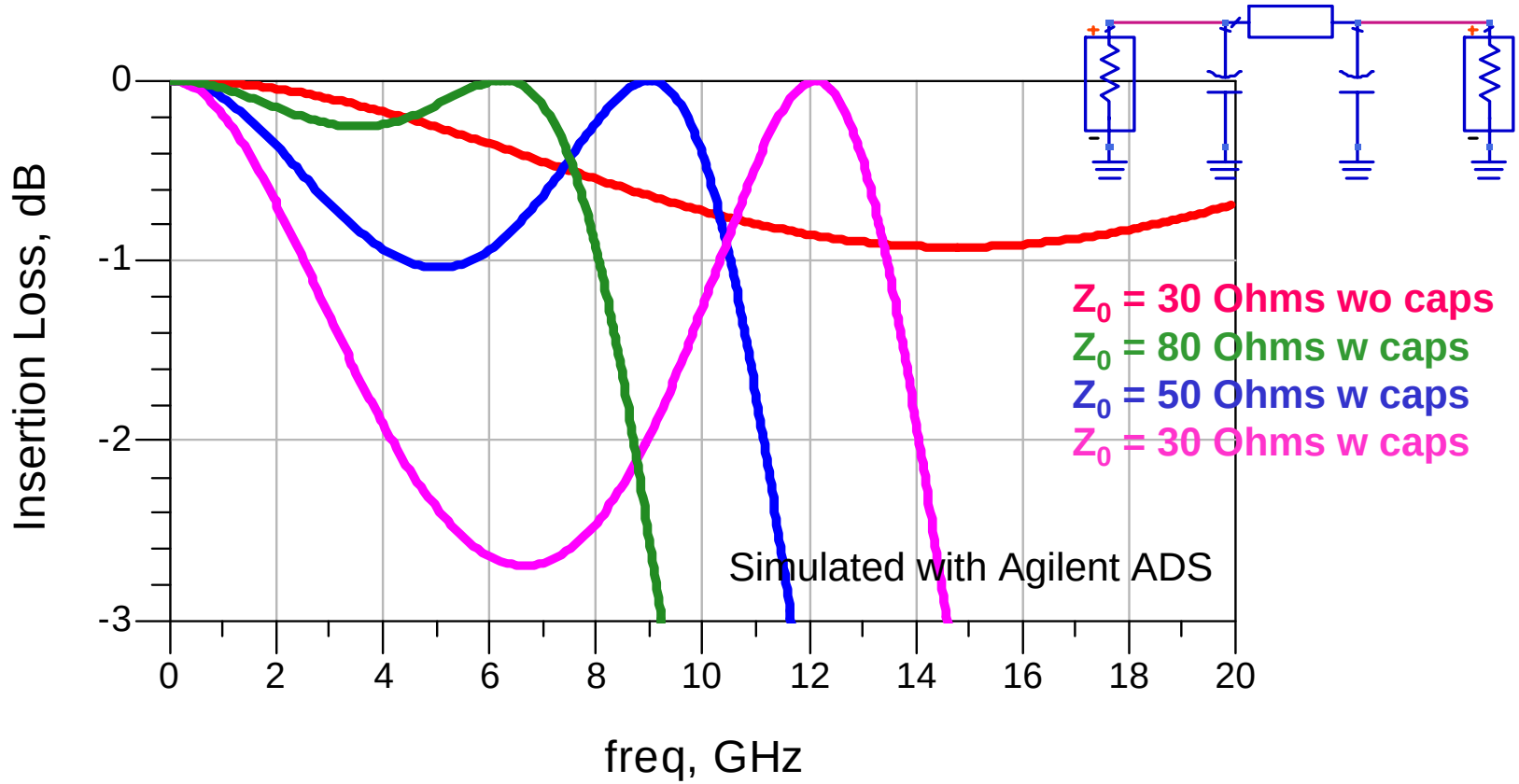
Impact from 0.5 pF Pads on Either Side of 50 Ohm, lossless, Ideal Socket





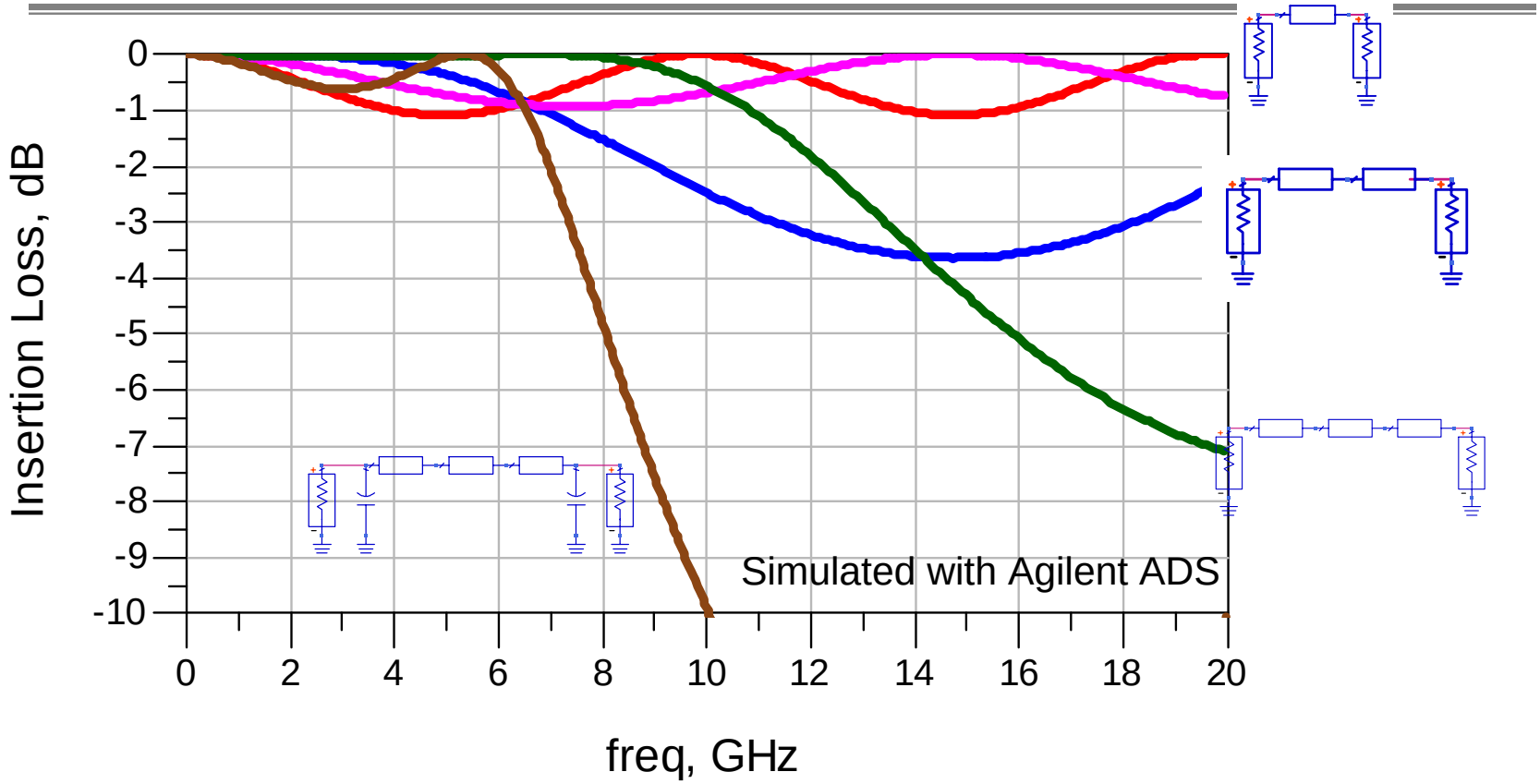
- **Pad capacitance can easily dominate insertion loss measurements**
- **For matched socket, best performance is with no pad capacitance**

Non matched socket and 0.5 pF Pad Capacitance



- **Lower the socket impedance, the greater the impact from pad capacitance**
- **An optimized socket will be degraded by pad capacitance**

Uncontrolled Impedance and Pad Capacitance



Impedance discontinuities can be disastrous

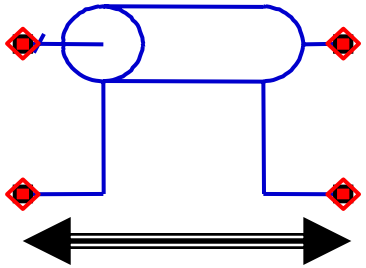
Minimizing Insertion Loss Principle #3: Minimize Pad Stack up Capacitance

- Pad stack up capacitance on test fixture/load board can and often does dominate insertion loss performance
- To first order, always try to minimize pad capacitance
- For best performance, optimize load board discontinuities to compensate: requires load board-socket-package co-design
  - ✓ Use 3D full wave solver
  - ✓ Use multiple test board launch designs to optimize pad stack up
  - ✓ Change socket and compensation may be off
  - ✓ When socket is well matched, performance is all about the load board

Time Delay and Length

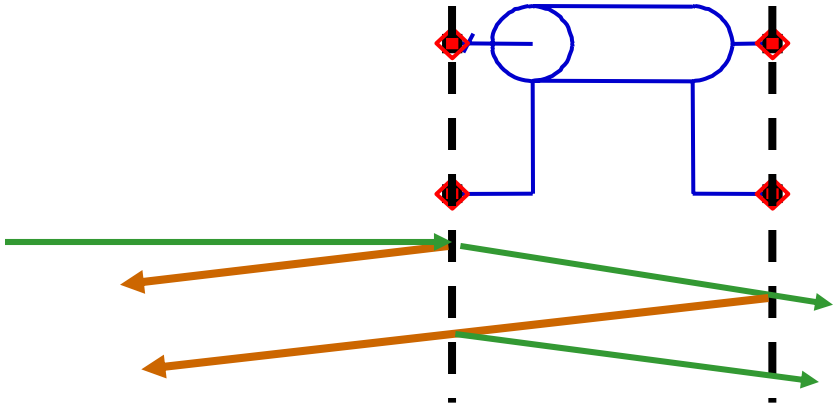
- Speed of signal ~ 6 inches/nsec = 150 mm/nsec in torlon, most polymers
- TD ~ Length / v = Len / 6 inches/nsec = Len x 160 psec/inch = Len x 6.7 psec/mm

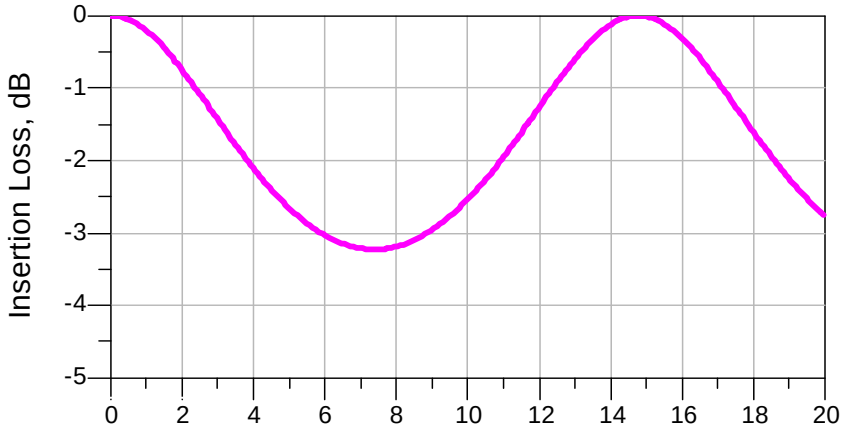
- Len = 100 mils, TD = 16 psec
- Len = 3 mm, TD = 20 psec



TD ~ 160 psec/inch
TD ~ 6.7 psec/mm

Insertion Loss and TD



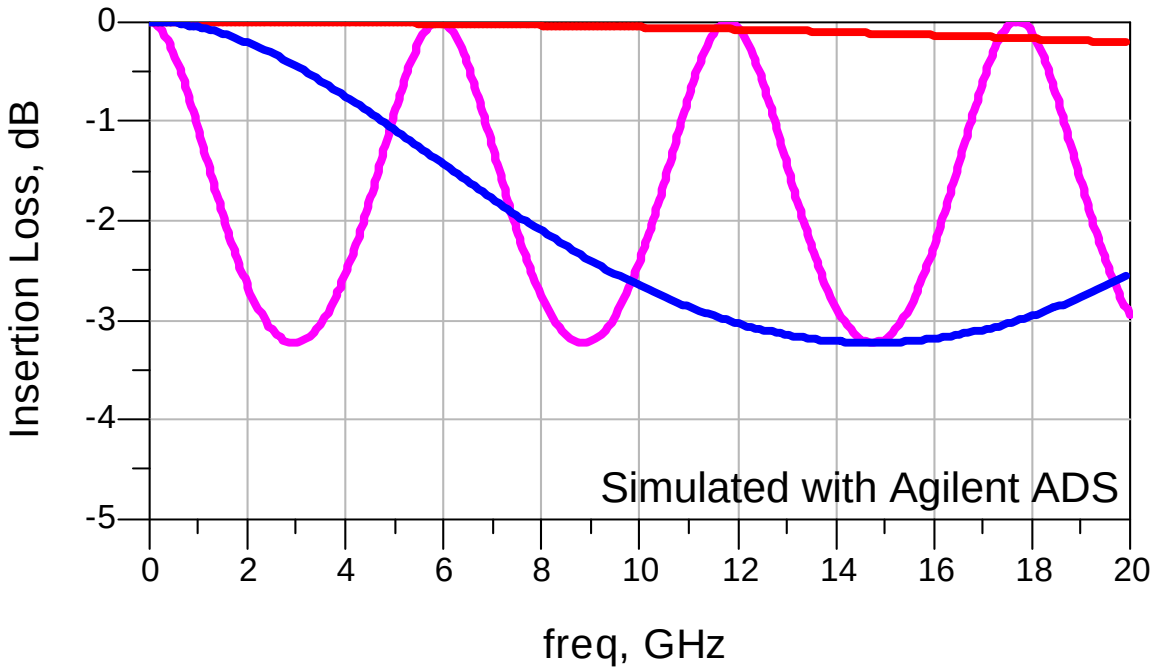


Simulated with Agilent ADS

- When Len << ¼ λ
  - ✓ Reflections from front and back, 180 deg out of phase
  - ✓ No reflection
  - ✓ All transmitted waves in phase and add
  - ✓ Max transmission
- When Len = ¼ λ
  - ✓ Reflected waves from front and back add
  - ✓ Maximum reflected signal
  - ✓ Transmitted waves 180 deg out of phase
  - ✓ Minimum transmitted signal

Same Impedance, changing Time Delay

Z_0 = 20 Ohms
Len = 10 mils (0.25 mm), 100 mils (2.5 mm), 500 mils (12.5 mm)



If Len << ¼ λ,
-1 dB insertion loss BW will be higher

Minimizing Insertion Loss: Principle #4

Try to keep length shorter than ¼ λ at the highest bandwidth

@ 1 GHz, ¼ λ = 1.50 inches, 38 mm

@ 10 GHz, ¼ λ = 150 mils, 3.8 mm

@ 20 GHz, ¼ λ = 75 mils, 1.9 mm

$$Len << \frac{1.5}{BW}$$

Len in inches
BW in GHz

$$Len << \frac{38}{BW}$$

Len in mm
BW in GHz

- If worst case insertion loss is less than -1 dB, TD may not be important
- If worst case insertion loss is greater than -1 dB, keep length << ¼ λ
- Minimize insertion loss by keeping length << ¼ λ
- Shorter is better, but long may be good enough

Attenuation from Dielectric Loss

$$\alpha = -4.34\left(\frac{R_L}{Z_0} + G_L Z_0\right) \text{ dB/length}$$

Conductor loss | Dielectric loss

$$G_L = \omega \tan(\delta) C$$

$$Z_0 = \frac{1}{\text{vel}\, C}$$

$$G_L Z_0 = \frac{\omega \tan(\delta)}{\text{vel}}$$

Independent of geometry!

$$\alpha_{\text{dielectric}} \approx -2.3 f \tan(\delta)\sqrt{\varepsilon_{\text{eff}}} \quad \text{dB/in}$$

S_{21} ~ - 2.3 x 0.02 x 2 x f = - 0.1 x f dB/inch, f in GHz

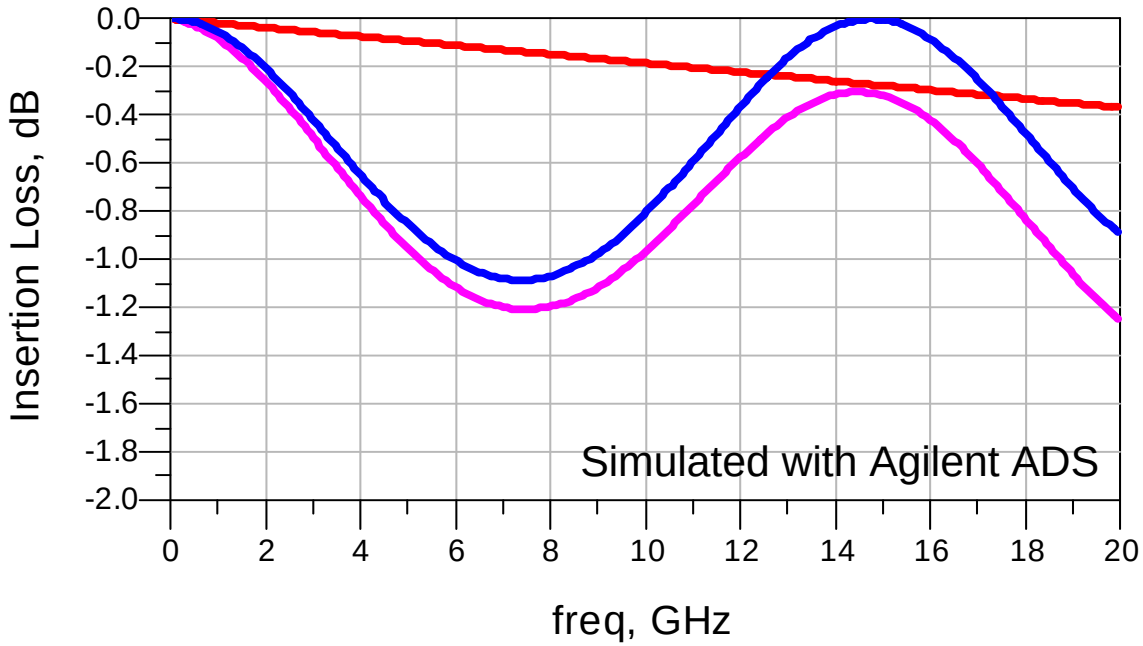
Insertion Loss From Dielectric Loss

Rule of thumb: lossy materials, tan(δ) = 0.02: α ~ - 0.1 dB/inch/GHz

S_{21} ~ -0.1 dB/inch x f (f in GHz)

Estimate: 0.2 inches, 10 GHz

S_{21} = -0.1 x 0.2 x 10 ~ -0.2 dB



50 Ohms, tan(δ) = 0.02
30 Ohms, tan(δ) =0
30 Ohms, tan(δ) = 0.02

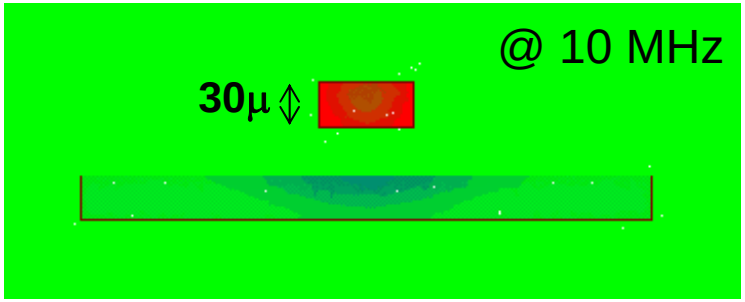
Minimizing Insertion Loss: Principle #5

- If impedance is matched, dielectric loss is only a problem for very long interconnects (Len > 0.5 inches)
- If impedance is not matched, dielectric loss has small impact
- Shorter is always better, but long be good enough

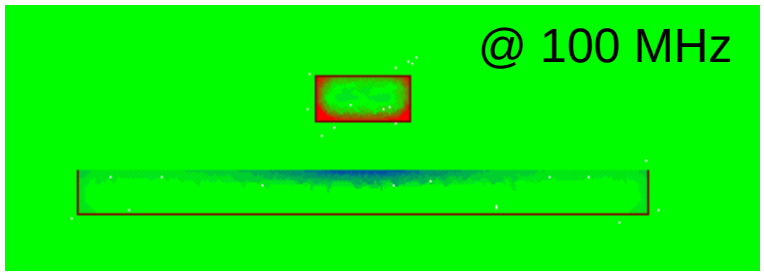
Current Distributions

- At DC, what is the current distribution?
- Current distributes to minimize the impedance
- Impedance is R + iωL
- As frequency goes up, minimizing loop L is more dominant
- To minimize loop L, two opposing forces:
  - ✓ Within each conductor, current will move as far apart as possible (minimize partial self inductance- **skin effect**)
  - ✓ Signal current will move as close as possible to return current (maximize partial mutual inductance- **proximity effect**)

Current Distributions Calculated with Ansoft 2D Field Solver



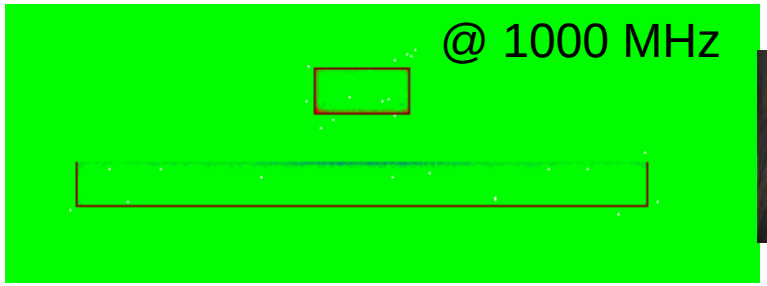
Microstrip:
50 Ohm, FR4
ε_r = 4.2
h = 38 μ
t = 30 μ (1 oz)
w = 75 μ



Above 10 MHz, all resistance is skin depth limited

$$\delta = \sqrt{\frac{1}{\sigma \pi \mu_0 \mu_r f}} = 2\mu\sqrt{\frac{1}{f}} \quad f \text{ in GHz}$$

in copper



Skin depth in copper ~ 2 microns @ 1 GHz

Conductor Loss

$$\alpha = -4.34\left(\frac{R_L}{Z_0} + G_L Z_0\right) \text{ dB/length}$$

Conductor loss **Dielectric loss**

α in dB/in
f in GHz
w is perimeter in mils
Z_0 in Ohms

OD = 10 mils
w = 3 x 10 = 30 mils

Simple first order model :

S_{21} ~ -0.02 dB/inch @ 1 GHz
(10% the insertion loss from dielectric loss)

$$\alpha_{conductor} \approx \frac{-22}{Z_0}\frac{\sqrt{f}}{w} \text{ dB/in}$$

@ 10 GHz, 0.1 inch long
S21 ~ -0.02 dB/inch x 0.1 inch x 3 = ~-0.01 dB

Minimizing Insertion Loss: Principle #6

- Current distributions above 1 GHz are all skin depth limited
- Series resistance from skin depth has no impact on insertion loss for most structures with OD > 1 mils

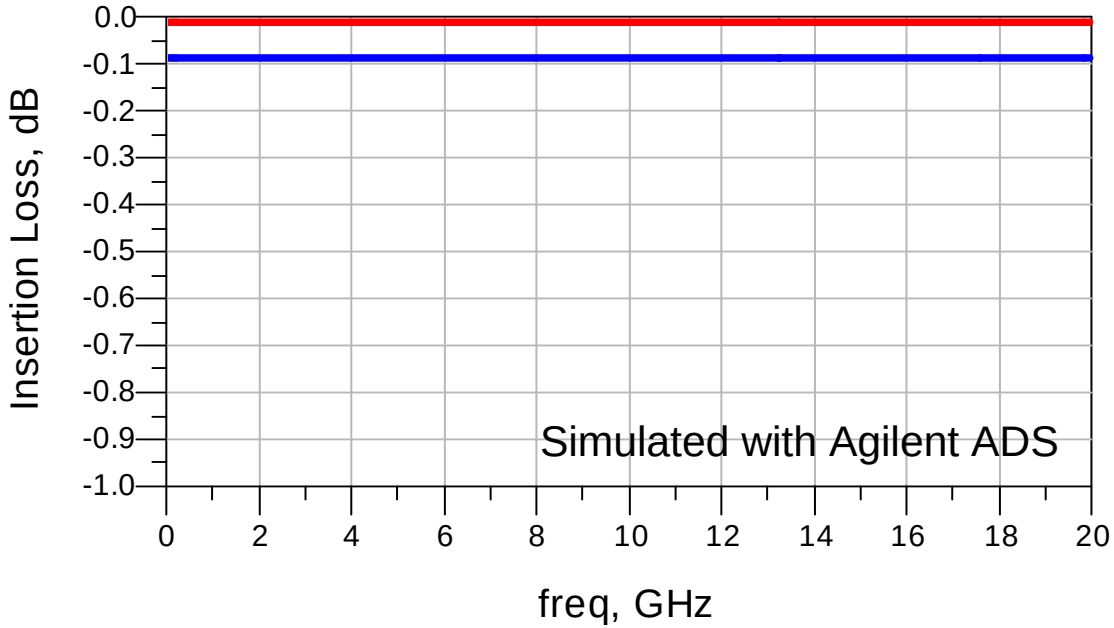
Impact from DC contact resistance

$$\alpha = -4.34\left(\frac{R_L}{Z_0} + G_L Z_0\right) \text{ dB/length}$$

Conductor loss — Dielectric loss

$$S_{21} \sim -4.34\ x\ \frac{R_{dc}}{50} \sim -\frac{R_{dc}}{10}$$

If R_{dc} = 0.1 Ohms, S_{21} ~ -0.01 dB
If R_{dc} = 1 Ohms, S21 ~ -0.1 dB



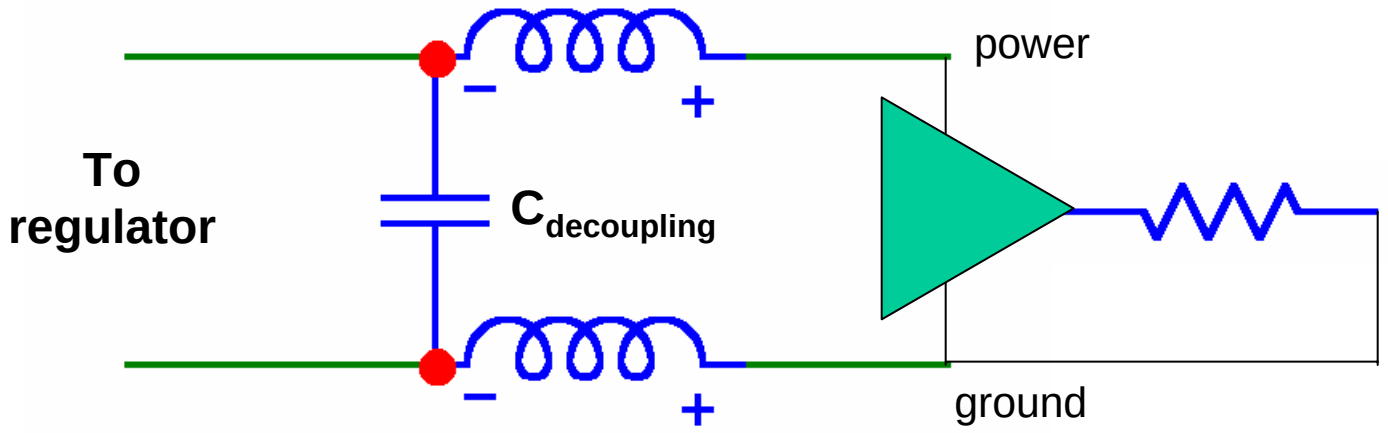
Minimizing Insertion Loss: Principle #7

- If contact resistance is so large that it affects insertion loss, you have a potential open problem, not an insertion loss problem

7 Principles of Socket Design for Optimized Insertion Loss

1. match characteristic impedance of socket to 50 Ohms
2. Keep the impedance constant through socket
3. Optimize (minimize) pad stack up capacitance
4. Keep socket short
5. Dielectric loss of socket not critical
6. Conductor loss of socket not critical
7. Contact resistance of socket not critical

Power Integrity



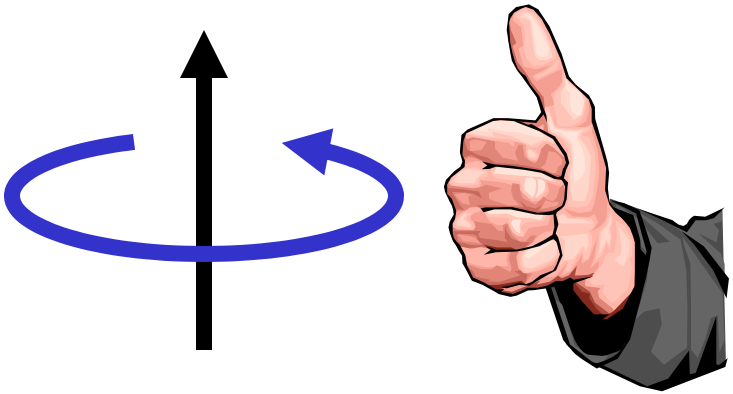
- Goal: keep the voltage across the power pins constant, even with current surges
- Strategy: minimize the impedance of the power distribution
- At high frequency, $Z = R + i\omega L$
- L is the loop inductance of the power and ground return path

What is inductance?

- ✓
- ✓
- ✓
- ✓

Inductance Principles -1

1. Magnetic field lines are around all current carrying conductors



Right hand rule

wire carrying a current

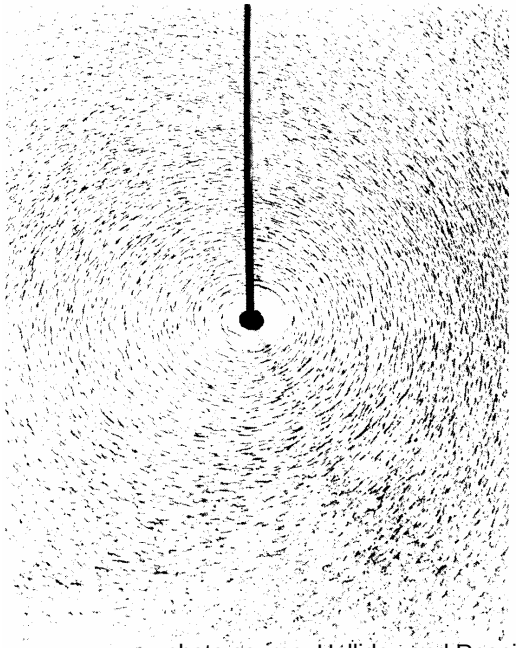
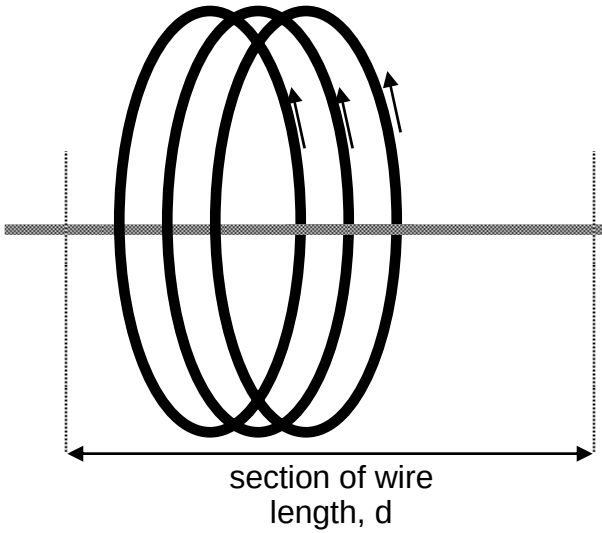


photo source: Halliday and Resnick, Physics, 1962

What influences the number of field lines?

Counting Magnetic Field Lines

How many field lines completely surround this section of the wire?



Current

# of field lines ~ current in the wire

Right hand rule determines direction

A ***Weber*** of field lines

Inductance Principles -2

2. Inductance is related to the number of field lines around the conductor, per amp of current through it

L = # of field lines around conductor, per amp of current

Units: Webers/amp = Henry
nH more common

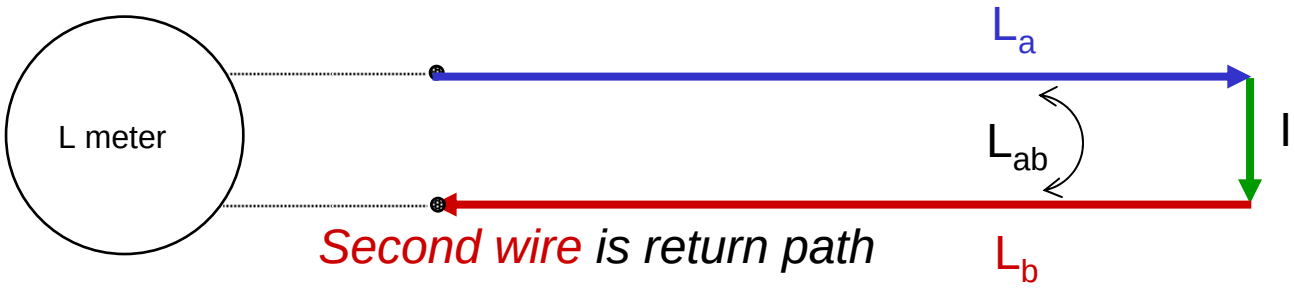
Many flavors of inductance:

self - mutual

loop - partial

total, net or effective

Loop Inductance



$$L_{loop} = L_a + L_b - 2L_{ab}$$

To reduce L_{loop}, what do we want to do to:

L_a

L_b

L_{ab}

How?

Four principles for minimizing Loop Inductance

1. Short lengths
2. Wide conductors
3. Closely spaced return path
4. Multiple power-return conductors in parallel

Estimating Loop Inductance from Characteristic Impedance

- For any controlled impedance interconnect, by definition:
  - ✓ $L_{loop} = TD \times Z_0$
  - ✓ Example 1: 50 Ohms, TD ~ 20 psec, L_{loop} = 1 nH
- L_{loop} ~ 170 psec/inch x Z_0 x Len = 6.8 psec/mm x Z_0 x Len
- Examples:
  - ✓ Z_0 = 50 Ohms, Len = 3 mm L_{loop} = 6.8 x 50 x 3 = 1 nH
  - ✓ Z_0 = 50 Ohms, Len = 1.5 mm L_{loop} = 6.8 x 50 x 3 = 0.5 nH
  - ✓ Z_0 = 20 Ohms, Len = 3 mm L_{loop} = 6.8 x 20 x 3 = 0.4 nH
  - ✓ Z_0 = 50 Ohms, Len = 0.1 mm L_{loop} = 170 x 50 x 0.1 = 0.8 nH
  - ✓ Z_0 = 70 Ohms, Len = 0.15 mm L_{loop} = 170 70 x 0.15 = 1.8 nH

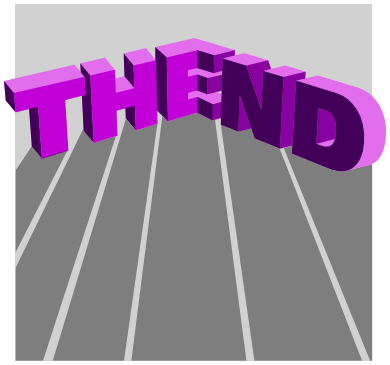
How to minimize Loop Inductance

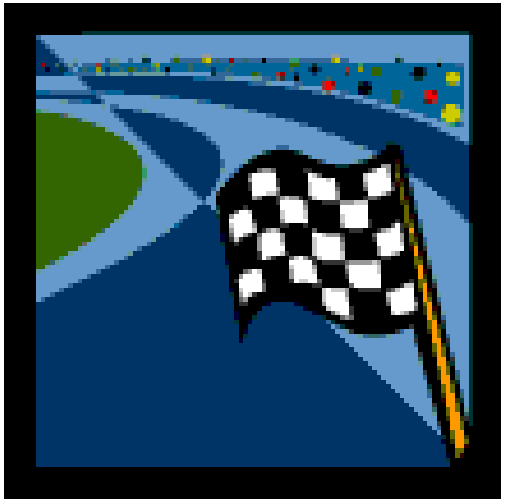
- How to minimize loop inductance:
  - ✓ Shorter socket
  - ✓ Lower impedance- close spacing, larger diameter pins, multiple return paths
- Use 2D or 3D field solver to estimate loop inductance

Signal Integrity of Sockets: Topics

- What does it mean to “work”?
- Signal integrity
  - ✓ Insertion loss
  - ✓ Bandwidth
  - ✓ Characteristic impedance
  - ✓ Time delay
  - ✓ Dielectric loss
  - ✓ Conductor loss
- Power integrity
  - ✓ Loop inductance
- Other:
  - ✓ Return loss
  - ✓ Differential impedance
  - ✓ Cross talk
  - ✓ Ground bounce

The End





SYNERGETIX®

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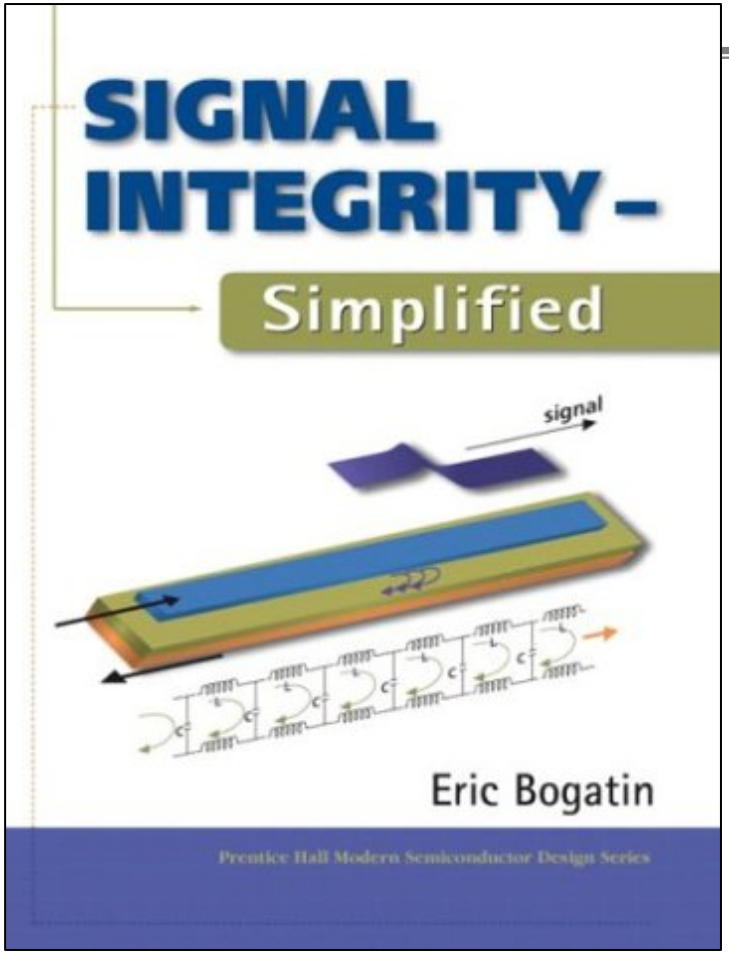

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