Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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Burn-in & Test Socket Workshop

Technical Program

Session 8
Wednesday 3/09/05 10:30AM

MANAGING FINE PITCH

"Challenges In Contactor Alignment For Fine Featured Packages"

Jon Diller – Synergetix
Kiley Beard – Synergetix **Ron Meek** – Synergetix

"Socketing The Unsocketable – Comparing Geometric Tolerances Of Semiconductor Devices To Burn-in And Test Sockets"

Thomas Allsup – Anida Technologies

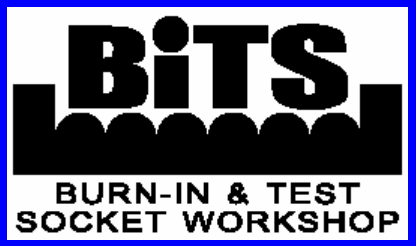
"A Review Of Contacting Systems For Burn-In Sockets At Pitches Of 0.5mm And Below"

James Forster – Texas Instruments **Prasanth Ambady** – Texas Instruments

Challenges in Contactor Alignment for Fine Featured Packages

2005 Burn-in and Test Socket Workshop

March 7 - 10, 2005

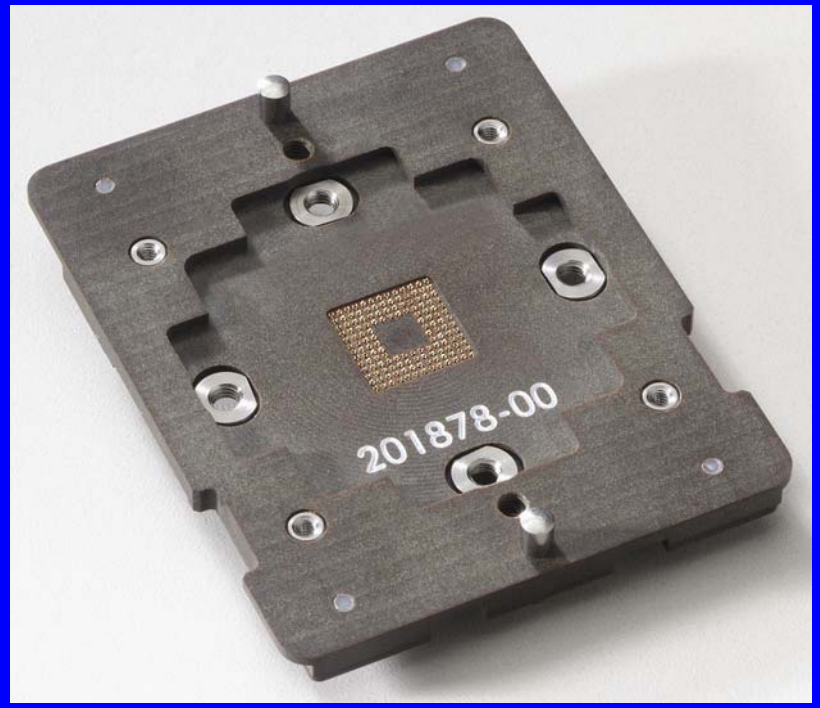


Jon Diller, Kiley Beard, and Ron Meek
Synergetix

Introduction

- Alignment critical for yield and throughput
- Situation worsening
- Focus on the contactor will have limited benefits

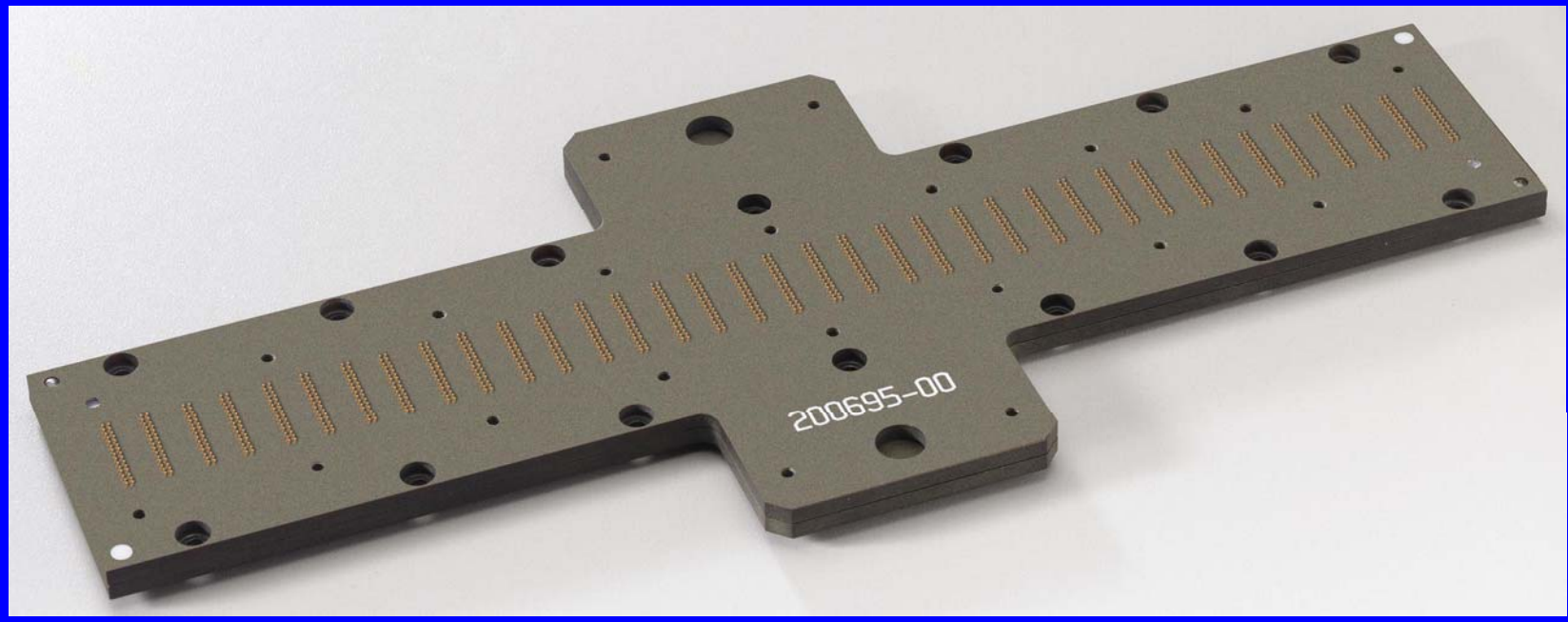
Methods of Alignment



- Edge (contactor or handler feature)

Methods of Alignment

- Optical Alignment (In-Strip or Singulated)

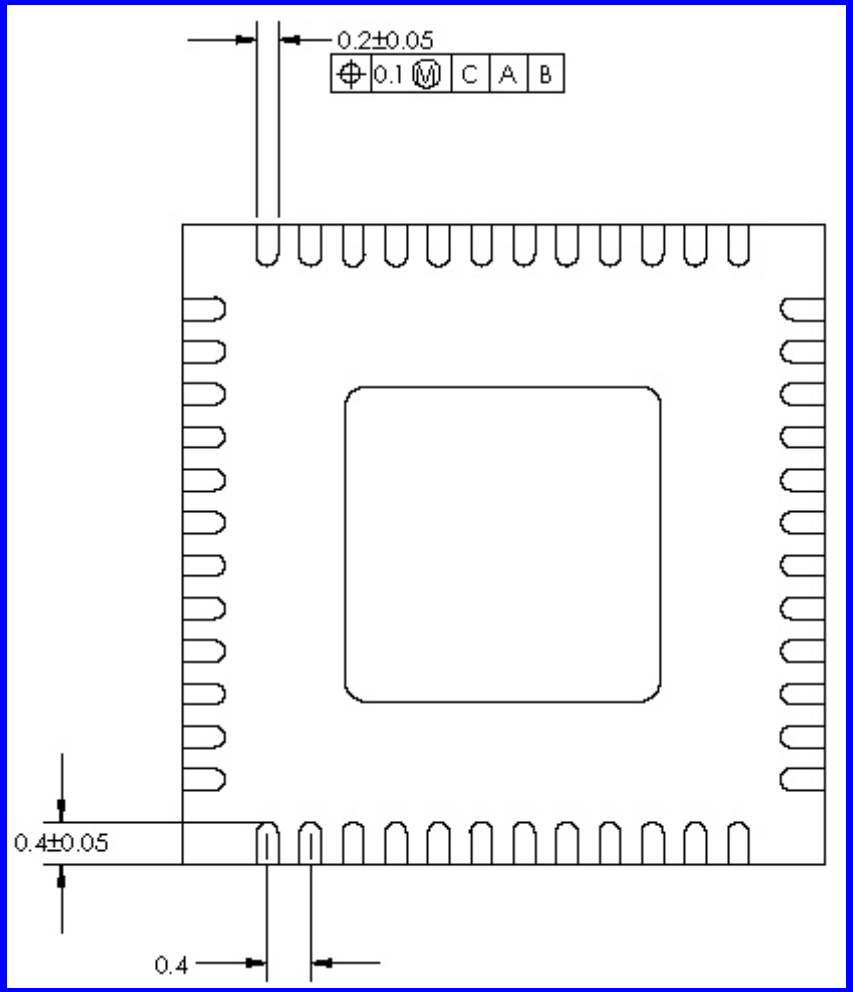


Effects of Poor Alignment

- Coarse alignment versus fine
- Extended setup
- First pass yield impact
- Shorting
- Stuck device
- Degrading alignment
- Contact wear

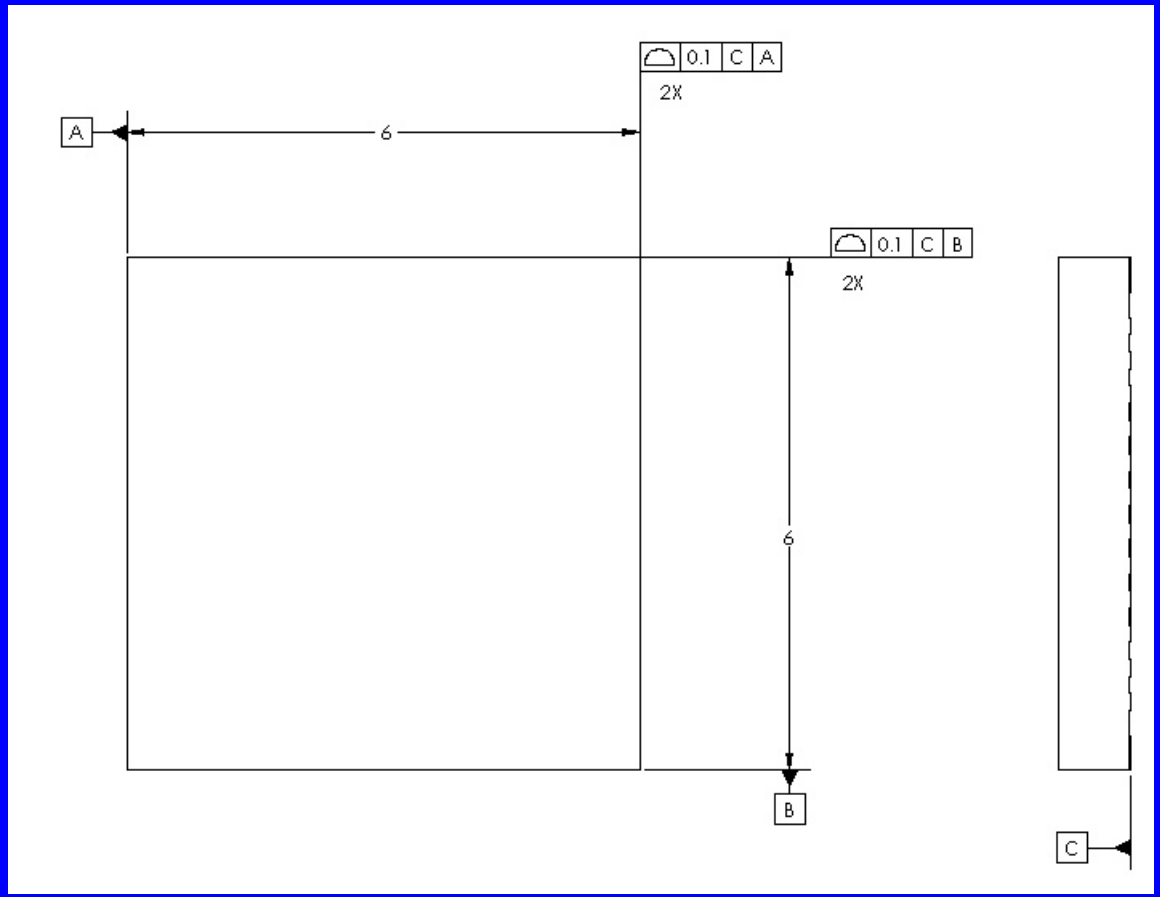
Factors in Alignment

- Package tolerances defining the target:
  - Lead size
  - Lead true position



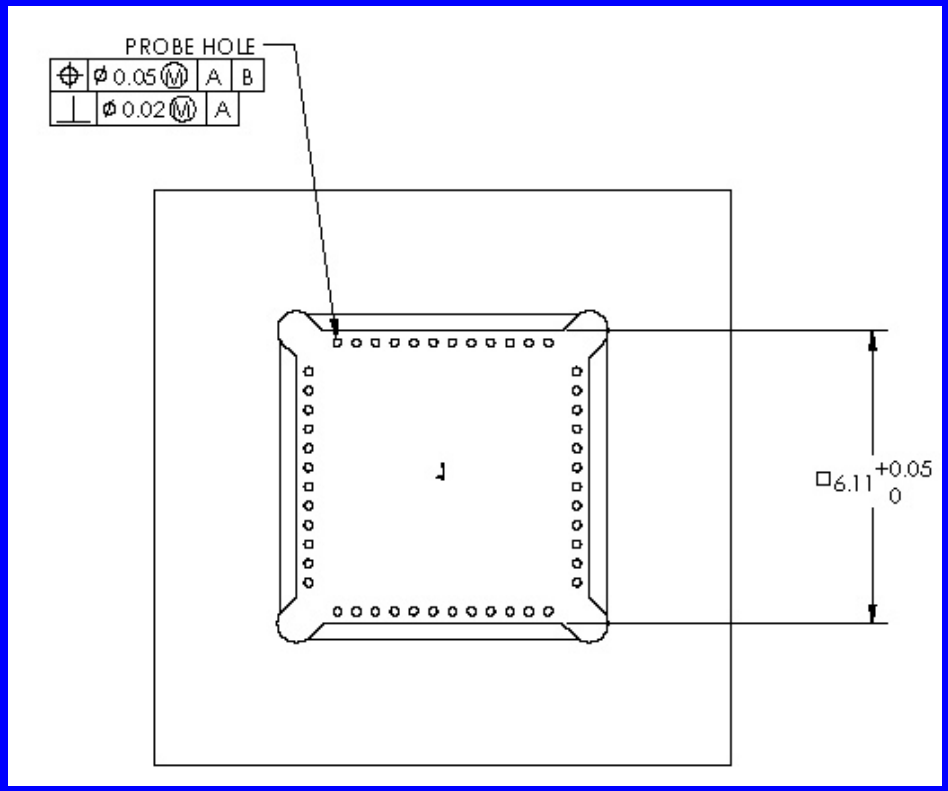
Factors in Alignment

- **Package tolerances limiting edge alignment:**
  - **Body size**



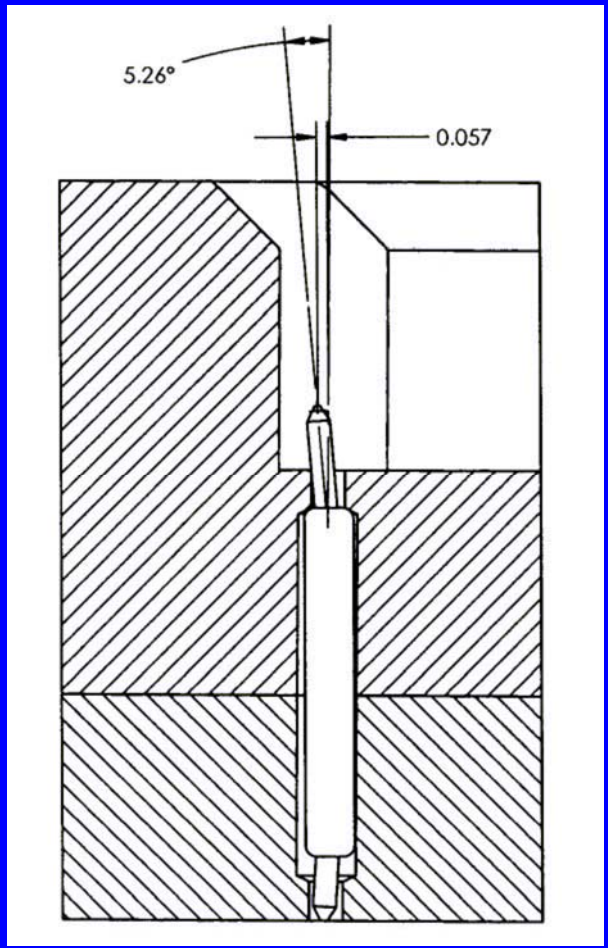
Factors in Alignment

- Contactor tolerances defining accuracy:
  - Pocket width
  - Contact hole true position
  - Contact position



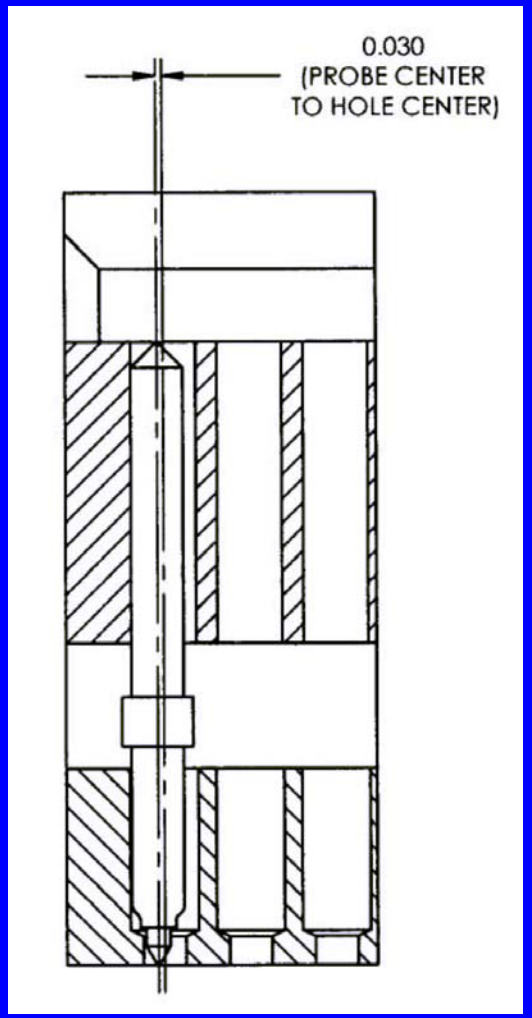
Contact Position: Lean

- Some columnar contacts lean
  - In 0.4 pitch, 3 mm length example, deviation was 0.06 mm



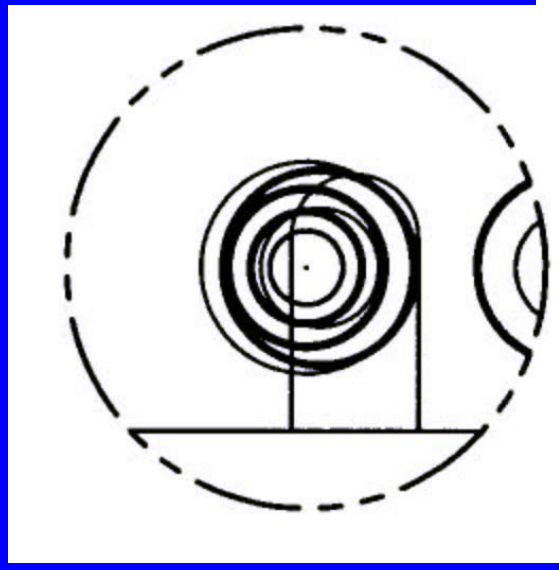
Contact Position: Shift

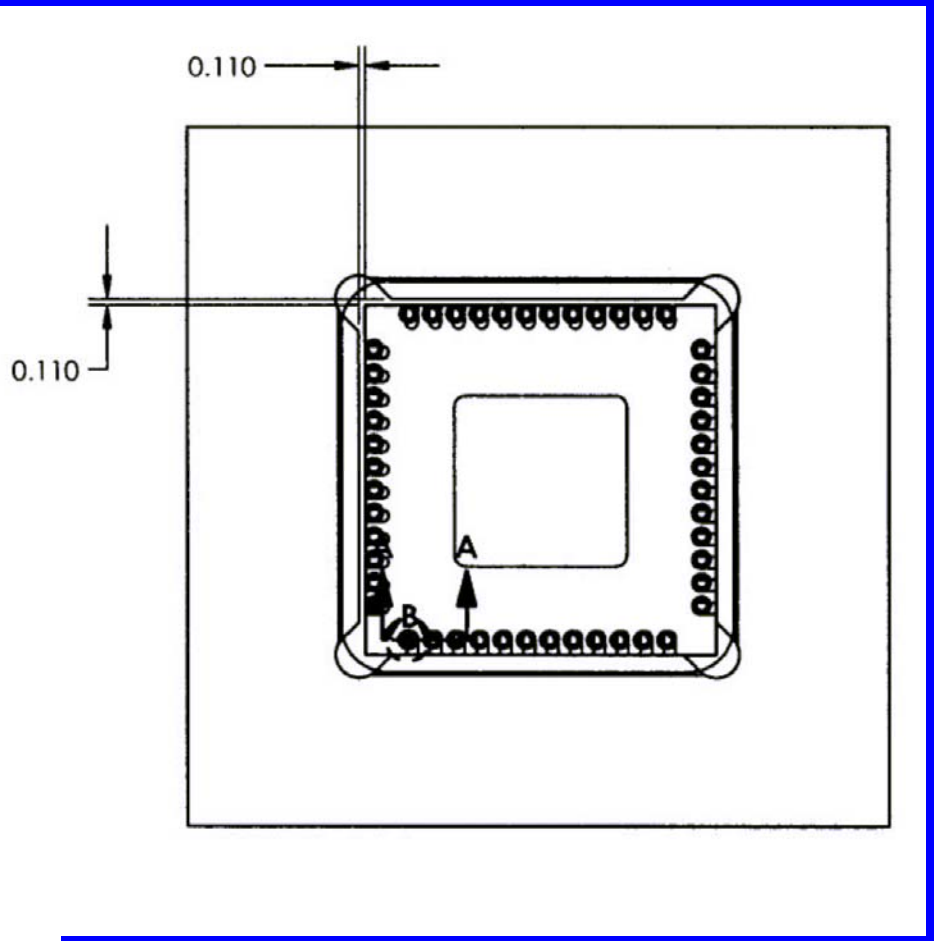
- Some columnar contacts shift
  - In 0.4 pitch, 3 mm length example, deviation was 0.03
  - Shift presumed in this paper



Device Shift

- **Device shifts diagonally in pocket**





Total Effect

Worst Case Tolerance Stack

Device Variables		
Maximum Device Width/Length (A)(mm)		6.100
Minimum Device Width/Length (B)(mm)		5.900
Maximum Pad Width (C)(mm)		0.250
Minimum Pad Width (D)(mm)		0.150
Pad True Position (E)(mm)		0.100
Socket Variables		
Device to Device Pocket Clearance Value (F)(mm)		0.010
Contact Shift (G)(mm)		0.030
Contact Hole True Position (H)(mm)		0.050
Pocket Edge Tolerance (per side) (J)(mm)		0.025
Equations		
Maximum Device Pocket (K)(mm)	=A+F+(J*2)	6.160
	=((K-B)/2)	
Centerline to Centerline Shift (Probe Contact Area to Device Pad) (L)(mm)	+(E/2)+(H/2) +G	0.235
Resulting Probe to Device Pad miscontact	=(D/2)-L	-0.160

Contactor Features Roadmap

- Contact true position from 0.05 to 0.025
- Pocket tolerance from 0.05 to 0.025
- Pocket gap from 0.02 to 0.01

Roadmap Effects

Worst Case Tolerance Stack (Improved Contactor Tolerances)

Device Variables		
Maximum Device Width/Length (A)(mm)		6.100
Minimum Device Width/Length (B)(mm)		5.900
Maximum Pad Width (C)(mm)		0.250
Minimum Pad Width (D)(mm)		0.150
Pad True Position (E)(mm)		0.100
Socket Variables		
Device to Device Pocket Clearance Value (F)(mm)		0.010
Contact Shift (G)(mm)		0.030
Contact Hole True Position (H)(mm)		0.025
Pocket Edge Tolerance (per side) (J)(mm)		0.013
Equations		
Maximum Device Pocket (K)(mm)	=A+F+(J*2)	6.135
	=((K-B)/2)	
Centerline to Centerline Shift (Probe Contact Area to	+(E/2)+(H/2)	
Device Pad) (L)(mm)	+G	0.21
Resulting Probe to Device Pad miscontact	=(D/2)-L	-0.135

Potential Improvement

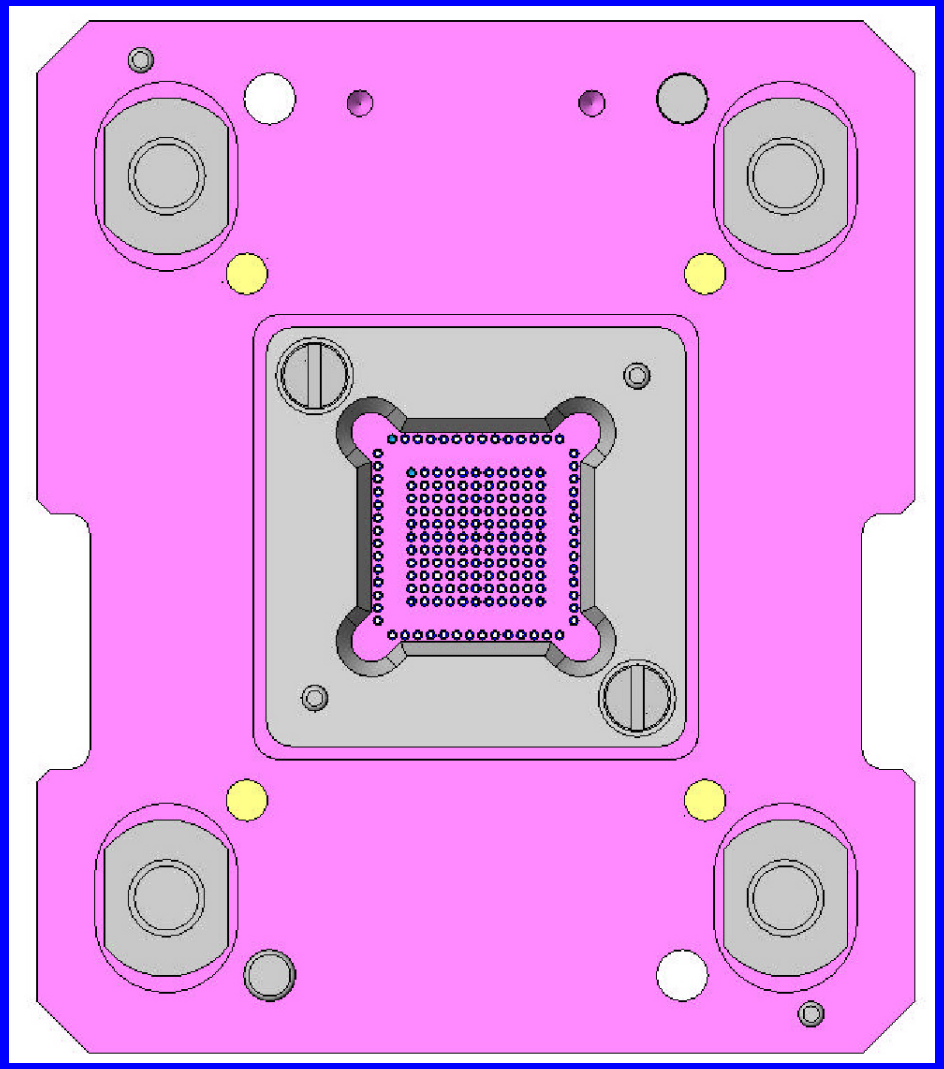
- **Singulated optical alignment**
- **Gang optical alignment (strip test)**

Worst Case Tolerance Stack (Optical Alignment)

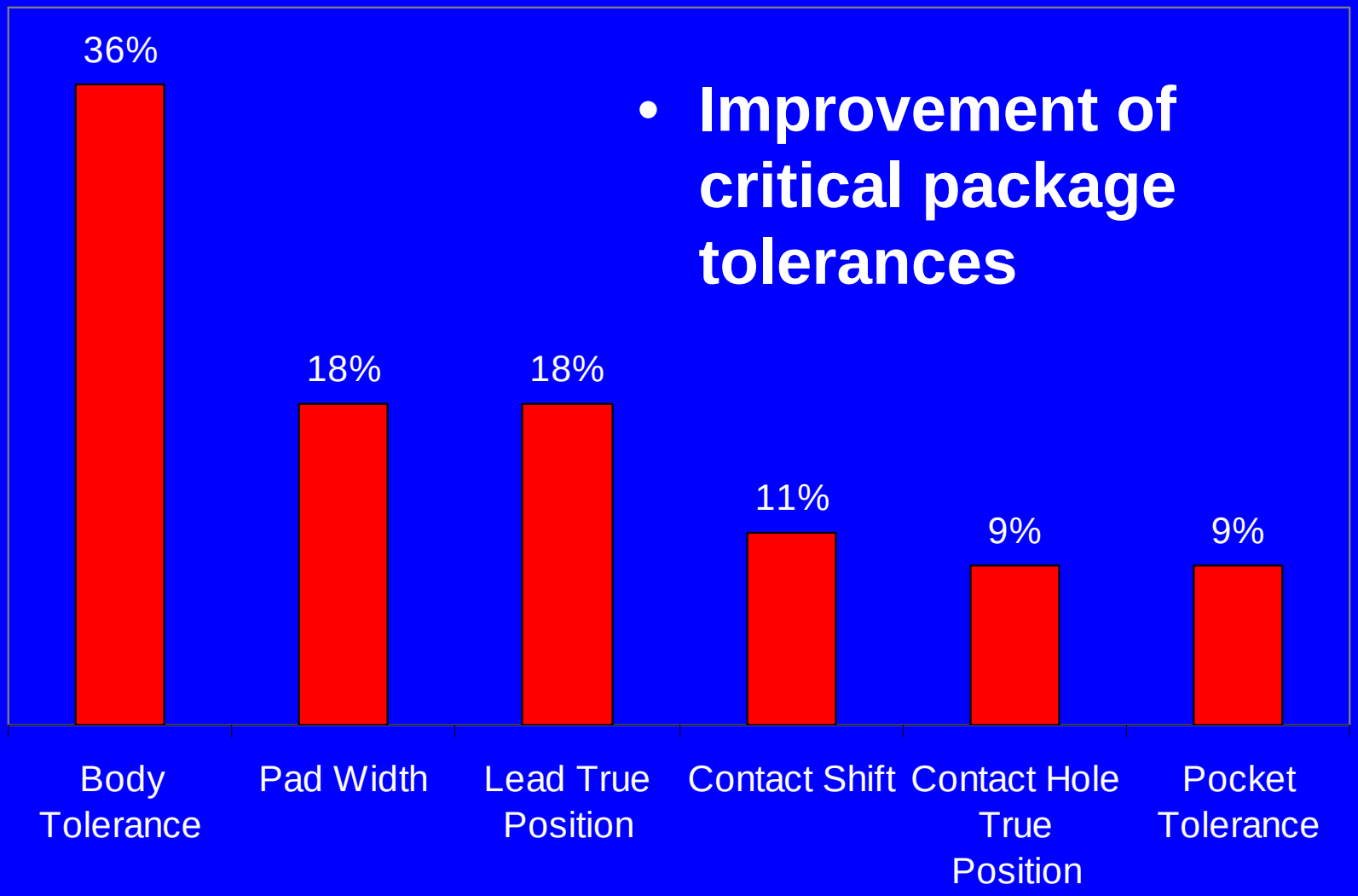
Device Variables		
Maximum Device Width/Length (A)(mm)		N/A
Minimum Device Width/Length (B)(mm)		N/A
Maximum Pad Width (C)(mm)		N/A
Minimum Pad Width (D)(mm)		0.150
Pad True Position (E)(mm)		0.100
Socket Variables		
Device to Device Pocket Clearance Value (F)(mm)		N/A
Probe Pointing Accuracy (G)(mm)		0.030
Probe Hole True Position (H)(mm)		0.050
Pocket Edge Tolerance (per side) (J)(mm)		0.025
Equations		
Maximum Device Pocket (K)(mm)	N/A	N/A
Centerline to Centerline Shift (Probe Contact Area to Device Pad) (L)(mm)	=(E/2) +(H/2)+G	0.105
Resulting Probe to Device Pad miscontact	=(D/2)-L	-0.030

Potential Improvement

- Sized sockets or removable nests
  - Adds a tolerance
  - Adds a maintenance step
  - Could address wear



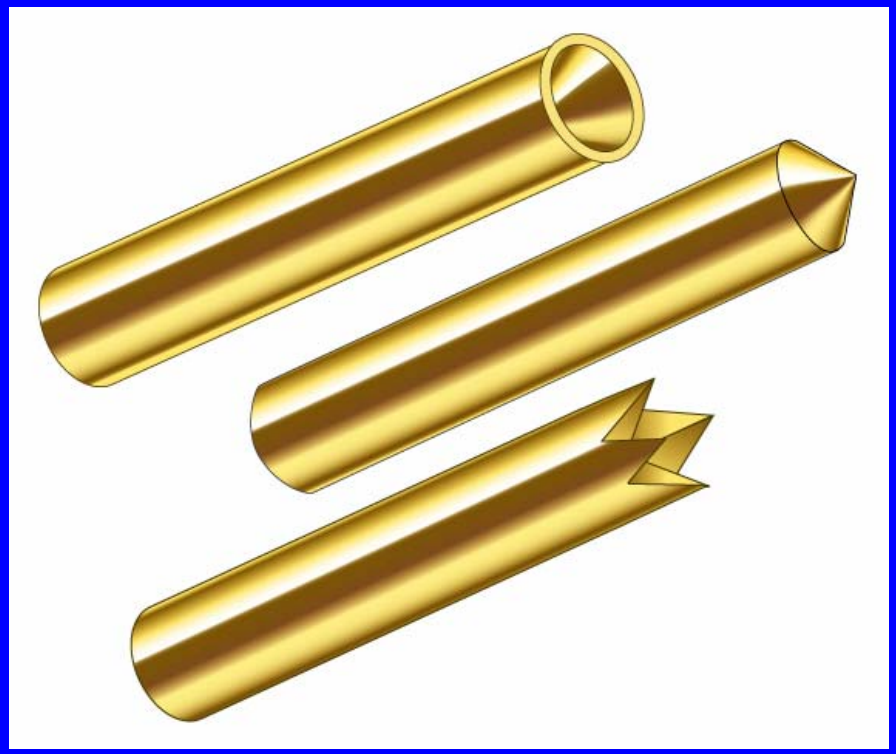
Possible Improvements



- **Improvement of critical package tolerances**

Possible Improvements

- Larger contact surface
  - Reduces contact pressure
  - Easier to contaminate
  - Potential for shorting



Conclusion

- Alignment is a critical, current issue
- Improvement through contactor refinement is at best a stopgap

- Optical alignment most promising
- Contactor and package design must respond

Socketing the Unsocketable

Comparing Geometric Tolerances of Semiconductor Devices to Burn-in and Test Sockets

BiTS™
Burn-in & Test Socket Workshop

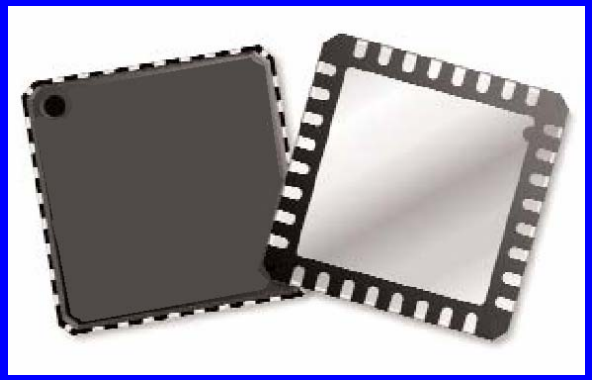
Thomas Allsup
Manager - Technology

anida technologies

Why Unsocketable?

Through hole semiconductor packages have leads that go into holes in a PCB.

Burn-in and Test sockets can easily duplicate PCB holes and align the package by the leads.



Surface mount semiconductor devices are designed to float on liquid solder and center themselves on the pads of a PCB.

It is difficult to approximate surface tension retention in Burn-in and Test sockets.

Outline

- **The Problem So Far**
  - *Once Upon a Time*
- **The Problem Is *Growing***
  - *Attack of the Incredible Shrinking Device*
- **Reading Device Drawings**
  - *Geometric Dimensioning for Dummies*
- **The Size of a Perfect Nest**
  - *We're going to need a bigger boat.*
- **Conclusion**
  - *And they all lived happily ever after.*

The Problem So Far

- Leadless semiconductor packaging designers are concerned with thermal performance and electrical characteristics and couldn't have cared less what about the outer package tolerances.
  - *Thankfully for socket manufacturers the pitch of semiconductors was many times larger than the package tolerance so the sockets worked well.*
- However, it didn't take long for the pitch of the semiconductors to approach the same magnitude as the package tolerance.

The Problem Is Growing

- Today, leadless semiconductor devices have pitches that are commonly very close to the package tolerance.
  - Common package tolerance is +/- 0.15mm profile tolerance about the perimeter.
  - Common package pitches are as low as 0.4mm and moving quickly to 0.25mm
- Every day, the pitch is continuing to shrink but the package tolerance remains constant.

Reading Device Drawings

- There's a foreign dialect to be learned if you are going to read package drawings called Geometric Dimensioning and Tolerancing:
  - *Also known as "GD&T"*
- There's some sub-dialects if you are reading ISO1101, MIL-STD-100, or ASME Y14.5M-1994 but the basics are all the same.
    - GD&T doesn't have a lot of new dimensioning, it is mainly just a refinement of tolerances.

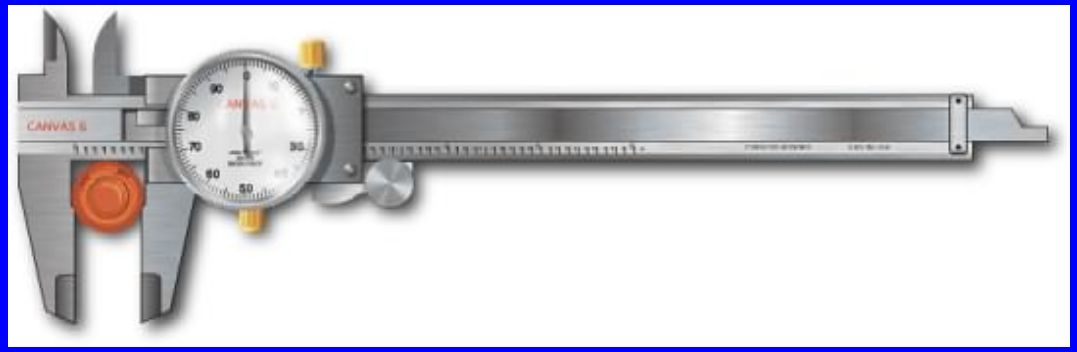
Size Isn't Important

- Physical features are grouped into two distinct regimes:
  - Features that do not depend on size
    - Single surfaces, planes, lines, etc.
  - "Features of size"
    - Plates, holes, slots, balls, ***center planes***, etc.
- Geometric tolerances for features of size can be ***modified*** according to the "size of the feature"

The “Caliper” Check

During GD&T training, you learn that features of size are things that you are measure with a pair of calipers using:

- Inside Jaws
- Outside Jaws
- Depth Gauge



What Does the Circled Letters Stand For?

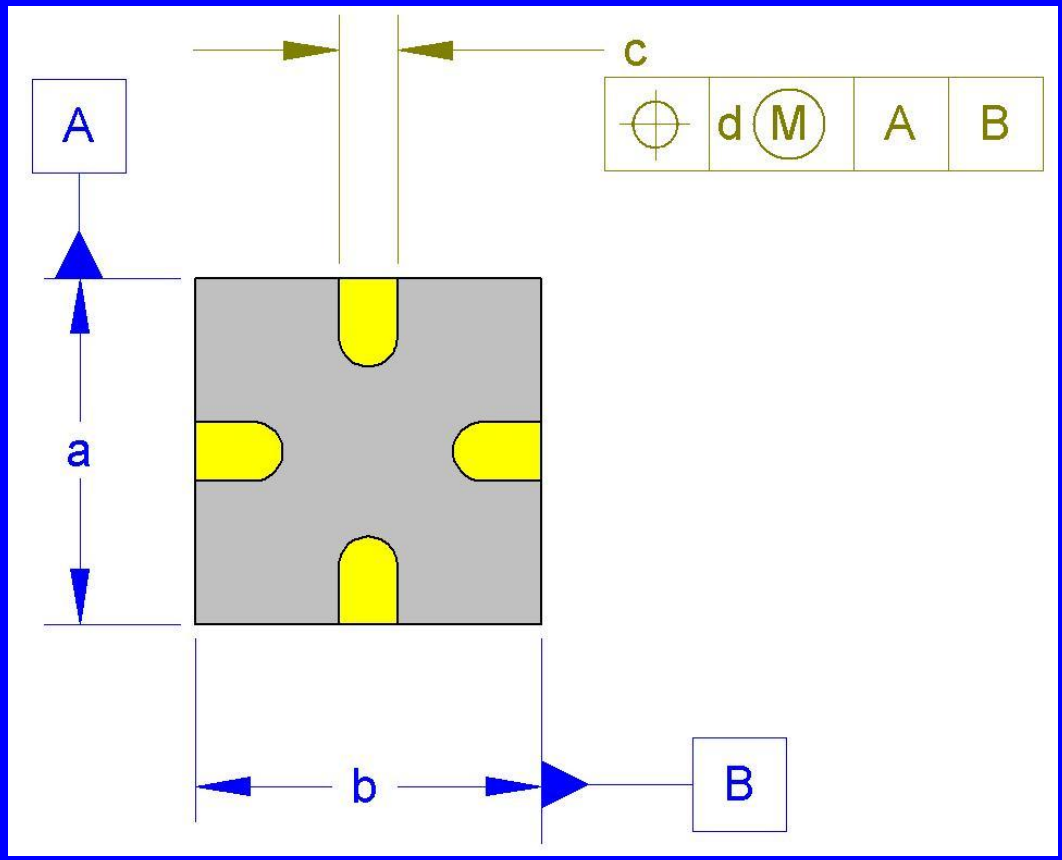
- The geometric tolerance for features of size can be modified in several methods but the two most important are:
  - Regardless of Feature Size (RFS)
  - Maximum Material Condition (MMC)
- There is also LMC, Tangent Plane, and Free State
  - For a good time, ask an ISO1101 person for an explanation of the Envelope modifier.

A Possible Bonus Tolerance?

- Regardless of Feature Size
  - This is the default if no modifier is given.
  - The tolerance zone is not affected by the actual size of the feature.
- Maximum Material Condition
  - The stated tolerance applies when the most material is there.
  - The tolerance zone increases when there is less material – you get a "***bonus tolerance***" if a hole is large.

How Does This Apply to Packages?

- Pads are features of size.
- Center datums based on the outer package are features of size.



In Practice The Theory Doesn't Work

- Theory: According to GD&T standards, the pad location tolerance would depend upon the actual size of the pad but not size of the package.
  - The outer package has to be "squeezed" by a vise like apparatus to establish the center plane.
- Practice: The pad location tolerance is highly dependent upon the pad size and the outer package.

The Size of a Perfect Nest

- The perfect socket nest that simulates the typical geometric tolerance callout requires the device must be gripped or squeezed together to establish the center plane of the device.
- Present sockets are designed to hold the largest possible device.
  - Designs are based on MMC of device.
  - Tolerances are RFS of device.

This Hasn't Been A Problem Before?

- When the pitch of devices was larger then the pads were larger.
  - Large being relative to the geometric tolerance.
  - Manufacturers have always produced the highest quality sockets.

But…

- Pitches and pads are getting smaller.
  - Better quality fixed position sockets won't handle the problem much longer.

Possible History Analogy

- The alignment of fiber optic electronic components to fiber optics evolved using the following techniques and was driven by shrinking size and tolerances.
  - Mechanical Alignment
  - Active Alignment
  - Video Alignment
- If Burn-in and Test sockets follow this path then the next generation of sockets will have active alignment.

Conclusion

- The purpose of this presentation wasn't to stop anyone from designing, buying, using, and / or cursing fixed size mechanical nests.
  - They work most of the time.
- The purpose of this presentation was two-fold:
  - The design of Burn-In and Test sockets will be evolving - probably sooner than later…
  - Everyone should learn another language – ***GD&T!***

A Review of Contacting Systems for Burn-In Sockets at Pitches of 0.5 mm and Below.

James Forster and Prasanth Ambady,
Texas Instruments,
Interconnection Business Unit
Sensors & Controls, Attleboro, MA

2005 Burn-in Test Socket Workshop
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BiTS
Burn-in & Test
Socket Workshop
™

Texas Instruments

Agenda

- Introduction
- Socket Technology and Roadmap
- Contacting Technologies
- Issues
- Concluding remarks

Introduction/Objective

- A review of some of the issues associated with designing sockets for the newer BGA packages with pitches of 0.5 mm and below
- Not a detailed introduction to socket design
- Educate and inform
- BUT MOST OF ALL
  - our objective is that this will be interesting and will stimulate you to think about the products and technology we work with every day and ..... to have some fun

Introduction – Early Technologies

– Its always been the Communication Age

Man's Need to Communicate - From the beginnings of human existence man has needed to communicate - whether by wall drawings, smoke signals, fires or drum beats.





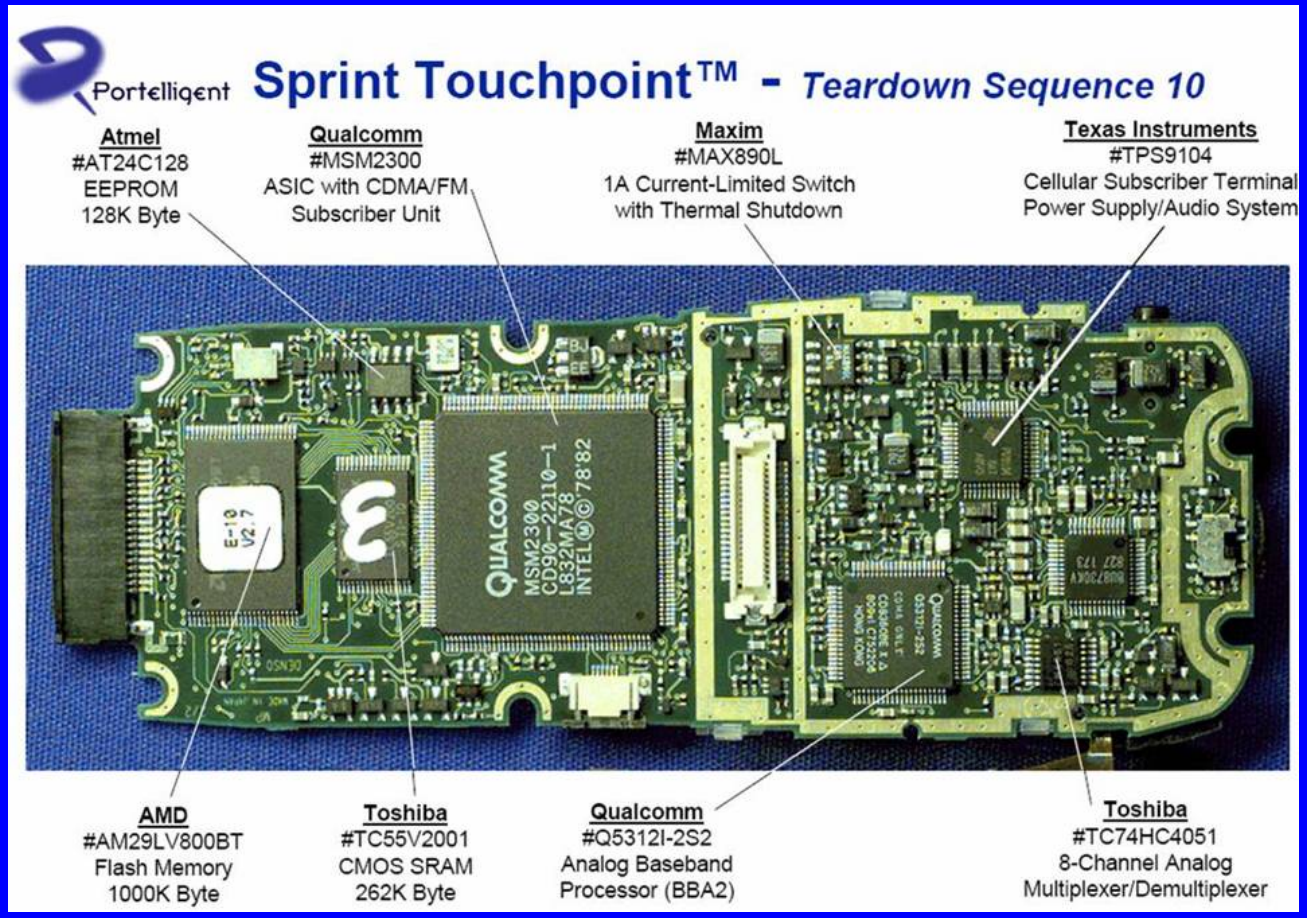


Introduction – Today's Technologies

The last 100 years – It's still the Communication Age

Man's Need to Communicate – From pigeon post to telephone to cell phone to PDA. It's all about the speed of communication and getting information to those who need it - ASAP

Changing Packaging Technology
Sprint Touchpoint 1999



Courtesy Portelligent, Austin Texas

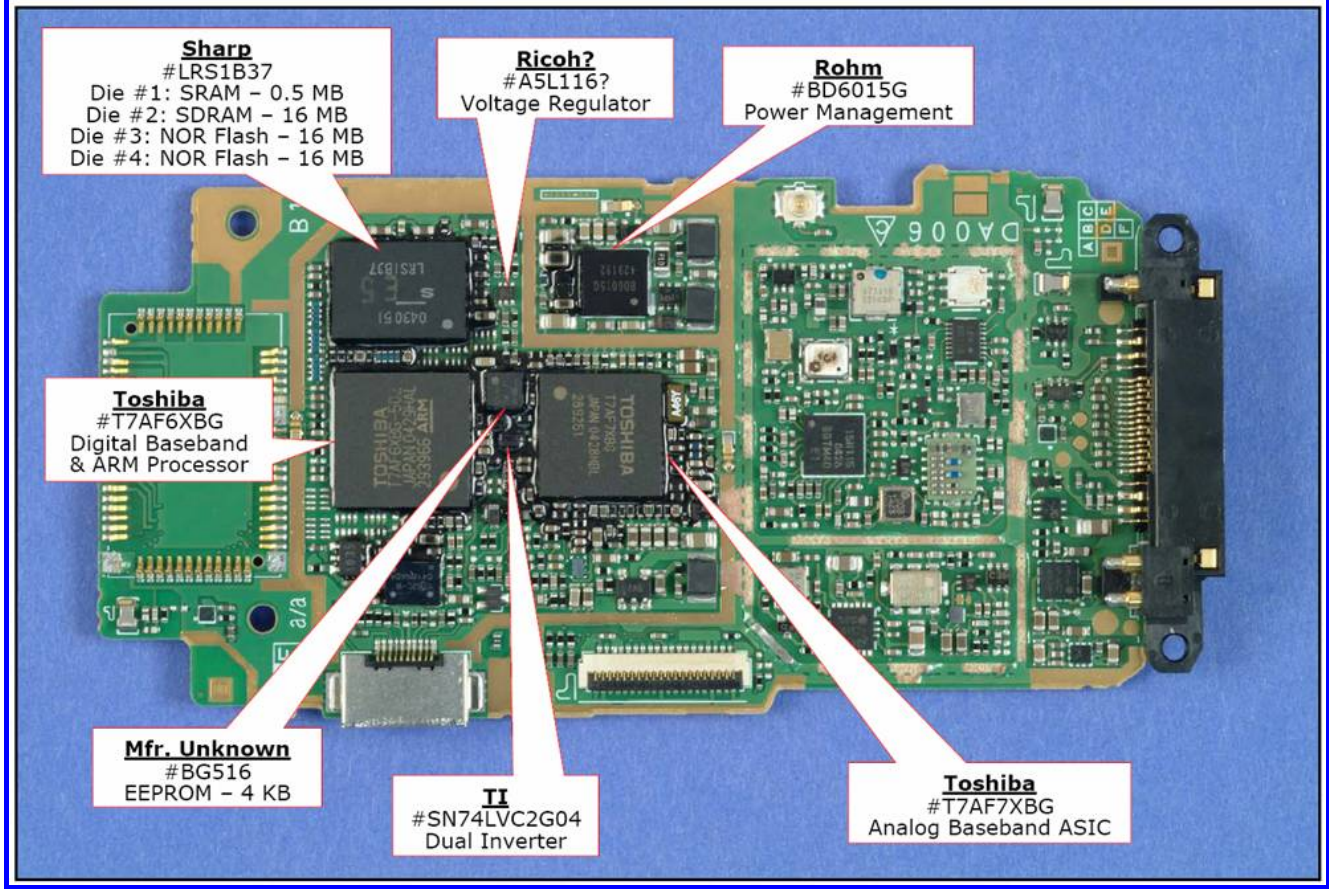
Key package type and pitch

# I/O	Type	Pitch
8	SOP	1.27
16	SOP	0.65
20	TSOP I	0.50
20	TSOP II	0.65
48	TQFP	0.50
176	TQFP	0.50

Changing Packaging Technology

Sharp PDCV402 Camera phone 2004

Portelligent **Main Board** (Side 1 IC Identification)

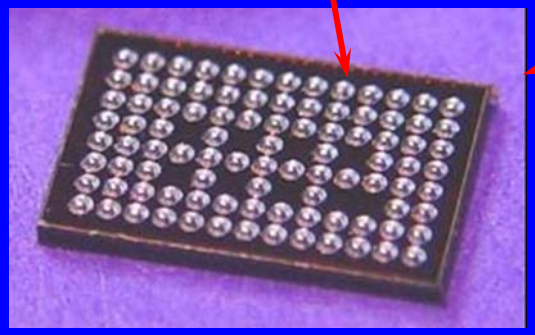


Key package type and pitch

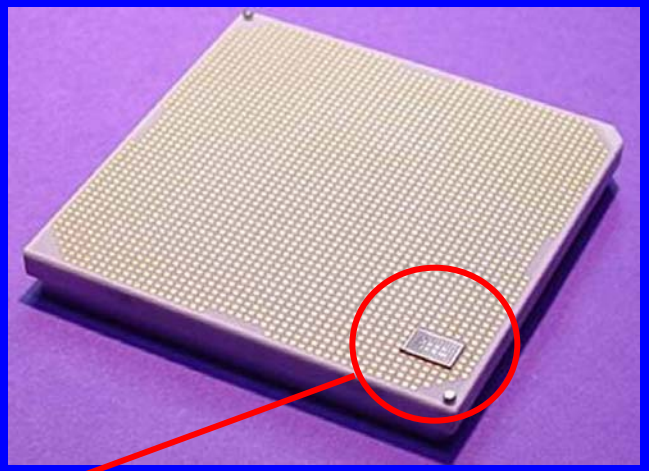
# I/O	Type	Pitch
208	PBGA	0.40
176	PBGA	0.50
320	PBGA	0.5
12	QFN	0.75
20	QFN	0.5
6	SOT	0.4
4	SOT	1.0
45	Flip-C	0.5
16	TSOP II	0.4
6	MLP	0.80

Macro Technology Trends
Packages

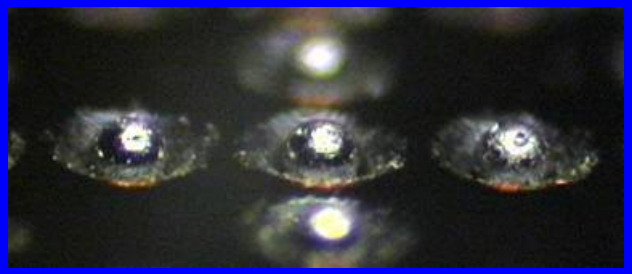
- **Packages are getting bigger and smaller**

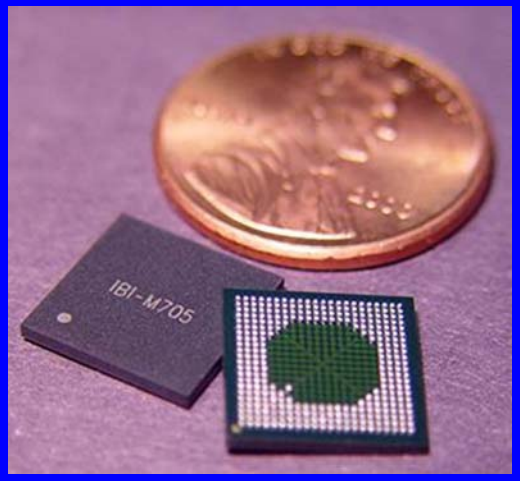


0.4 mm pitch CSP
5.8*3.8 mm package
96 I/O Pb-free bumps



1.0 mm pitch LGA
52*52 mm package
2601 I/O Gold Lands





0.4 mm pitch CSP
10*10 mm package
313 I/O Pb-free balls

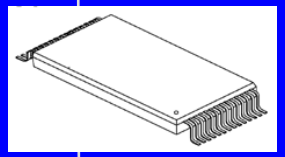
Function Drives Pitch

Simple phone

Voice, Camera, Internet
GPS, Video, TV, Music

Increasing functionality
Increasing I/O density
Reduced package area
Reduced package volume (thickness)


Courtesy Portelligent



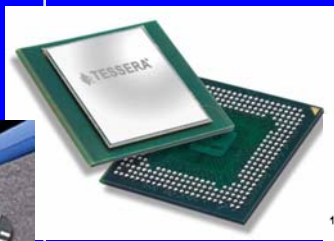
CSP (0.8)

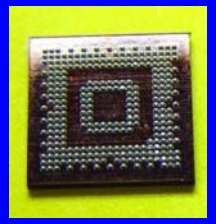
TQFP
(0.5)

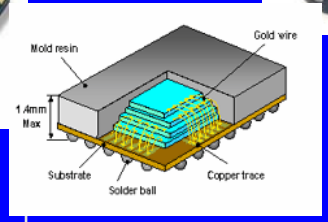
TSOP
(0.5, 0.4)

QFP

CSP (0.5)
QFN





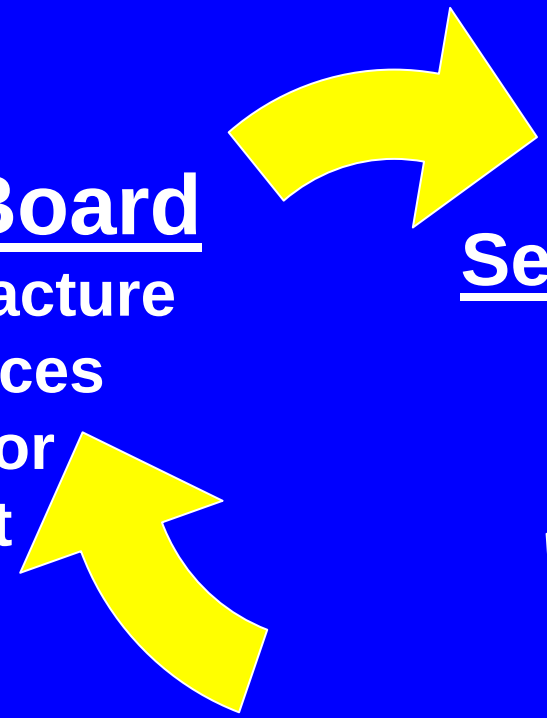


Stacked Die
Stacked Package
0.4mm Pitch CSP

96 2000 2004

Reliability – Burn-in

- Product reliability is assured by forcing early life failures using burn-in – Key players



Burn-in Board

Design/Manufacture
Lines and Spaces
Compression or
Surface mount

Semi-Conductor Packaging

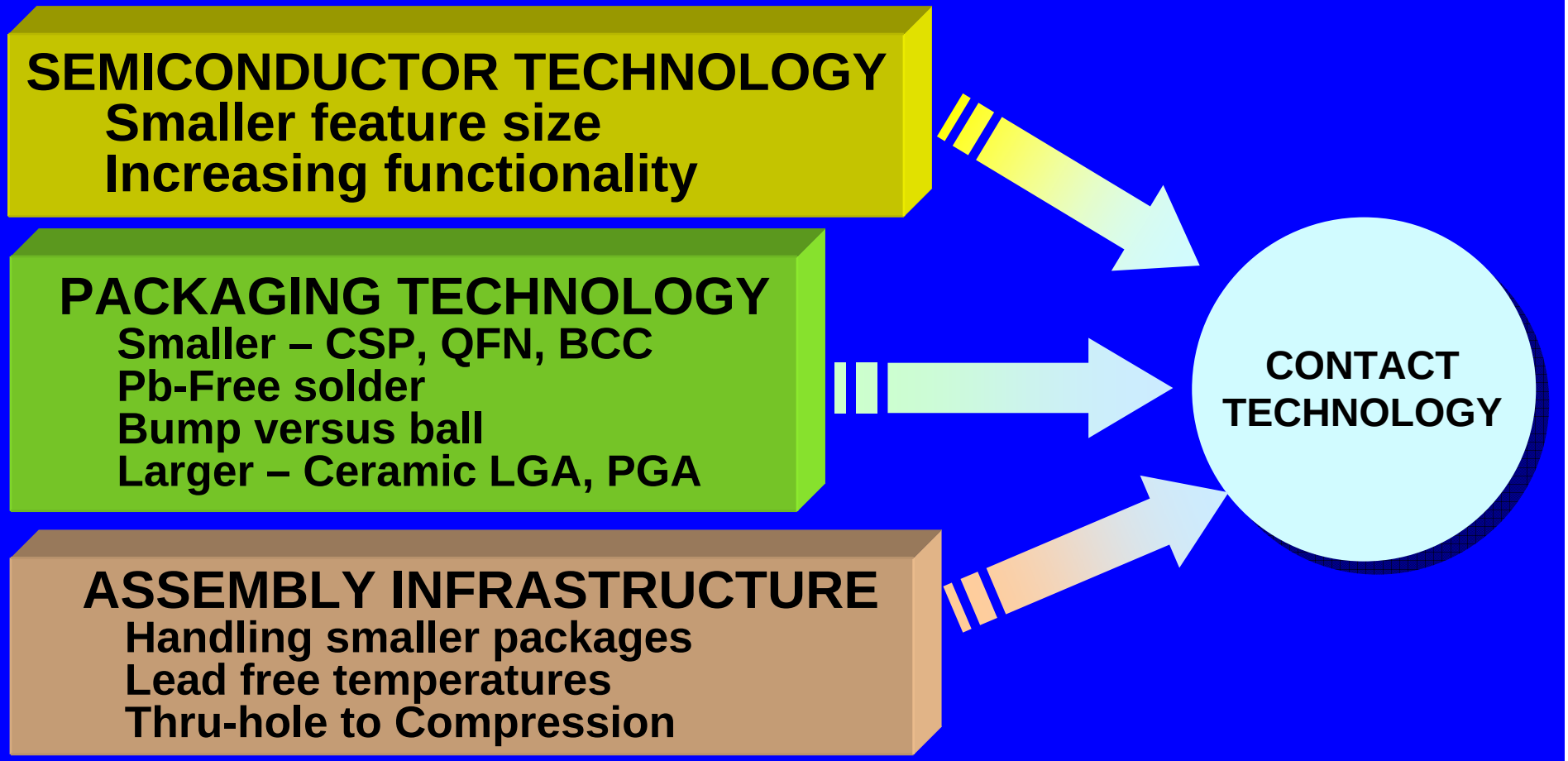
Type of I/O BGA. LGA
Number of I/O
Package size

Burn-in Socket

Metal stamping and forming
Plastic molding
Assembly

Socket Design
- Requirements Driven by Technology

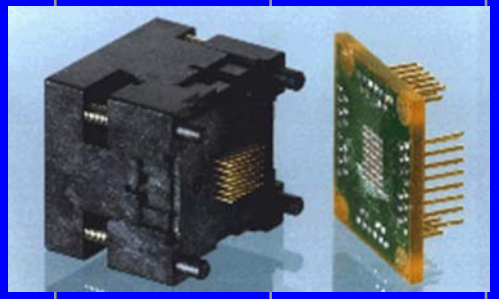
- **Most important feature is the contact.**



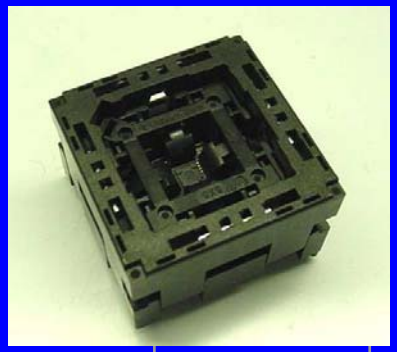
The Pitch Problem
- Looking Back at BiTS

- For socket and BIB manufacturers it's all about "pitch"
- The issue of how to deal with pitch is not new.
- Searching the BiTS archives:
  For "Design" finds 51 results
  For "Fine Pitch" finds 17 results.
- In 2000 - "Challenges of Burn-in Socket Design For Fine Pitch (0.5mm) CSP/uBGA " by Yoshinori Egawa
- In 2003 - "Contact Technology For 0.5 mm Pitch and Below " by Prasanth Ambady et al.
- In 2004 – "0.4mm BGA Burn-in Socket in Compression Mount, Another Breakthrough in Socket Technology " by Helge Puhlmann et al.
- **Pitch drives everything.**

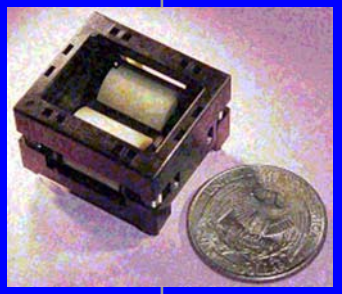
Socket Technology History



Fan Out Interposer introduced



0.5 mm CSP Thru-hole production

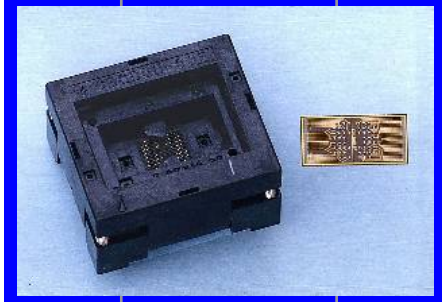


CLGA CSP

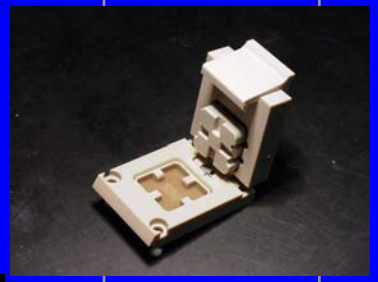
0.4 mm pogo compression mount

?

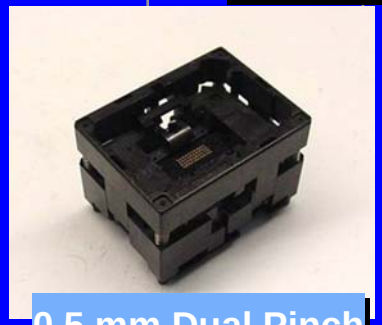
0.4 mm production Compression mount development



0.75mm CSP socket



0.5mm development



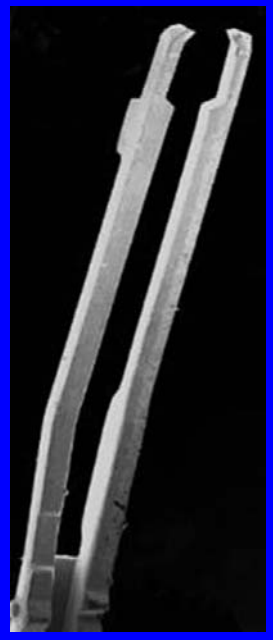
0.5 mm Dual Pinch

0.5 mm Compression mount production

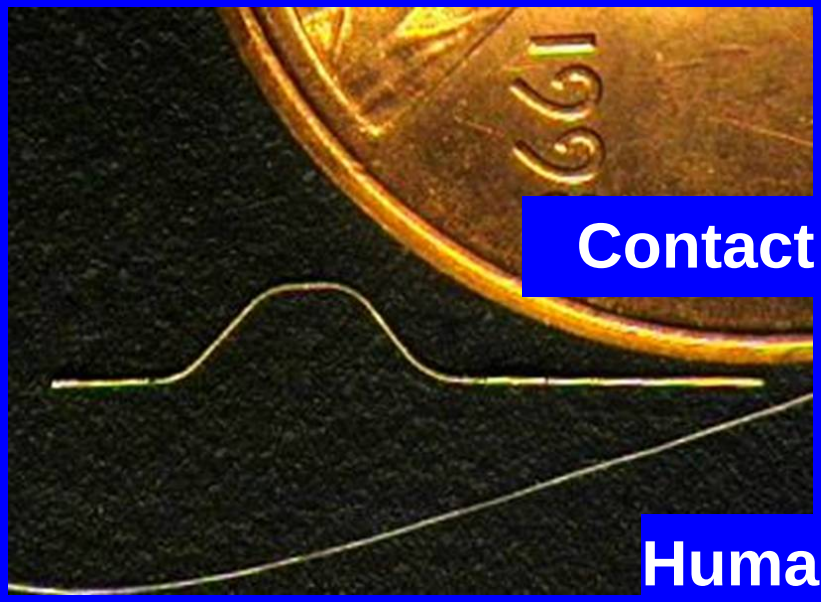
97 98 99 00 01 02 03 04 05

Contact Technology

- Finer pitch requires development of new contacting technologies
- Move from thru-hole to compression mount



Dual pinch style contact for 0.75 mm and above



Buckling beam compression style contact for 0.5 mm and below

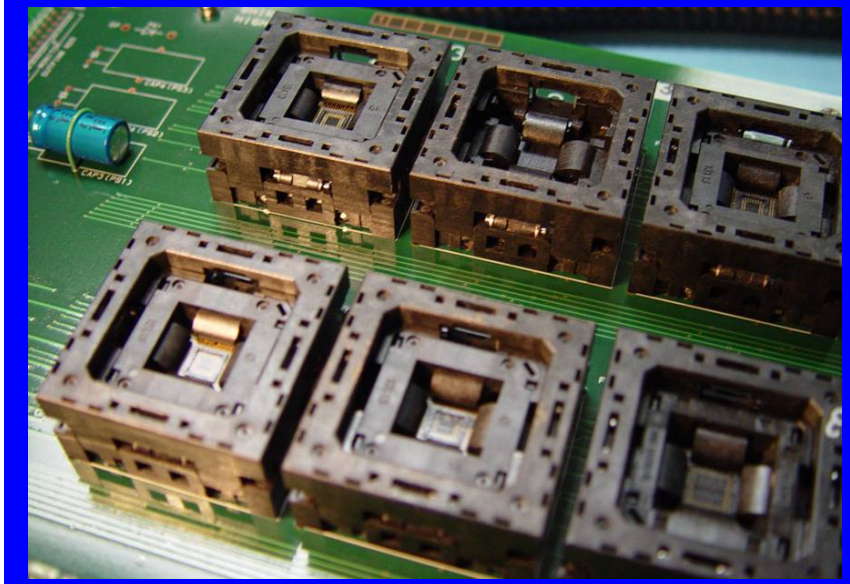
Contact Technologies
Compression Mount V's Thru-Hole

For pitches of 0.5 mm and below move to compression mount

	Compression Mount	Thru-Hole Mount
+	Manufacturability of the BIB Lower cost burn-in boards for fine pitch devices. Socket replacement	Proven mechanical and electrical interconnect Good thermal interconnect to board for higher current carrying capability.
-	Reliability of electrical interconnect Cost of hard gold on pads Alignment pin accuracy to ensure that socket mates to pads on board Board Assembly time	Assembly difficulties – alignment of small leads into holes. Assembly difficulties – solder bridging Not easily replaced/repaired Limited BIB suppliers

0.5 mm Burn-in Boards

When asked about thru-hole BIB suppliers a purchasing manager said .... "There are two vendors in the world who can make 0.5 mm thru-hole boards – and they both live in Japan"

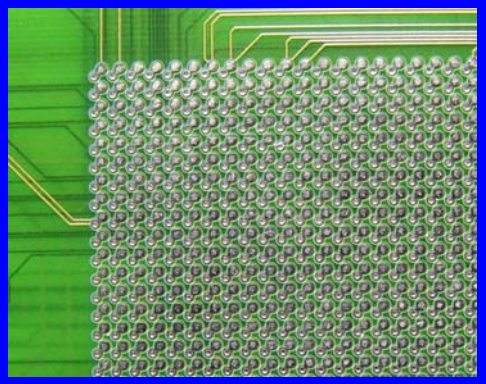


Photograph of production BIB with 0.5 mm thru-hole Sockets

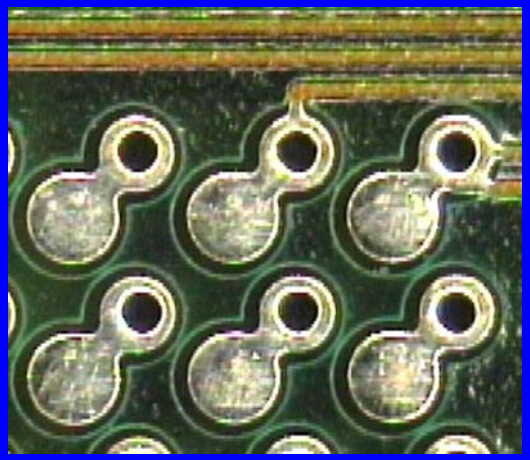
- **0.5 mm BIB's are at the leading edge of PWB capabilities.**
- **Selection of the PWB manufacturer is important.**
- **Today PWB suppliers have technology - Compression mount boards available world wide.**
- **Thru-hole boards only available from Japan.**

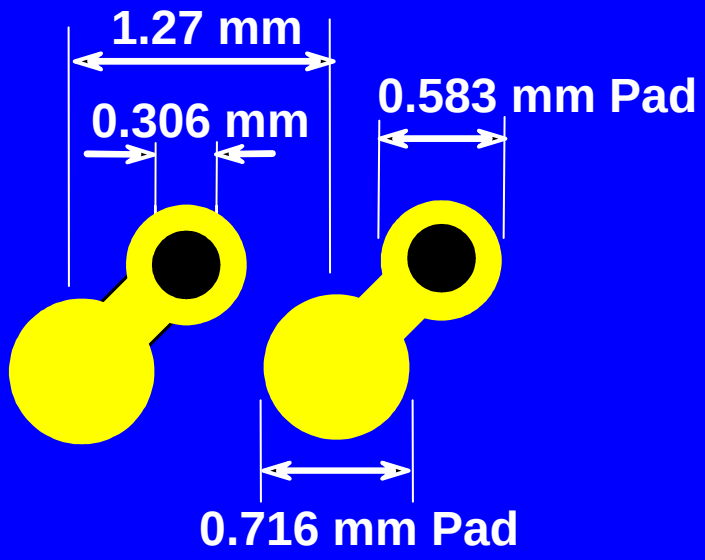
1.27 mm Surface Mount Board

Photograph of top surface of test board

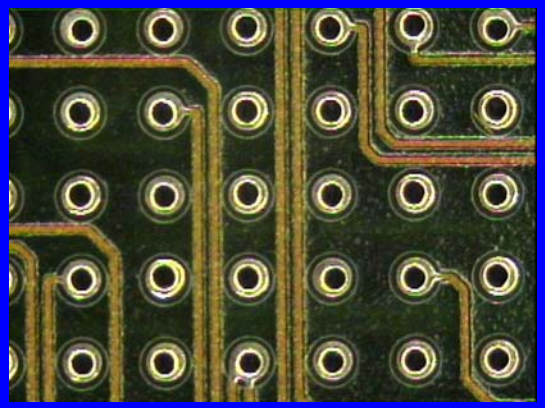


Top





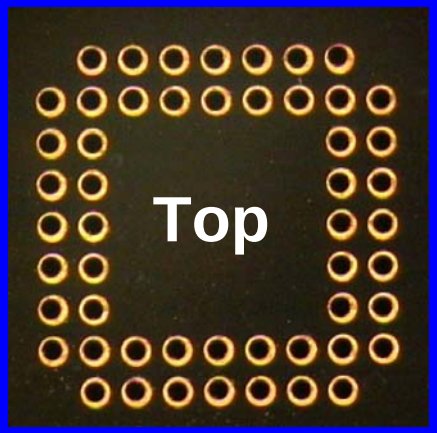
Bottom

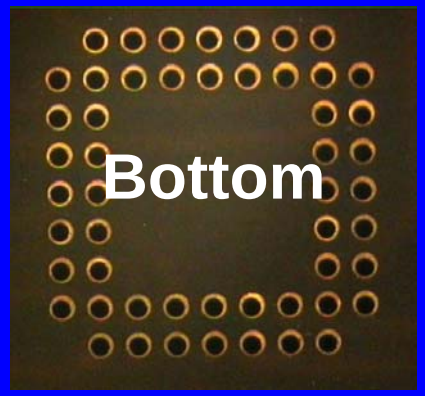


Example of a 1.27 mm SMT test board
Traces on inner and bottom layers
Key hole or dog-bone via off pad.
Line width 0.085 mm

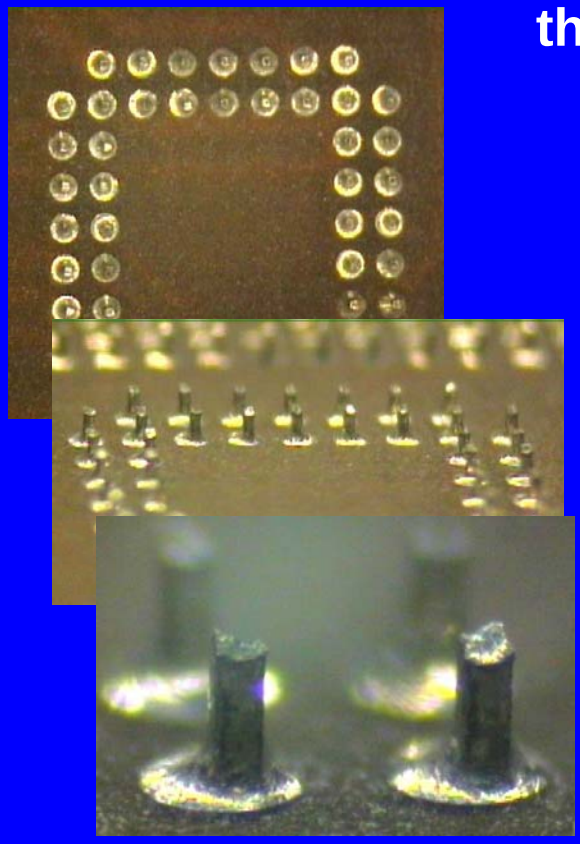
0.5 mm Thru-hole BIB

Supplier 1 - Japan

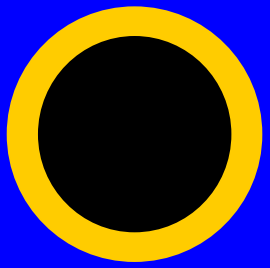




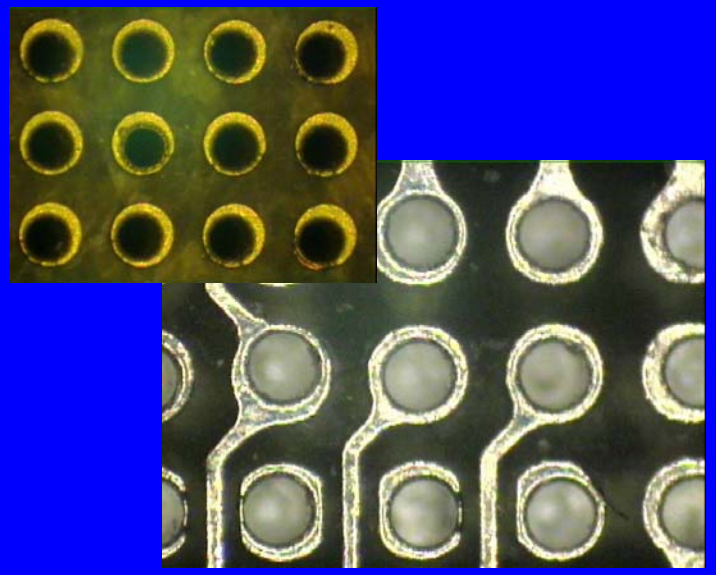
Bottom of board



Pad dia 0.345 mm
thru-hole 0.225 mm

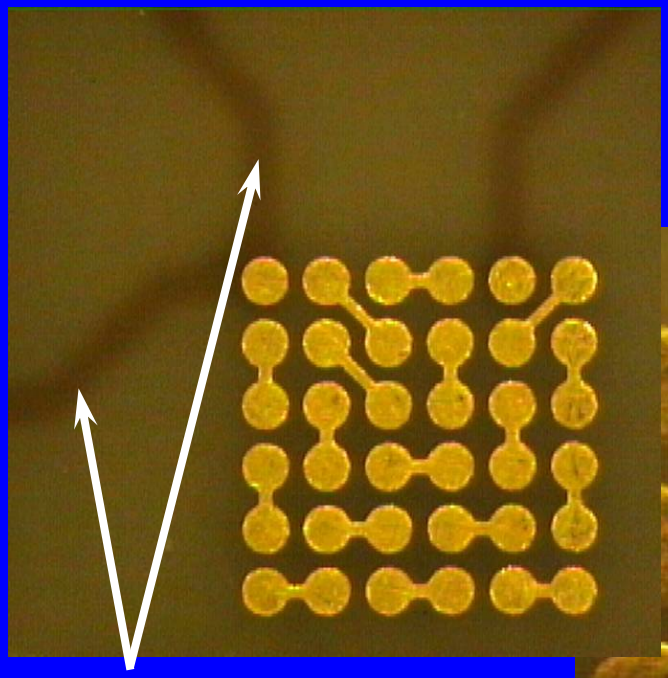


Supplier 2 - USA



0.5 mm Compression Mount BIB

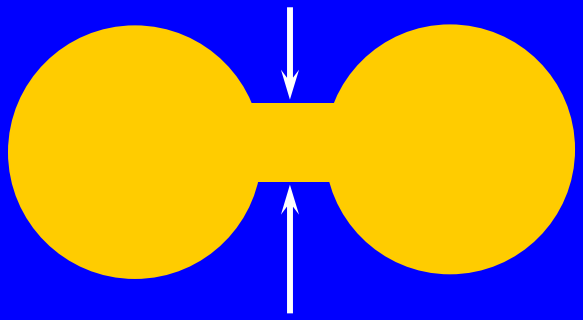
Photograph of 2 layer daisy chain test board



Traces on bottom of board

Pads on 0.5 mm CMT board Technology - filled via in pad Filling via and planarizing can be an issue.

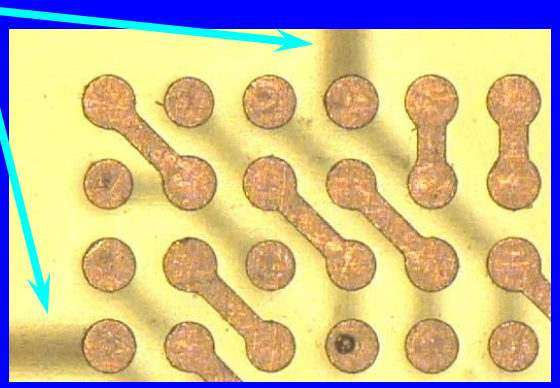
Pitch 0.5 mm
Pad dia 0.39 mm



Line width 0.11mm

0.4 mm Compression Mount BIB

Traces on bottom of board



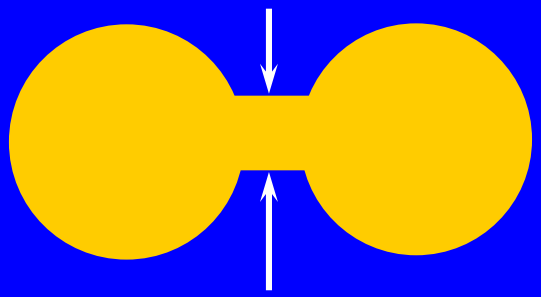
Photograph of 2 layer daisy chain test board

0.4 mm CMT boards test boards can be made but the yield for large BIBs is poor.

Pads on 0.4 mm CMT board are filled via in pad

- Via Fill and planarizing is difficult.

How do we resolve difficulty/cost?



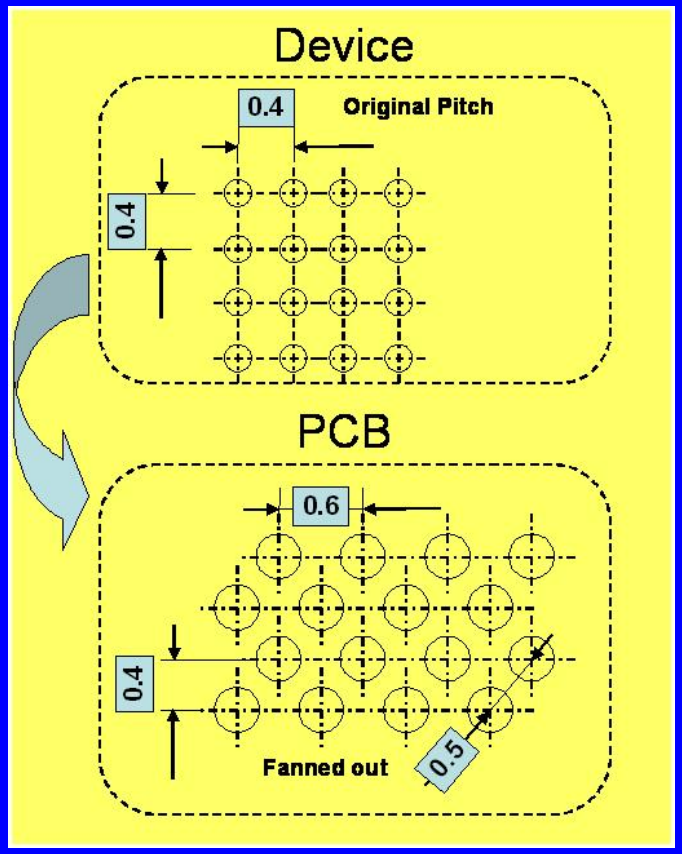
Pitch 0.4 mm
Pad dia 0.25 mm
Line width 0.11mm

0.4 mm Compression Mount BIB

How can we resolve?

Change the pitch at the BIB to one which can be "easily" made by the BIB suppliers.

Pitch change package to board



Pitch translation shown last year in presentation by Helge Puhlmann

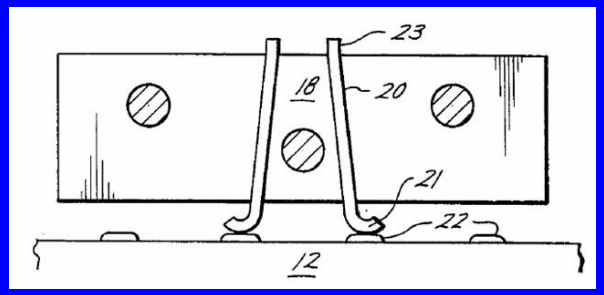
The pitch can be translated in either 1 or 2 dimensions

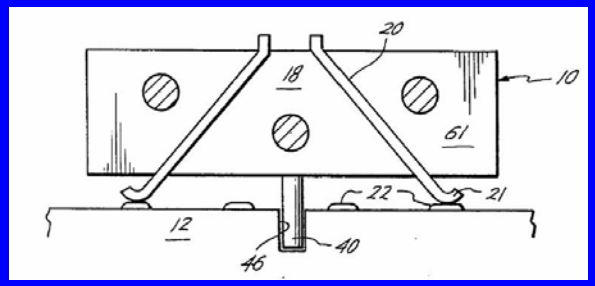
How?

0.4 mm Compression Mount BIB

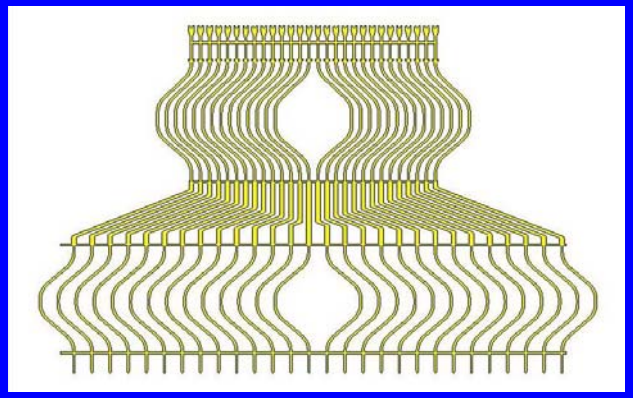
Use a lead frame type contact.

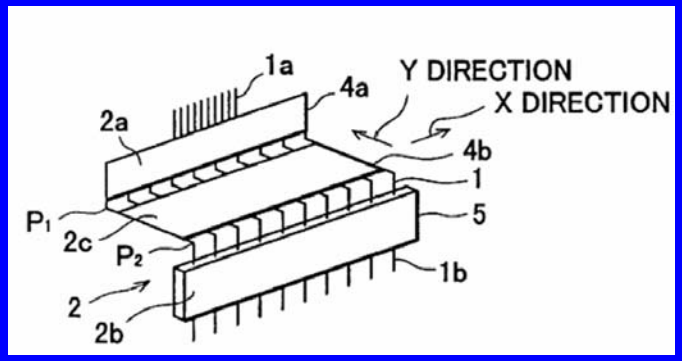
Pitch translation in ‘X’



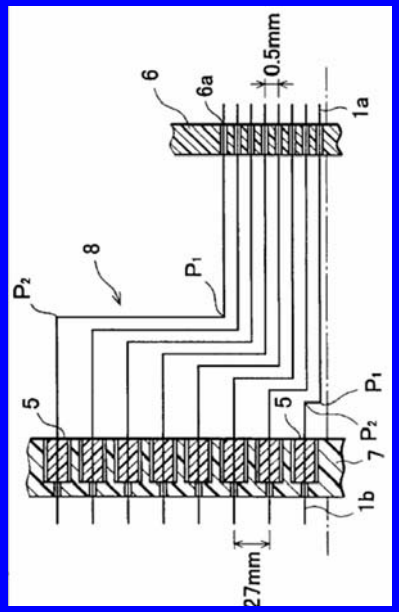


US Patent: 4,871,316



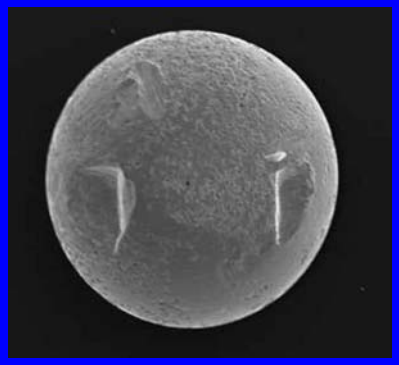


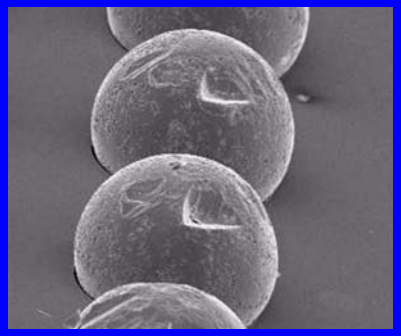
Pitch translation in ‘X’ and ‘Y’



US Patent: 6,123,552

Issues/Challenges/Opportunities





- Reducing pitch.
- Contacting lead free solder balls.
- Contact witness marks.
- Package flatness
- Increasing power:-
  - Thermal loads higher and more variable during burn-in
  - Current capability for contacts
- Known Good Die/Flip Chip
  - Pitches of 0.2 and less

The Future

- Semiconductor companies are producing packages at 0.4 mm pitch today.
- Roadmaps show increasing I/O
- Product ideas have phones, PDA, music, TV all coming together into handheld devices.
- Packaging houses will continue to develop innovative packages – SiP and stacked, to use the existing infrastructure.
- The “Back-End” infrastructure must develop solutions to accelerate the introduction of these packages.