Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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Technical Program

Session 7
Wednesday 3/09/05 8:00AM

THERMAL MANAGEMENT

"Thermal Characterization And Specification For Test And Burn In"

David Gardell – IBM Microelectronics

"A Cost Effective, Flexible Approach To Automated Thermal Control During Burn-In"

Chris Lopez – Wells-CTI **Brian Denheyer** – Wells-CTI
Michael Noel – Freescale **Don VanOverloop** – Freescale

"High Efficiency Passive Heat Sinks for 5-20 W Applications"

Natarajan "Ram" Ramanan – Applied Thermal Technologies, LLC
Mike Ramsey – Plastronics, Inc.

Thermal Characterization and Specification for Test and Burn In

2005 Burn-in and Test Socket Workshop

March 6 - 9 2005

David Gardell
IBM Burlington Vt.

Overview

- Thermal Characterization
- Temperature measurement methods
  - Examples
- Passive vs. active heat sinks
- Equipment specifications

Thermal Characterization

- Measure Chip temperature under controlled conditions:
  - vs chip power
  - vs Time
- Fit equations to the measured data
- Extrapolate results to other conditions
  - Other powers or times
  - Other chip sizes or package types

Thermal Characterization

- Heat transfer mechanisms may be complex and non intuitive
- Predicting performance of future products requires understanding of fundamental heat transfer mechanisms
- Important to verify performance with product

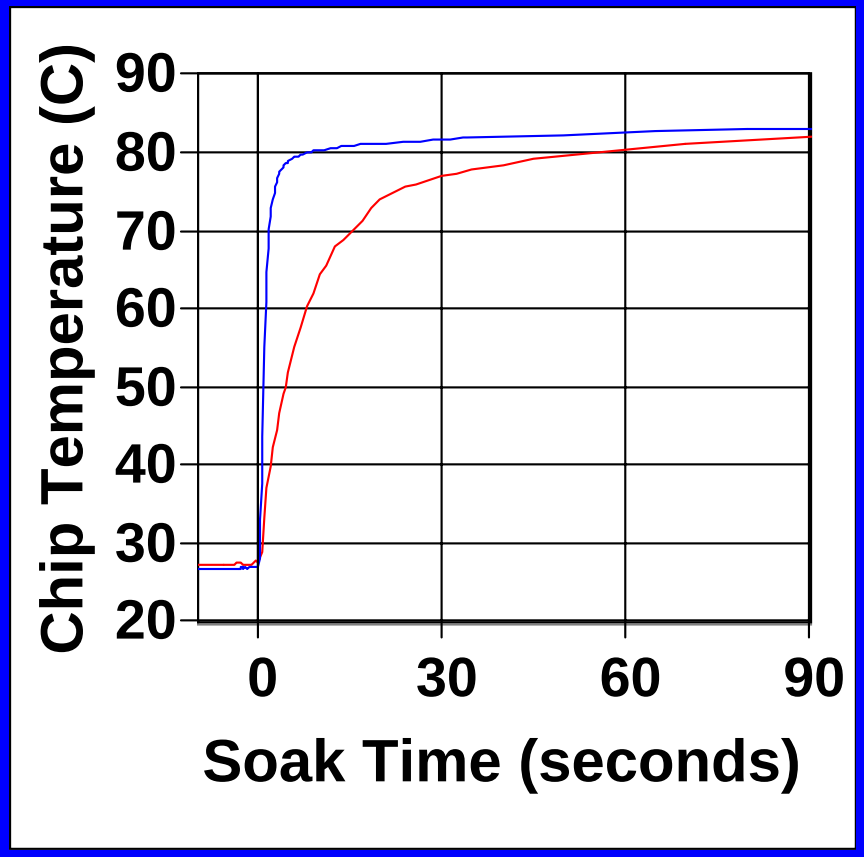
Thermal Characterization

- Investigate each thermal phenomena independently
  - Module soak time
  - Temperature change with plunge
  - Temperature increase with chip power and time
  - Temperature gradients across the chip
  - Heat sink force and centrality
  - Heat sink thermal resistance vs flow
  - Power limits for actively controlled heat sinks

Temperature Measurement Methods

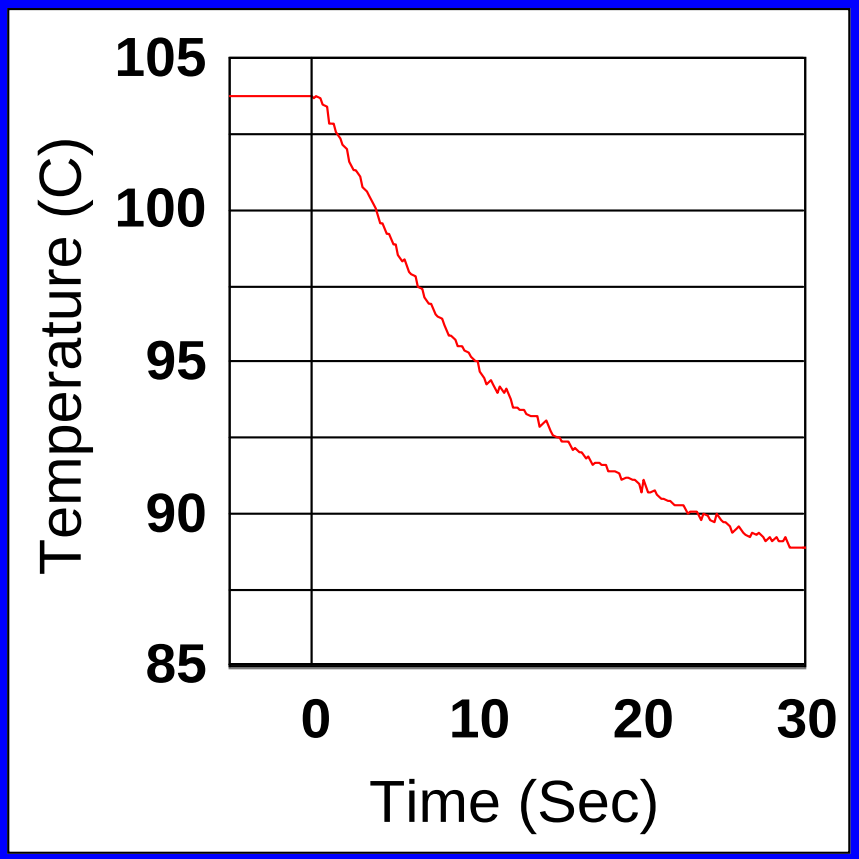
1. Thermocouple contacting the product chip
2. Temperature sensitive circuit on product module
3. Thermal test chip
   - Known power dissipation
   - Multiple temperature sensors on one chip

Example: Soak Time for Passively Controlled Heat Sink @ 85 C



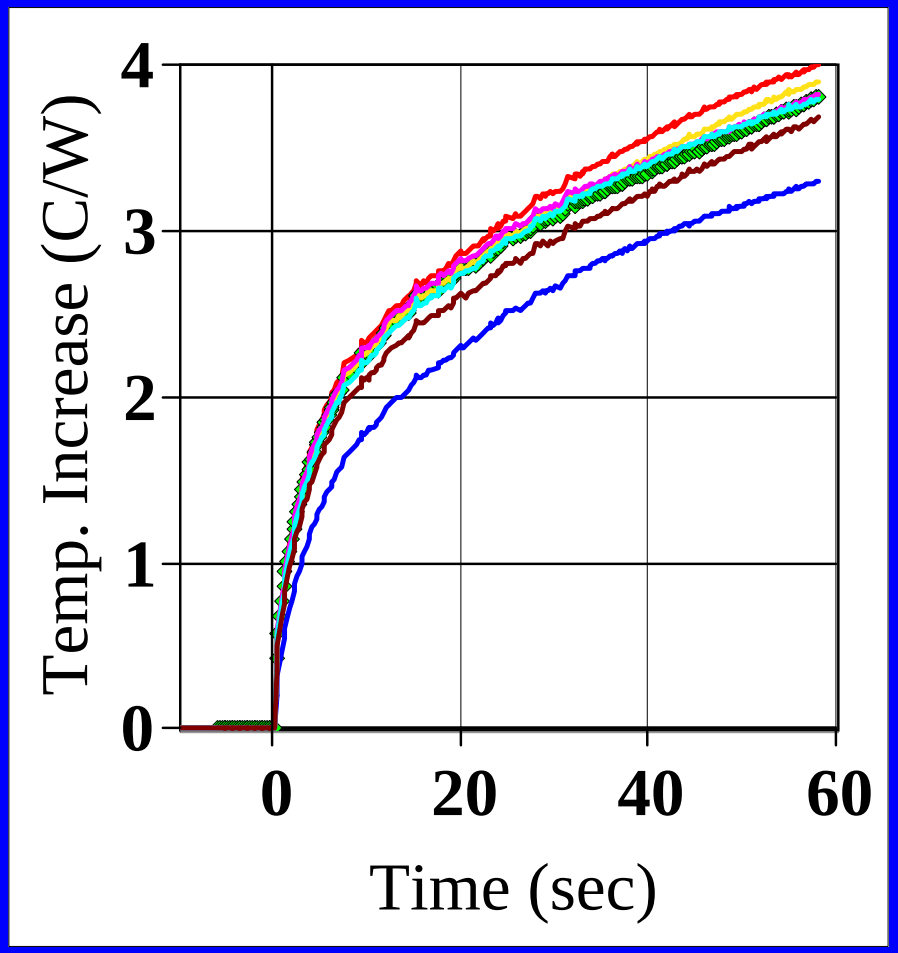
- Elevated temperature test
- Thermocouple on un-powered product
- Red - lidded module
- Blue - bare die modules

Example: Temperature Drop With Plunge, Chamber Tool, No Heat Sink



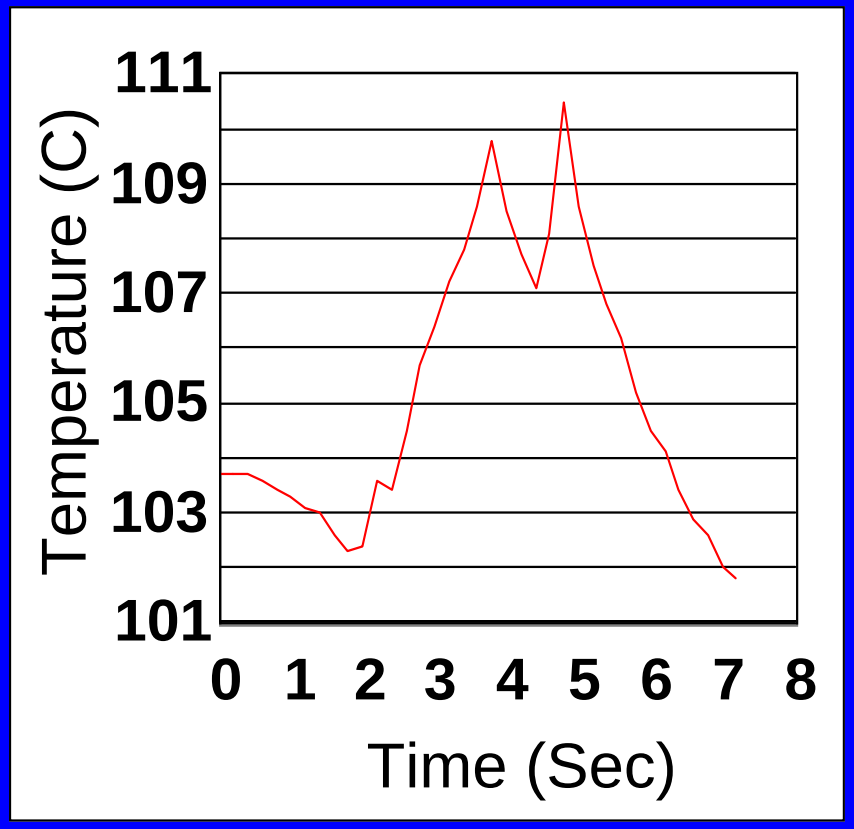
- Module initially at core temperature, 102 C
- Thermocouple on un-powered product
- Heat loss to socket and test head

Example: Temperature Increase With Chip Power, No Heat Sink



- Thermal test chip
- Uniform power applied at t=0
- Multiple temperature sensors on chip
- 1 C/W at 2 sec
- Predictable with lumped mass model

Example: Temperature Gradients Across Test Time



- Functioning product module test
- Chamber tool, no heat sink
- Thermocouple glued to center of product chip or OCTS
- Chip power varies with time and location on chip

High Power Module Test

- Generally requires some sort of heat sink contacting the chip
- Heat sinks may be passive or actively controlled

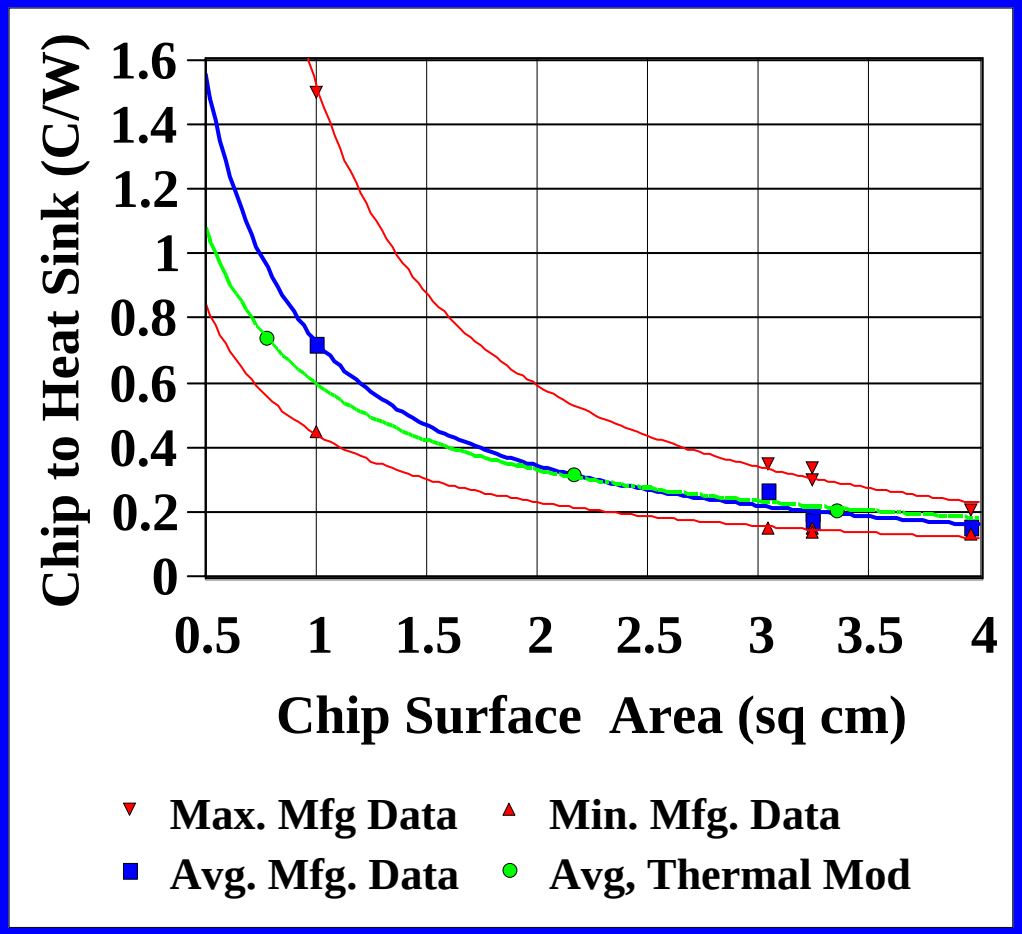
Heat Sink to Chip Thermal Resistance

- Dependent on:
  - Heat sink and chip flatness and surface finish
  - Surface contamination
  - Heat sink force
  - Heat sink force centrality
  - Thermal interface material or pad
  - Heat sink size vs chip size

Heat Sink to Chip Thermal Resistance

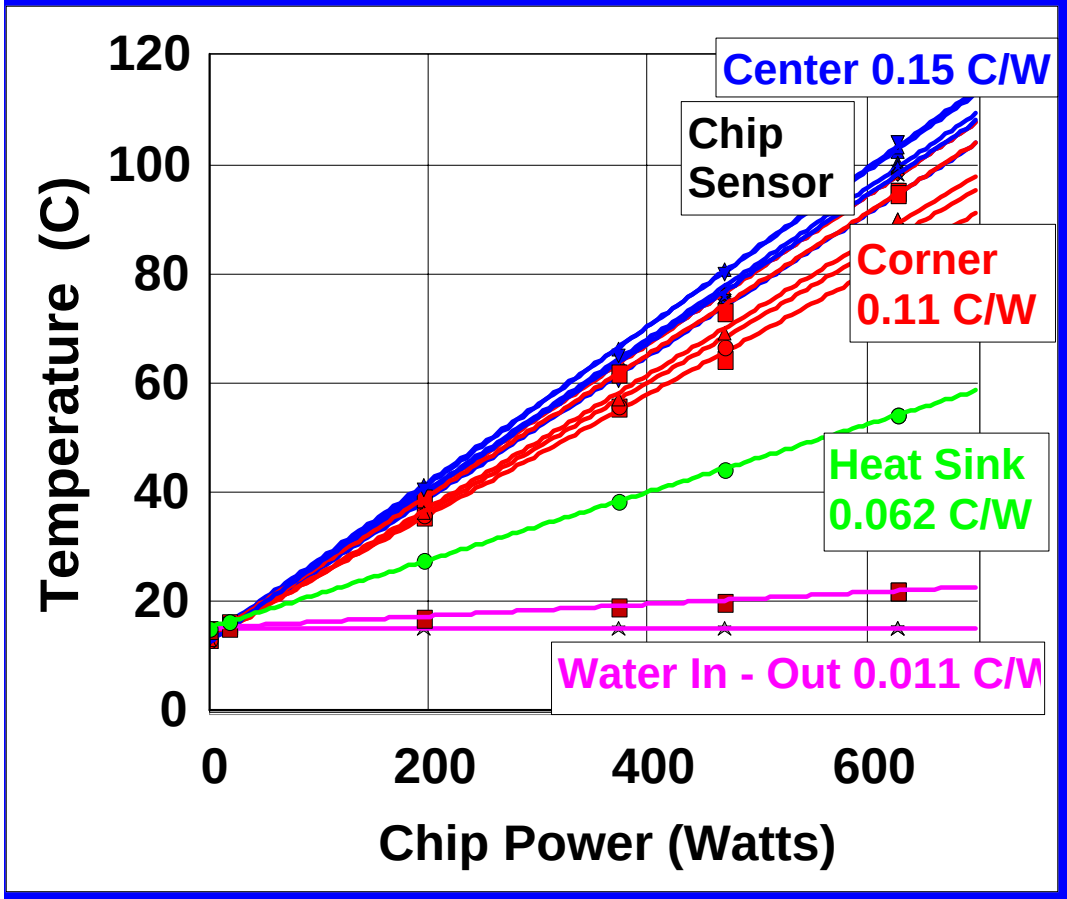
- Across chip temperature gradients
  - Investigated with thermal test chips
- Chip to chip variations
  - Resistance measured on each chip during production test and burn in

Resistance Variations in Manufacturing



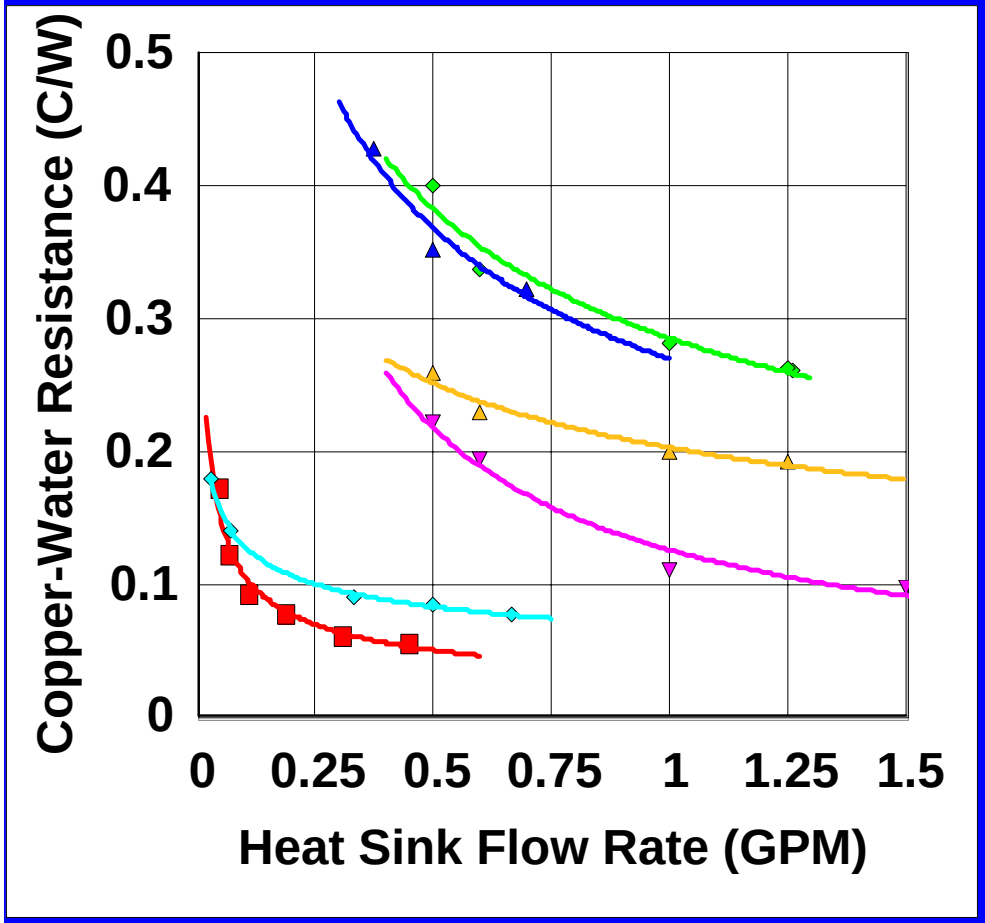
- Large sample mfg. data
- Various chip sizes
- Same thermal interface
- Some “identical” chips 3X hotter than others
- R max=1.53 *A^-1.37

Interface and Heat Sink Characterization and Optimization



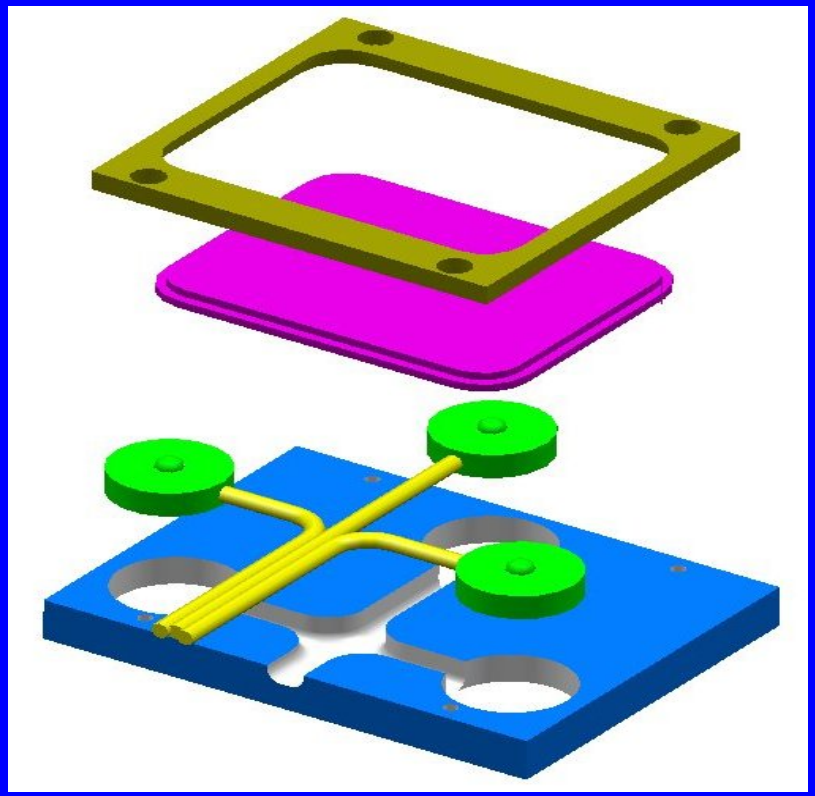
- Multiple sensors on uniformly powered chip
- Room temperature, passive heat sink
- Should be linear
- Slope is thermal resistance
- Thermal resistance independent of power

Heat Sink Characterization vs Flow Rate



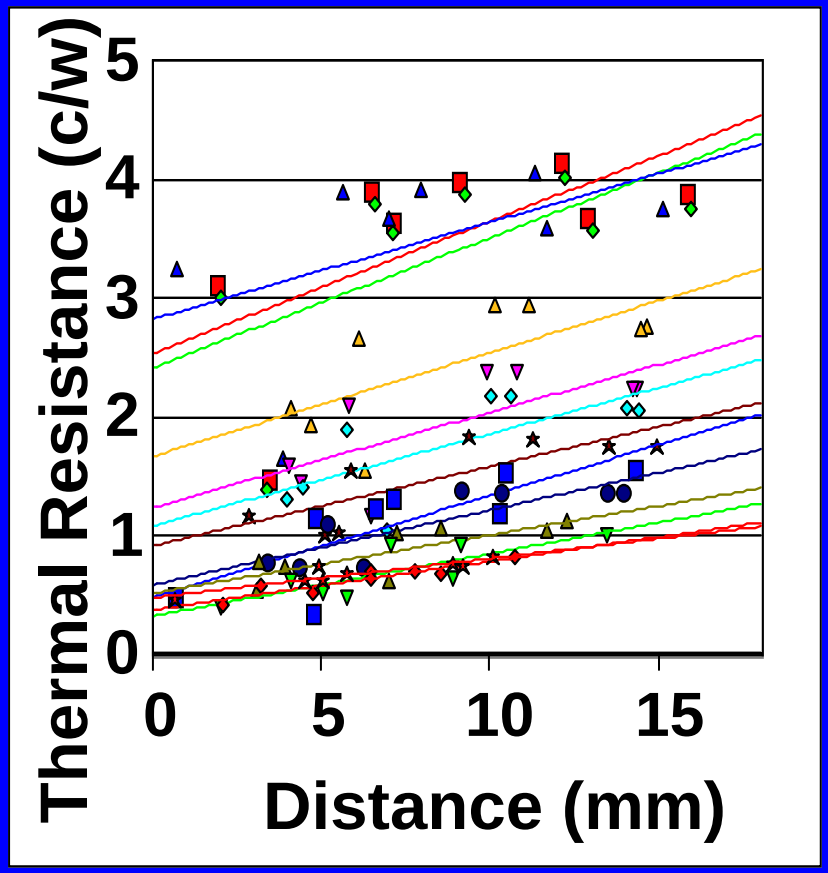
- Various water cooled heat sinks
- Small thermocouple embedded base of heat sink
- Heated with small test chip
- Also measured pressure drop

Heat Sink Force and Force Centrality Load Cell Assembly



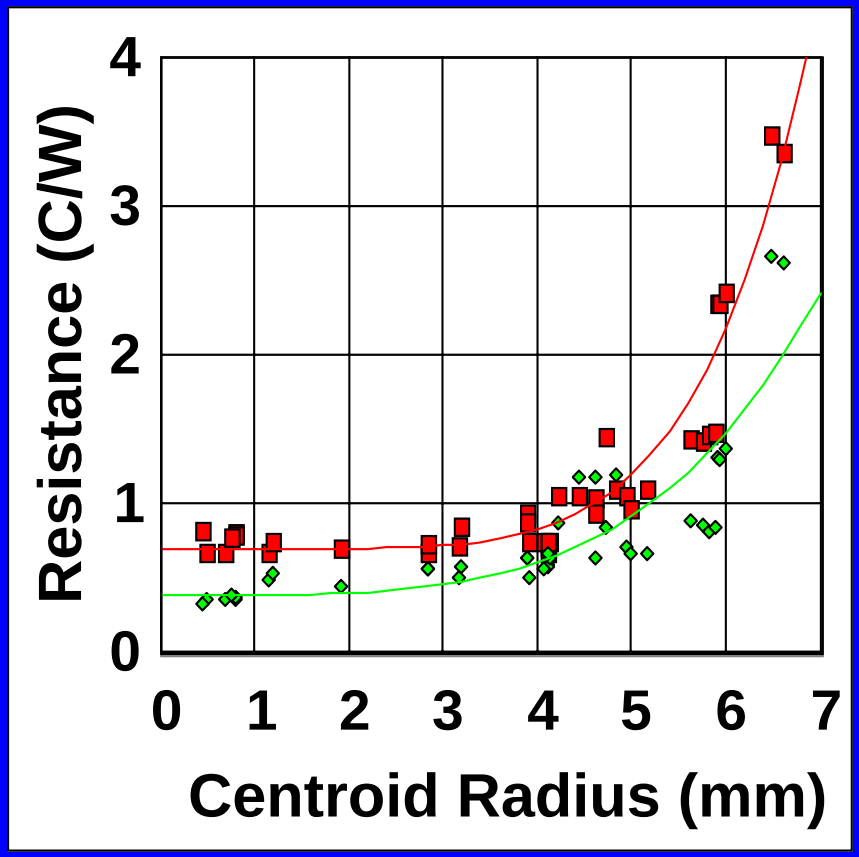
- Replaces module in socket
- Metal plate supported by three load cells
- Determines total force and force centroid
- Quantifies effects of hoses, wires, springs, friction and impact forces

Local Chip Temperature vs. Distance to Heat Sink Force Centroid



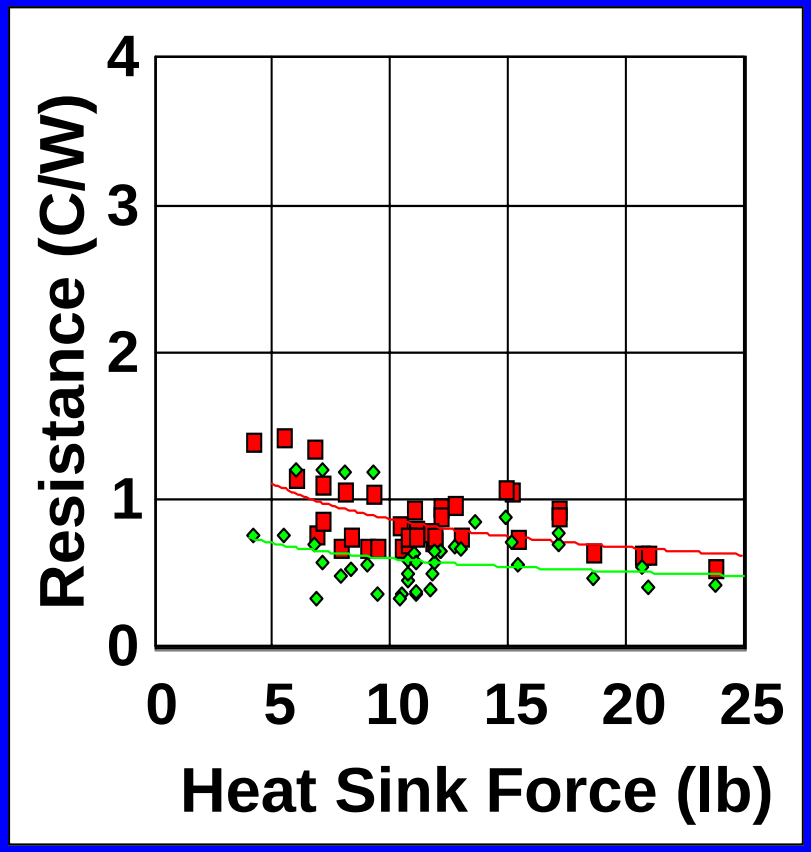
- 14.7 mm bare die, uniform power
- Passive heat sink
- Multiple tests
- Coolest point on chip is closest to centroid
- Average resistance is related to across chip gradients

Chip to Heat Sink Resistance vs Location of Heat Sink Force Centroid



- Red - Average of eight sensors on chip
- Green - Temperature gradient across chip
- Centroid needs to be in center 1/2 of chip

Chip to Heat Sink Resistance vs. Heat Sink Force

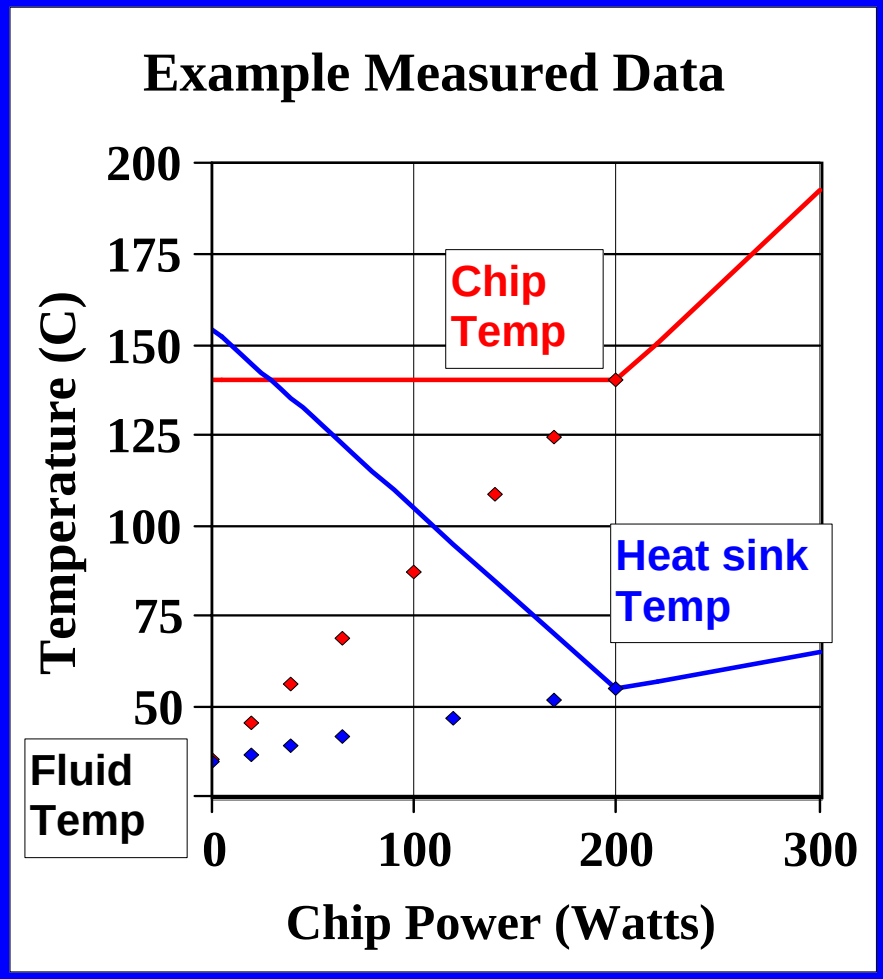


- Red - Average chip-HS resistance of eight sensors on chip
- Green - Temperature gradient across chip
- Force has smaller effect on resistance

Heat Sink Mounting

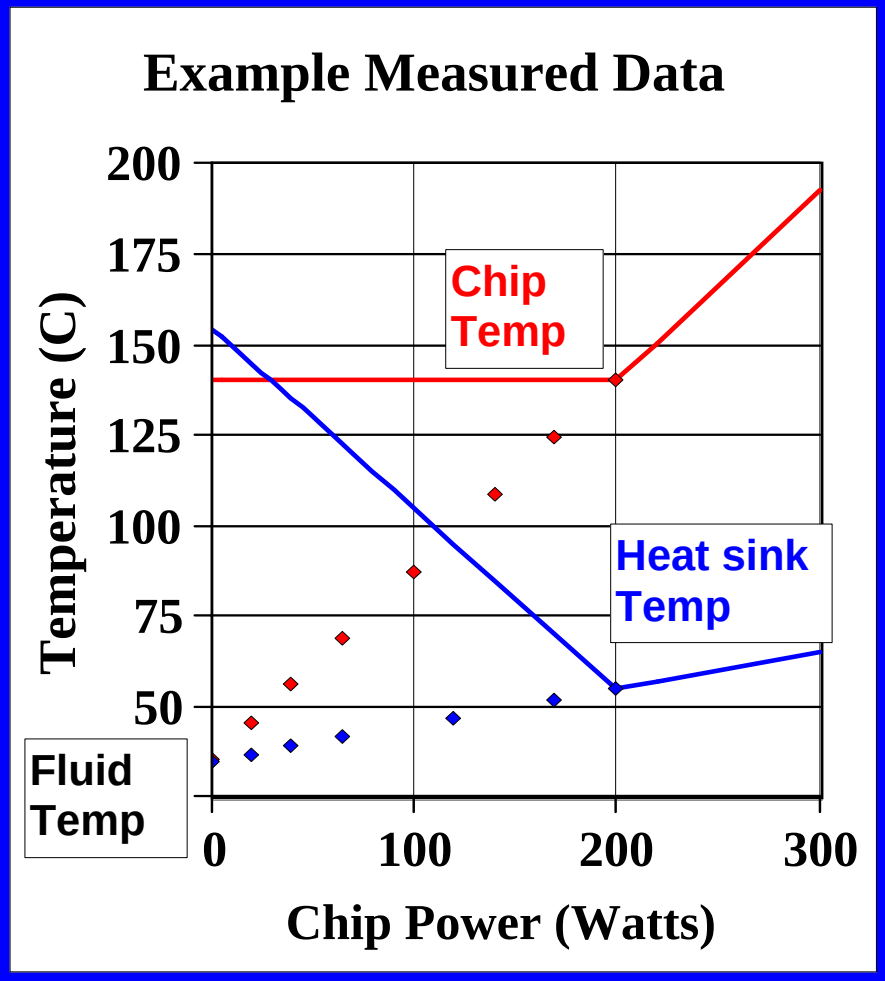
- Flexible tubing and wires
- Spring force applied near chip plane
- Alignment features near chip plane
- Co axial bellows

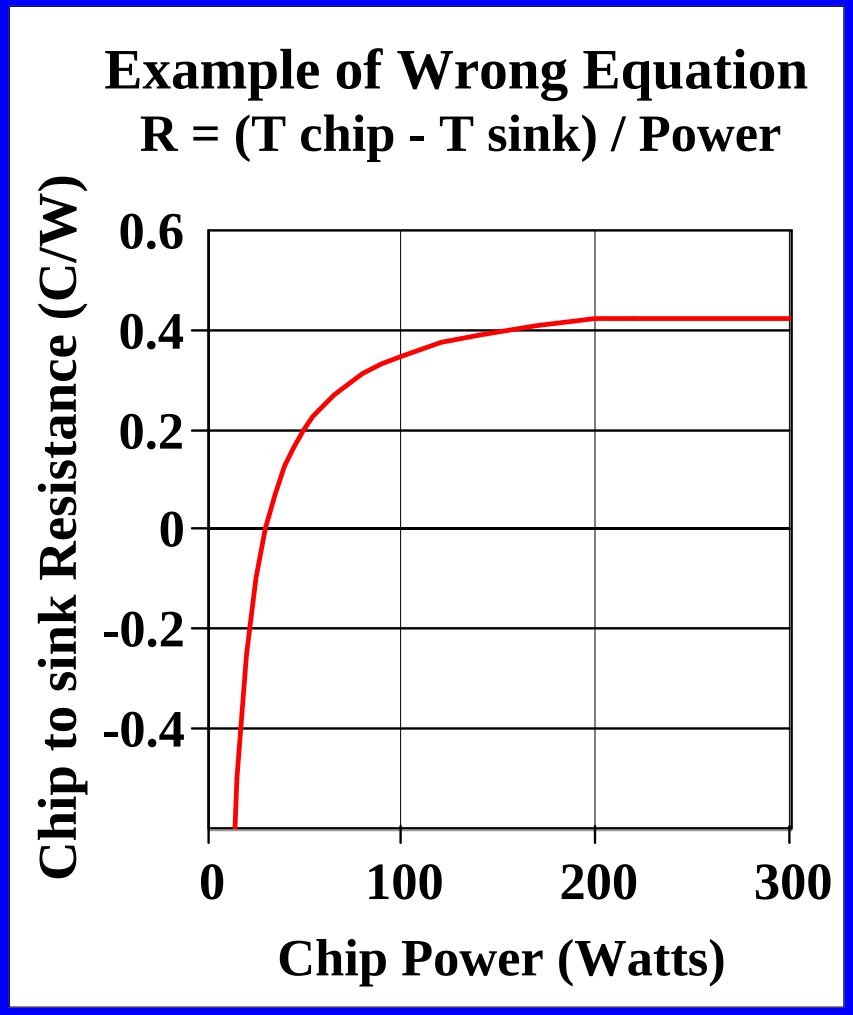
Actively Controlled Heat Sink Steady State Thermal Response



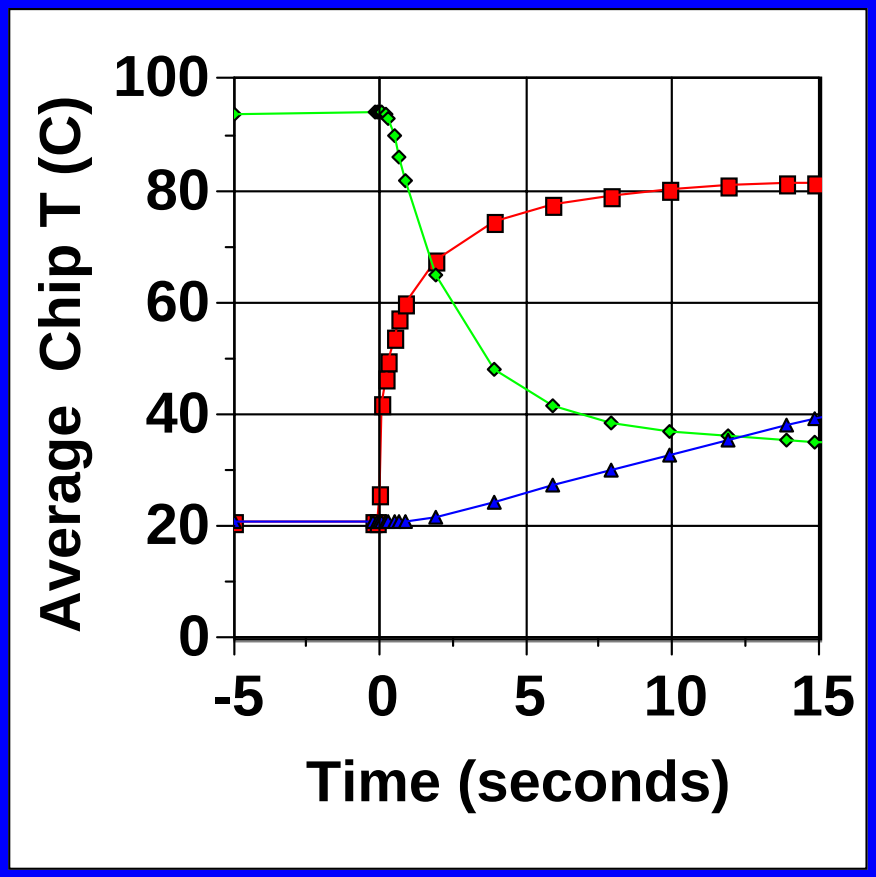
- Power is slowly increased
- Chip temperature held constant
- Decreasing heat sink temperature
- T vs P is linear before and after point where control is lost

Actively Controlled Heat Sink
Steady State Thermal Response



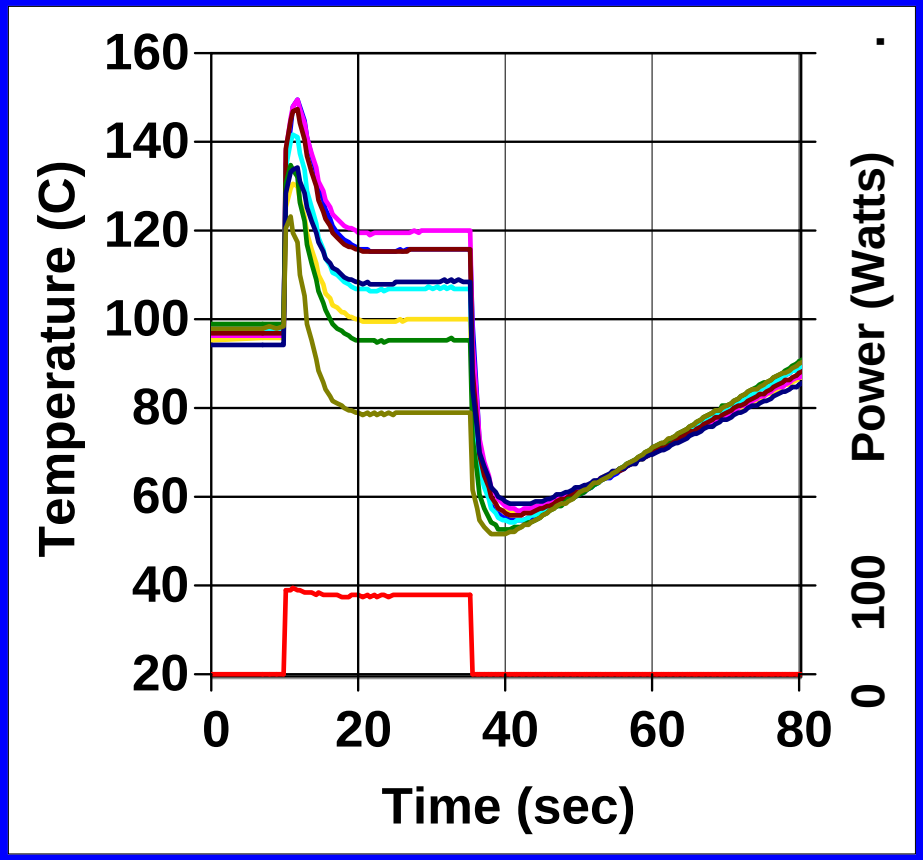


Actively Controlled Heat Sink Thermal Transient Response



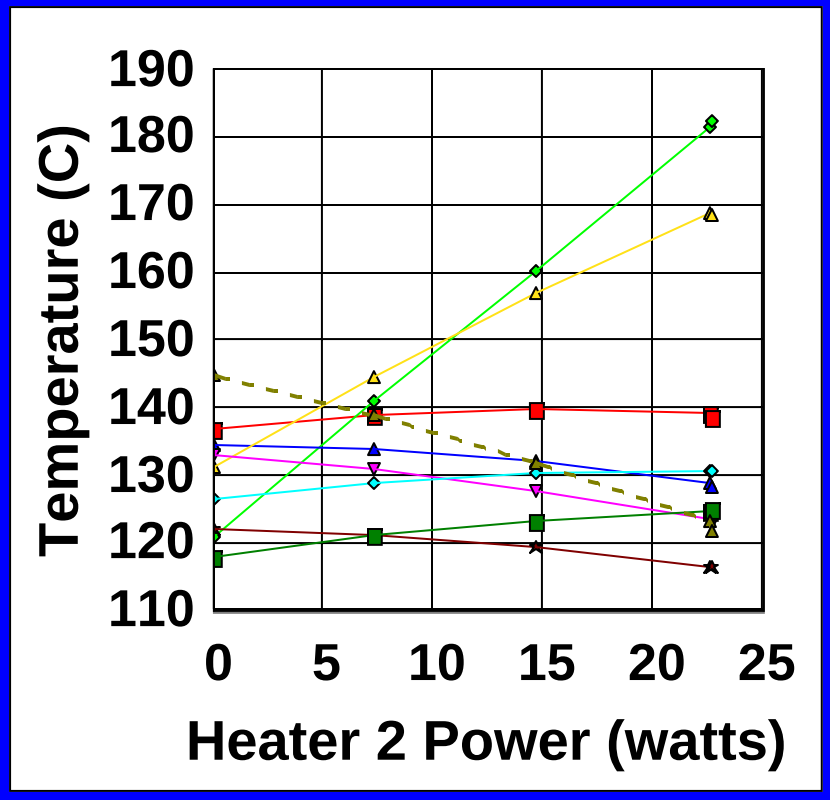
- Red - step change in chip power, 125 W, 150 C/sec
- Green - step change in fluid flow, 17 C/sec
- Blue - step change in heat sink heater, 88 W, 1.3 C/sec
- Predictable from lumped mass analysis

Chip Temperature on Actively Controlled Heat Sink



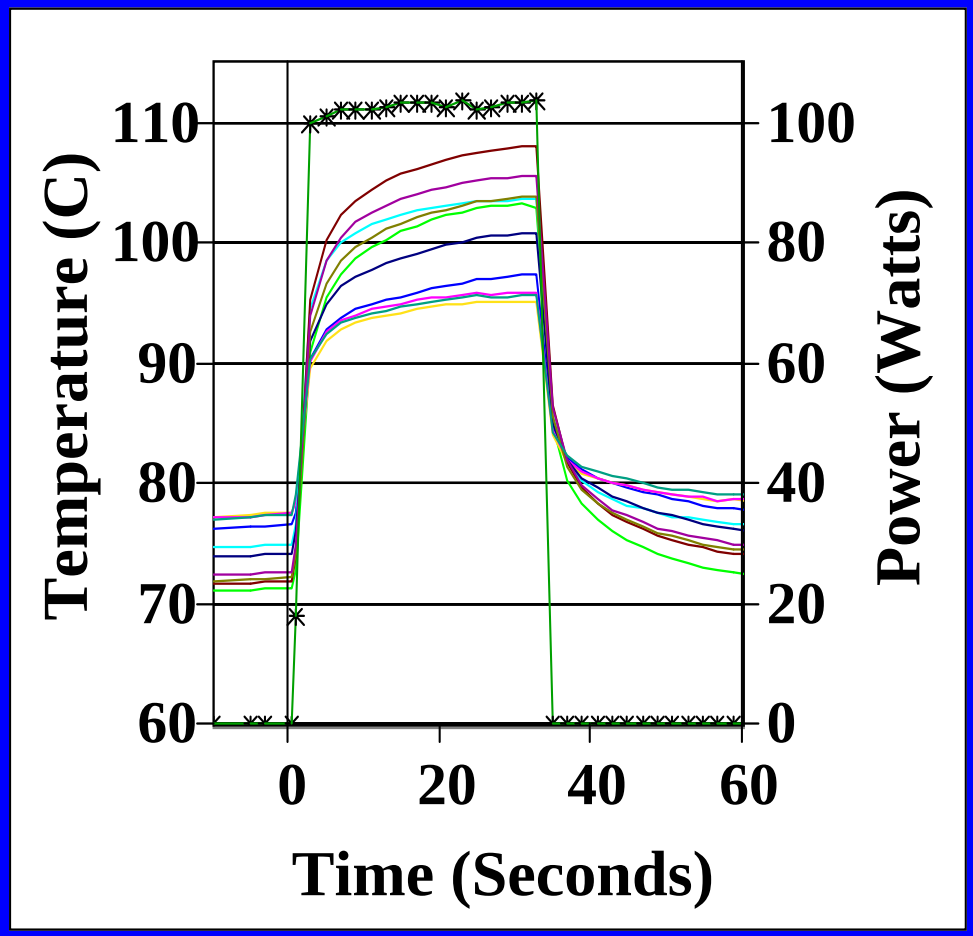
- Uniform P=90 W from t=0.0 to 25 sec
- 8 sensors on chip
- Some temperatures below set point
- Max chip temperature gradient = 40 C at SS
- Max test temperature gradient = 100 C

Chip Temperature vs. Power, High Temperature, Non Uniform Power



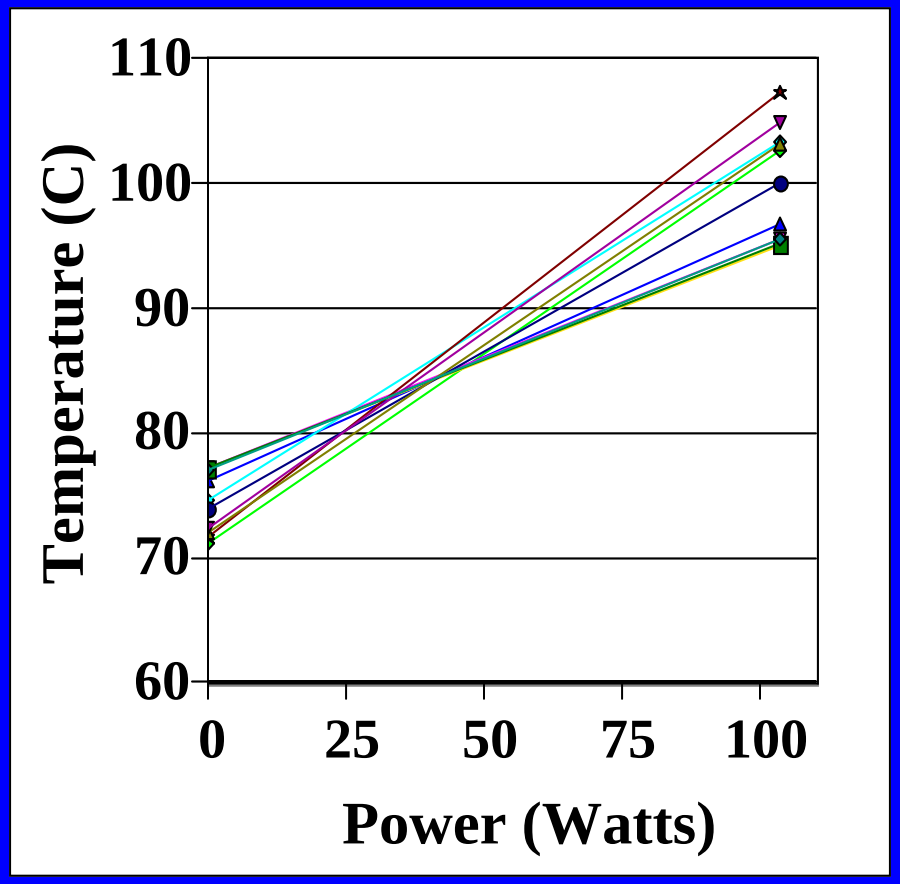
- Active heat sink
- Controls center temperature
- SS Power on one quadrant heater
- Temperature gradients at all powers
- Temperature still linear WRT power

High Temperature Test On a Passively Controlled Heat Sink



- Uniform P=100 W from t=0.0 to 35 sec
- Max test temp gradient = 38 C
- Max chip temp gradient = 12 C
- Avg chip temp increase = 0.27 C/W

Steady State Temperature Gradient vs. Power



- Same data
- Steady state chip temperature plotted vs. power
- Gradient across chip
- Average temperature increase

High Power Tester Characterization

- Performance measured with a thermal test chip
- Uniform power across chip (W/sq mm)
- Multiple temperature sensors on chip
- Plot all temperatures vs. time, before, during and after step power change
- Plot all temperatures vs. power (2 points)

Tester Specifications

- Max temperature gradient across chip and across entire test time
- Max temperature gradient across chip at zero and full power
- Average temperature increase with steady state power
- Heat sink force
- Heat sink force centrality

Conclusion

- Investigate each thermal phenomena independently
- Evaluate heat sink and interface with room temperature fluid.
- Fit equations to measured data
  - Not necessarily preconceived definitions of thermal resistance
- Evaluate across chip temperature gradients with uniformly powered thermal test chips

A Cost Effective, Flexible Approach to Automated Thermal Control During Burn-In

Chris Lopez, WELLS-CTI

Brian Denheyer, WELLS-CTI

Michael Noel, Freescale Semiconductor

Don VanOverloop, Freescale Semiconductor

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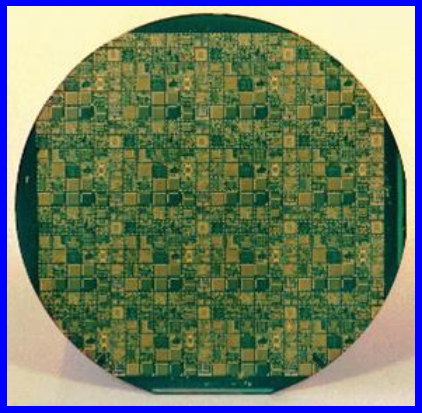
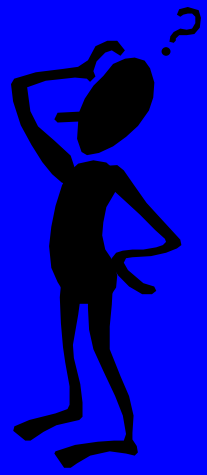
All IC devices are not created equal….

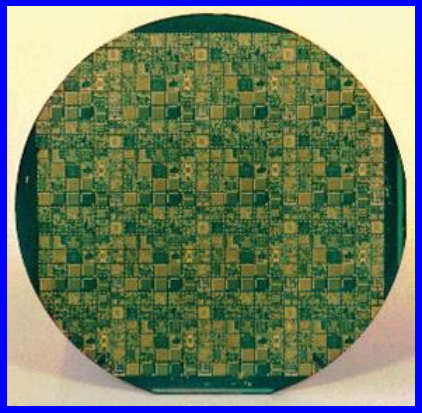
The Problem

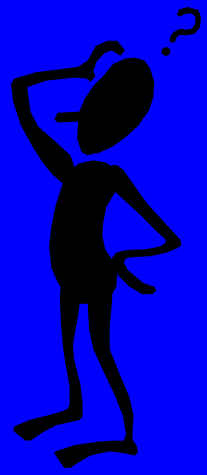




- Smaller devices
- Higher power products
- Larger power variances
- Increased demand for tighter temperature control
- Thermal runaway
- Smaller gate, greater leakage

The Problem





- Smaller devices
- Higher power products
- Larger power variances
- Increased demand for tighter temperature control
- Thermal runaway
- Smaller gate, greater leakage

How do we deal with all of this without raising the cost of ownership?

Technology Drivers

- Maintain cost control
- Maintain yields
- Maximize visibility
- Minimize the need for sort
- Maximize utilization
- Meet increasing demands of higher power, higher variance devices

Technology Drivers

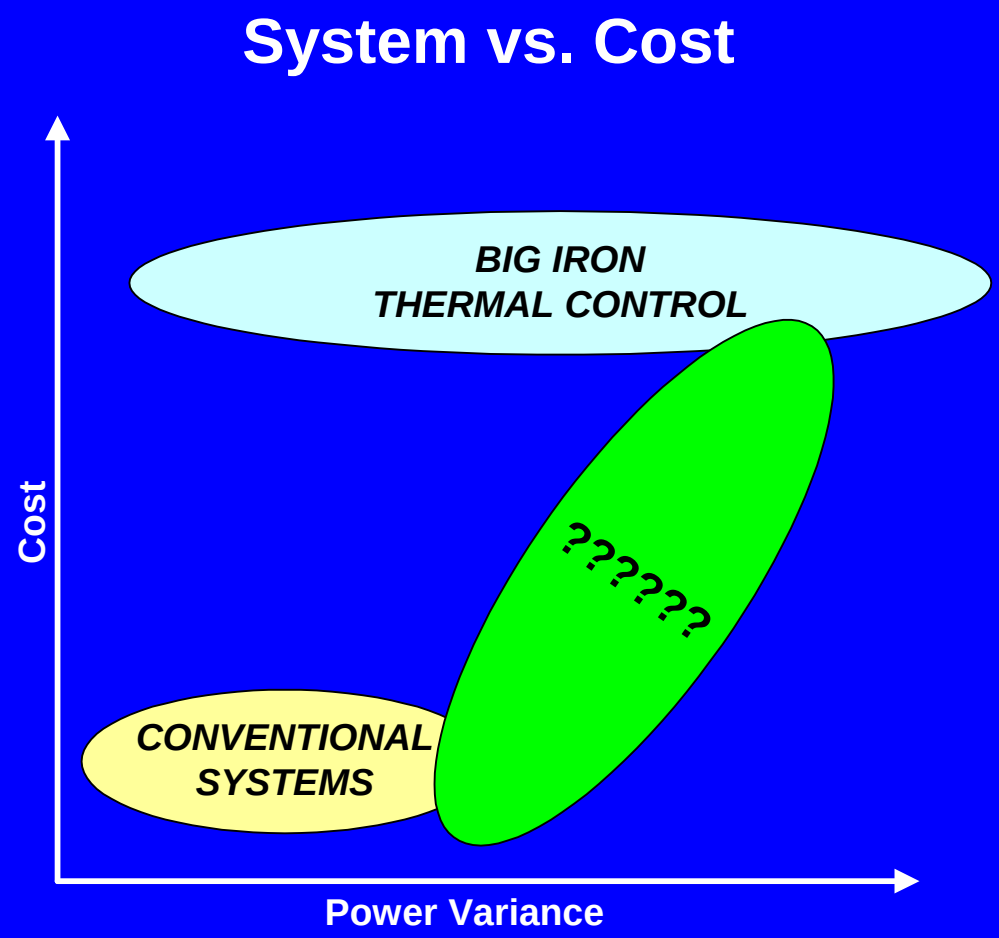
- **Maintain cost control**
- **Maintain yields**
- **Maximize visibility**
- **Minimize the need for sort**
- **Maximize utilization**
- **Meet increasing demands of higher power, higher variance devices**

"Commodity Products Require Commodity Means"

Present Technologies

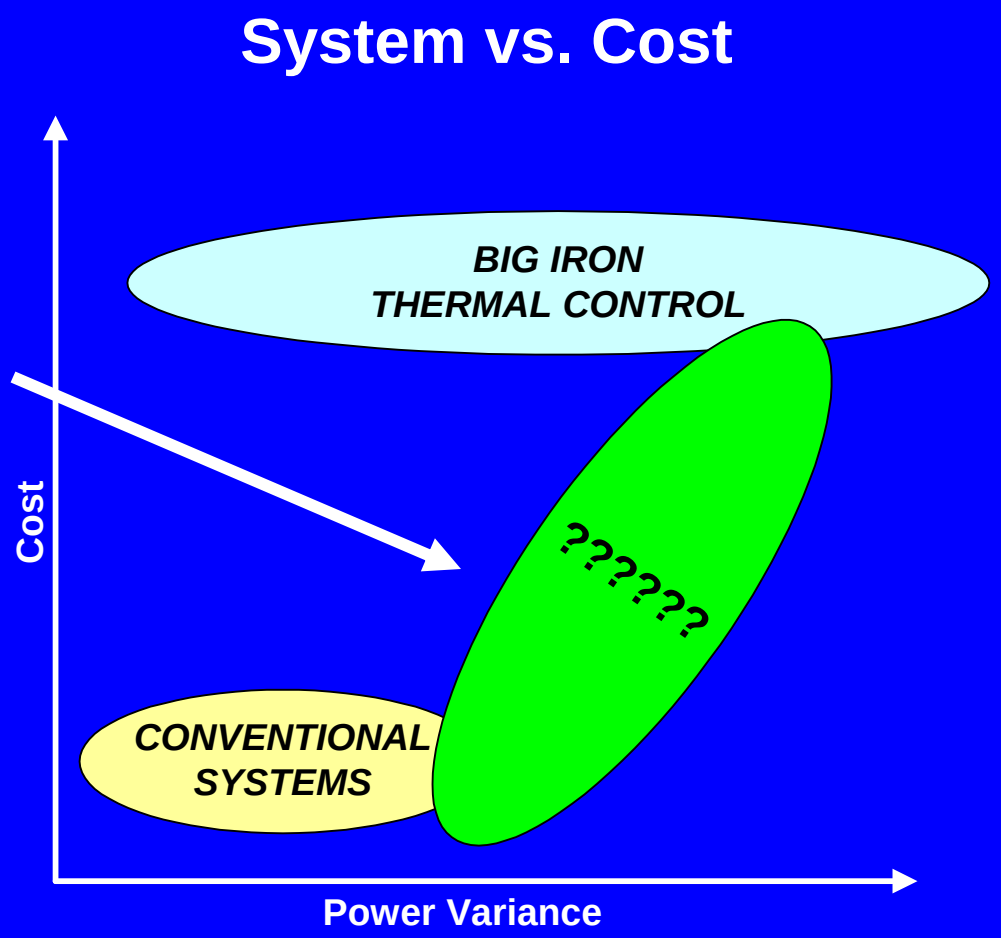
- Thermal control methods
  - Passive
    - Inexpensive, but does not solve the variance problem
  - Porting, valves, and fans –
    - Higher cost, with reduced density, but does resolve the variance issue…. maybe
  - Liquid
    - Higher cost, for higher power devices involving more maintenance… not for low cost commodity products

Present Technologies



Present Technologies

How do we fill the gap while keeping the existing high volume infrastructure?



Other Avenues

- **Bias Reduction – Are we really stressing the part, or are we just hiding?**
- **Burn-In longer at lower temperatures**
- **Sorting, binning… they are all cost adders**

Requirements Definition

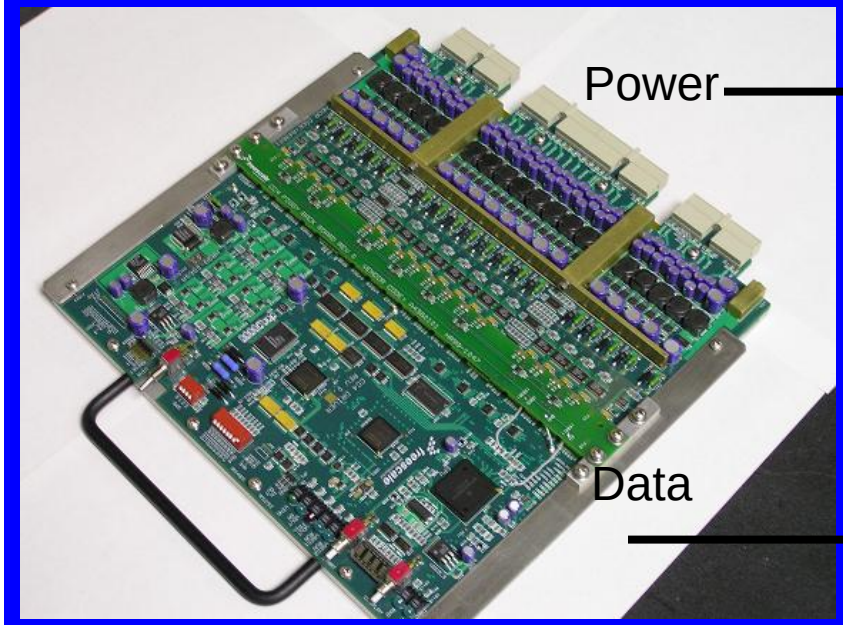
- Cost effective
- Independent device control
- Low risk
- Flexible, reusable for a variety of devices
- Maximum reuse of equipment and technology
- Minimal chamber modifications

Collaborative Effort

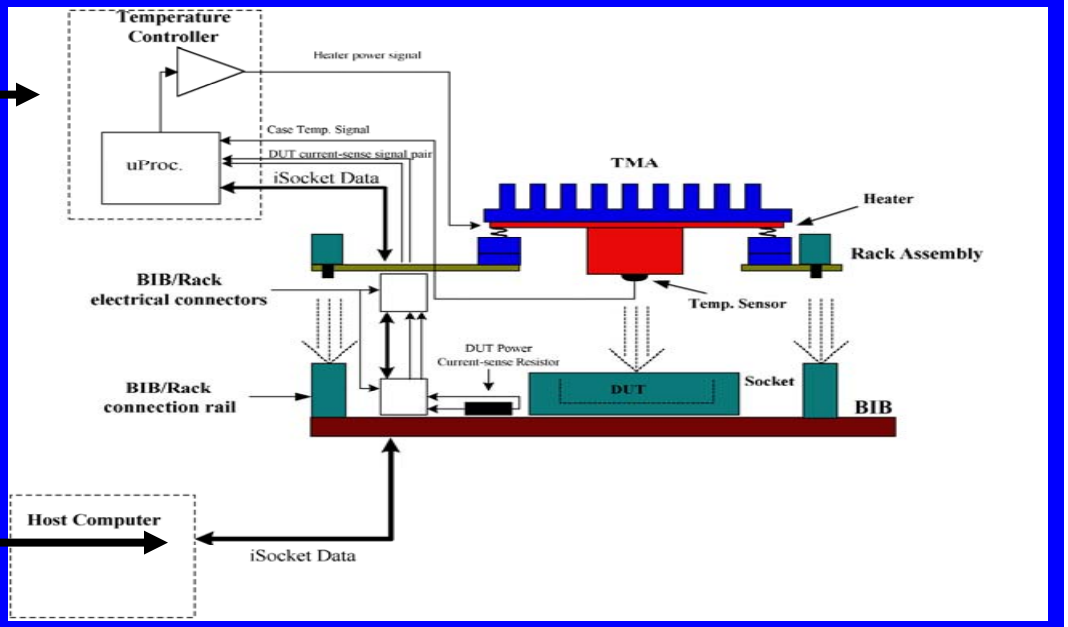
- Joint design with Freescale Semiconductor
- These requirements were analyzed to provide a gap filling solution
- Expertise brought together
  - Freescale Semiconductor
    - Driver
    - Software
    - Chamber
  - WELLS-CTI
    - iSocket
    - Controller
    - Firmware algorithms

Solution Overview

Freescale Semiconductor CC4 Driver



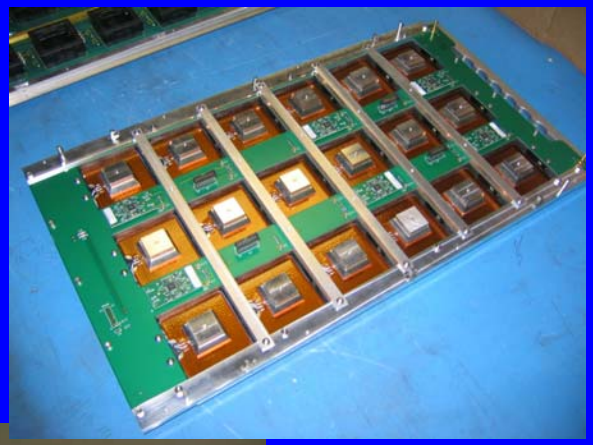
WELLS-CTI iSocket™



- **Low resource requirement**
  - **2 pins for communication**
- **Standard chamber configuration**

The Solution

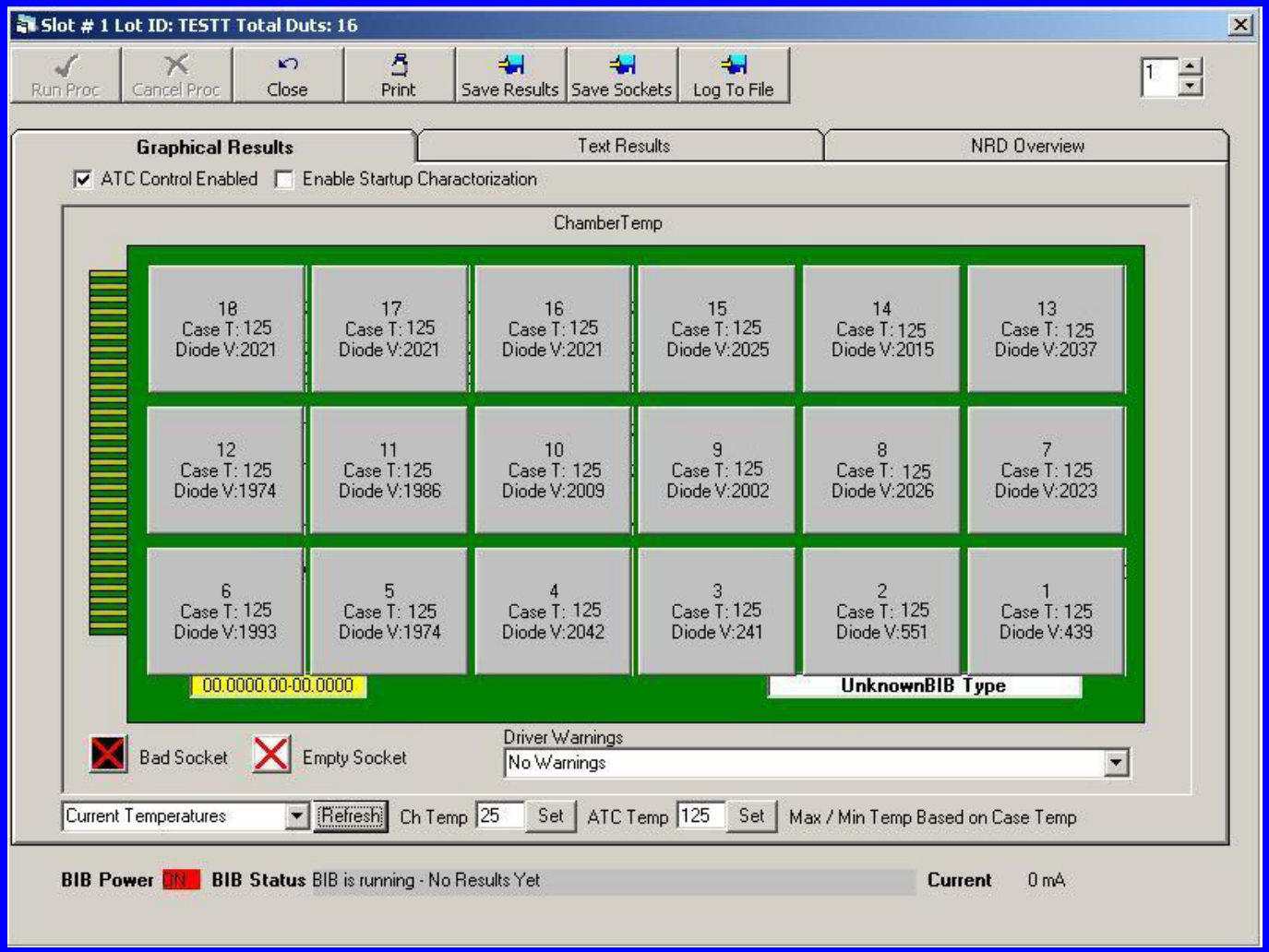
- Each site independently set to maintain temperature without outside monitoring or control
- Individually addressable
- Temperature feedback and control when DUT diode is not present
- Standardize across multiple devices
- Entire solution must maintain center to center spacing in chamber



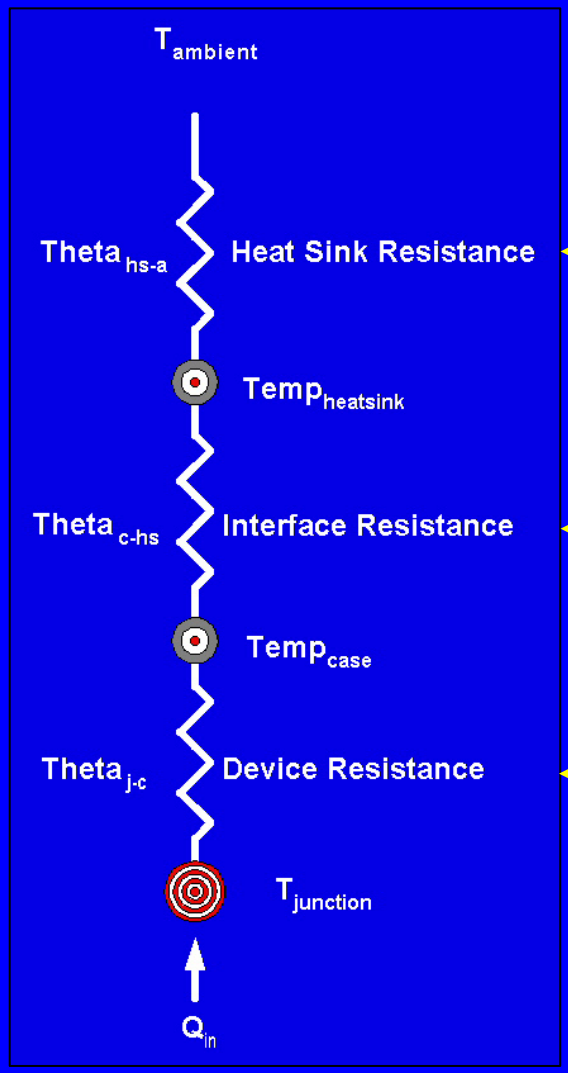
The Solution

- Autoloader compatible
- Field upgradeable firmware
- Diode calibration capability
- Self-contained
- Solid state solution

Integration / Visibility



Thermal Circuit

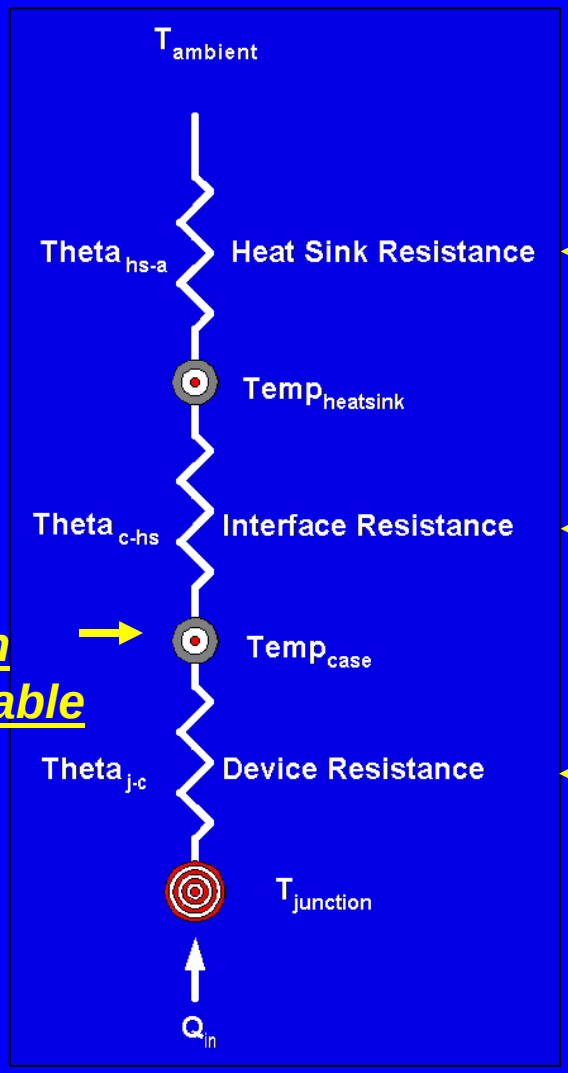


Variable due to chamber airflow instability

Unpredictable and variable

Predictable due to manufacturing stability in process for packaging, conductive heat transfer is very well understood

Thermal Circuit



Case measurement required when diode unavailable

Variable due to chamber airflow instability

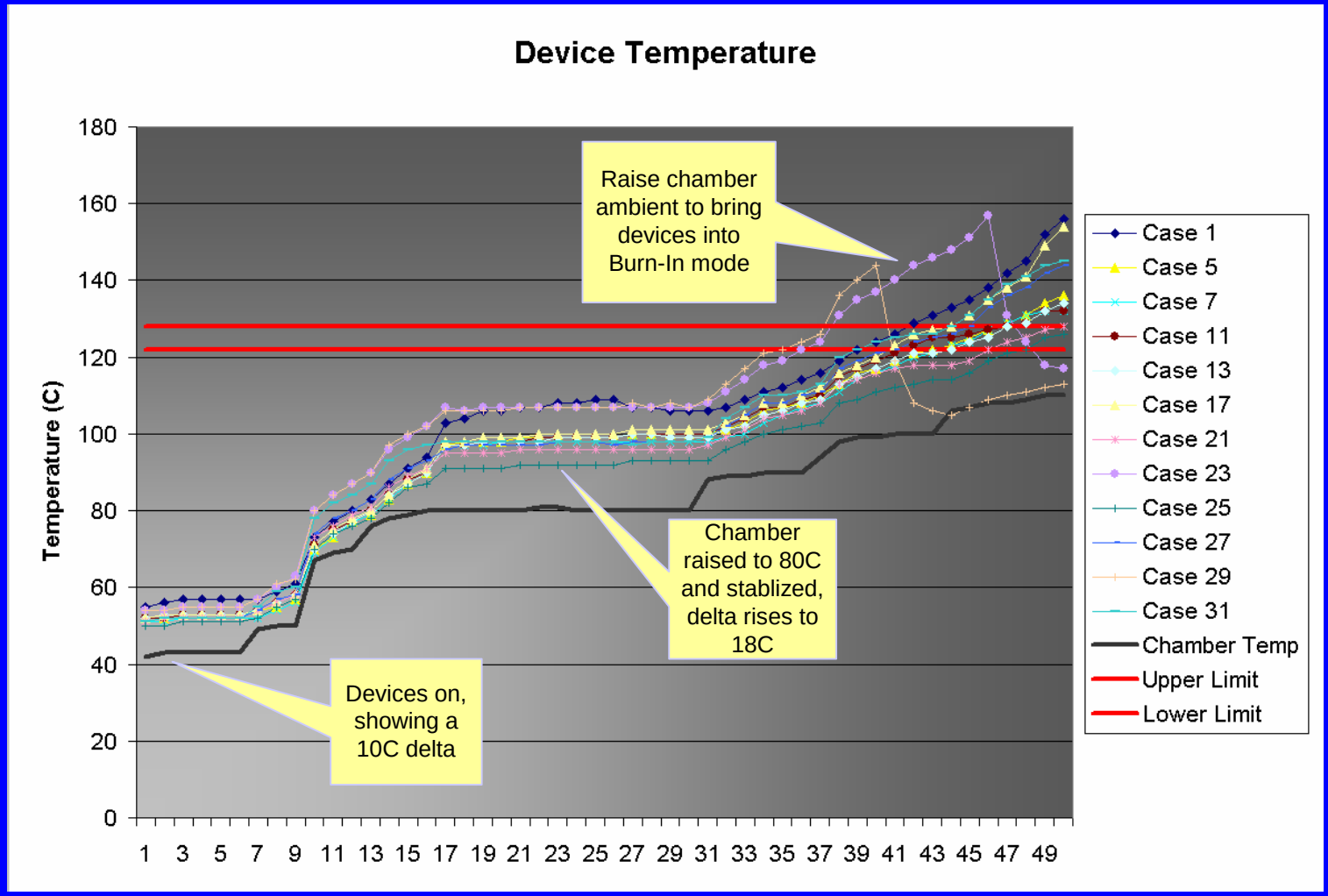
Unpredictable and variable

Predictable due to manufacturing stability in process for packaging, conductive heat transfer is very well understood

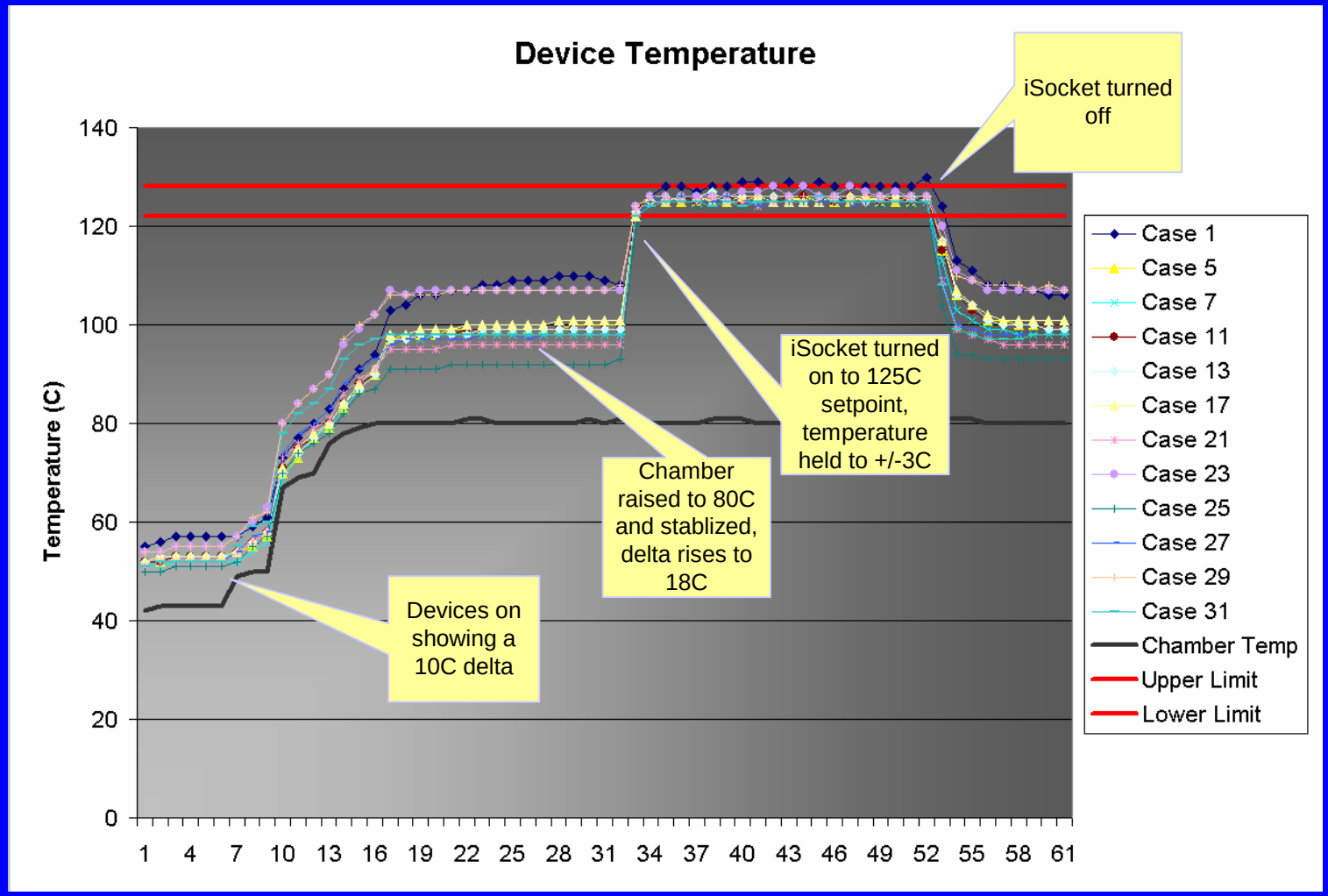
Case Study

- 20W Device
- 10W Maximum Variance
- Flipchip BGA with Integrated Heat Spreader (IHS)
- 16 devices per board
- 64 boards per chamber
- 1024 devices per chamber

iSocket™ Disabled



iSocket™ Enabled



The Benefits

- Improved system ramp time
  - Increased system utilization
- Reduced Burn-In duration
  - Increased system utilization
- Thermal control for over temperature
  - Reduces socket and BIB costs due to damage
- Precise control of DUT temperature
  - Eliminates binning
  - Eliminates sorting
  - Increased system utilization

The Benefits

- System upgrade vs. procurement
  - Lower implementation costs
- Seamless control of devices for biasing and precise temperature control
  - Higher confidence in burn-in effectiveness
  - More accurate burn-in
- Maintains automation

Conclusion

- **Flexible, automated self contained solutions are required for today's burn-in systems to reduce ownership costs**
- **Thermal control is required for many of today's products and cannot be operated in conventional systems without the integration of active thermal control**
- **Care must be taken to understand device characteristics to provide the most effective solution**
- **Today's solutions are much more involved than just removing the heat……**

Special Thanks

- Eric Zahl – WELLS-CTI
- Dan Wilcox – Freescale Semiconductor
- Doug Grover – Freescale Semiconductor

High Efficiency Passive Heat Sinks for 5-20 W Applications

Natarajan “Ram” Ramanan

Applied Thermal Technologies, LLC

Mike Ramsey

Plastronics Inc.

Objectives of This Study

- Design a high efficiency passive heat sink suitable for 5-20 W applications
- Thermal analysis of heat sinks
- Build prototypes and test heat sinks
- Recommendations for heat sinks and interface materials

Background

- Many burn-in chamber manufacturers with different oven configurations
- Airflow Ranges from 50 fpm to 1200 fpm. Typical airflow is 200 fpm
- Number of boards range from 10 to 50
- Spacing between boards can be as low as 1.6” [40 mm – 1U Size]
- Can skip every other board for 2U spacing [80 mm]

System Analysis

- Burn-in ovens
  - Flow side to side or bottom to top
  - Up to 56 boards

Thermal Resistance

- $\Theta_{ca} = (T_{case} - T_{ambient})/Power$
- $\Theta_{ja} = (T_{junction} - T_{ambient})/Power$

- Many different packages, boards – Hard to define thermal conduction into the boards due to the variations
- (To be conservative), we will assume heat transport to be (mainly) through the heat sink

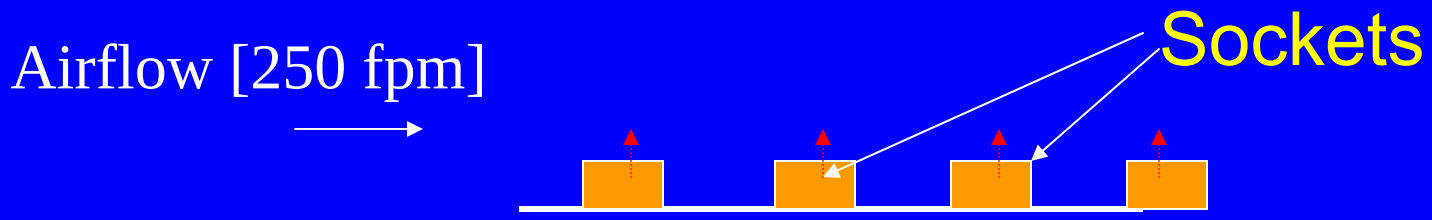
System Variables

- Airflow = 50 fpm to 1200 fpm
  - Influences pre-heat
  - Influences heat sink performance
- Die Power = 5 - 20 Watts
  - Influences pre-heat
- Board restrictions
  - Spacing between boards = Impact on heat sink height
  - Spacing between sockets = Impact on heat sink foot print

Burn-in Requirements

- Minimum case (die) temperature = 130 °C
- Maximum case (die) temperature = 150 °C
- Socket temperature < 170 °C

Pre-heat



- With rows of Sockets, Preheat is 0.5 °C/W for 250 fpm, 0.25 °C/W at 500 fpm
- 5 Watt Sockets: 4 Sockets in sequence => 10 °C [temperature rise], 120 °C (in), 130 °C (out). Need 2 °C /W Heat sinks.
- 10 Watt Sockets: 4 Sockets in sequence => 20 °C [Temperature rise], 120 °C (in), 140 C (out). Need 1 °C/W Heat sinks.

System Analysis

- 20 Watts: at 500 fpm, 5 °C per socket preheat. 110 °C in, 130 °C out. Need 1 °C/W Heat sink.
- 20 Watts: at 1000 fpm, 2.5 °C per socket preheat. 110 °C in, 120 °C out. Need 1.5 °C/Watt Heat sink.
- Spreadsheet for predictions

Heat sink (θ_{ca}) °C/W
T=110-120 °C, 4 Sockets in Row

Power	200 fpm	500 fpm	1000 fpm	Ambient
5 W	1.6 °C/W	4 °C/W	8 °C/W	130 °C
10 W	0.9 °C/W	1.4 °C/W	1.6 °C/W	110-120 °C
20 W	0.5 °C/W	1 °C/W	1.5 °C/W	110-120 °C
30 W	0.34 °C/W	0.7 °C/W	1.5 °C/W	110-120 °C

Thermal Model

- Socket with pins modeled
- Board with FR4 properties –
  - K (plane) = 30 W/m K
  - K (thickness) = 0.38 W/m K
- Better die-board resistance will only reduce thermal resistance. Current work is conservative
- TIM = 0.1 °C/W [0.020” thick, 4.5 W/m K, 20 psi, Gelvet MC-8 like interface material]
- ICEPAK © Electronics cooling software

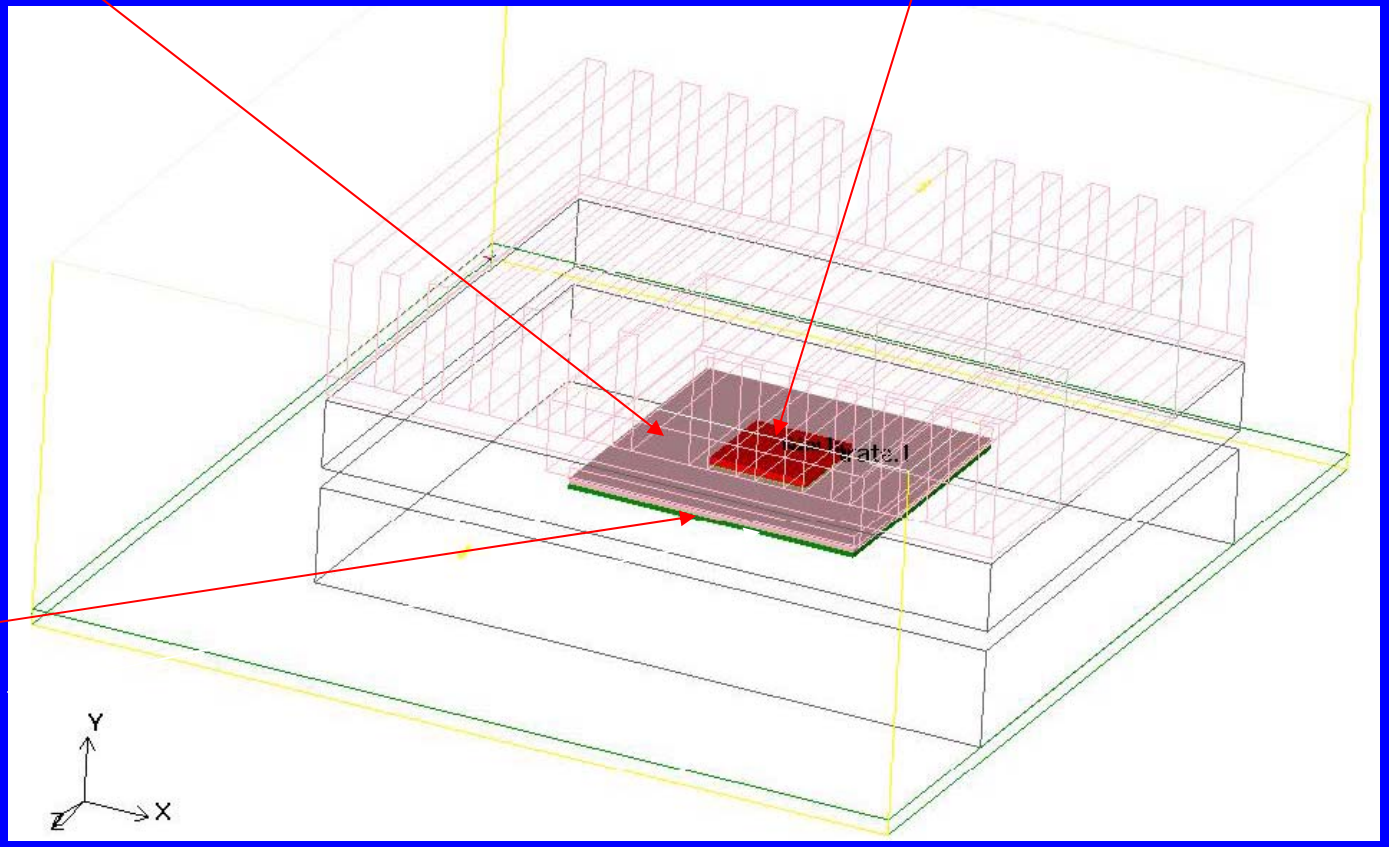
BGA Package Compact Model

Package 30 x 30 x 1.2 mm

Die 10x10 mm

Substrate

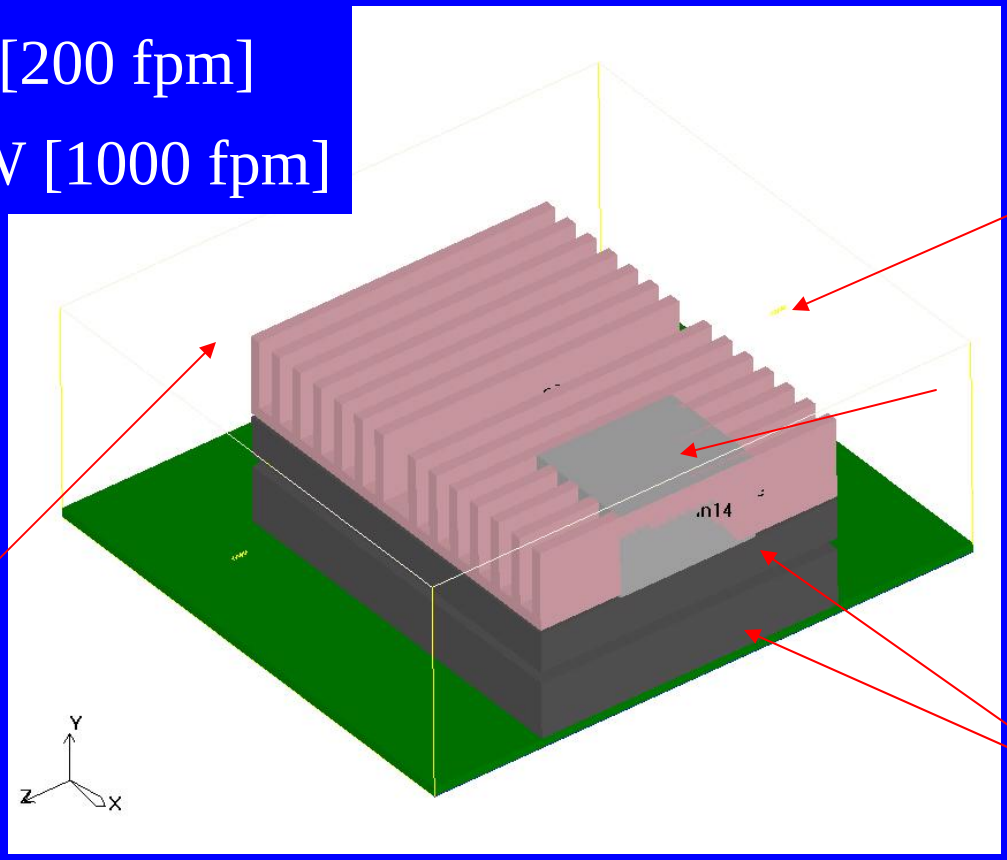
Ball grid



Heat Sink – Current Design, 1U [1.5” Spacing]

Θ_{ca} = 2 °C/W [200 fpm]

= 1.1 °C/W [1000 fpm]



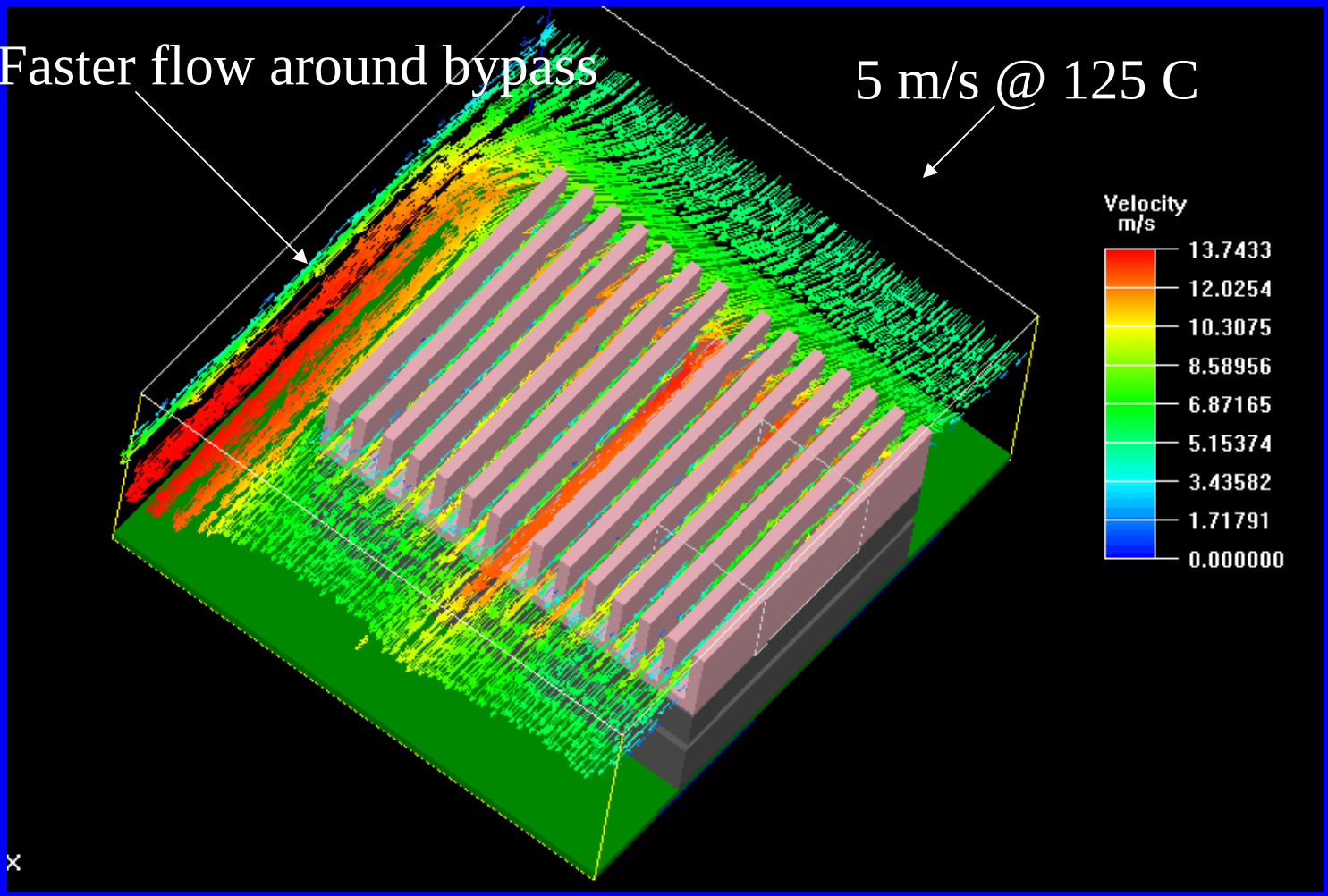
Airflow

Milled for access To clasp

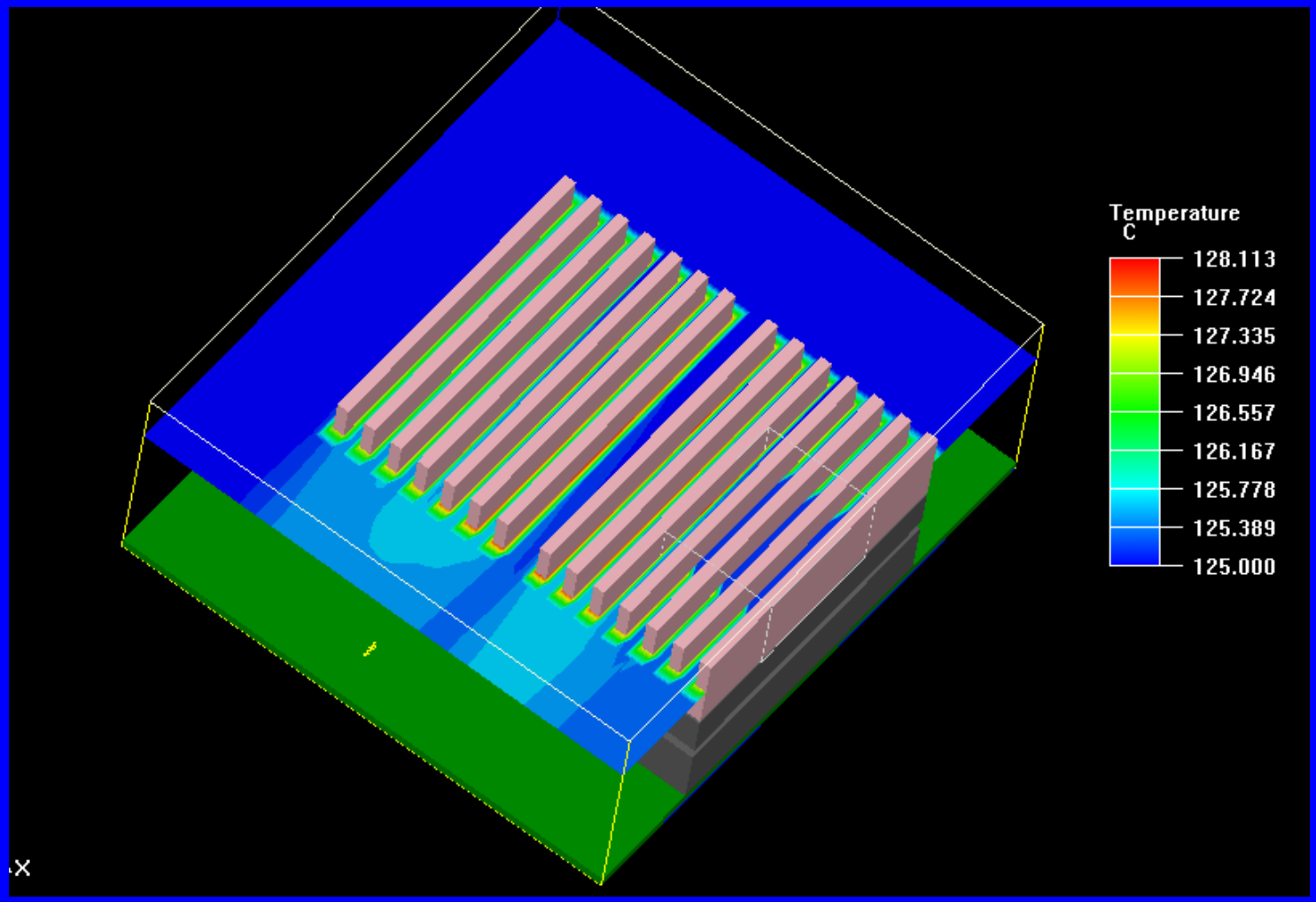
Bypass at the side = 4/5”

Socket

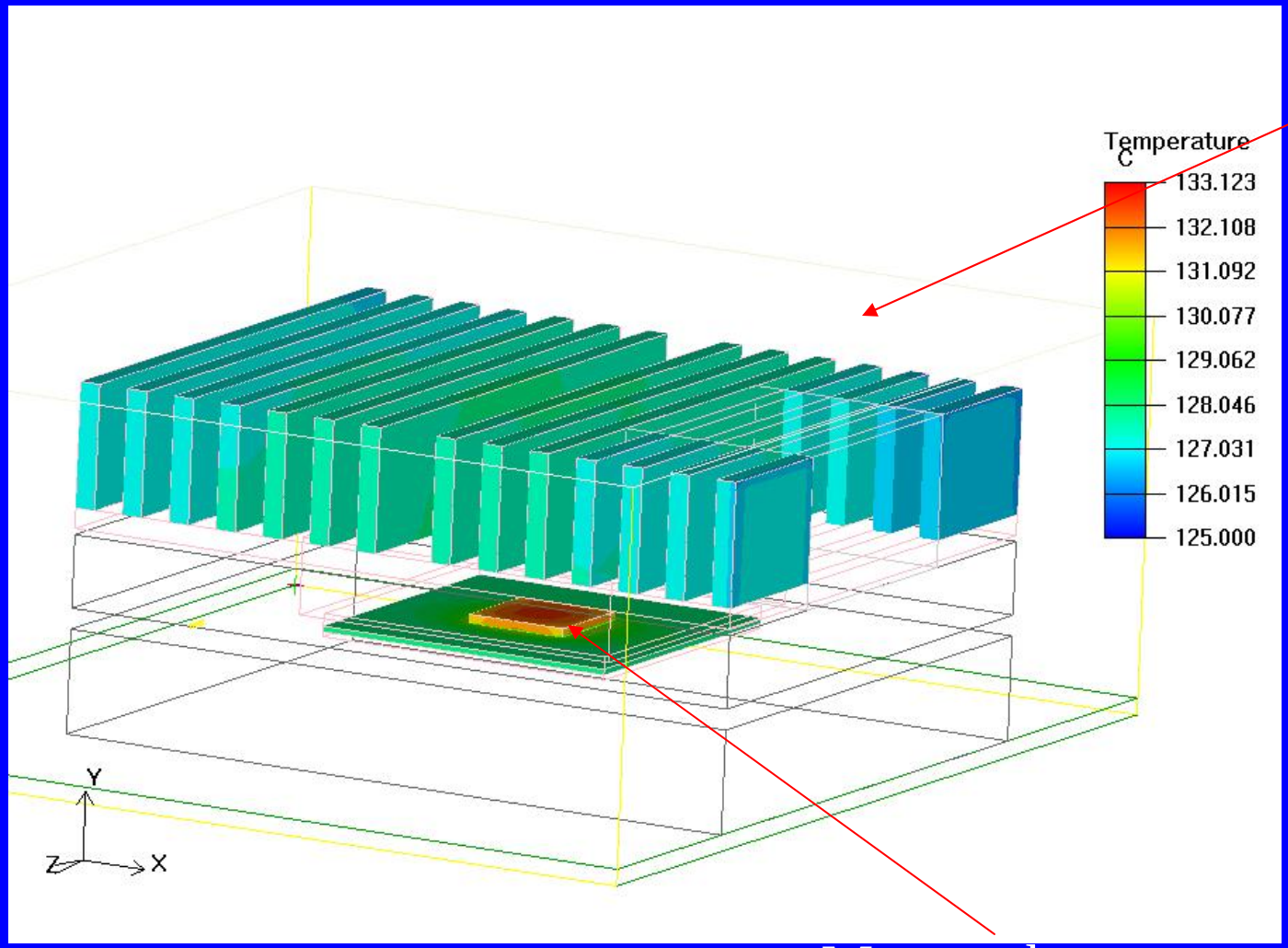
Heat Sinks – Velocity Field (1000 fpm= 5 m/s)



Air Temperatures



Temperature distribution (fins)



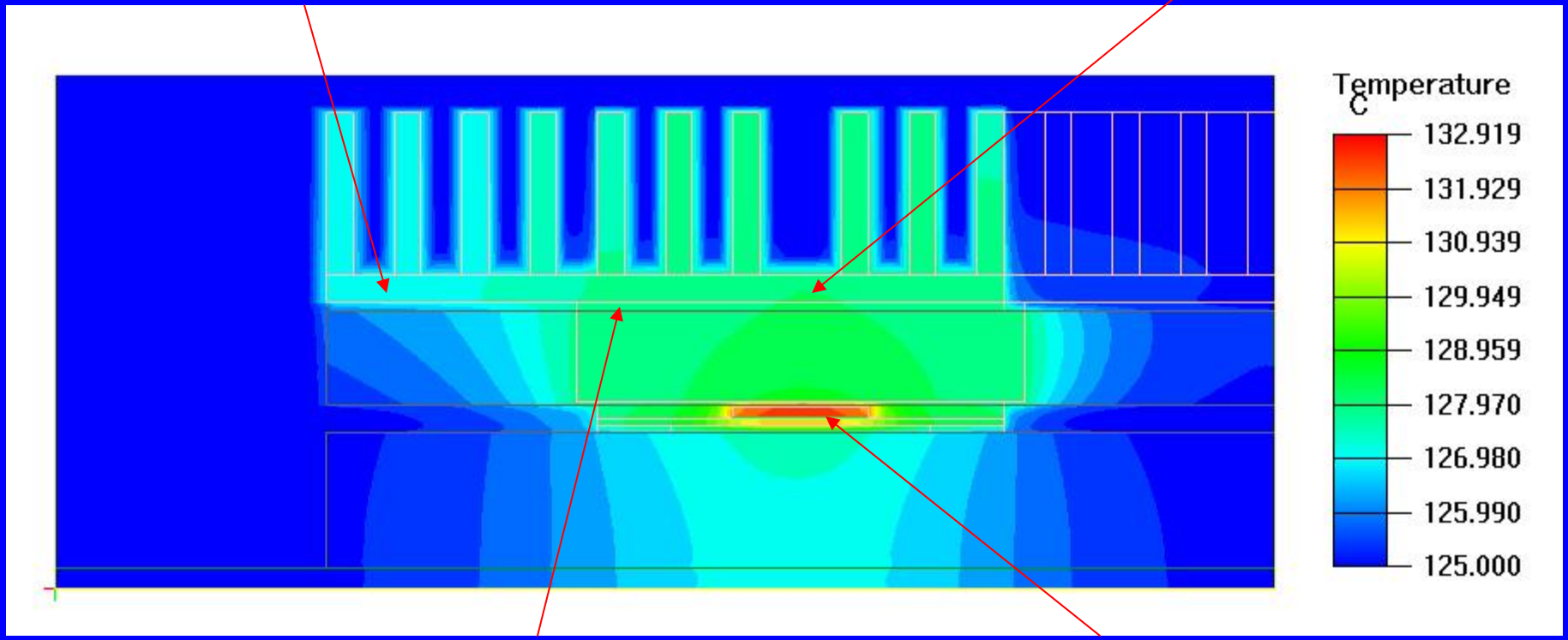
5 m/s @ 125 C

Max package temp = 133.5

Temperature Distribution – Section @ middle of the die/heat-sink

Cooler edges

Hot center



Spreading resistance in the base

Die

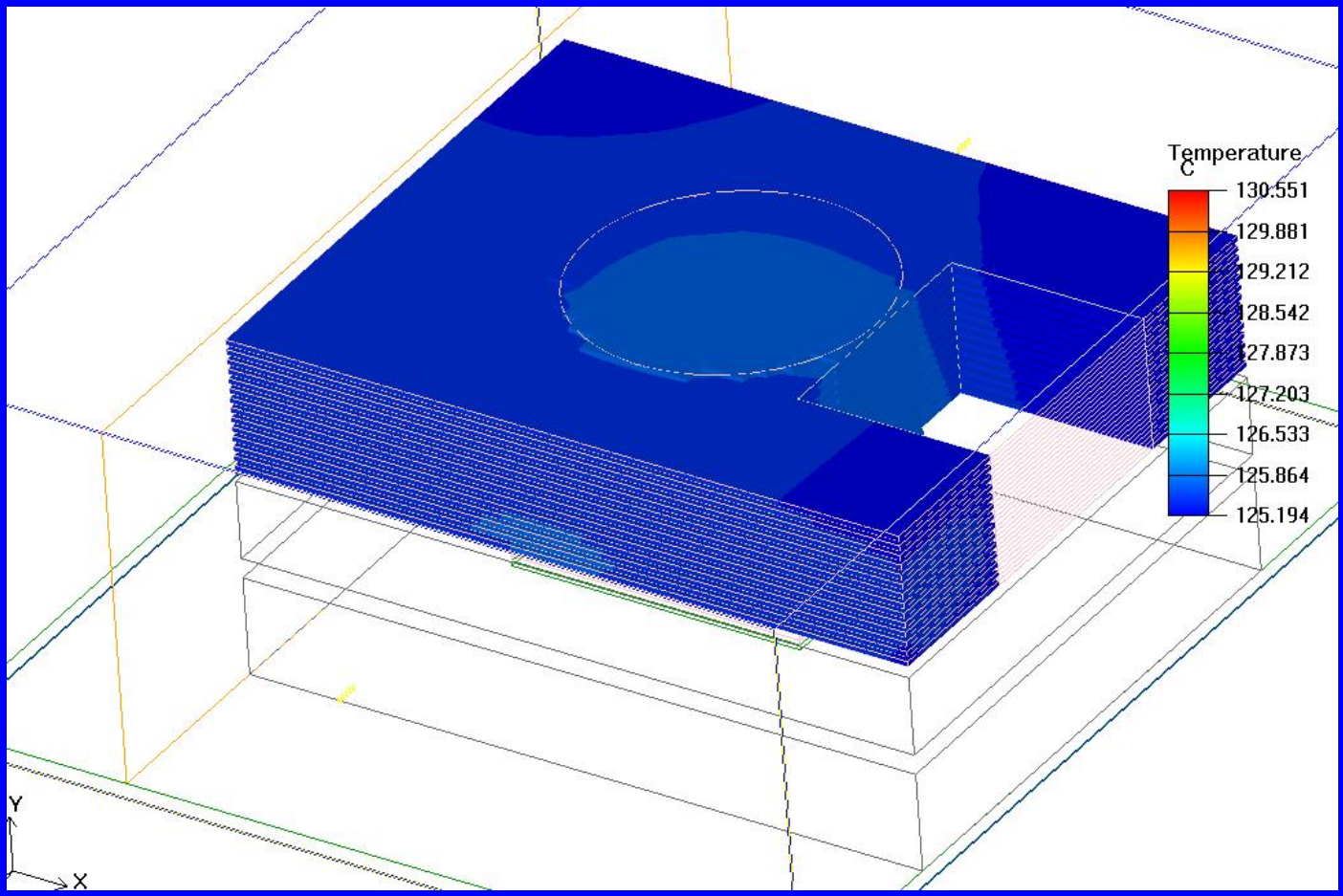
Heat sink resistance break-up

- Θ_{ja} = 1.7 °C/W
  - = 0.1 °C/W [Bottom-Base]
  - + 0.1 [Top-base]
  - + 0.9 [Fin-air]
  - + 0.1 [interface pad]
  - + 0.5 [Package resistance]
- Θ_{ca} = 1.1 °C/W @ 1000 fpm

Observations & Analysis

- Heat sink performance is a direct function of
  - Surface area available [Fin-air]
  - Spreading resistance in the bases
- Cutting bypass flow around heat sink improves performance by 3%
- Heat pipes do help with reducing spreading resistance.
- Best option (cost & performance) found is a copper column-type heat sink shown next

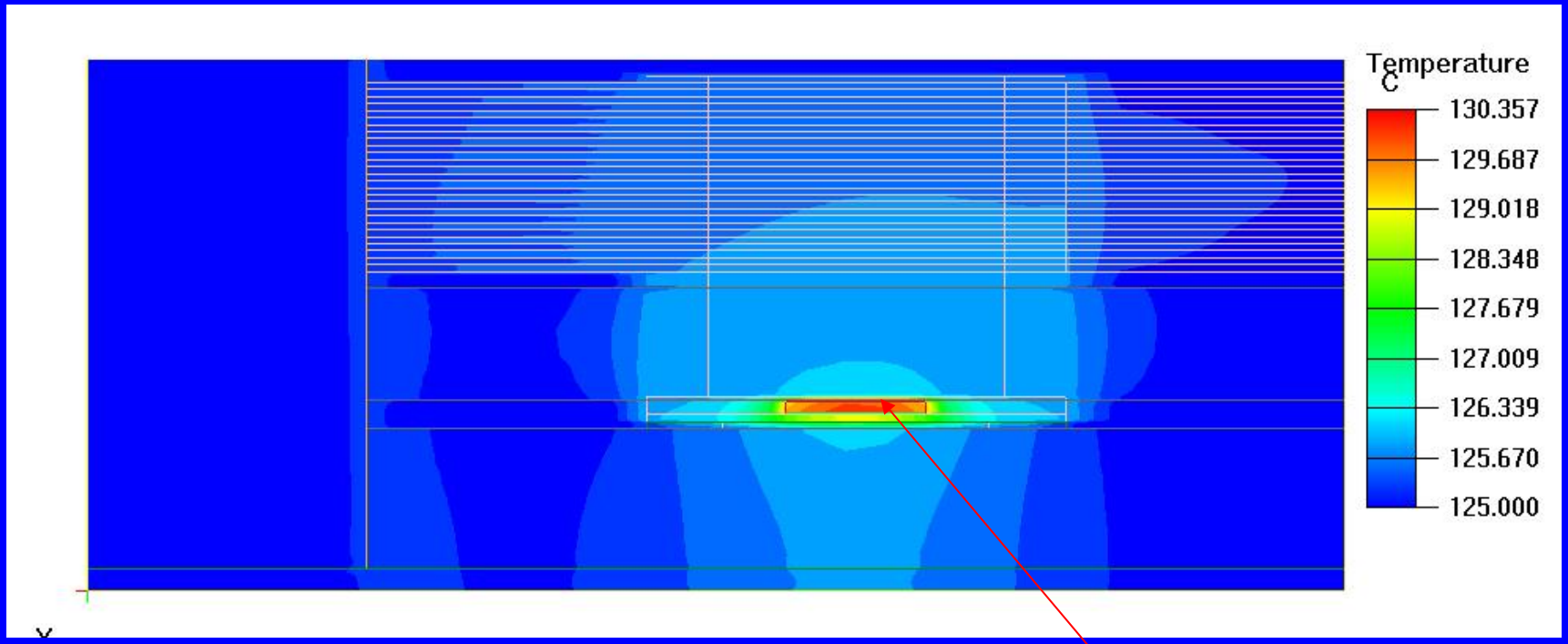
1U-Copper column/disc fins



Θ_{ca} =0.65 C/W at 1000 fpm

½ mm thick Cu fins, ½ mm gap [12- 14 fins soldered to Cu core]

1U-Copper Column/Disc



Thermal Performance vs. airflow

Airflow	Pressure Drop (inches of water)	Θ_{ca}
200 fpm	0.31	1.08 ◦C/W
500 fpm	1.4	0.8 ◦C/W
1000 fpm	2.88	0.68 ◦C/W

Cost Considerations

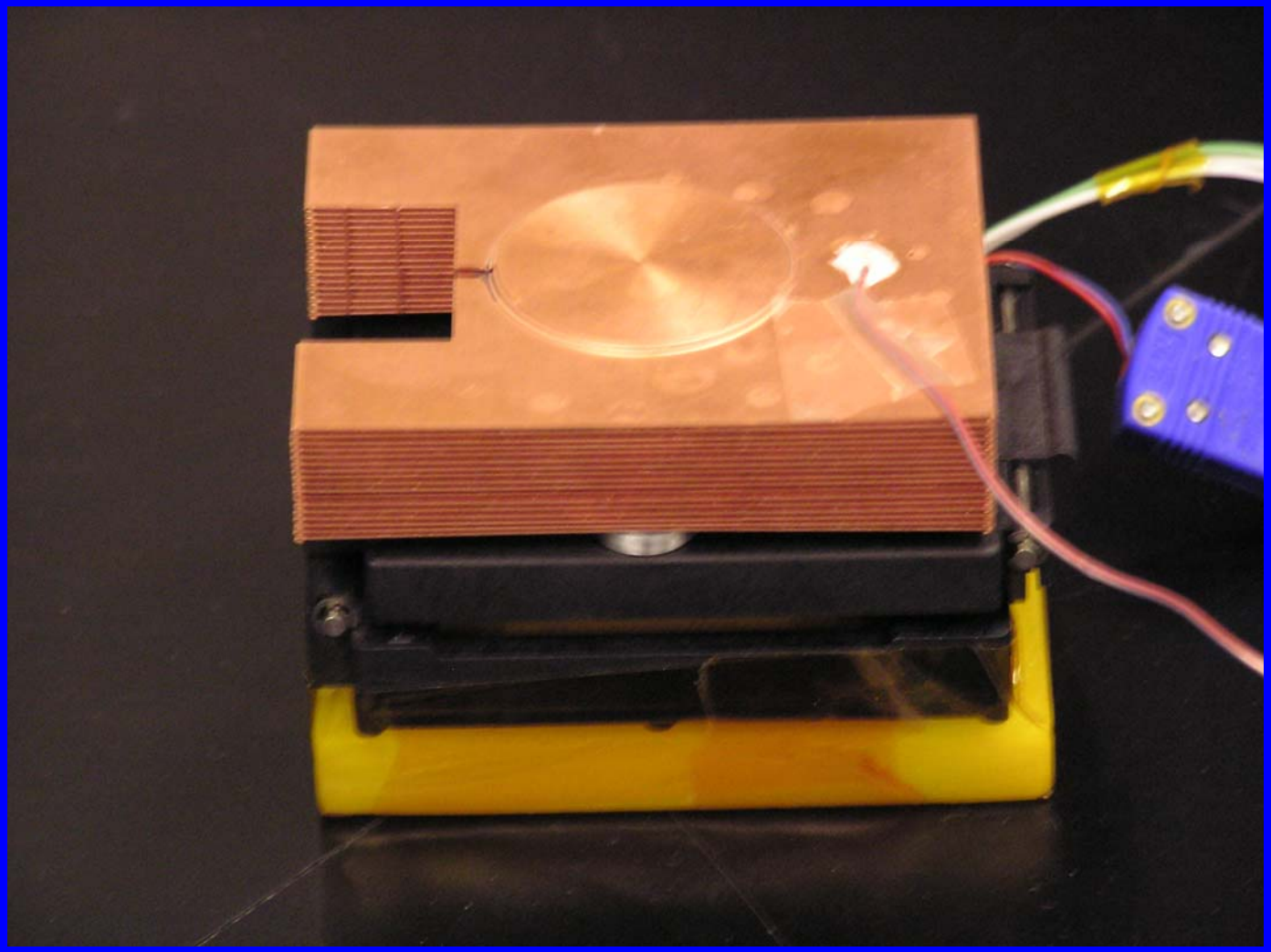
- Aluminum fins with nickel plating is more expensive than un-plated copper fins
- Copper column with ½mm thick Copper fins & ½ mm spacing appears to the best performance/cost option
- 2U size with 1 mm spacing offers almost 1/3 pressure drop for same thermal resistance

Next Steps

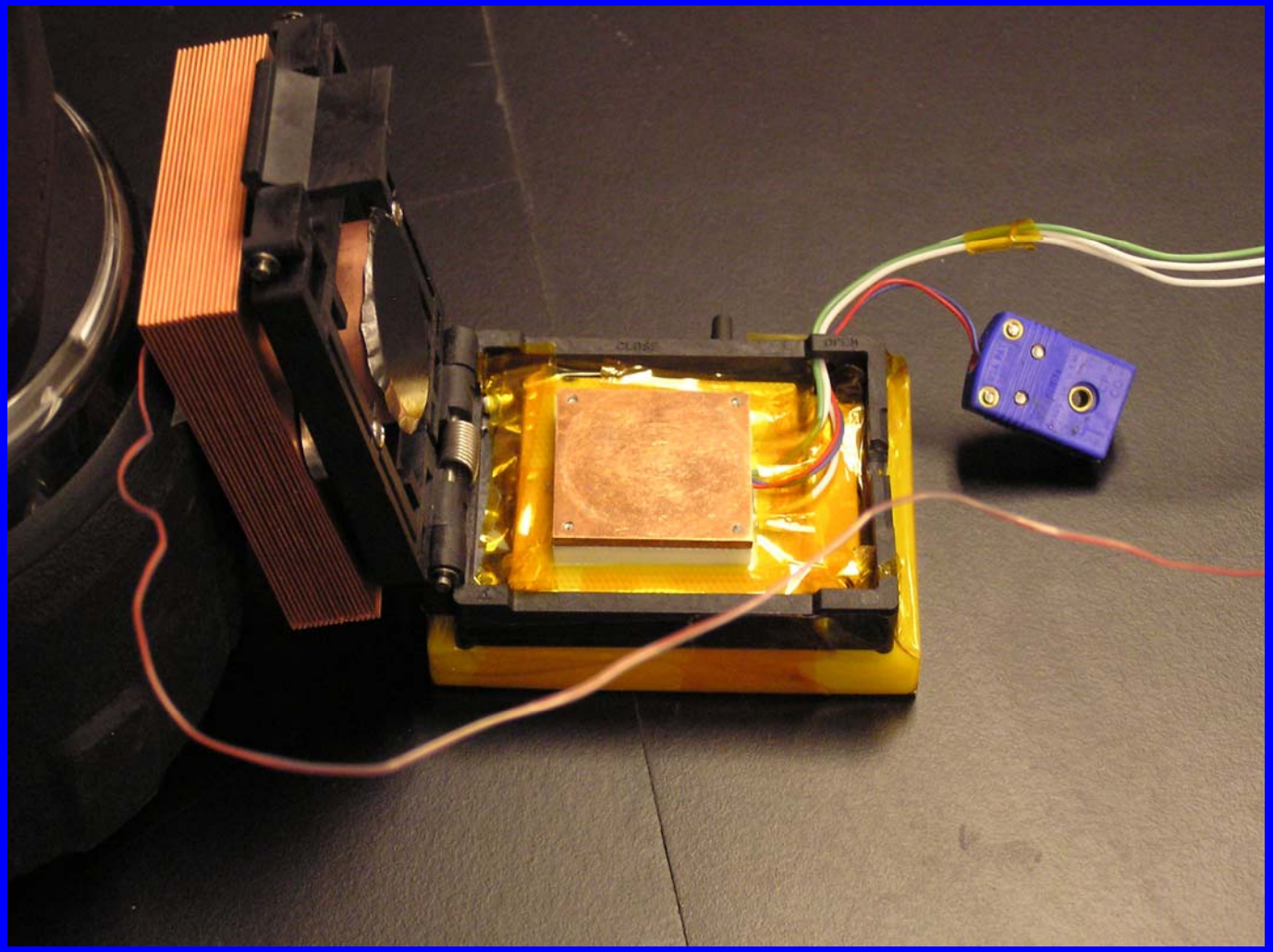
- Build prototypes
- Test heat sink performance vs. airflow
- Identify other improvements & gaps in analysis
- Attachment options & interface pressure

Prototype Heat Sink

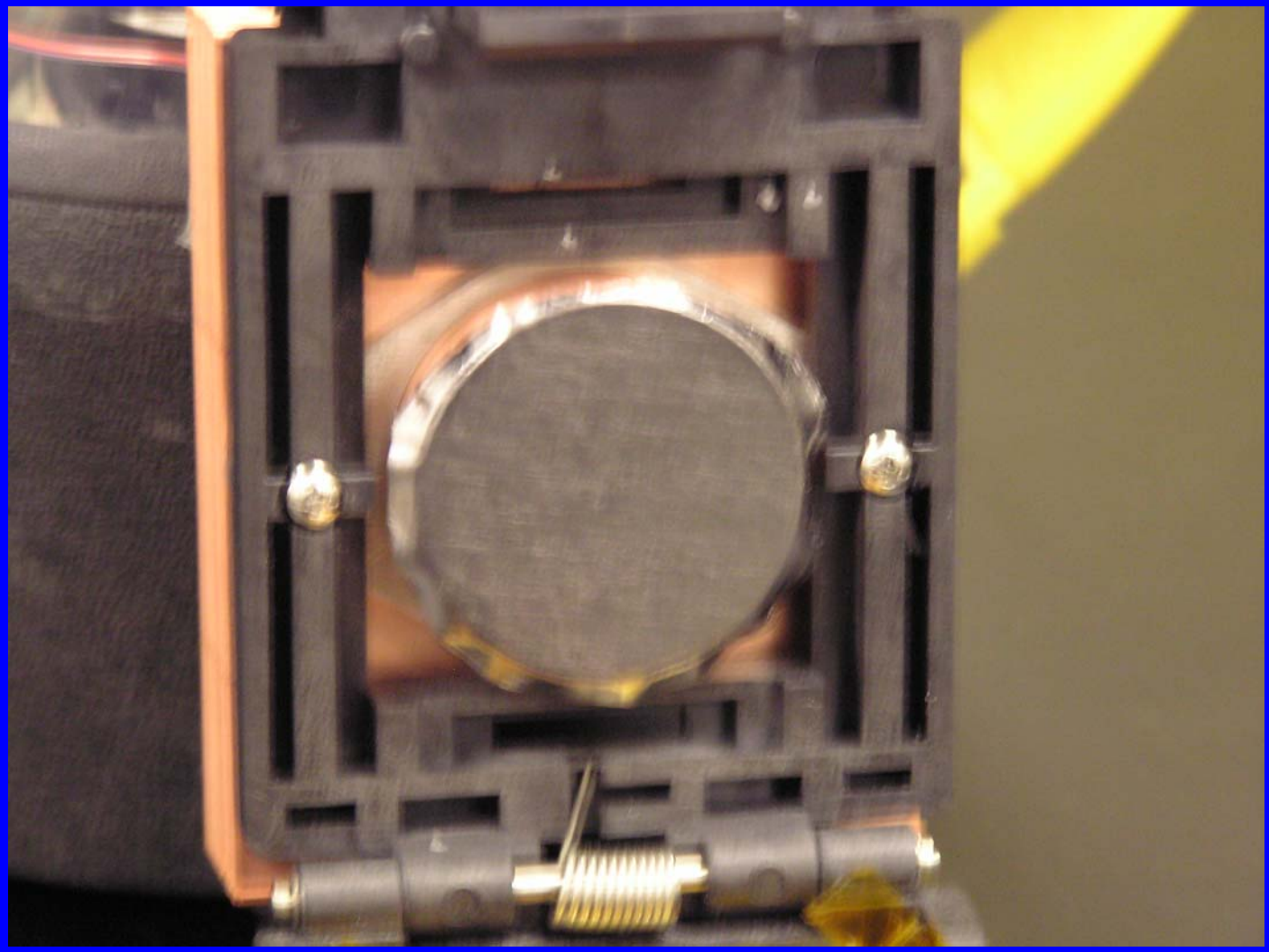
Heat sink with socket



Socket Open with Heater



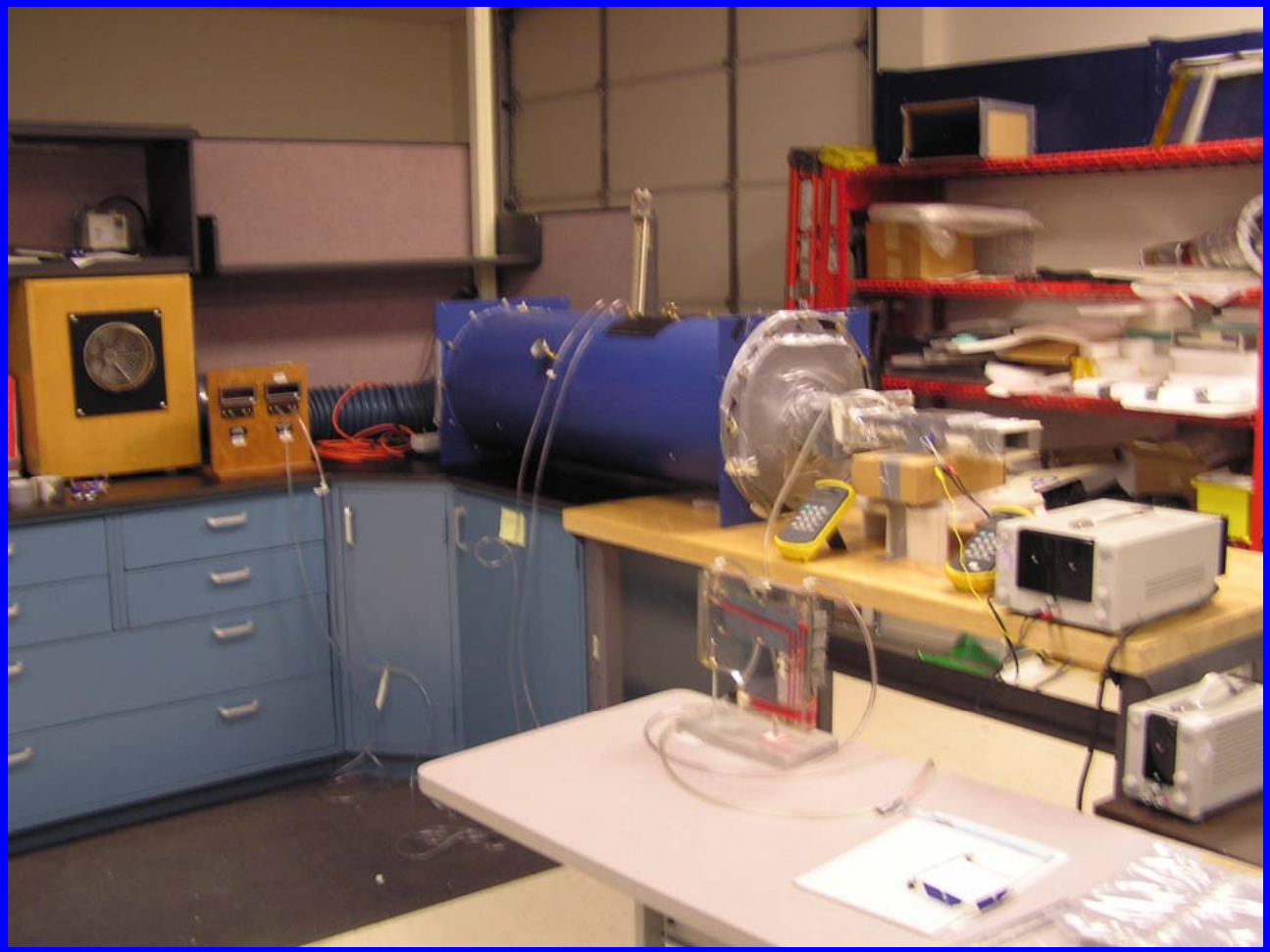
Interface Material



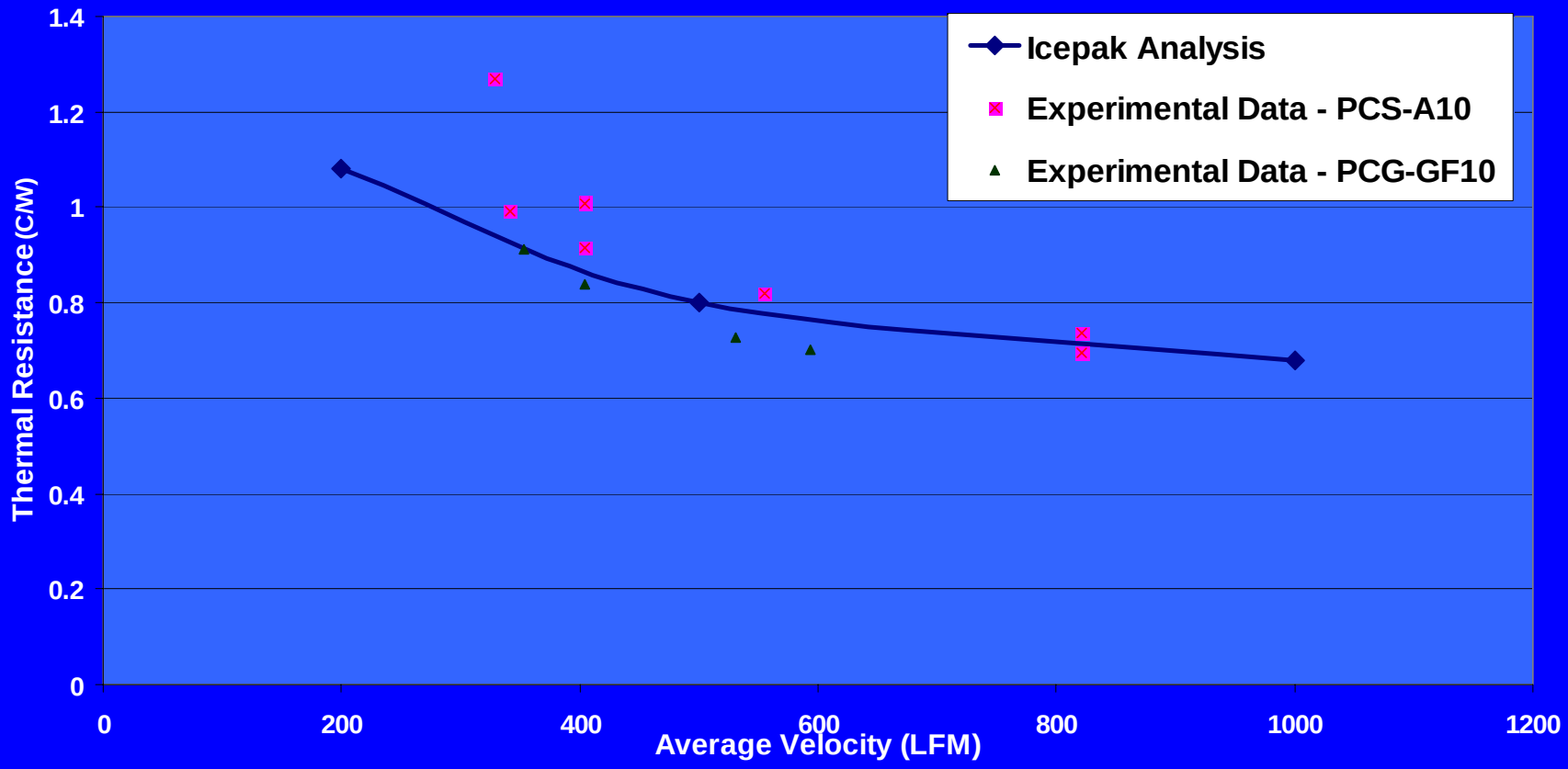
Test Setup

- Ceramic heater [25mm x25mm] with a copper substrate used as the heat source
- Thermocouple embedded at the surface of the copper substrate
- Heater attached a board which is placed on a plastic substrate
- Wind tunnel with variable speed blower for varying airflow [10 cfm to 40 cfm]

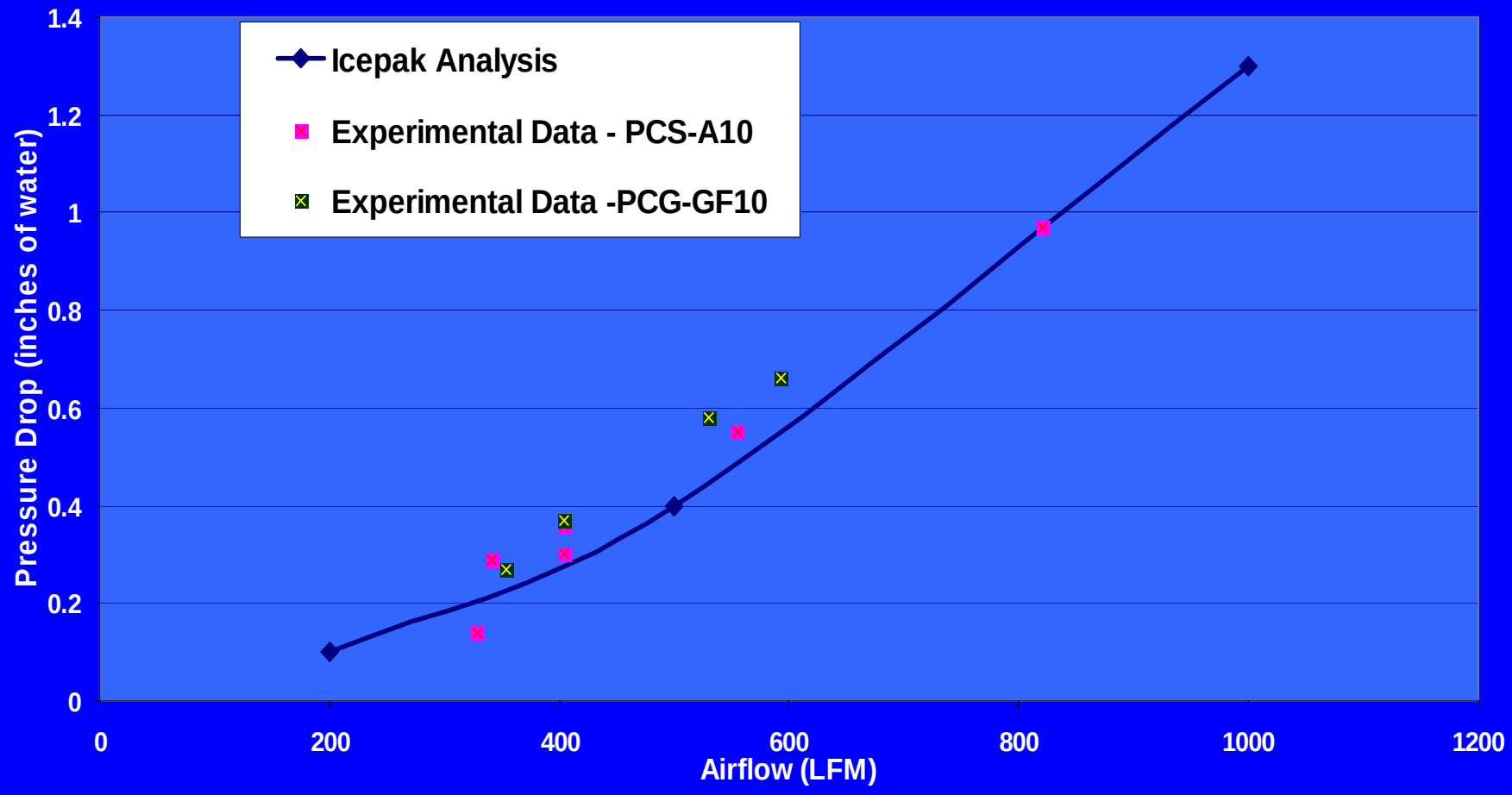
Experimental Setup



Experimental Data



Experimental Data



Interface Materials

- PCS-A10 : 110 micron, Aluminum-backed phase-change material. Thermal resistance is 0.1 °C/W at 5 psi.
- PCG-GF10: 185 micron, Grafoil-based phase change material, Thermal resistance is 0.075 °C/W at 5 psi.
- At low pressures (under 5 psi), Grafoil has lower thermal resistance than PCS-A10.
- At higher pressures PCS-A10 has lower thermal resistance than Grafoil.

Influence of interface pressure

- Interface pressure applied was less than 2 psi
- Under these low pressures, the data also indicates better performance by Grafoil

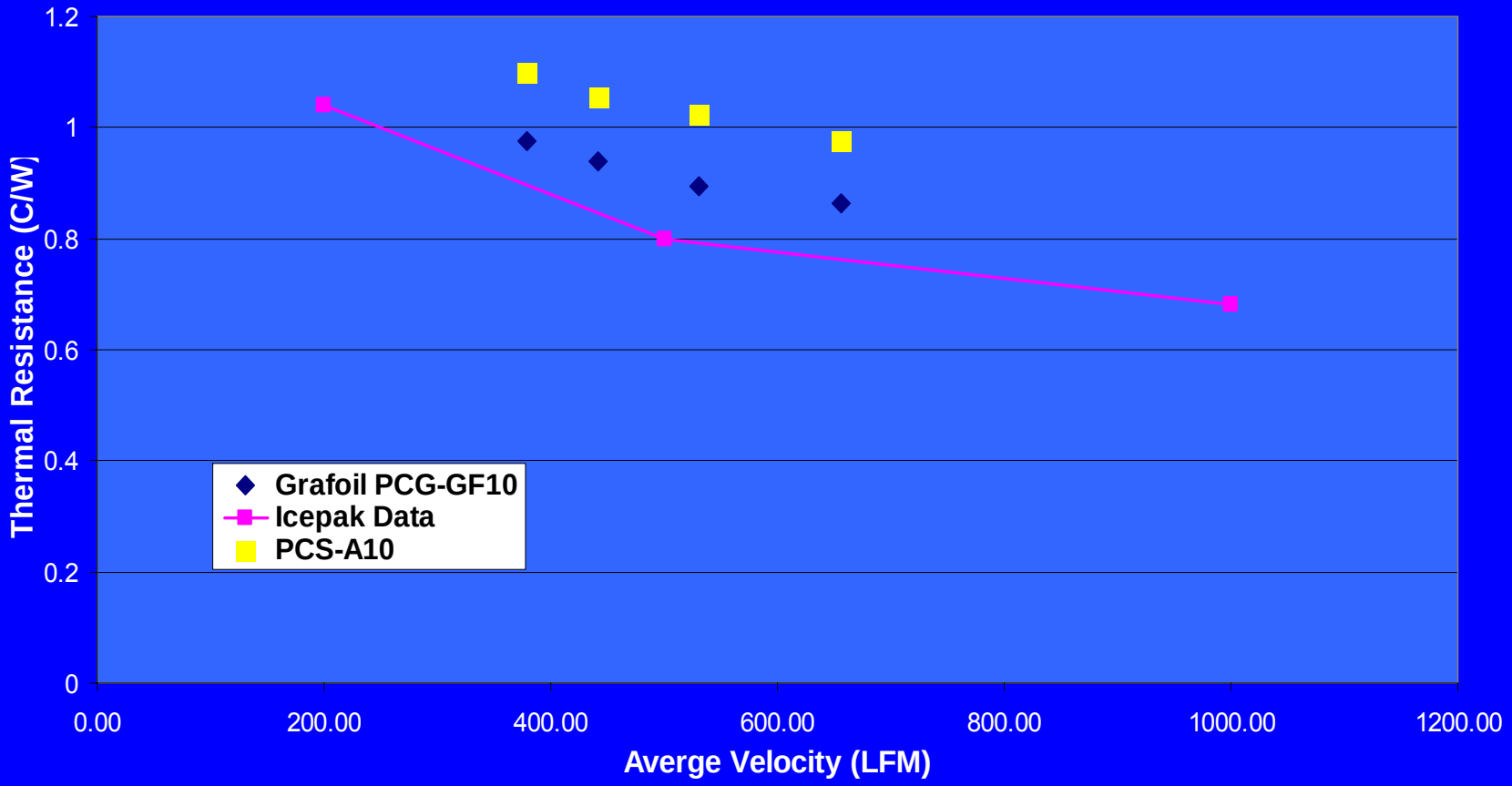
Optimization of heat sink

- More optimal performance with lower pressure drop can be achieved with a larger spacing
  - Doubling the spacing will reduce pressure drop by a factor four (theoretically)
  - However, the thermal resistance will increase (less number of fins and surface area)
  - Tight spacing also has risk of dust accumulation

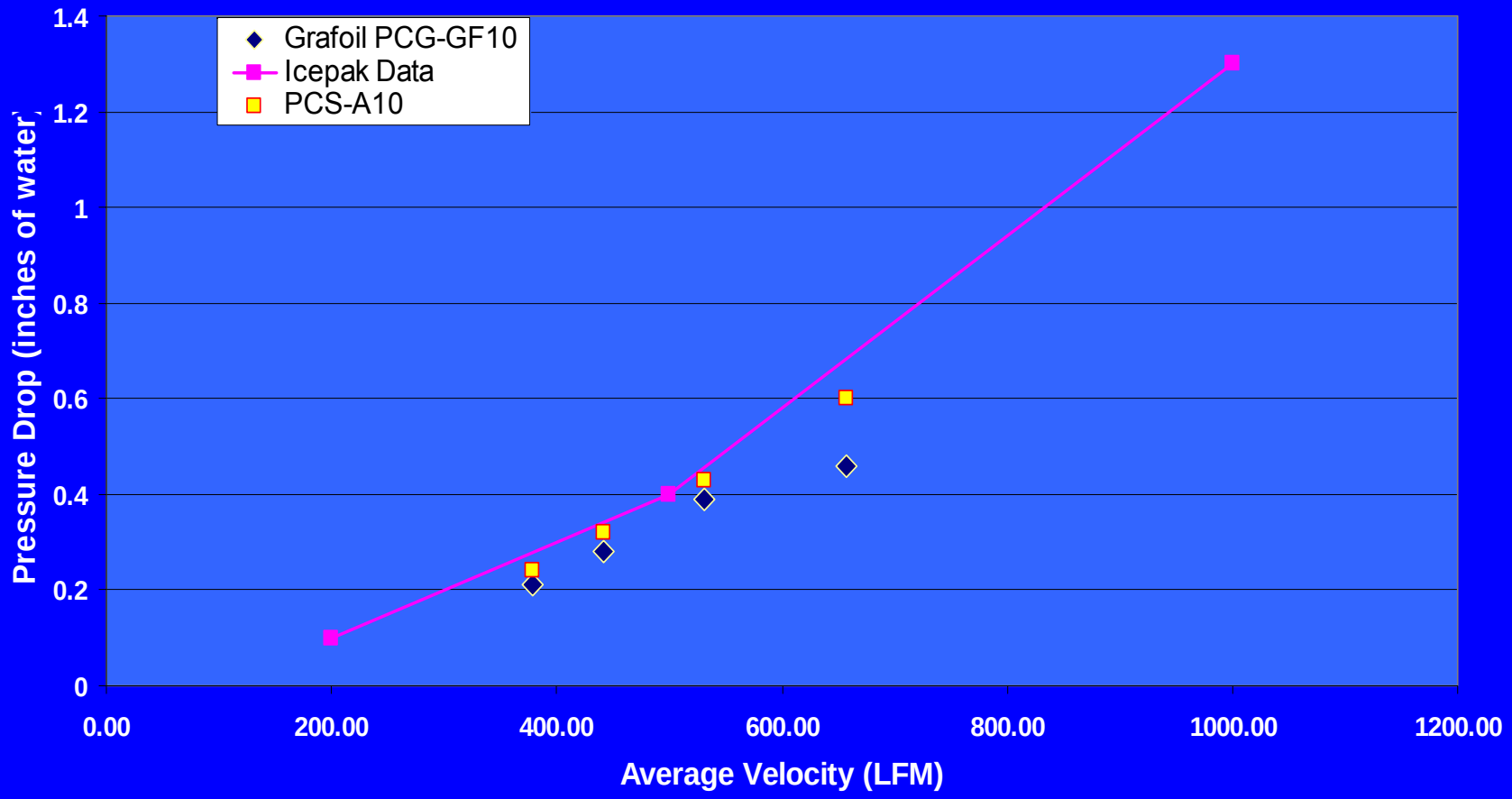
Thermal Performance vs. airflow [1-mm spacing]

Airflow	Pressure Drop (inches of water)	Θ_{ca}
200 fpm	0.1	1.14 ◦C/W
500 fpm	0.4	0.9 ◦C/W
1000 fpm	1.3	0.8 ◦C/W

Experimental Data [1-mm Gap]



Pressure Drop



Conclusions

- A high efficiency passive heat sink for 5-20W applications has been developed.
- Thermal resistance ranges from 1 to 0.7 ^{0}C/W based on airflow from 200 to 1000 fpm.
- Experimental data compares within 10 to 15% of analytical predictions.
- To reduce the pressure drop, the fin spacing was optimized to be between 1.0 and 1.5mm.
- To reduce thermal resistance even further, a taller heat sink (2U) can be used with larger spacing.
- It was found that the Grafoil based interface material performs much better than aluminum foil.

Future Study

- Improve performance by higher interface pressures
- Optimization of heat sinks based on fan characteristics of ovens
- A system-level study is needed to design a more optimal heat sink that has a high performance [Thermal resistance/Pressure drop]
- It is likely that we can have different heat sink choices (fin spacing) based on airflow supported by the oven and power (die) dissipation