Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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Burn-in & Test Socket Workshop

Technical Program

Session 6
Tuesday 3/08/05 1:00PM

TEST AND BURN-IN OPERATIONS

"The Trouble With Carriers"

Jay Stutzman – Micron Systems Integration **Dan Cram** – Micron Systems Integration

"Innovations For Reducing Burn-In Costs For Known Good Die"

Steve Steps – AEHR Test Systems

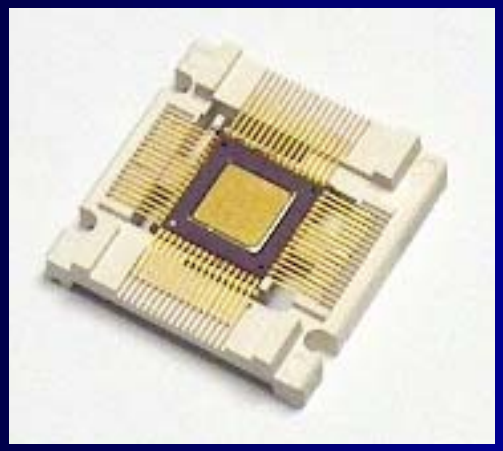
"Burn-In Acceleration By Better Temperature And Voltage Control"

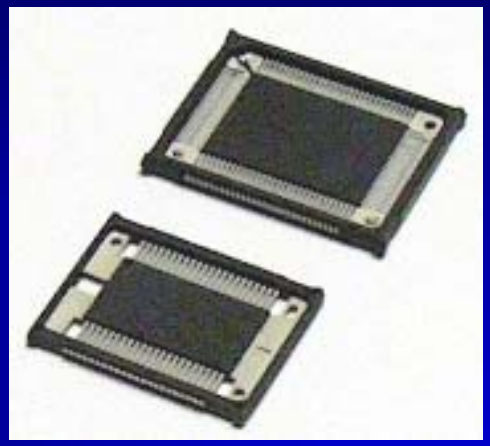
Larry Friedrich – Unisys Corporation **Jim Babcock** – Unisys Corporation

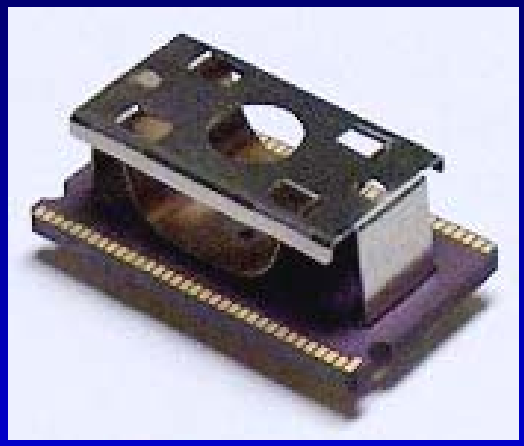
"Approaches And Methodologies For High Resolution Burn-In And Test Data Management"

Tamás Kerekes – NplusT Semiconductor Application Center

The Trouble With Carriers







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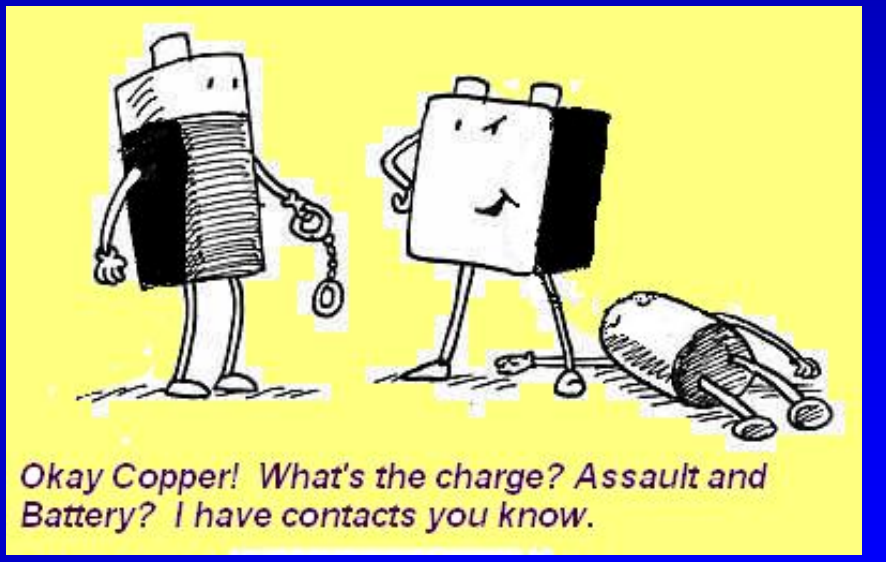
BiTS™
Burn-in & Test
Socket Workshop

Jay Stutzman
Dan Cram

Micron
Systems
Integration

Agenda:

- Carrier history
- Typical reasons for implementing carrierized solutions
- Various carrier types
- Conclusions / Summary



Carrier History:

- For decades integrated circuit device carriers have been utilized in backend test flows for a variety of reasons, though most often for device protection and/or to facilitate device handling

Carrier History:

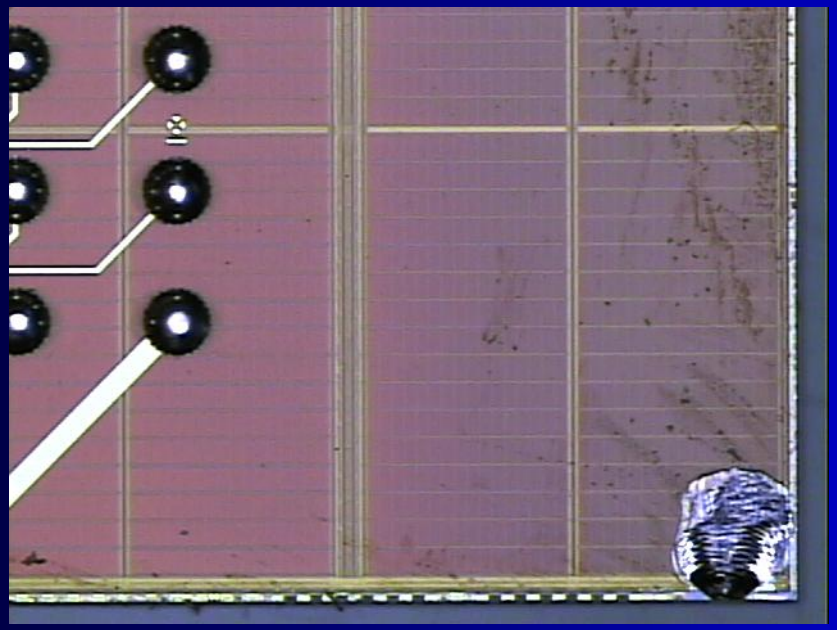
- Carriers have been used or proposed to facilitate processing of a variety of IC devices, including:
  - Periphery leaded devices (TSOP, QFP, etc…)
  - Area array devices (BGA, PGA, CSP, etc…)
  - KGD and others
- The use of these carriers has generally represented
  - Additional cost (carrier component, tooling NRE, etc…)
  - Additional processing steps (loading/unloading, inspection, testing)

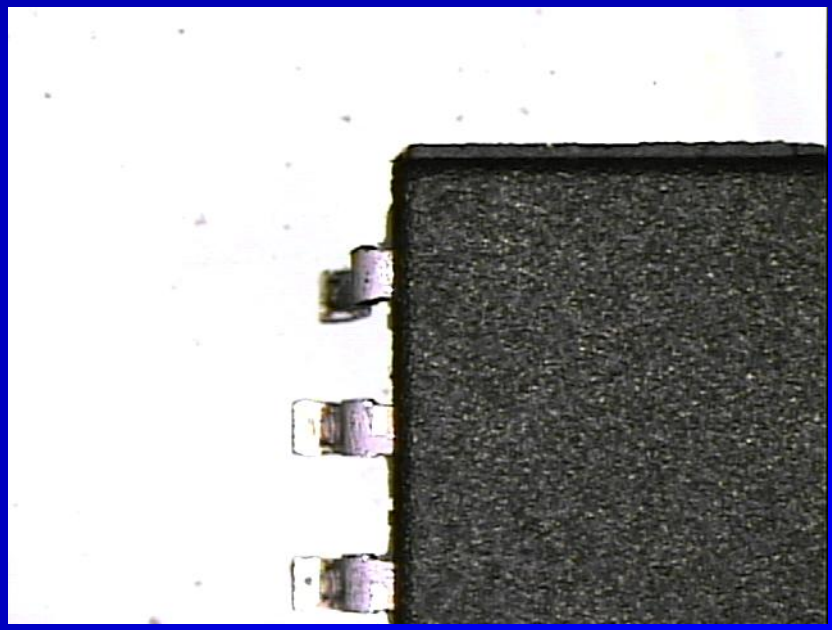
Carrier History:

- In some cases cost models have/continue to support carrier use
- In other cases, more cost effective solutions have circumvented the need for a carrierized approach
- When viewed in a broader context
  - Wafer level or film frame arrays
- Carriers continue to have relevance today (though not necessarily as traditionally defined)

Typical reasons for use:

1) Provide protection and support for
   - Contacting delicate lead frames
   - Protecting fragile package structures (i.e. bare die flip-chip devices)





Typical reasons for use:

2) Commonality of reference/alignment features to contacting mediums
   - Leveraging common features (lead frames, solder ball, land pad matrix)
   - Allow a single contacting system
     - Interchangeable contacting elements for various pitch/lead-count configurations

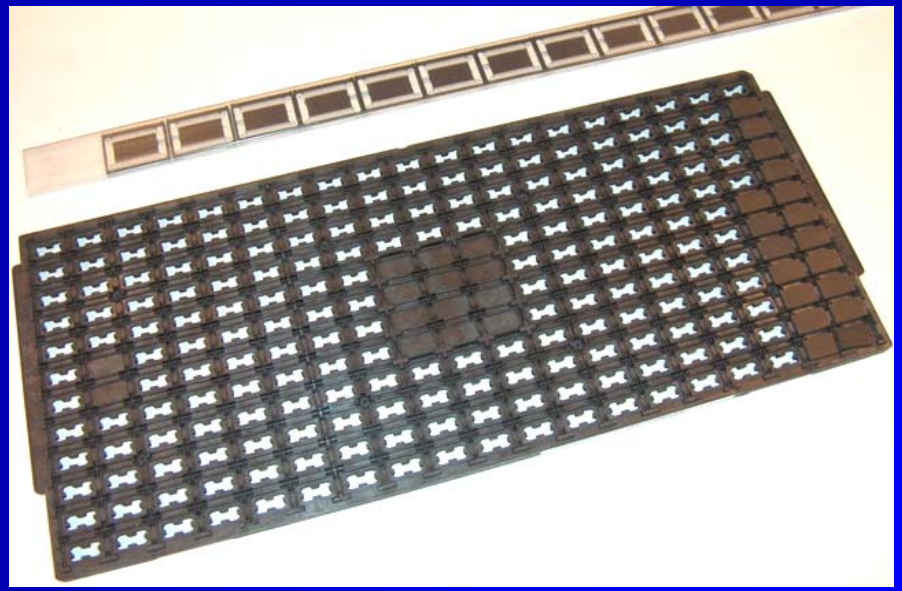
Typical reasons for use:

3) Efficiency

- Some “carrier” approaches gang parts together
- Improve processing efficiencies
- Reduced handling / movement times
- In contrast to singulated device flows

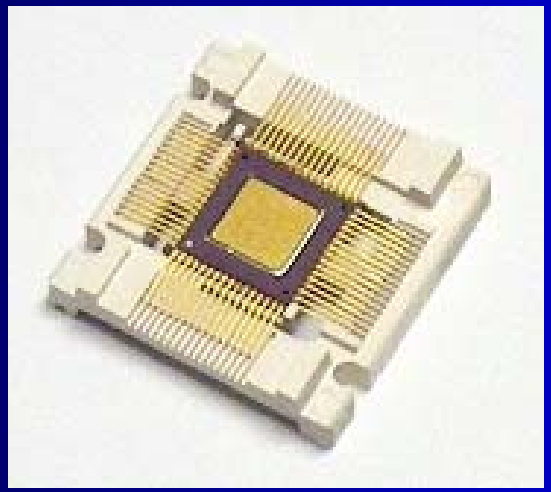
Typical reasons for use:

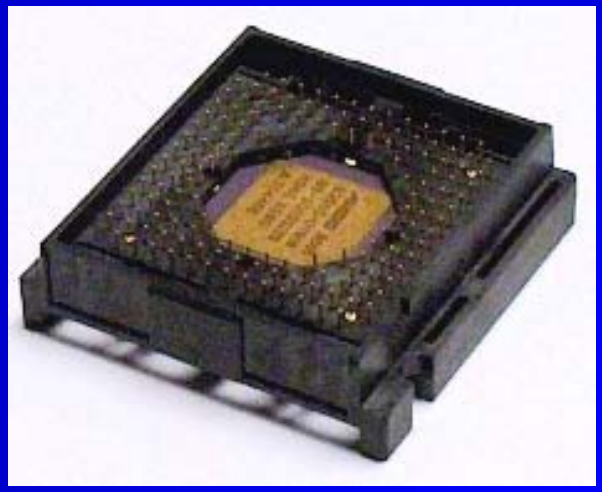
4) Utilization - extend the life of existing handling infrastructures
   - Size commonality afforded by carriers
   - May prolong the useful life of older, lower technology handling / processing infrastructures
   - For example: Tube based/ gravity feed handlers vs. pick-and-place tray based machines



Carrier types:

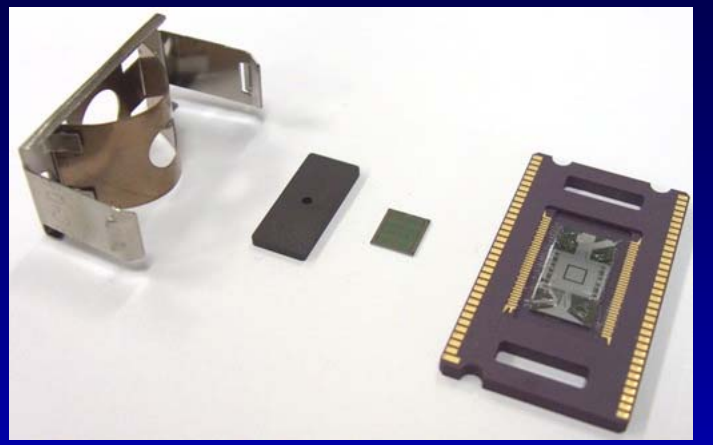
- Individual device carriers
  - Passive
    - individual component or component assembly meant to temporarily carry a single IC device through backend processes
    - primarily for the purposes of protection and to facilitate handling

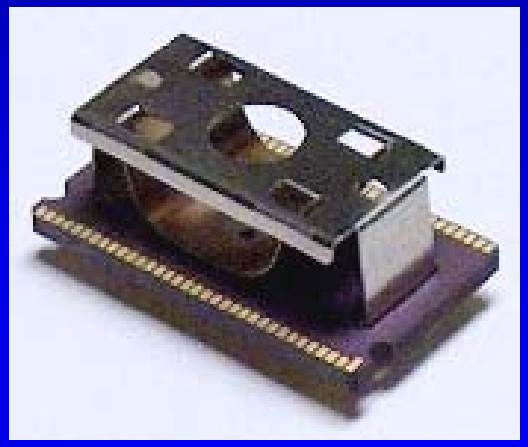




Carrier types:

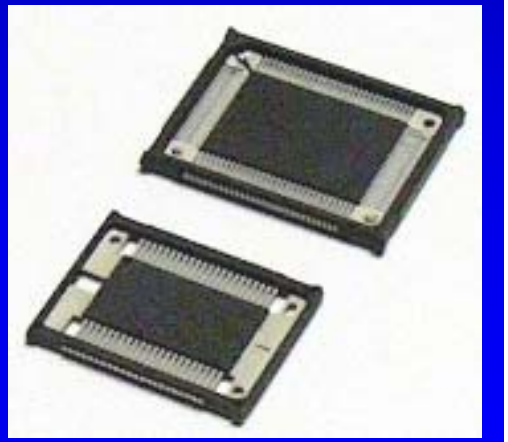
- Individual device carriers
  - Active (KGD carriers)
    - Ext of the passive def.
    - Typically with an integrated force distribution system
    - Interconnect structure to fan out an electrical path from bond pad pitch structures to more conventional socket/contactor pitches (i.e. .5mm, .8mm, 1mm, etc…)





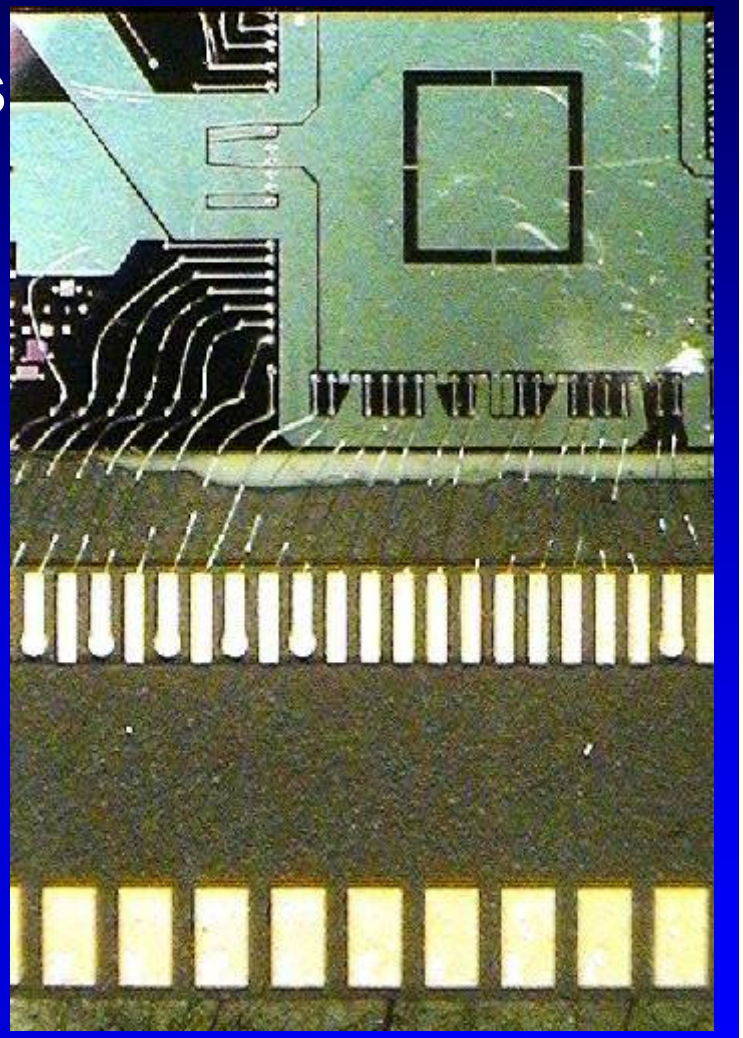
Carrier types:

- Individual device carriers
  - Integrated (i.e. molded carrier rings)
    - Also a further extension of the passive carrier concept
    - Integrated structures rather than a truly separate/reusable component into which the device is installed and subsequently removed
    - fabricated around/on the device during assembly
    - permanently removed and discarded prior to shipping the finished product



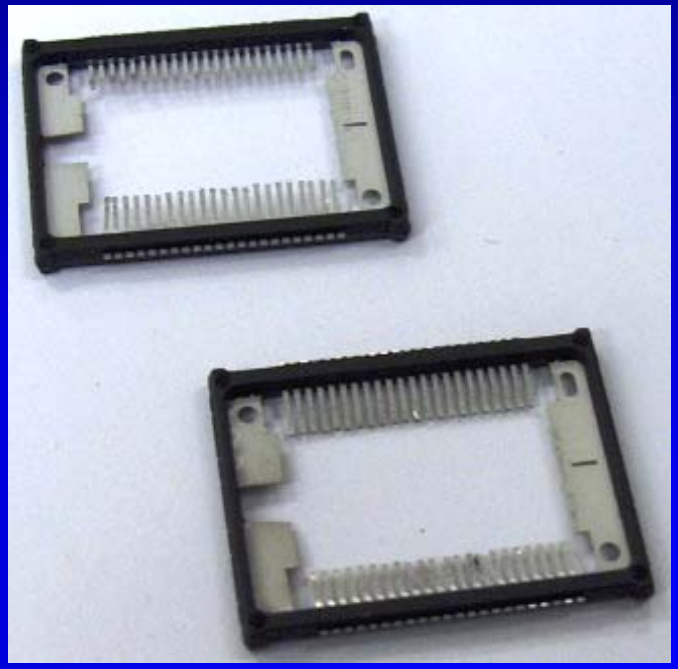
Carrier types:

- Individual device carriers
  - Discussion
    - Simplicity
    - Provide protection
    - Potentially leverage existing handling infrastructures
    - Reusability / non-reusability
    - Active redistribution interconnects (KGD device carriers)



Carrier types:

- Individual device carriers
  - Discussion (cont)
    - Potential NRE for each package outline
    - Additional component that is required for each part processed
    - Ongoing purchases if carrier is disposable (consumables)
    - Scrap costs (molded carrier ring waste)



Carrier types:

$$\frac{\text{CARRIER COST X RUN RATE}}{\text{AVERAGE SELLING PRICE}} \times 10 = \text{EQUIVALENT SCRAP DPM}$$

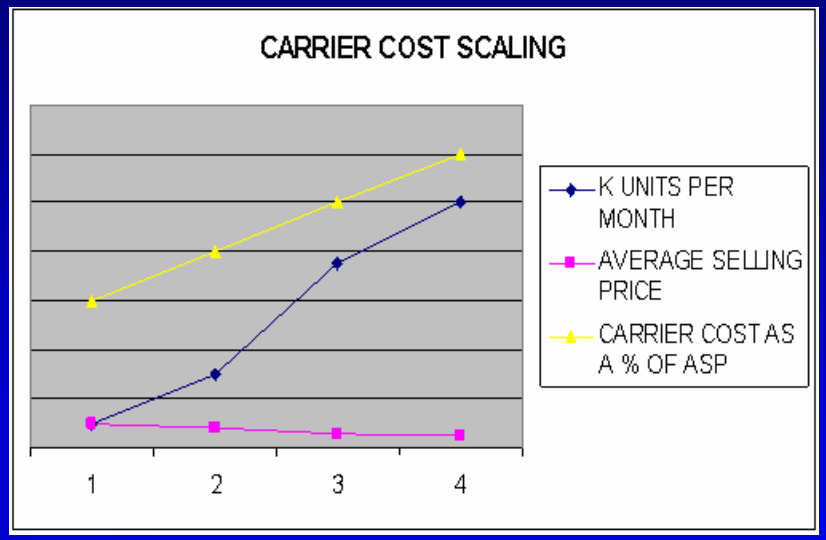
- Individual device carriers
  - Discussion (cont)

<u>Basic</u> cost justification Ex…

Assume cost of carrier =$0.60

Assume 100K in WIP at any given time

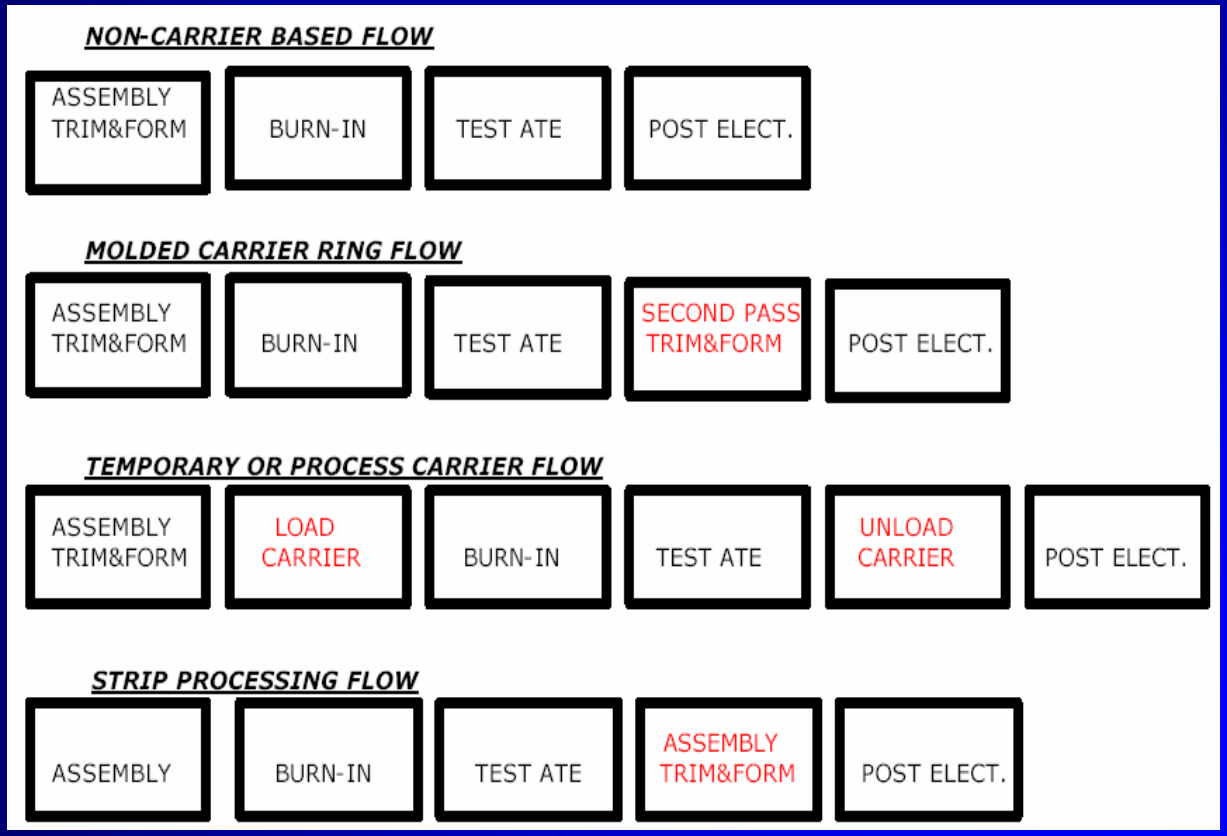
Assume ASP = $5



- This example suggests that a non-carrier process could support a scrap DPM of 120K and still break even
- Or to restate… the equivalent scrap DPM is the scrap that could be generated if a carrier was not used at all

Carrier types:

- Individual device carriers
  - Discussion (cont)
    - Additional process steps, capital equipment



Carrier types:

- Individual device carriers
  - Discussion (cont)
    - BIB densities / MCR TSOP RING2
      8X16 (128 SITES) ➡ 16X16 (256 SITES)
    - BIB densities / MCR QFP RING4
      8X8 (64 SITES) ➡ 12X12 (144 SITES)

Carrier types:

- **Multiple device carriers**
  - **parts are oriented or keyed and presented to a testing contacting medium in unison**
  - **Examples (JEDEC trays or any rigid array based structures**

Carrier types:

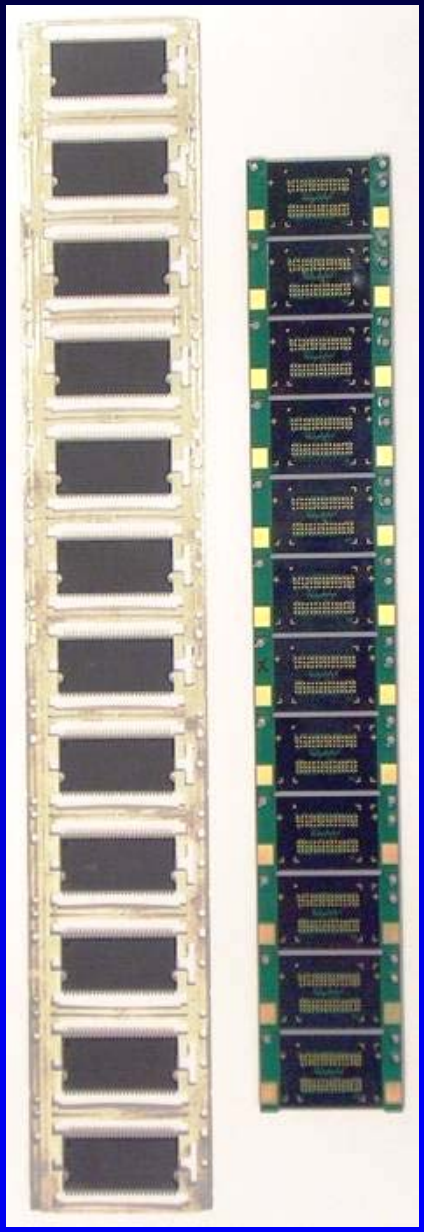
- Multiple device carriers
  - Discussion
    - Standardized tray outline
    - Already utilized in many back-end flows
    - Gangs parts together for mass parallel testing and handling
    - Real time sorting minimized or not possible creating inefficiencies in multi-step test processes

Carrier types:

- Multiple device carriers
  - Discussion (cont)
    - Test fixture sites must be maintained/repaired real-time to avoid unnecessary yield loss
    - Offline sorting of devices required
    - Additional capital equipment required for handling (high cost)
    - Tray outlines are standardized but still custom to each device outline
    - Accuracy of device presentation to a contacting medium

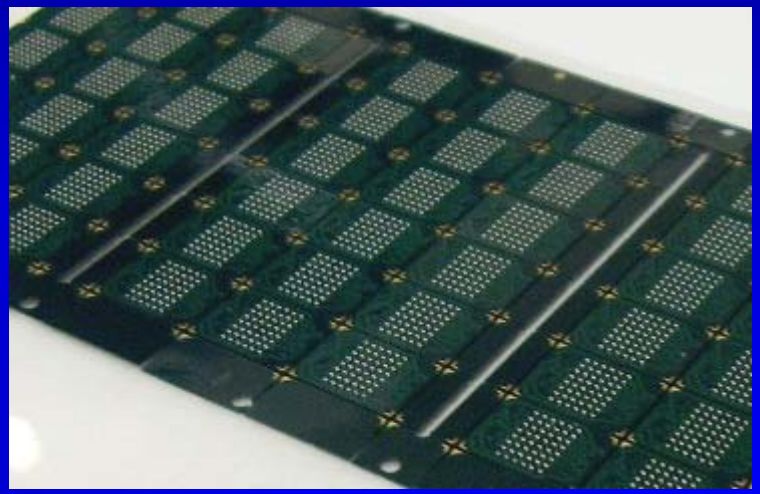
Carrier types:

- Strip / matrix arrays
  - Not a true carrier in the conventional sense
  - Perform some of the same functions as traditional carriers
    - Handled, aligned and possibly contacted on structures that would ultimately be removed or otherwise not part of the final finished singulated part
  - Examples: Alloy 42 lead-frame strips and organic substrate strips for BGA/FBGA



Carrier types:

- Strip / matrix arrays
  - Discussion
    - Facilitates the handling of multiple parts simultaneously through backend processes (efficiency)
    - Affords a certain level of protection to the finished singulated part
    - Alloy 42 lead frames
      - Delicate / easily bent
      - Processing stresses may allow some parts to break away from the lead frame resulting in scrap

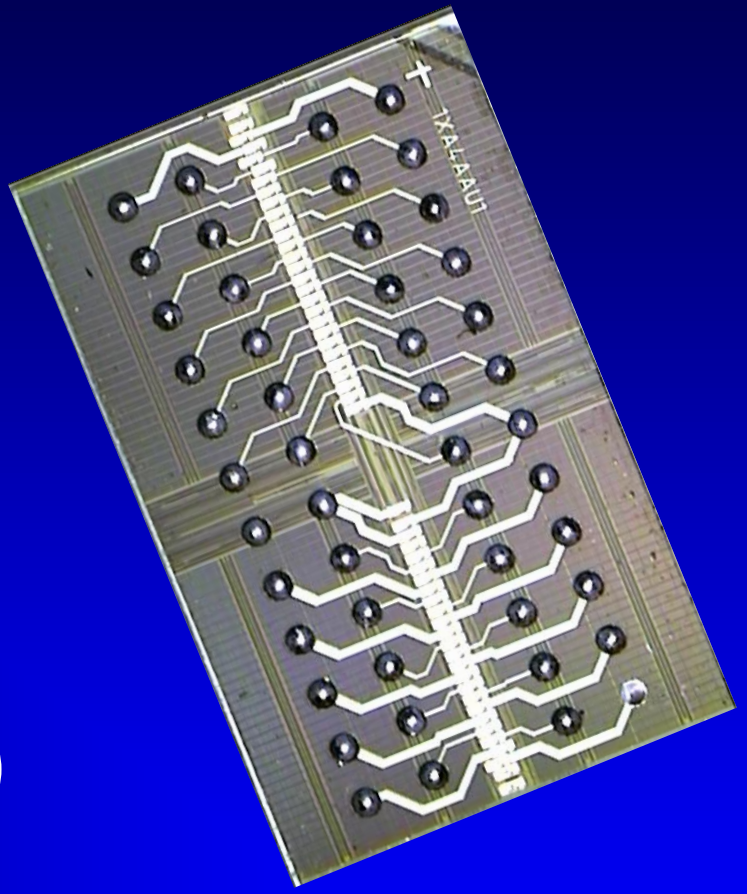


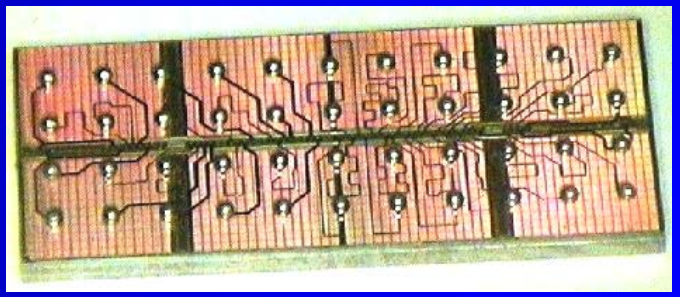
Carrier types:

- Strip / matrix arrays
  - Discussion (cont)
    - Isolating or removing a device during multiple test steps is very difficult resulting in site inefficiencies (unutilized sites)
    - Organic substrates must have each cell location isolated and/or excised first to ensure shared tester resources are not compromised
    - CTE mismatches may bind up strips in test sockets in environments where temperature is changed

So why all the fuss about carriers?

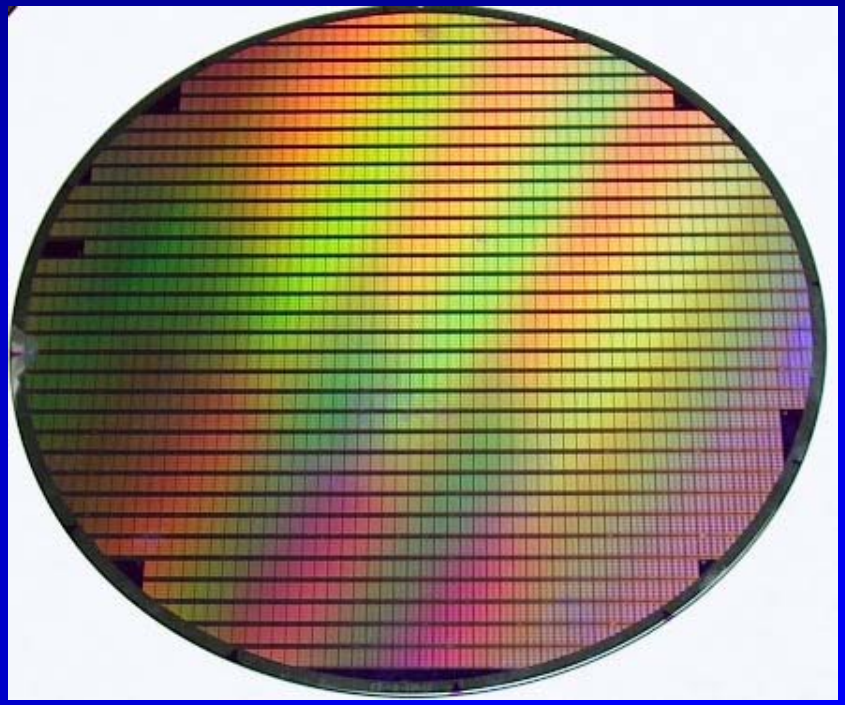
- ***Flip-chip/CSP***
  (bare die with RDL for ball attach)
- **Susceptible to damage… cracking, surface/edge/corner chips, outline standardization (i.e. CSP)**
- **Carriers might be the obvious first choice to facilitate processing through backend test flows, however…**





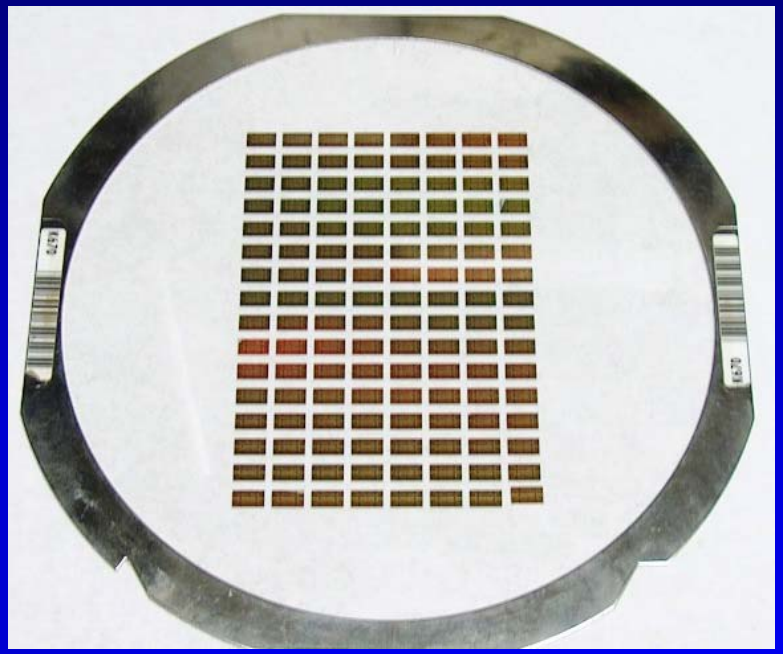
Carrier types:

- **Wafer / film frame arrays**
  - **A silicon wafer upon which IC structures have been fabricated could in its own right be considered a disposable carrier structure of sorts**
  - **Particularly if used in reference to backend wafer level burn-in/test processes**



Carrier types:

- Wafer / film frame arrays
  - The carrier definition can also quite easily and possibly more usefully be extended to include film frame arrays
  - Provide a temporary transport medium for a ganged array of parts
  - Common orientation / presentation to a contacting medium



Patent Pending
(Micron Technology)

Carrier types:

- Wafer / film frame arrays
  - Discussion
    - No cost yet spent on JEDEC trays or other mediums that are not already native to Fabs and front end Assembly
    - Large numbers of parts can be quickly processed with a relatively low number of movements due to the large grouping of devices on a common substrate
    - Wafer level contactors dedicated to a single die design / wafer diameter… die shrinks and revisions require new contactors

Carrier types:

- Wafer / film frame arrays
  - Discussion (cont)
    - Film frame arrays allow die to be redistributed, enabling hi-fix and BIB design to be accomplished with minimal difficulty and allow for pre-sorting out of the open/shorted die (dead soldier removal)
    - Handling infrastructures already exist, although not necessarily in/for backend processes
    - Wafer level test resources tied up on sites with known bad die

Electroglas

Carrier types:

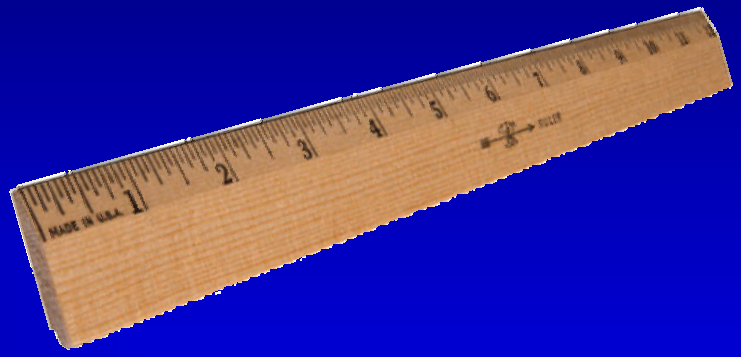
- Wafer / film frame arrays
  - Discussion (cont)
    - Interconnect expense for testing at bond pad pitches
    - Lack or difficulty of interconnect repairability
    - Additional equipment required to implement existing technologies for backend processes (capacity)
    - Film frame arrays – no edge referencing on individual die, protects edges/corners of die
    - Film frame arrays – <u>generic to part outline</u>

Conclusion:

- Certainly carriers have their place and can be justified in some cases or even mandated depending on the application
- Historically however carriers have represented a burden to the process
- Solutions like rebuilt/redistributed film frame arrays may provide better scaling and a more forward thinking approach to processing difficult or fragile products in high volumes

Conclusion:

So what is the trouble with carriers?



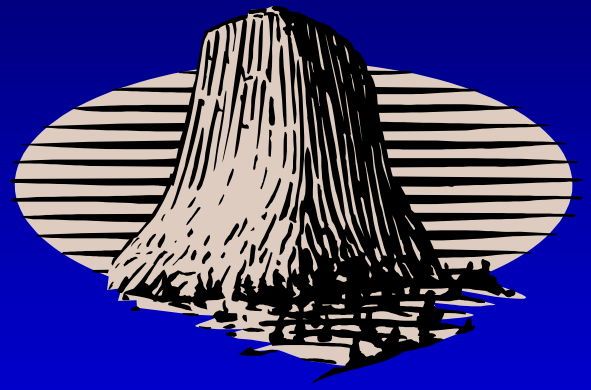
- **Do not scale well!**

- **As soon as a carrierized solutions is designed in, often steps are immediately undertaken to design away from those same solutions!**

CREDITS/ACKNOWLEDGEMENTS:

Thank you for your time!

Questions?



- Special thanks to Scott Hoagland, Dan Cram, Tom Vickery for their critique, feedback, and assistance
- “A Question of Carriers”, Dan Cram, April 2001, Micron internal presentation
- Carrier/contactor samples provided courtesy of WELLS-CTI

Innovations for Reducing Burn-In Costs for Known Good Die

2005 Burn-in and Test Socket Workshop

March 6 - 9, 2005

Steve Steps

Senior Director, Wafer-Level Burn-in and Test

Agenda

- Demand for Known Good Die (KGD)
- KGD Reliability implications
- Alternatives for producing Burned-In KGD
  - Wafer-Level Burn-in and Test (WLBT)
  - Temporary Die carriers
- Innovations for reducing the cost of Burned-In KGD
- Conclusions

Market Demands

- **Cellular telephones, PDAs, portable music, digital cameras, etc.**
  - **Lighter weight**
  - **Smaller size**
  - **Higher capability**
- **<u>Smaller and Lighter Commands a premium price</u>**





Size Versus Price Comparison

140% the price

75% as thick

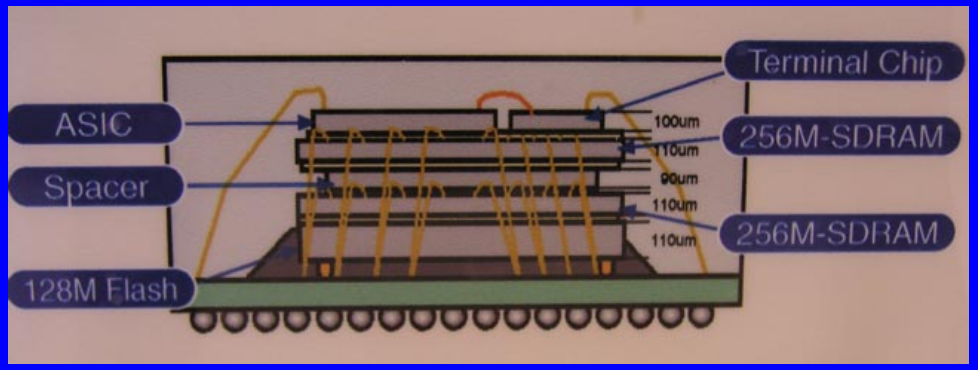
93% as heavy

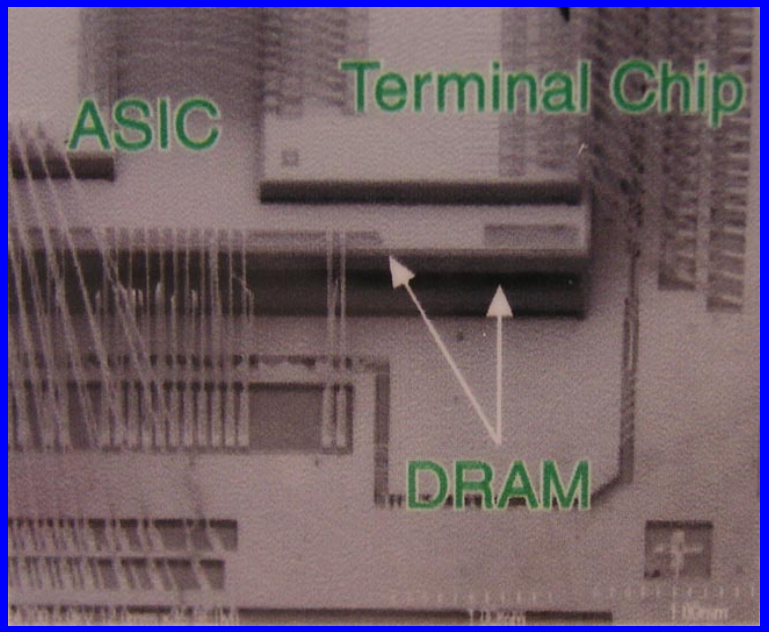
	EX-S100	EX-Z30
	delete	delete
Average Street Price	$349	$249
Camera Type	EXILIM CARD	EXILIM ZOOM
Dimensions	3.46"(W) x 2.24"(H) x .66"(D)	3.46"(W) x 2.24"(H) x 0.91"(D)
Weight	Approximately 4.0 ounces (excluding battery and accessories)	Approximately 4.3 ounces (excluding battery and accessories)

Source: Casio Website

Technology Solution

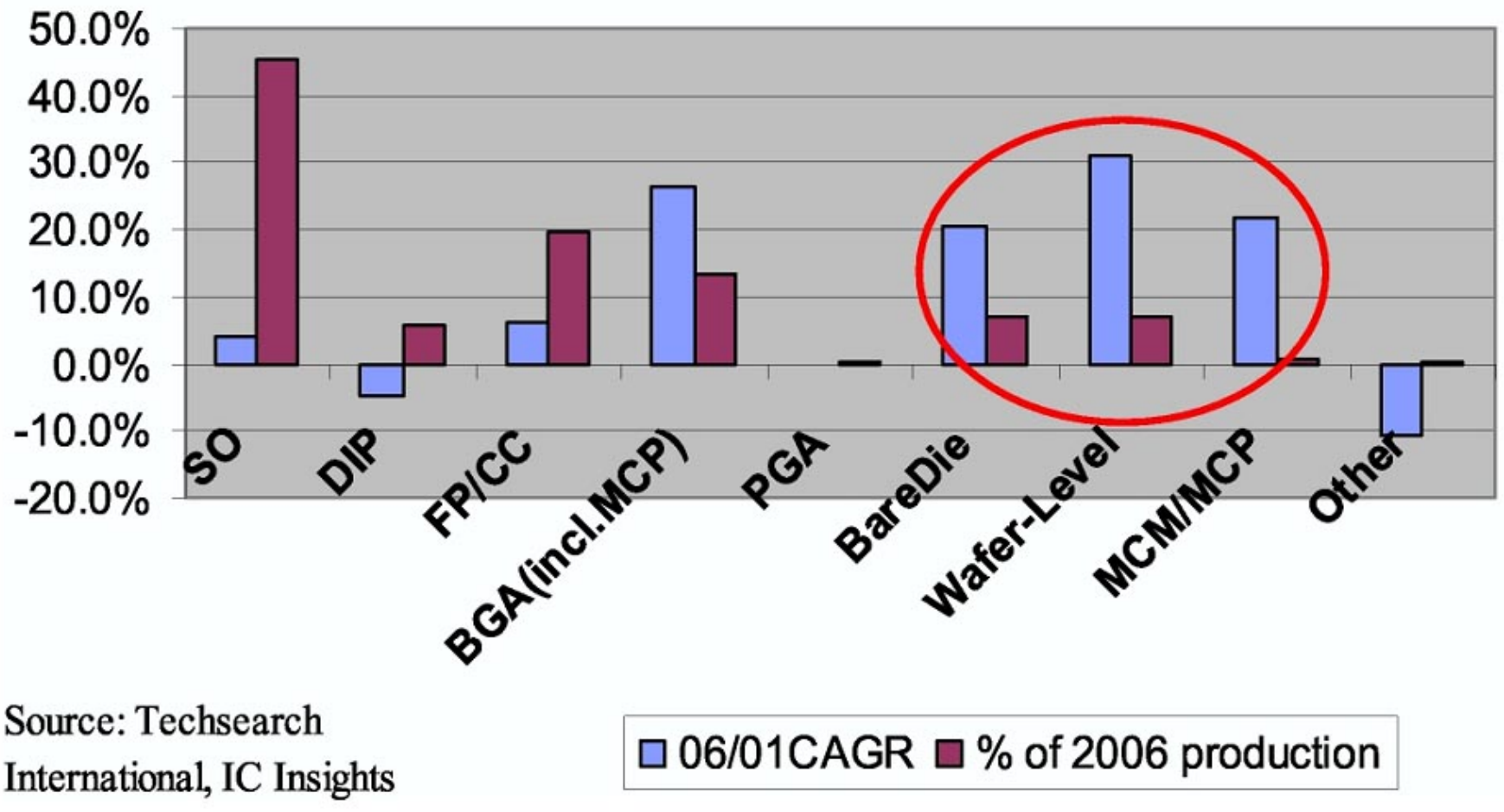
- **Multiple, bare die on a substrate (MCM, SIP, SOP, etc.)**
- **Mixture of wirebond, WLCSP and flip chip connections**
- **Emphasis on “3D” packaging**



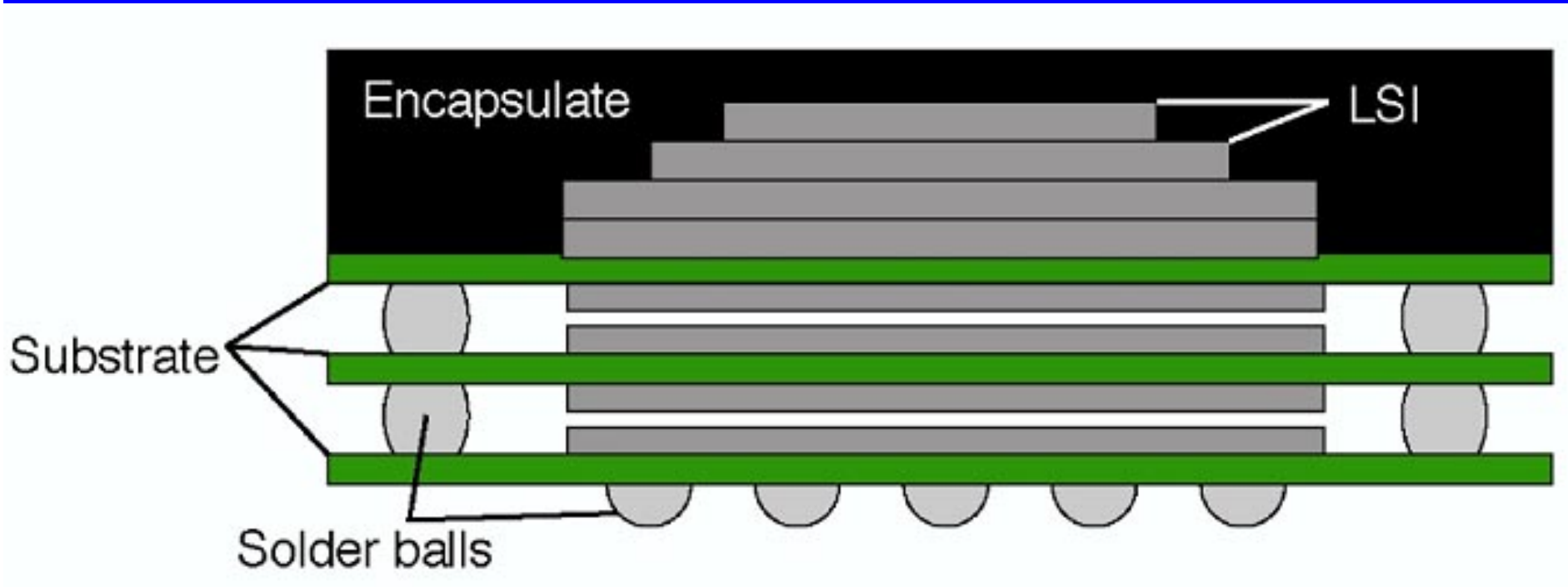


Photos from Renesas Booth at China IC 2004

IC Packaging Units



Fujitsu 8 Stacked SIP

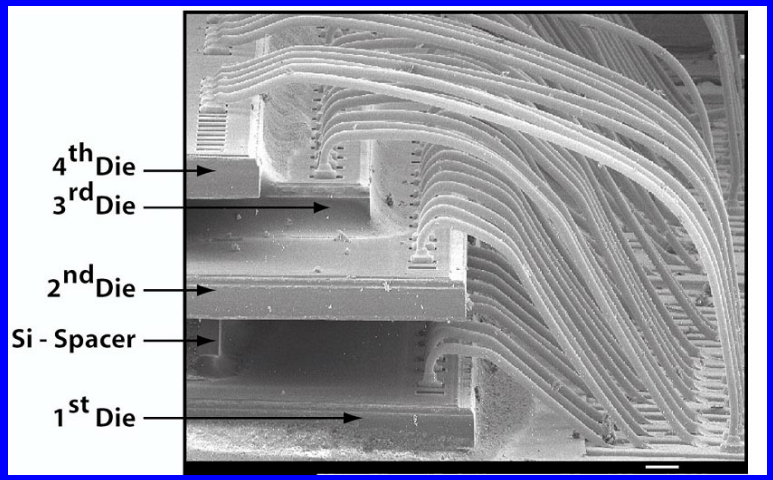


These very complex stacks of die are not repairable.

A failure of any die renders the whole stack useless.

Cost of Failure

- Module failure rate ; (die count)
- Module cost ; (die count)
- Failure cost = (Module failure rate) * (Module cost)
- Failure cost ;(die count)^2



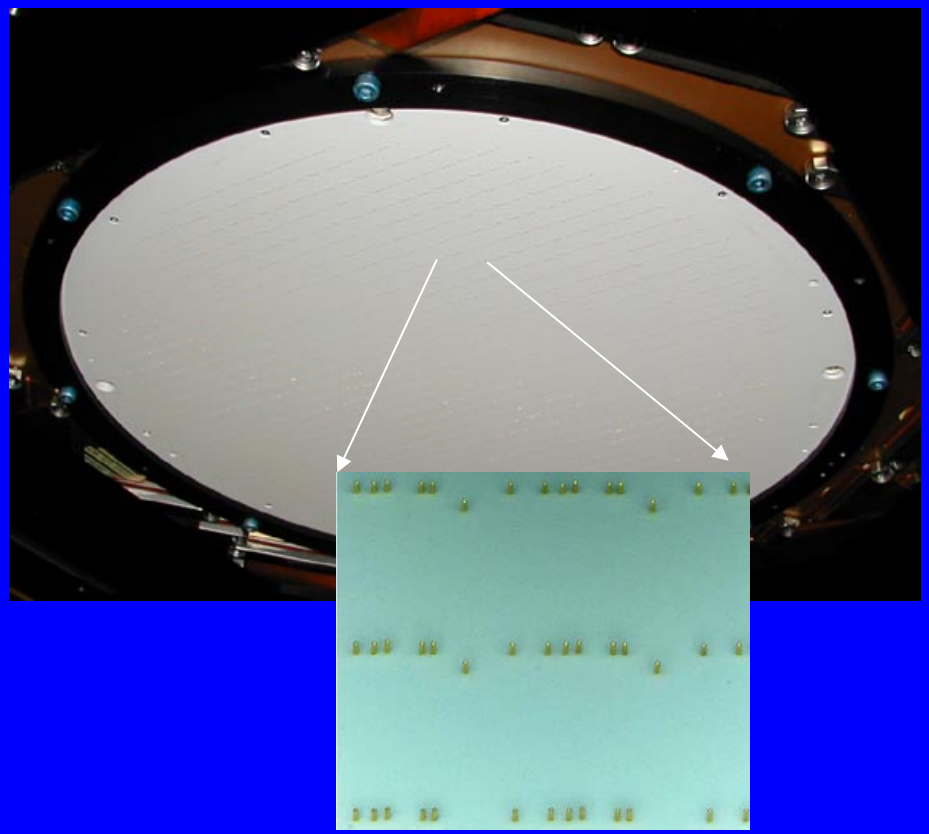
KGD Die Burn-In Alternatives

- **Wafer-Level Burn-in and Test (WLBT)**
- **Bare die temporary package (e.g., "DiePak")**
- **Wafer Probing**

DiePak® is a registered trademark of Aehr Test Systems

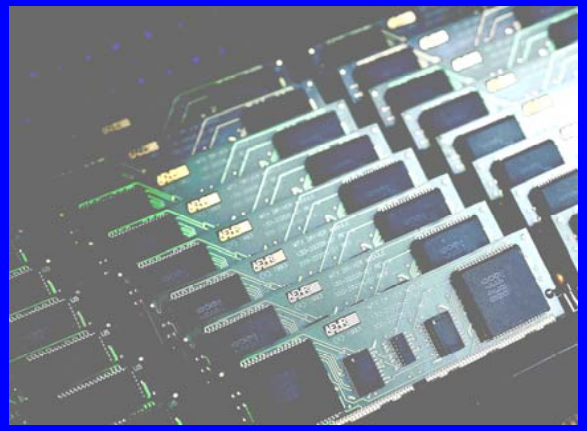
Wafer Level Burn-In and Test (WLBT)

- **Key Attribute: Full Wafer Contact**
- **Simultaneously burn-in and test**
  - **All of the die**
  - **All at once**

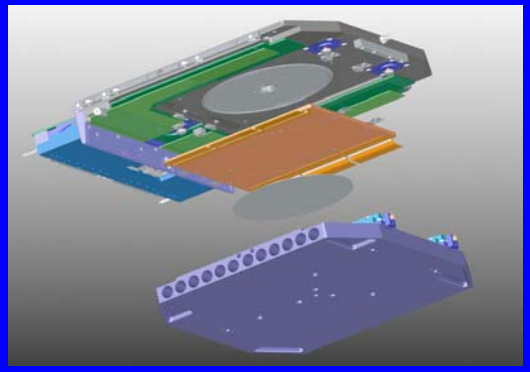


WLBT System Components

Thermal Stress Chamber

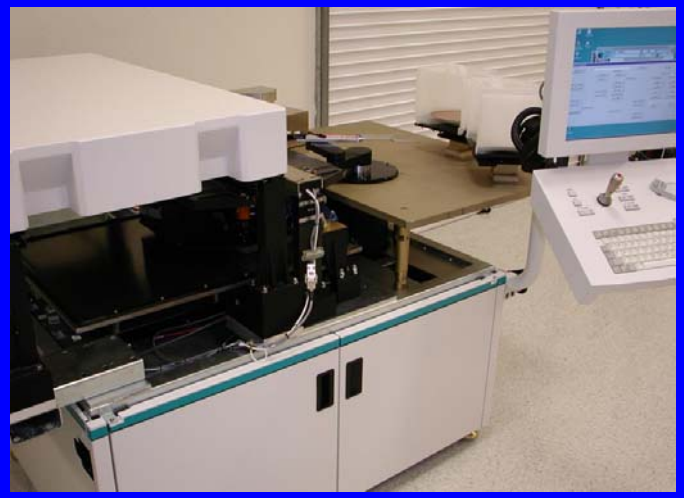


Parallel Test Electronics



Wafer Cartridge

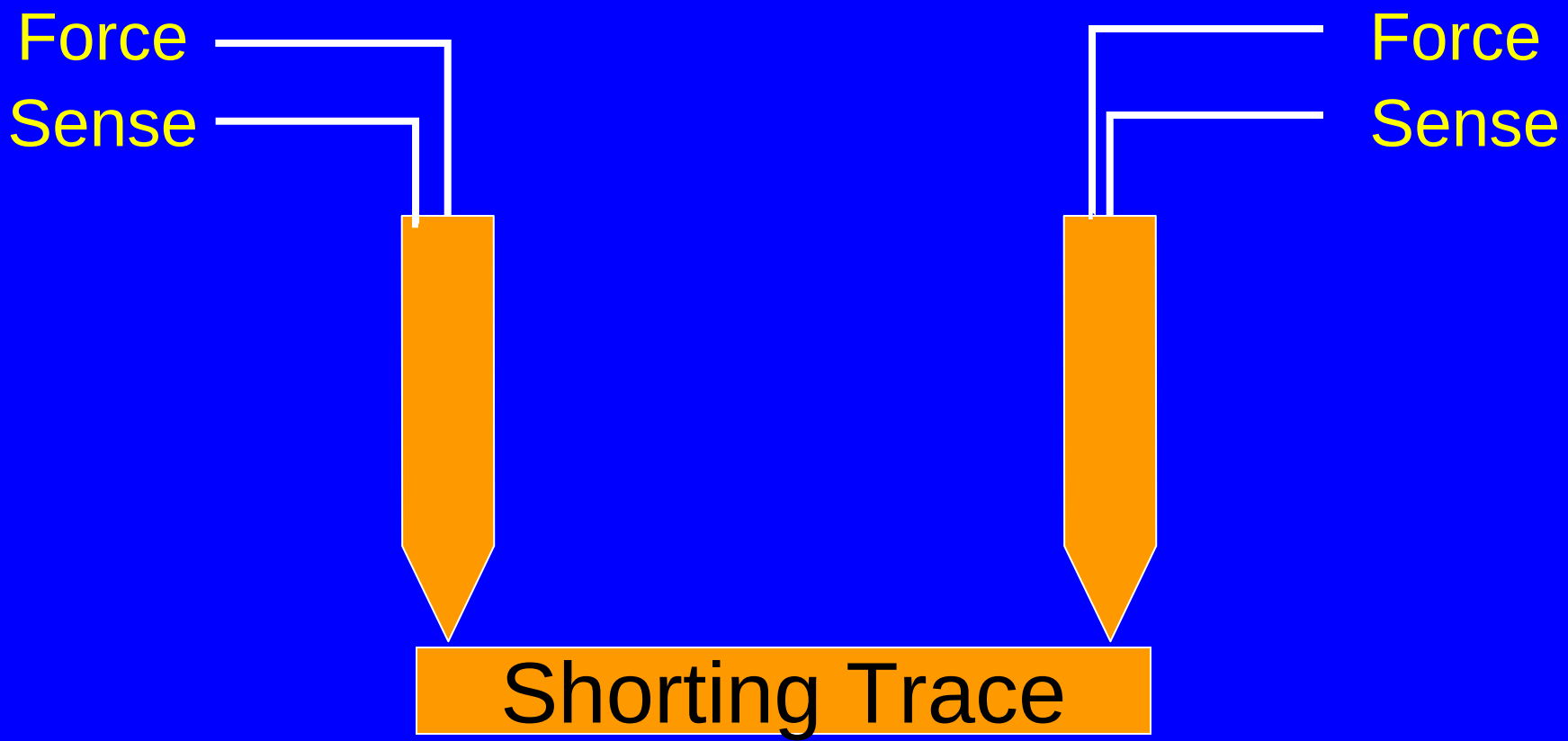
Load Station



Full Wafer Contact Challenges

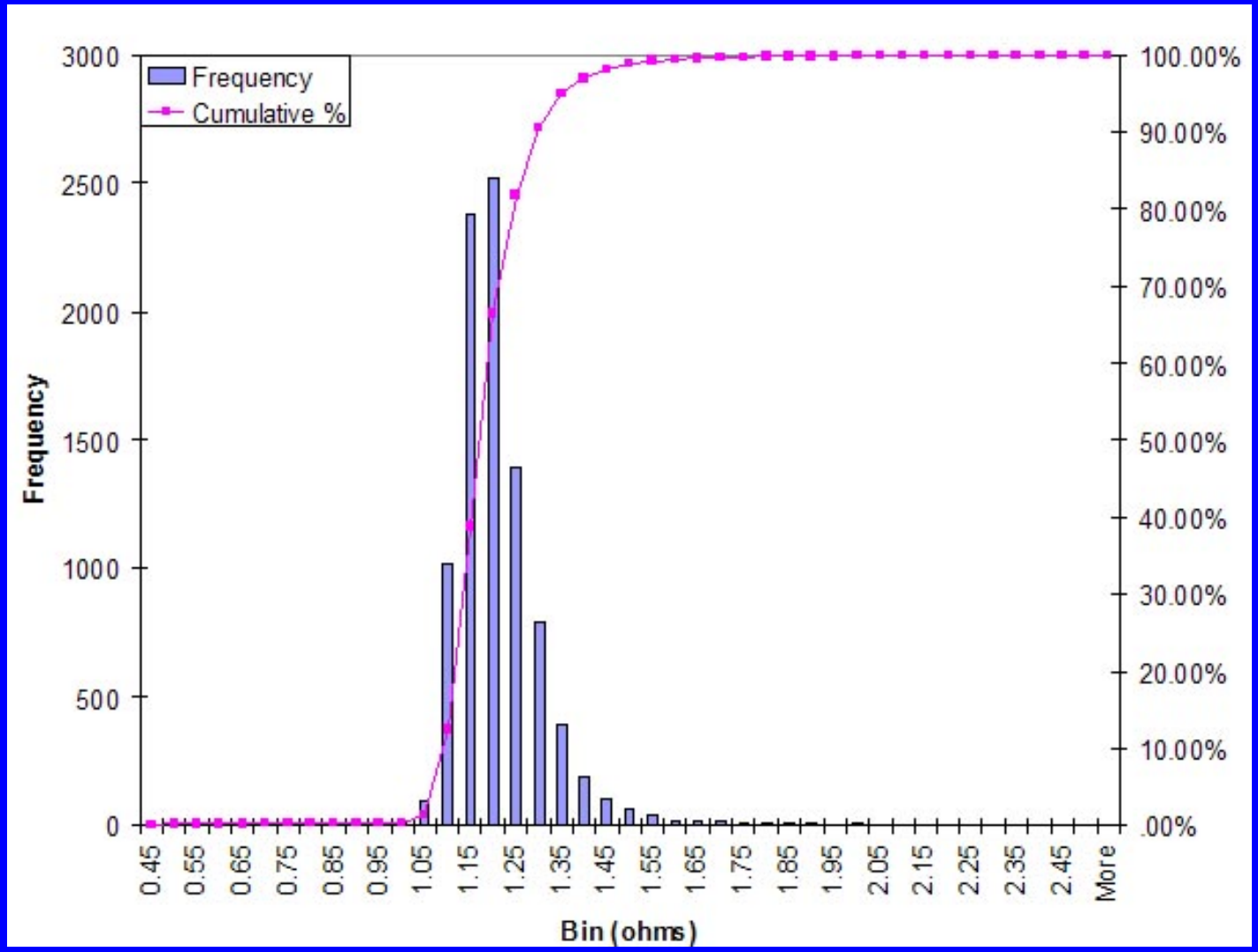
- **Must maintain Co-Planarity to less than 5-100 micron**
- **Very high forces**
  - **700 die per wafer**
  - **60 pads per die**
  - **= 42,000 contacts**
  - **10 gram-force each**
  - **= 420 kg total force**
- **Coefficient of Thermal Expansion mismatch**
  - **For 25 C to 150 C, 300mm: 19 microns/ppm CTE error**

Loop Resistance Diagram

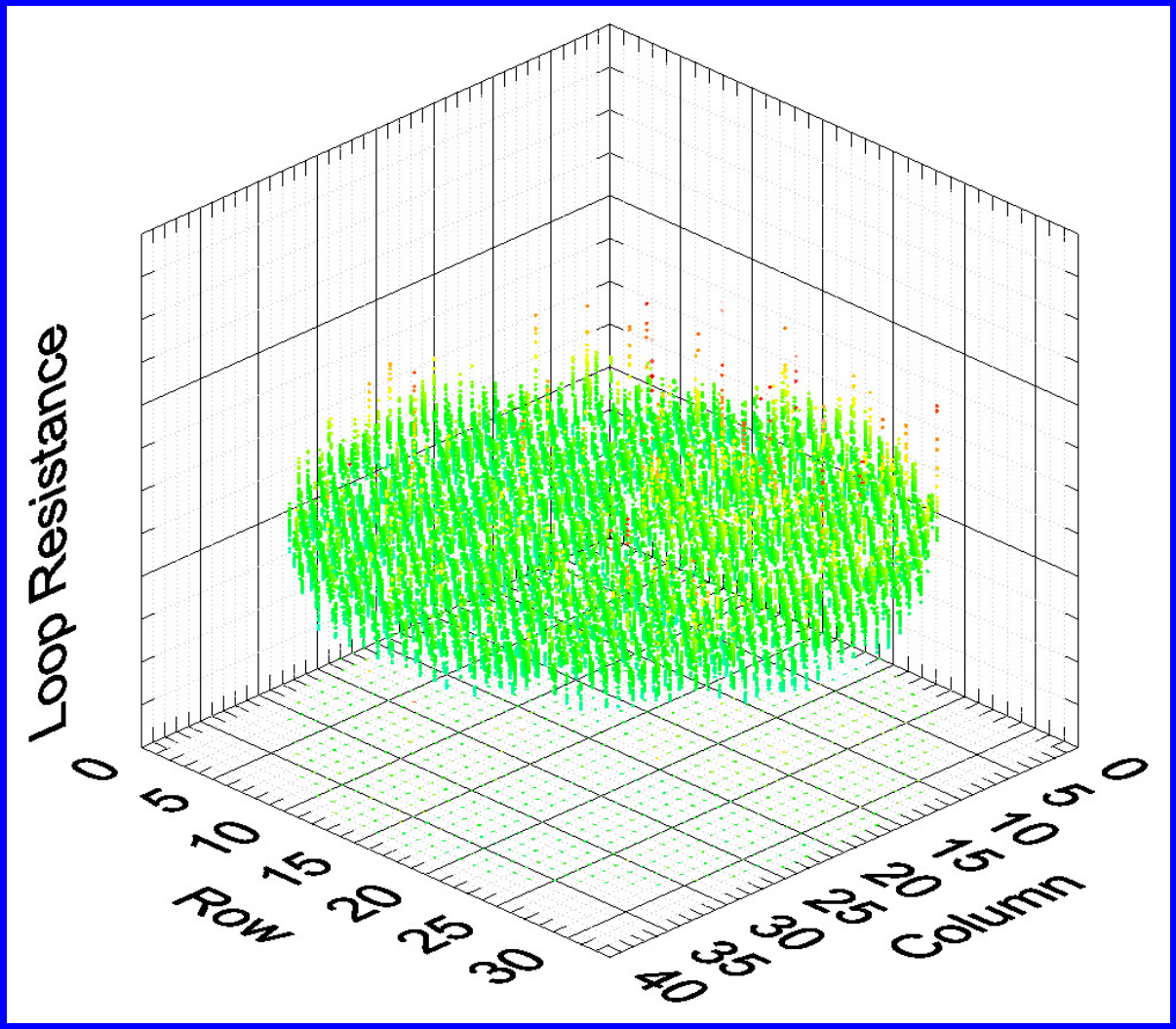


Loop Resistance =
Two contacts plus trace resistance

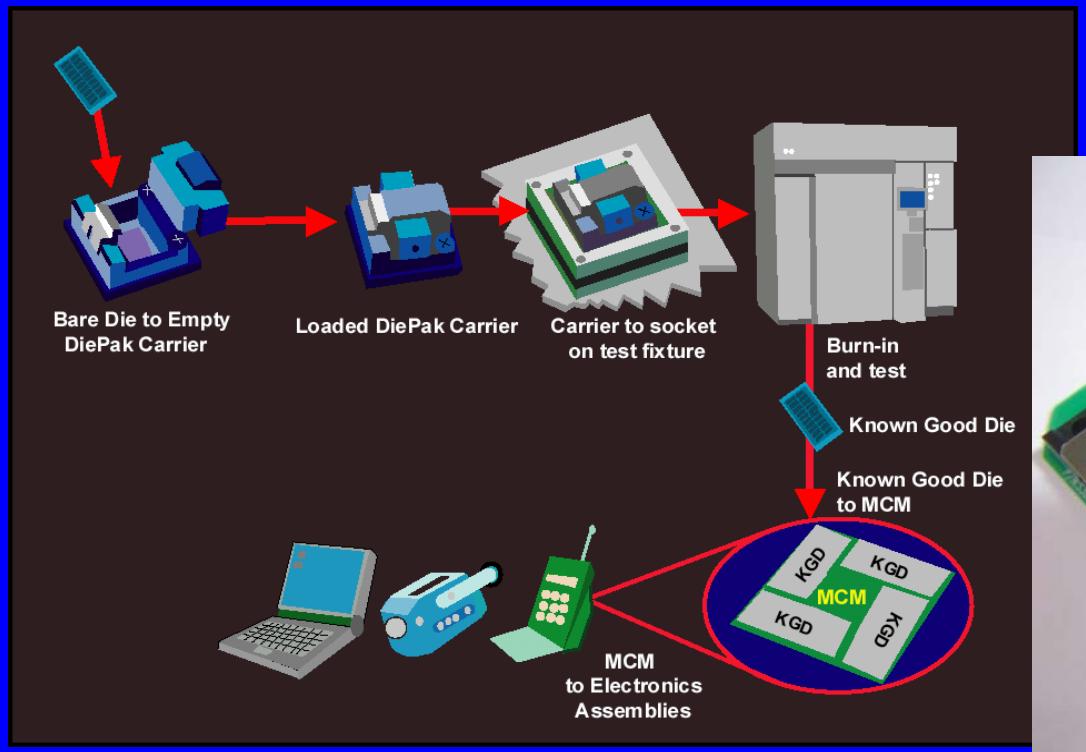
Histogram of Vcc to Gnd pin

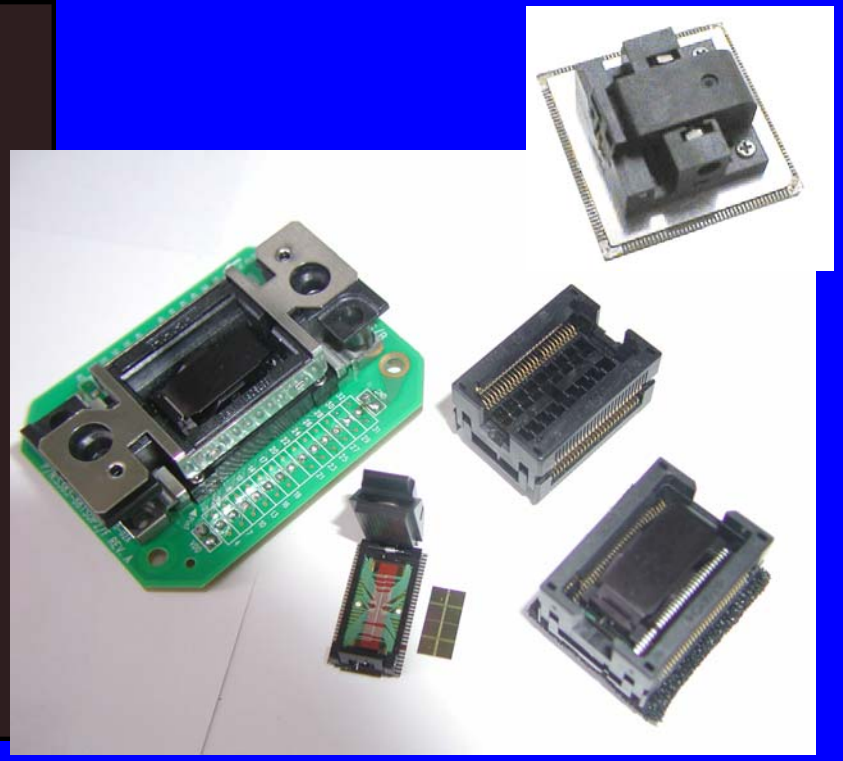


Full Wafer Contact Uniformity



Bare Die Carrier KGD Solution

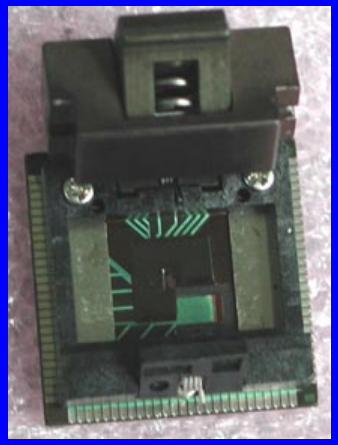




- A family of reusable temporary packages
- Enables burn-in and test of bare die and WLP devices
- For singulated burned-in KGD

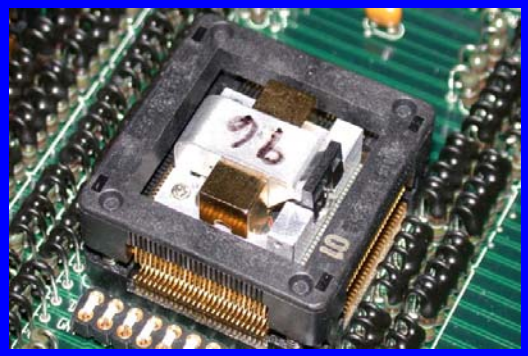
Sandia Labs Application

- **Using for part qualification**
  - **Burn-in**
  - **Test**



Aeroflex Application

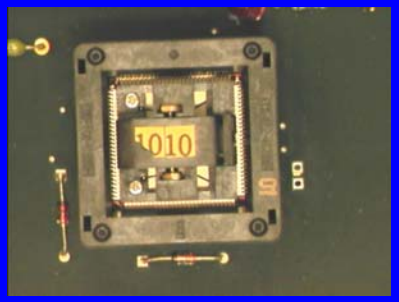
- **Production KGD screening**
- **Memory and Logic parts for high reliability MCM requirements**
- **Temperature range: -55 to +125 C**
- **Die Size: 585 x 585 to 83 x 83 mils**
- **Carriers: 320 pin and 108 pin**
- **Pad pitch: to 90 microns**

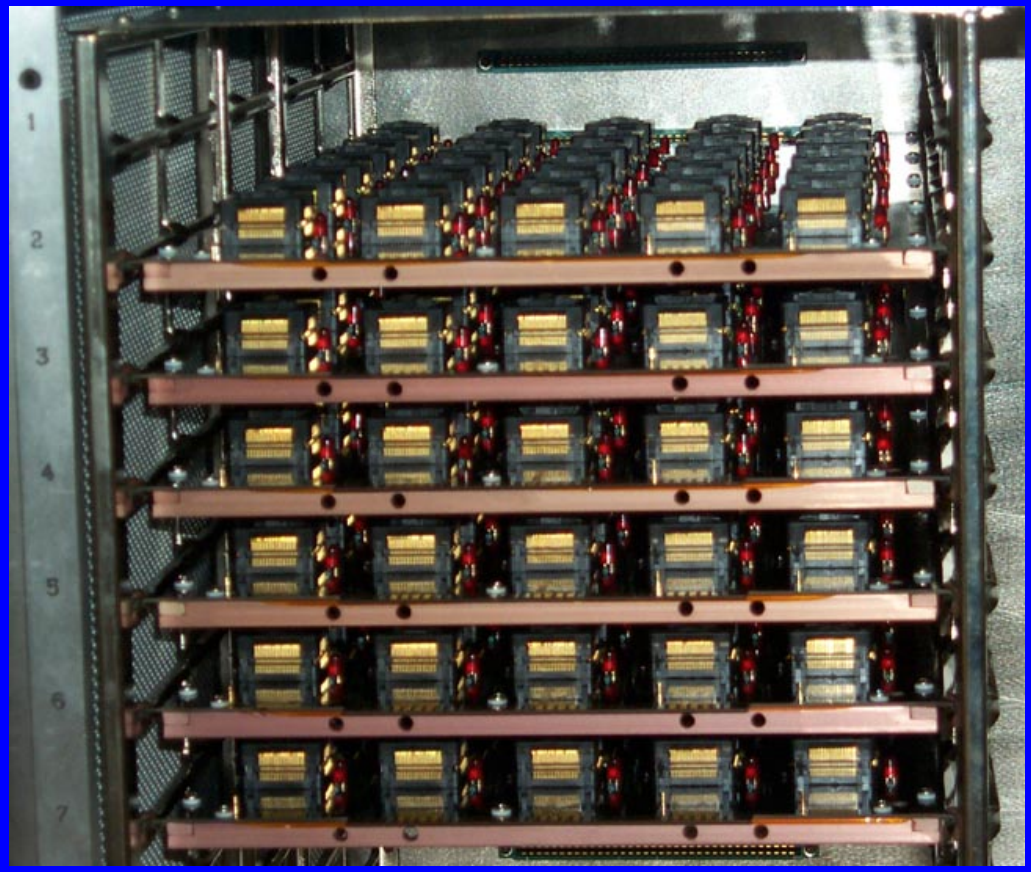


Photos courtesy of Aeroflex

IBM Application

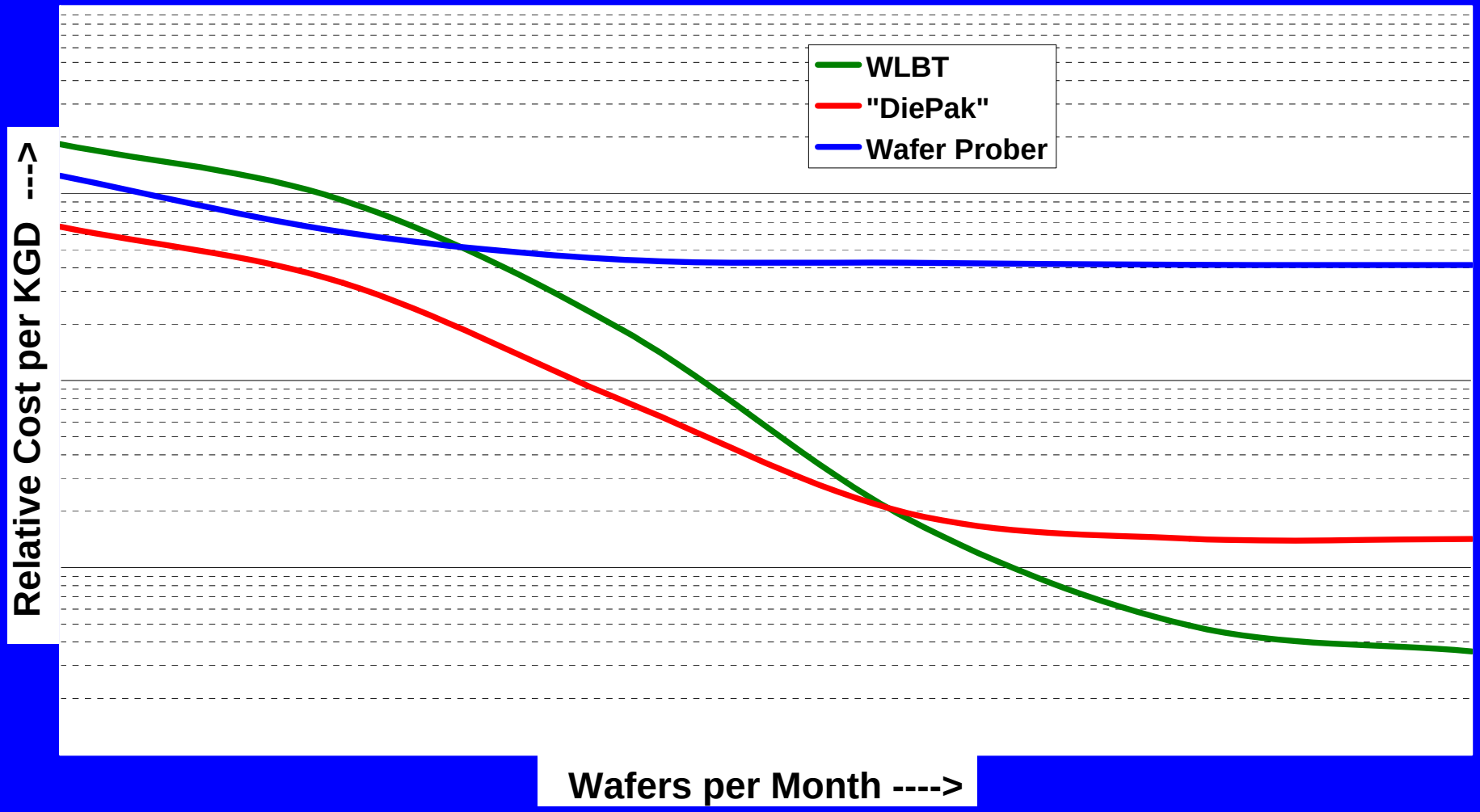
- Doing production Burn-in
- Reliability Screening



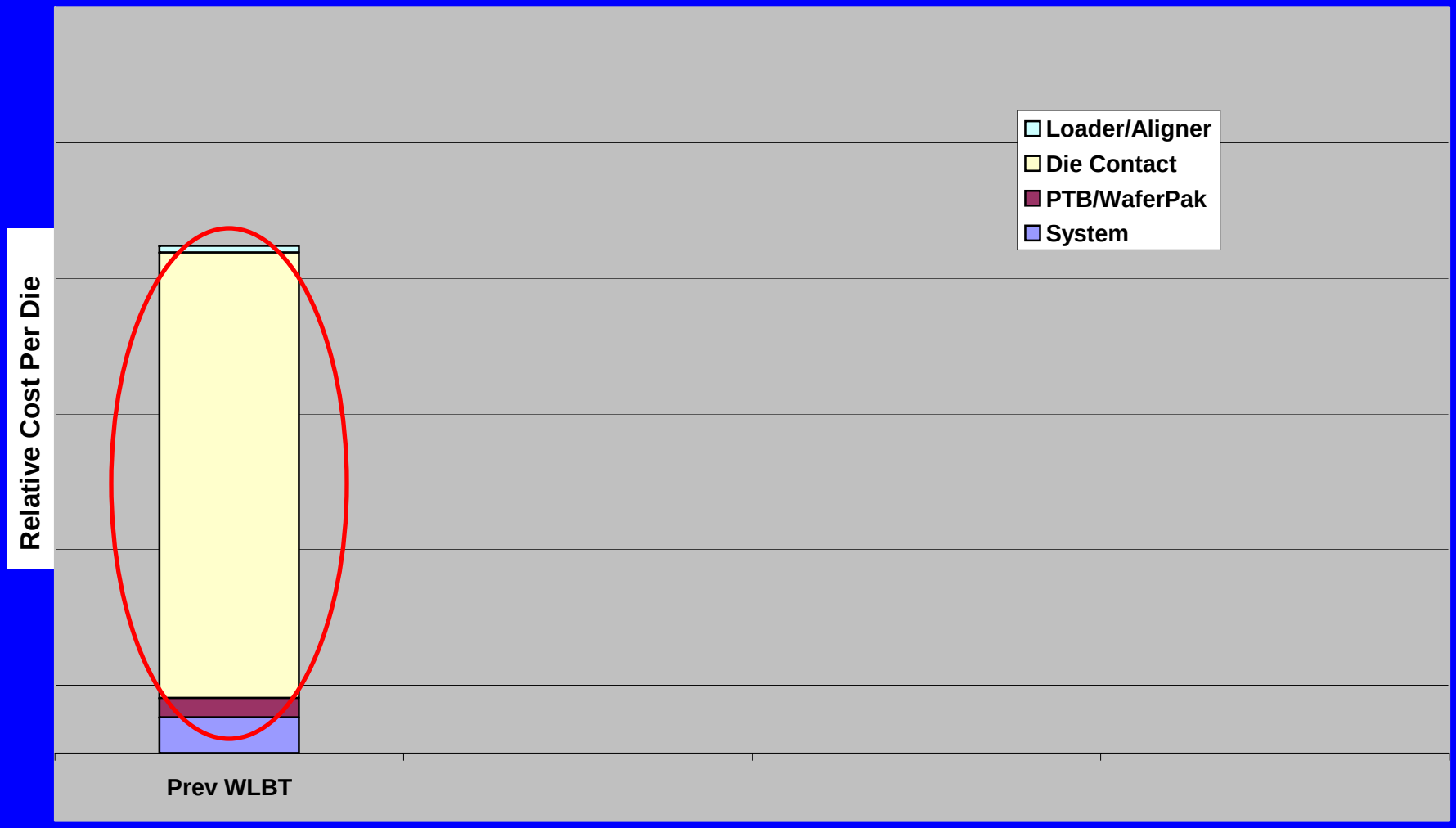


Photos courtesy of IBM

KGD Cost Versus Volume

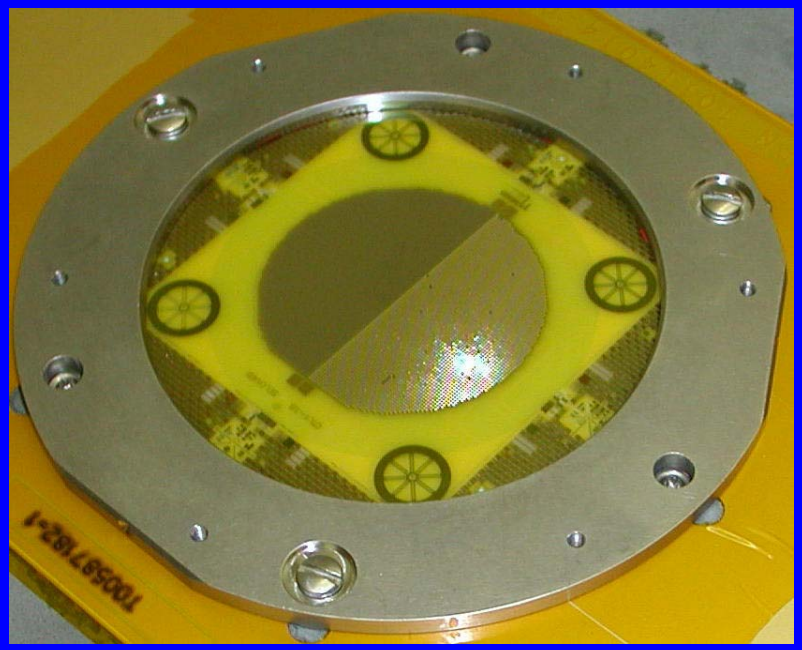


WLBT Cost Drivers

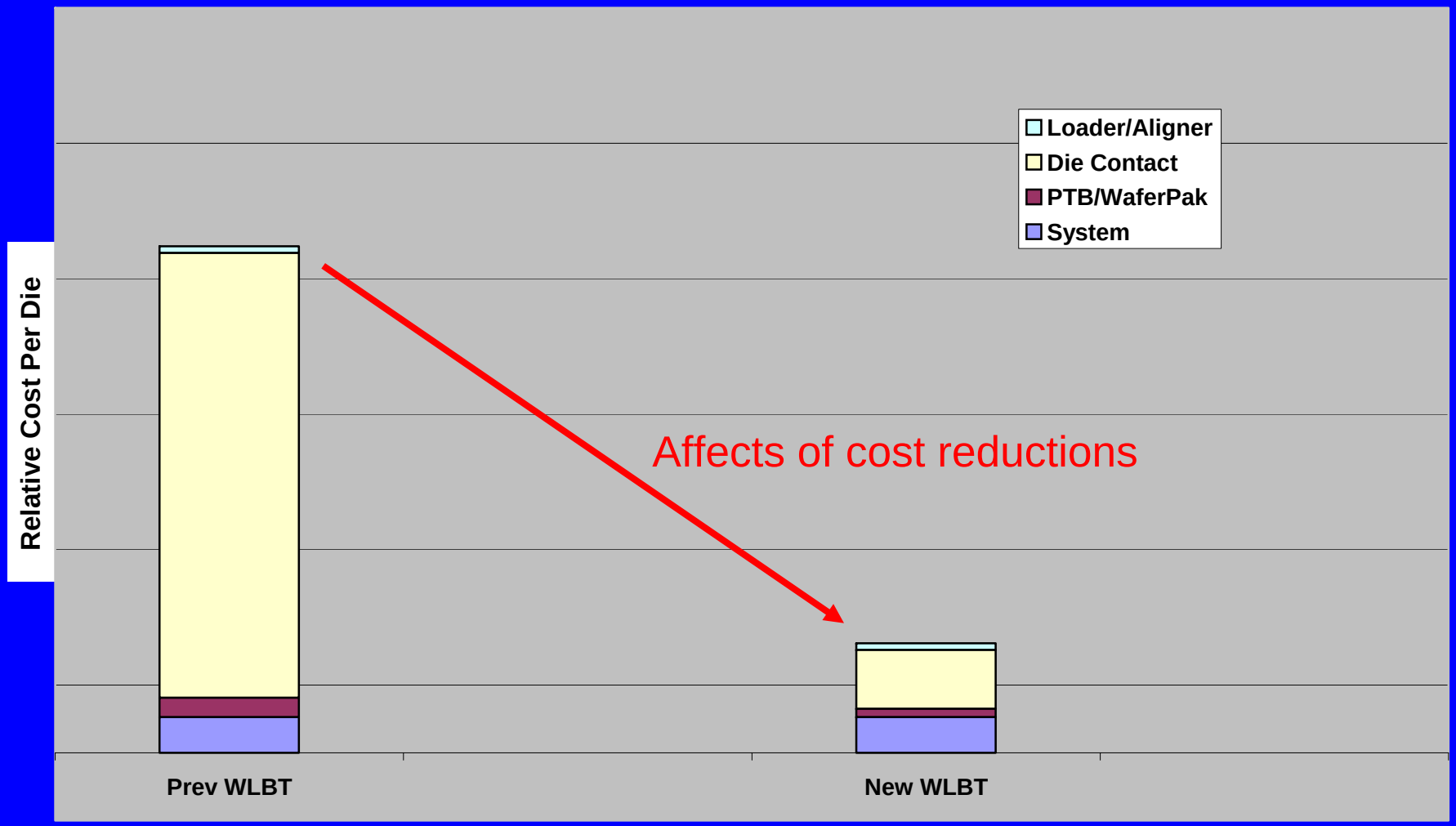


Recent WLBT Innovations

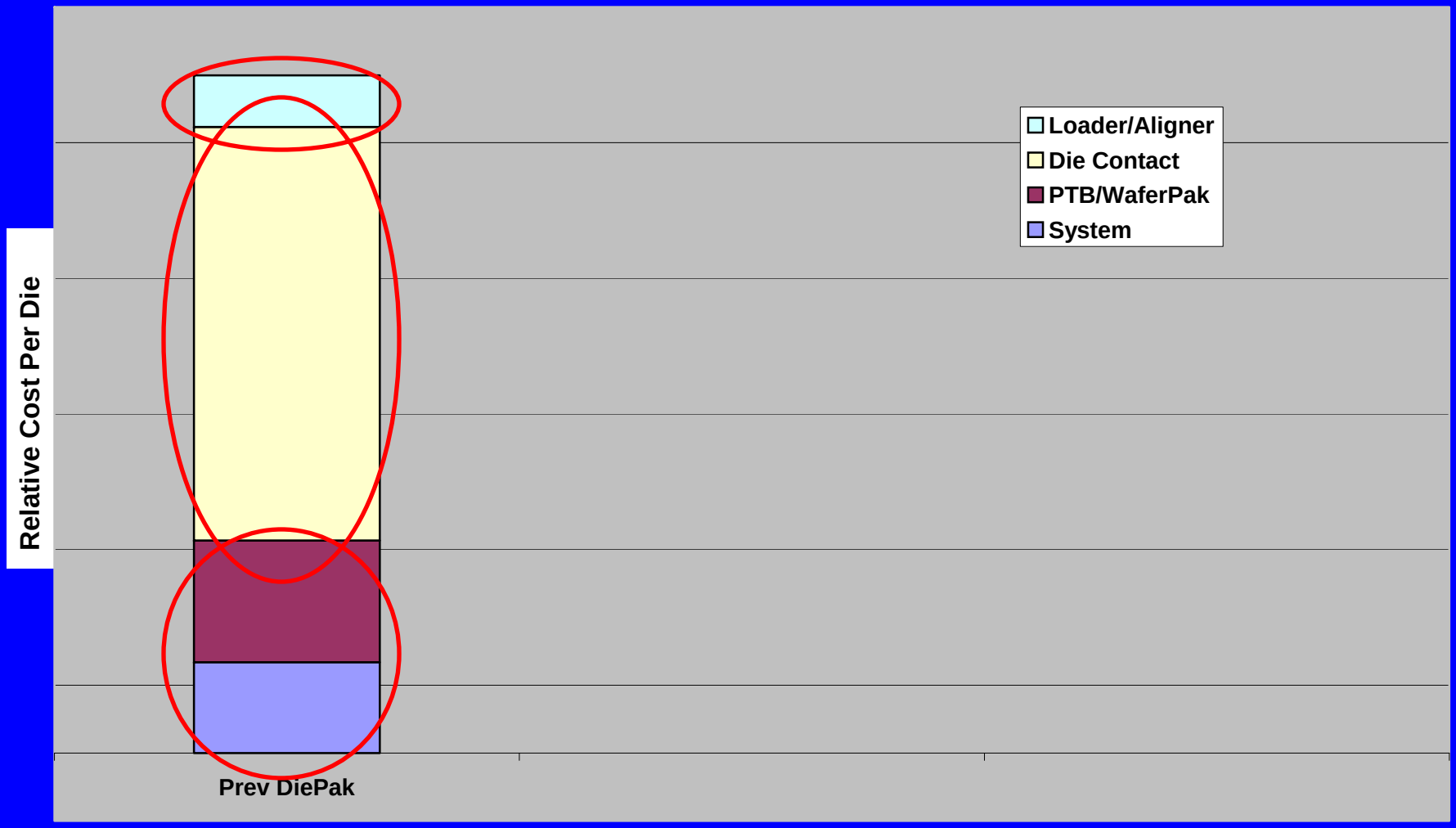
- Low cost contactor technologies
- Mechanical fixture cost reductions
- Electrical path cost reductions



WLBT Innovations Affect

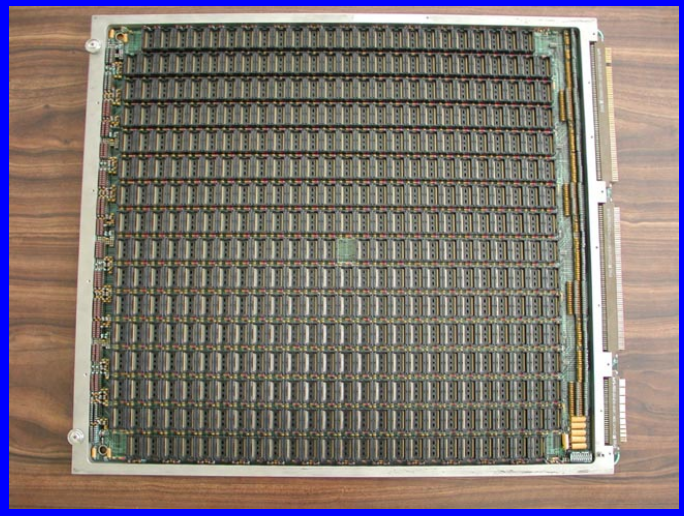


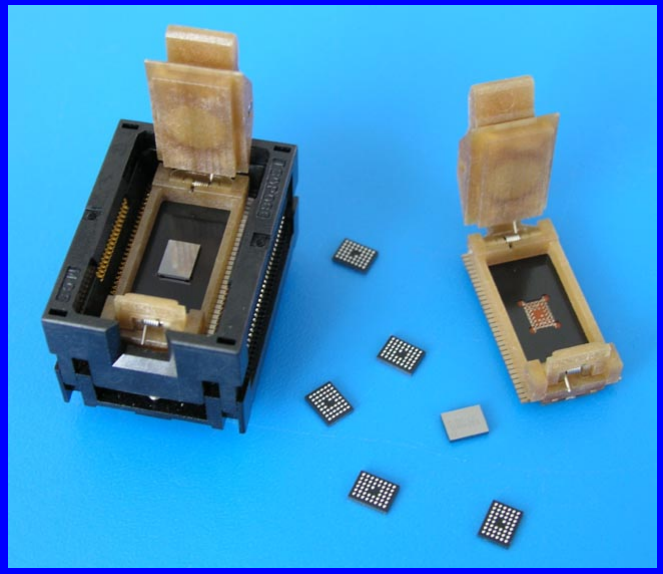
“DiePak” Cost Drivers



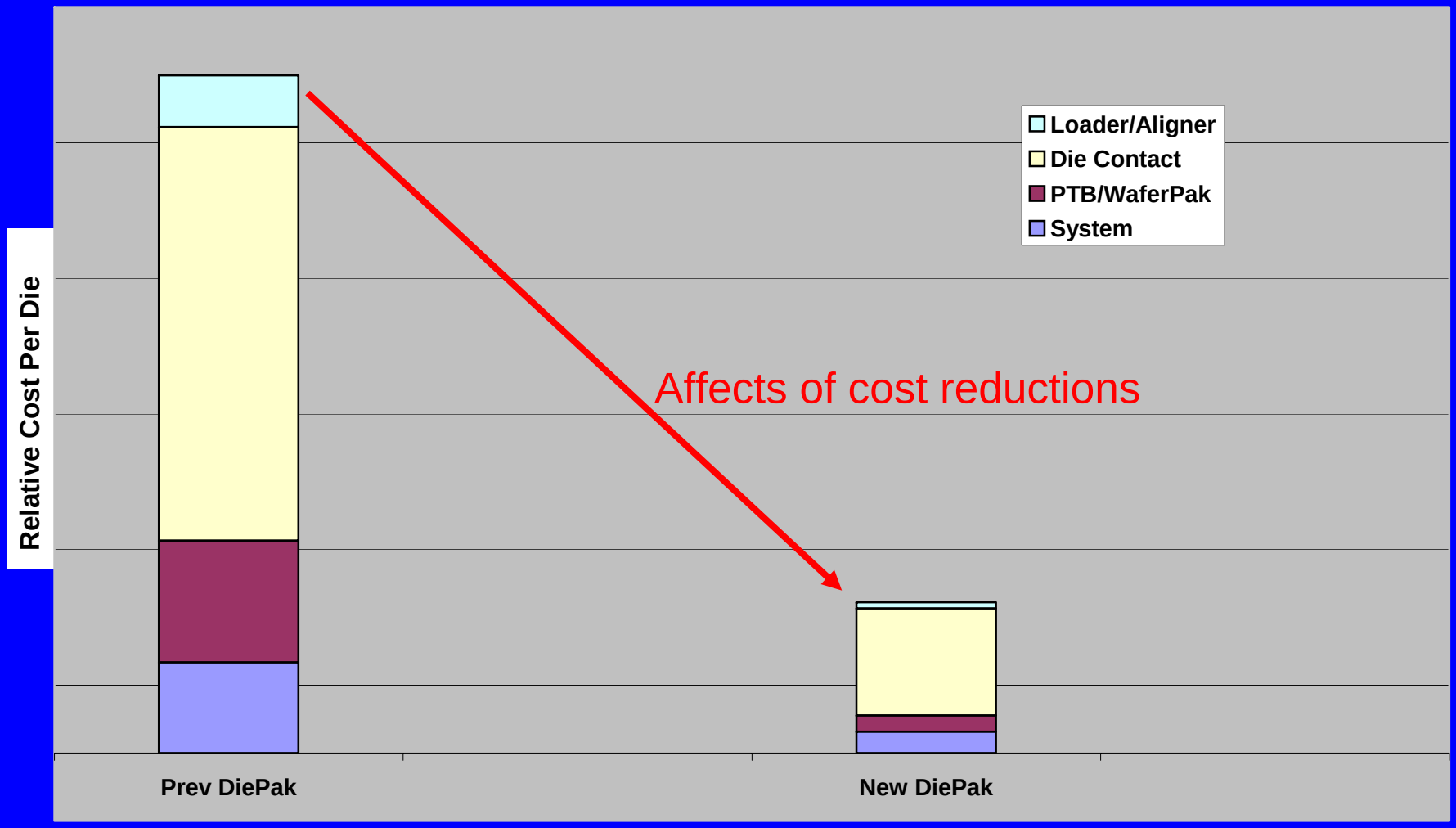
Bare Die Carrier Innovations

- "TSOP" Carrier
- Standard TSOP sockets
  - Lower cost
  - More per PTB
- Large TSOP PTB
  - More parts per PTB
  - Amortize system cost over more die
- Die can be loaded while in socket

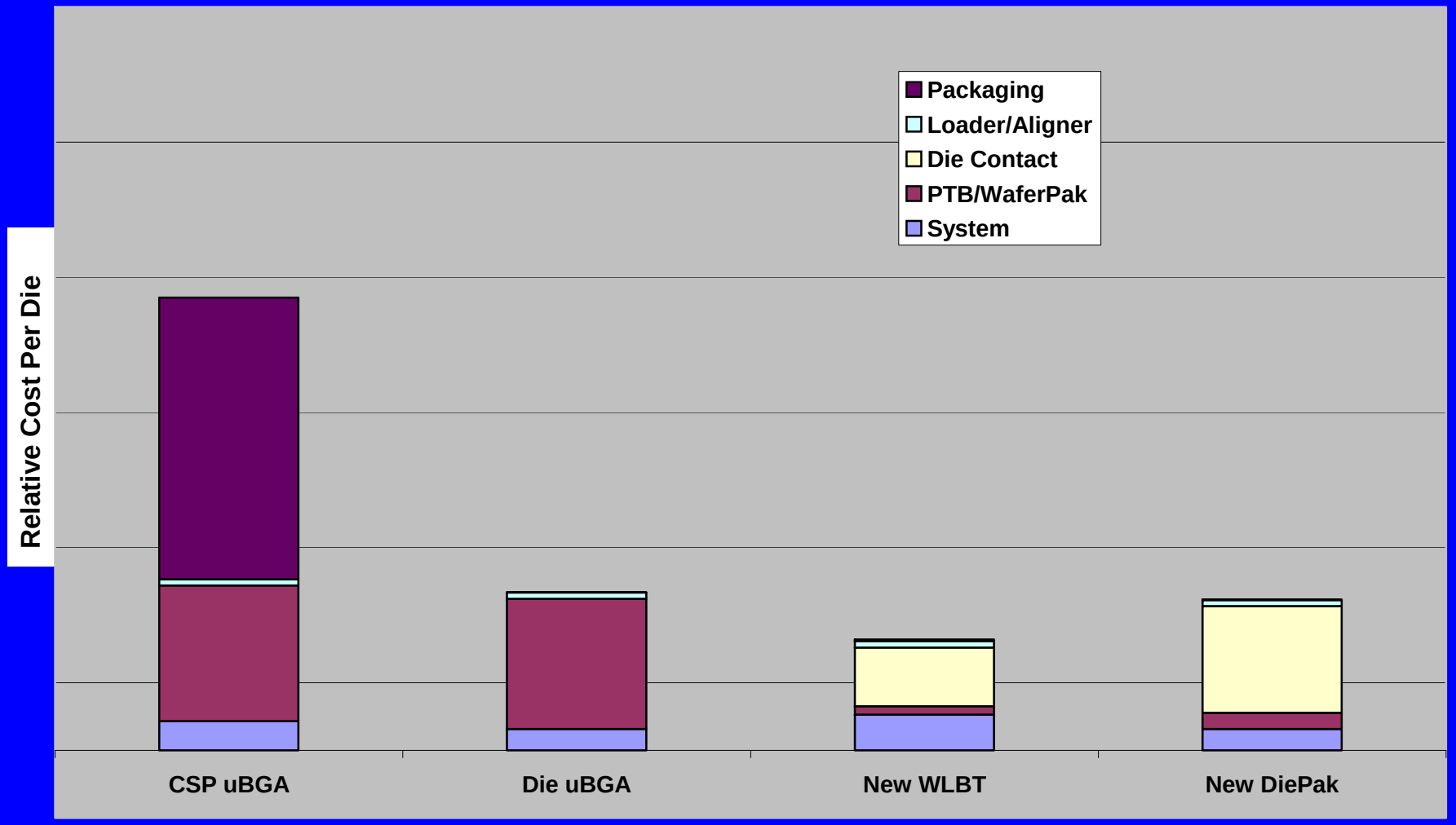




“DiePak” Innovations Effect

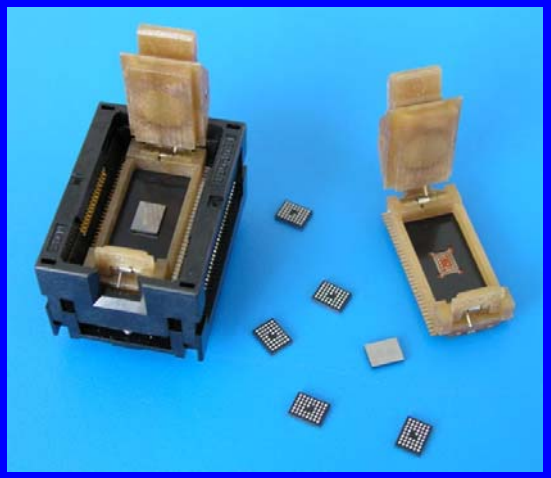


Comparison to µBGA



Conclusions

- **Both WLBT and singulated die burn-in are here today**
- **Demand for burned-in KGD will increase**
- **“DiePak” is lowest cost for low volume burned-in KGD; WLBT is the lowest cost solution for high volume**
- **The use of WLBT and “DiePak” will increase dramatically in the next few years**



Burn-In Acceleration by Better Temperature and Voltage Control

2005 Burn-in and Test Socket Workshop

March 6 - 9, 2005

BiTS™
Burn-in & Test
Socket Workshop

Larry Friedrich and Jim Babcock
Unisys Corp, San Diego, CA 92127

Agenda

- Introduction to Burn-in
- Burn-in Acceleration Models
- How to Optimize Burn-in
- Burn-in Cost Drivers
- Case Study

Introduction

- **Burn-in Today**
  - Cost is measured by capital equipment price
  - Burn-in is a manual batch process
  - Technology is stretched to meet high power demands
  - Burn-in optimization takes longer than the product life cycle
  - Socket utilization is not a consideration

Introduction

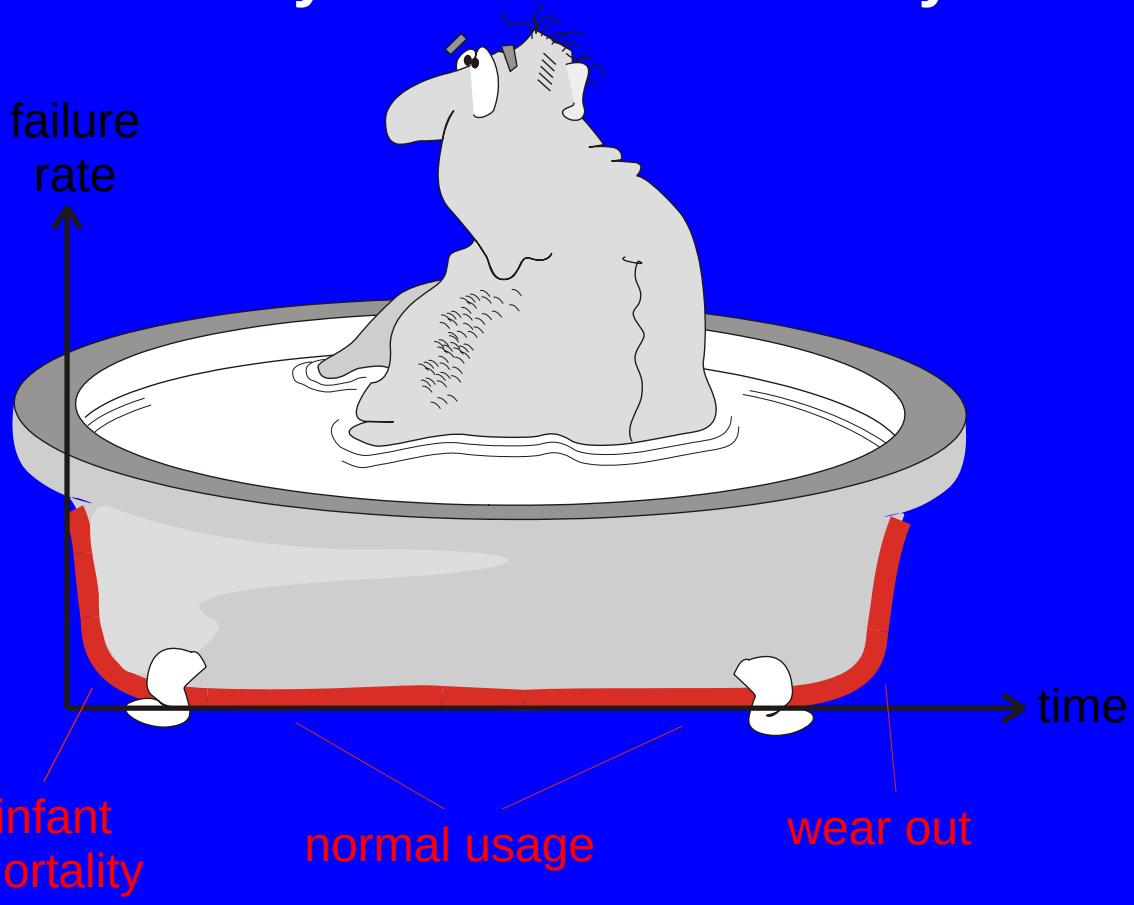
- **Burn-in Tomorrow**
  - Burn-in costs are measured by Total Cost of Ownership (TCO)
  - Burn-in is an automated, continuous flow process
  - Burn-in optimization is done at the beginning of the product life cycle
  - Socket utilization is critical

Burn-in Challenges

- Device power is increasing
  - 90 and 65 nanometer silicon is making the burn-in challenge worse! (>25W and up to 400W)
  - Leakage current is predominant at burn-in conditions
- Power delivery considerations – what you want is:
  - Low voltage drop delivery paths
  - Tight voltage control
- Thermal control – what you want is:
  - Low thermal impedance paths
  - Tight temperature control

What is burn-in and why is it done?

- **Burn-in is a process that stresses a semiconductor to accelerate early life / infant mortality failures**



Burn-in Acceleration

- Temperature and voltage are the most common burn-in accelerators
  - DUT junction temperatures are typically held in the 100°C to 150°C range
  - DUT voltages are typically 1.5 times the normal use voltages
- Burn-in duration is determined by:

$FT_{BI} = FT_U / (AF_V * AF_T)$

FT_{BI} = time to failure during burn-in

FT_U = time to failure at usage conditions

AF_V = voltage acceleration factor

AF_T = temperature acceleration factor

Burn-in Acceleration

- Burn-in duration (FT_{BI}) is reduced as AF_V and AF_T increase…. BUT
  - No DUT being burned-in can be allowed to exceed the maximum DUT voltage or junction temp
  - The top of the control bandwidth must be safely under the DUT maximum allowable temperature and voltage
  - The bottom of the control bandwidth must be used in the burn-in acceleration models to insure all DUTS get sufficient burn-in
- Tight control of DUT temperature and voltage optimizes burn-in acceleration factors

Temperature acceleration

- Thermal acceleration is given by the Arrhenius equation

$$A_T = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{TEST}}\right)\right]$$

Where:

E_a is the activation energy (see table in backup)

k is Boltzmann's constant (8.617E-05 eV/K)

T_{USE} is the DUT junction temperature at application use

T_{TEST} is the DUT junction temperature in burn-in

- Goal is to maximize T_{TEST} without damaging the device
- Burn in acceleration is determined by maximum allowable T_{TEST} minus control error band

Voltage Acceleration

- Voltage acceleration is given by:

$$AF_V = \exp[\beta \times (V_s - V_u)]$$

- Where:

  V_u and V_s are use and stress voltages, in volts

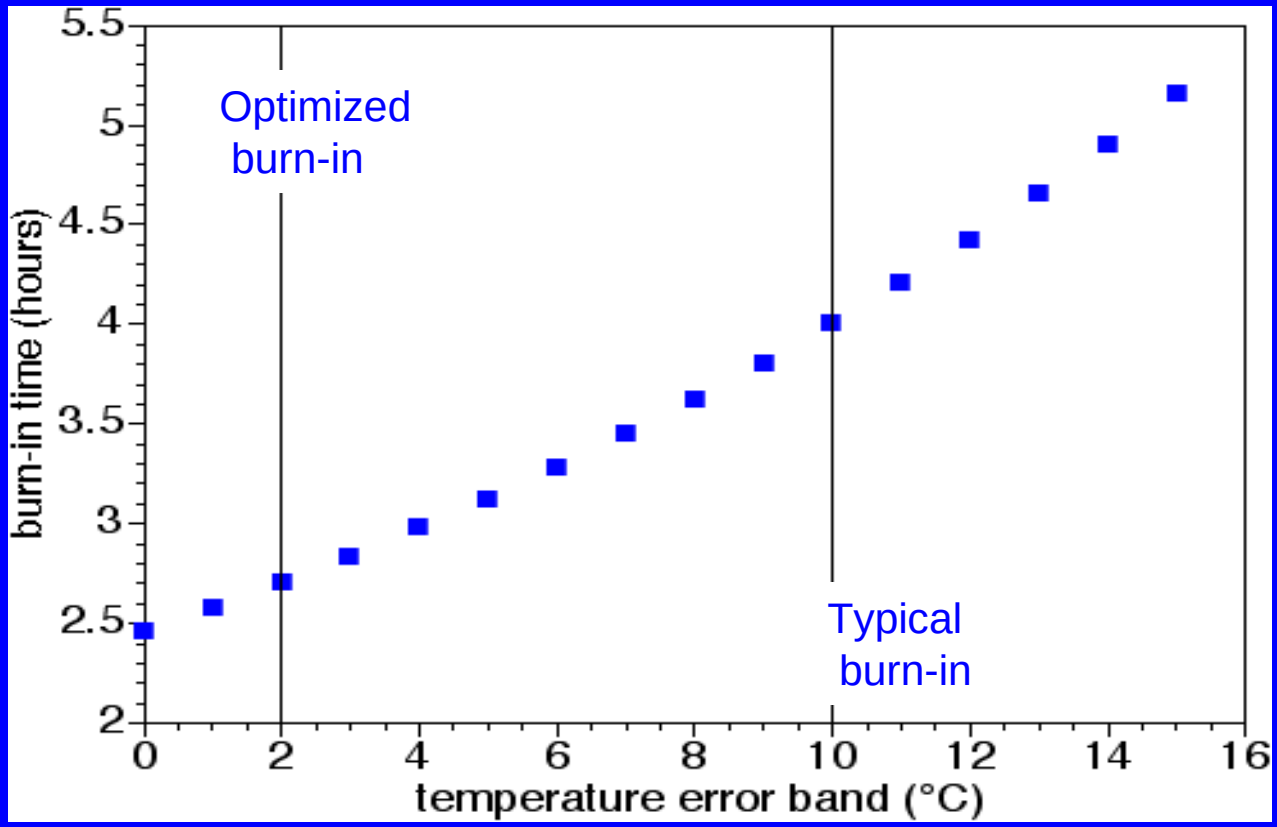
  β is the voltage acceleration term (4 per volt is typical)
- Goal is to maximize V_s without damaging the DUT
- Burn in acceleration is determined by using the maximum allowable V_s minus control error band

Burn-in Optimization

- In this example, we compare today's typical burn-in to optimized burn-in

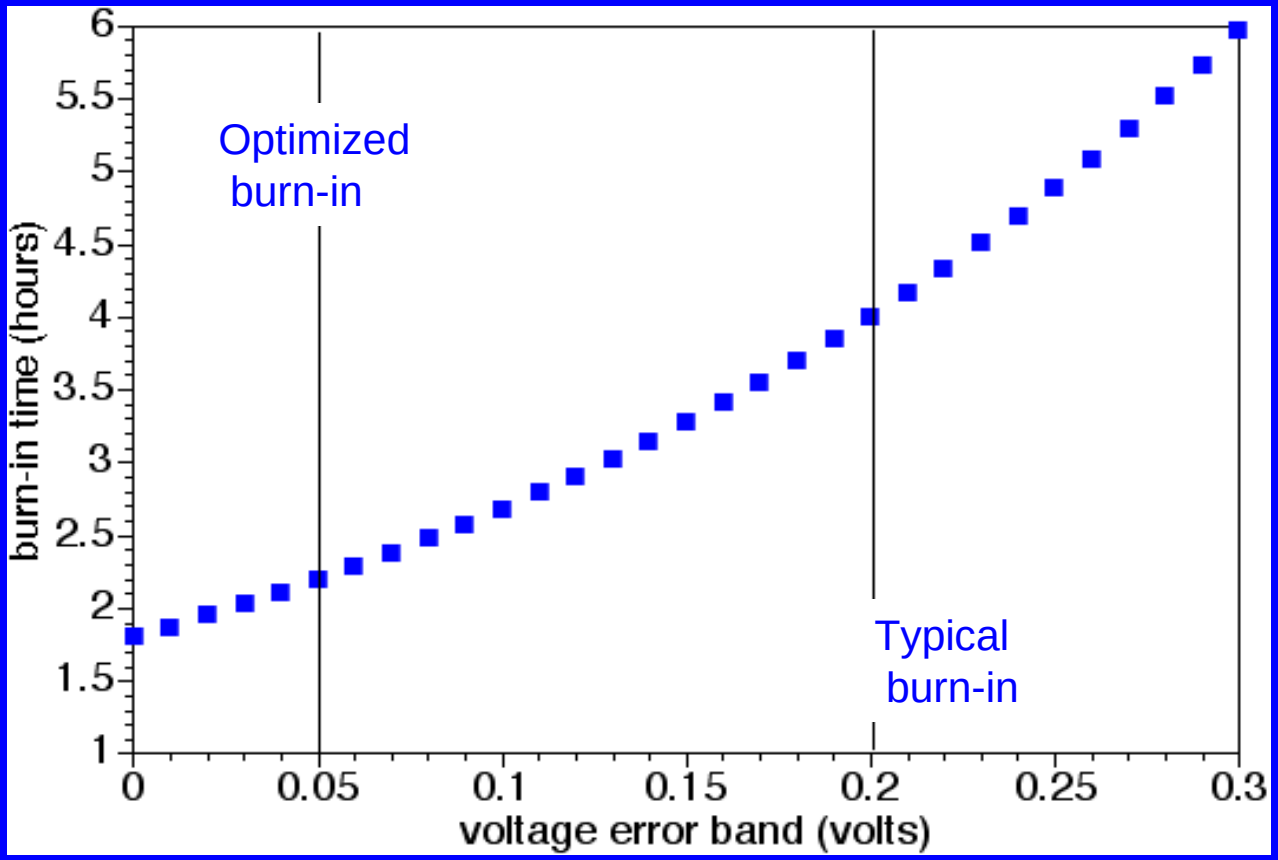
Typical burn-in control	Optimized burn-in control
Temp → ± 5ºC	Temp → ± 1ºC
Voltage → ± 100mV	Voltage → ± 25mV

Temperature Acceleration



- Burn-in time can be reduced from a 4 hour cycle to a 2.7 hour cycle with optimized DUT temperature control alone
- That is approximately a 33% time savings

Voltage Acceleration



- Burn-in time can be reduced from a 4 hour cycle to a 2.2 hour cycle with optimized DUT voltage control alone
- That is approximately a 45% time savings

Combined Temperature and Voltage Acceleration

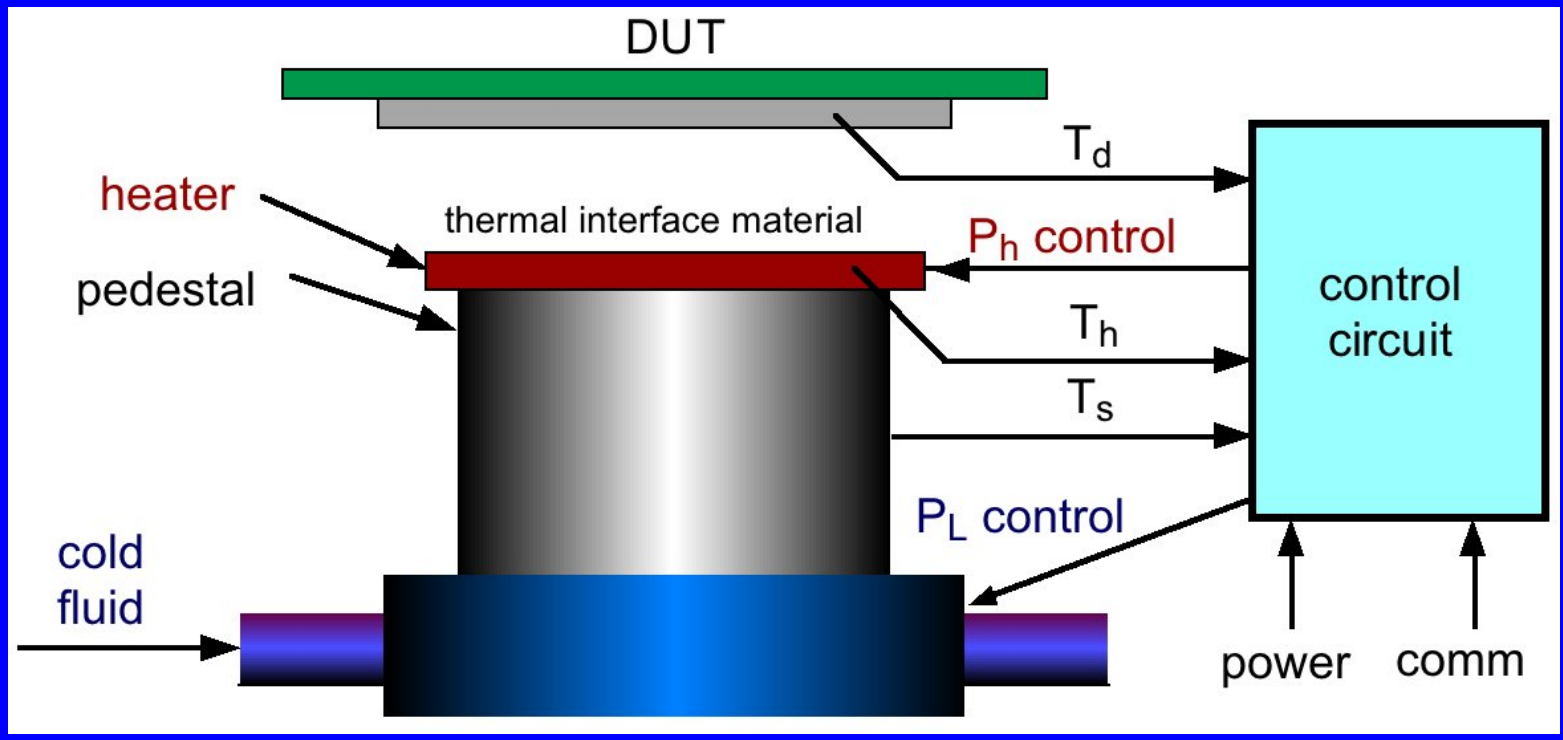
- Temperature acceleration ⇒ 67% original time
- Voltage acceleration ⇒ 55% original time
- The combined savings from both accelerations can yield a new burn-in that is 37% of the original time, a savings of up to 63%
  - 4 hour cycles → 1.5 hour
  - 24 hour cycles → 9 hours
  - 168 hours → 62 hours
  - 1,000 hours → 370 hours

Optimized Temperature Control

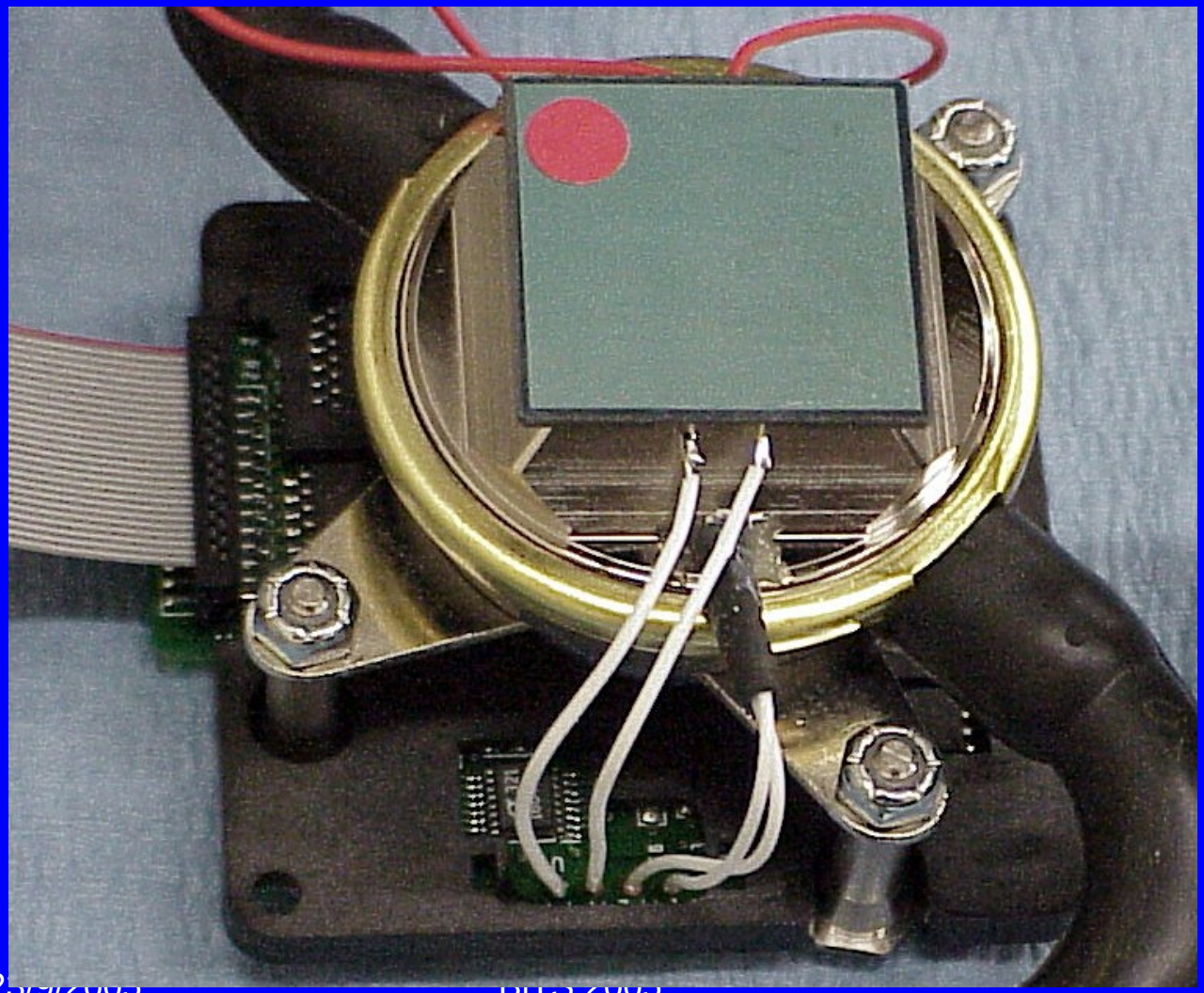
- The top challenges to achieving tight DUT temperature control are:
  - Thermal gradients within the burn-in system
  - Variations in the DUT package thermal resistance
  - Variations in DUT power
- To achieve tight control, the burn-in system must be able to dynamically compensate for the variations listed above
  - This requires Active Temperature Control (ATC) of DUT temperature at the individual DUT level

Active Thermal Control Pictorial

- Active thermal (temperature control)
  - Liquid cooled or phase change
  - Heater and/or coolant control

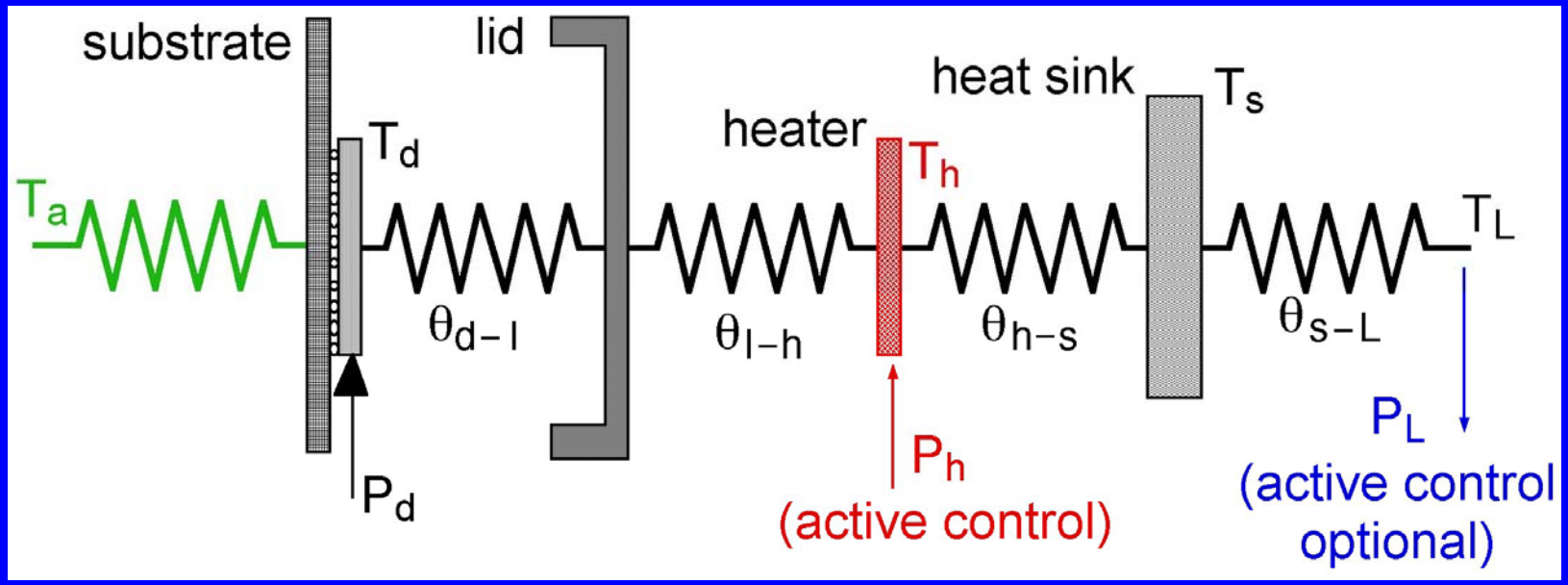


Cooling/Gimbal Assembly



Active Thermal Control

- Active cooling technology
  - Liquid
  - Low mass, highly conductive heater
    - Heater provides very fast dynamic response
  - Temperature control with or without DUT thermal sensor



Optimized Voltage Control

- The top challenges to achieving tight DUT voltage control are:
  - Voltage drops within the burn-in system
  - High variations of the DUT power within a burn-in lot
- To achieve tight control, the burn-in system must be able to dynamically compensate for the variations listed above
  - The power delivery path must be carefully managed
  - Individual voltage control at each DUT socket
  - Tight control feedback loop with fast dynamic response

Optimized Voltage Control

- For example:
  - A 100W DUT at 1.5VDC draws ~67Amps
  - Total power delivery path resistance must be <1milliohm (Yes…milliohm)
  - Remote voltage regulation (4 wire) at the DUT socket is needed to achieve voltage control within +/-25mV
- One way to accomplish this is to mount individual DUT power supplies very close to the DUT socket
- The BIBs can be hard docked in the burn-in system to eliminate power delivery interconnections

Burn-In Costs Drivers

1. Burn-In duration
   - The top burn-in cost driver is burn-in duration
     - Cut burn-in time in half and capacity/throughput doubles
2. Burn-in socket utilization
     - Need a robust method to keep the sockets filled
3. Handling and human factors
   - Device ESD damage, socket/BIB damage, ergonomic based injuries
   - Automated burn-in eliminates these costs with a fully controlled DUT handling environment

Burn-In Cost Drivers

4. Testability during burn-in - yield
   - "Time to fail" reporting optimizes burn-in duration
   - Automated "re-test" eliminates "false" fails
5. Capital equipment cost
   - Shorter burn-in duration and higher socket utilization means fewer systems are needed to deliver the same capacity
6. Consumables
   - The least amount the better!
7. Facilities
   - An integrated TCO burn-in approach minimizes costs

Case study
Optimized Vs Traditional Burn-in

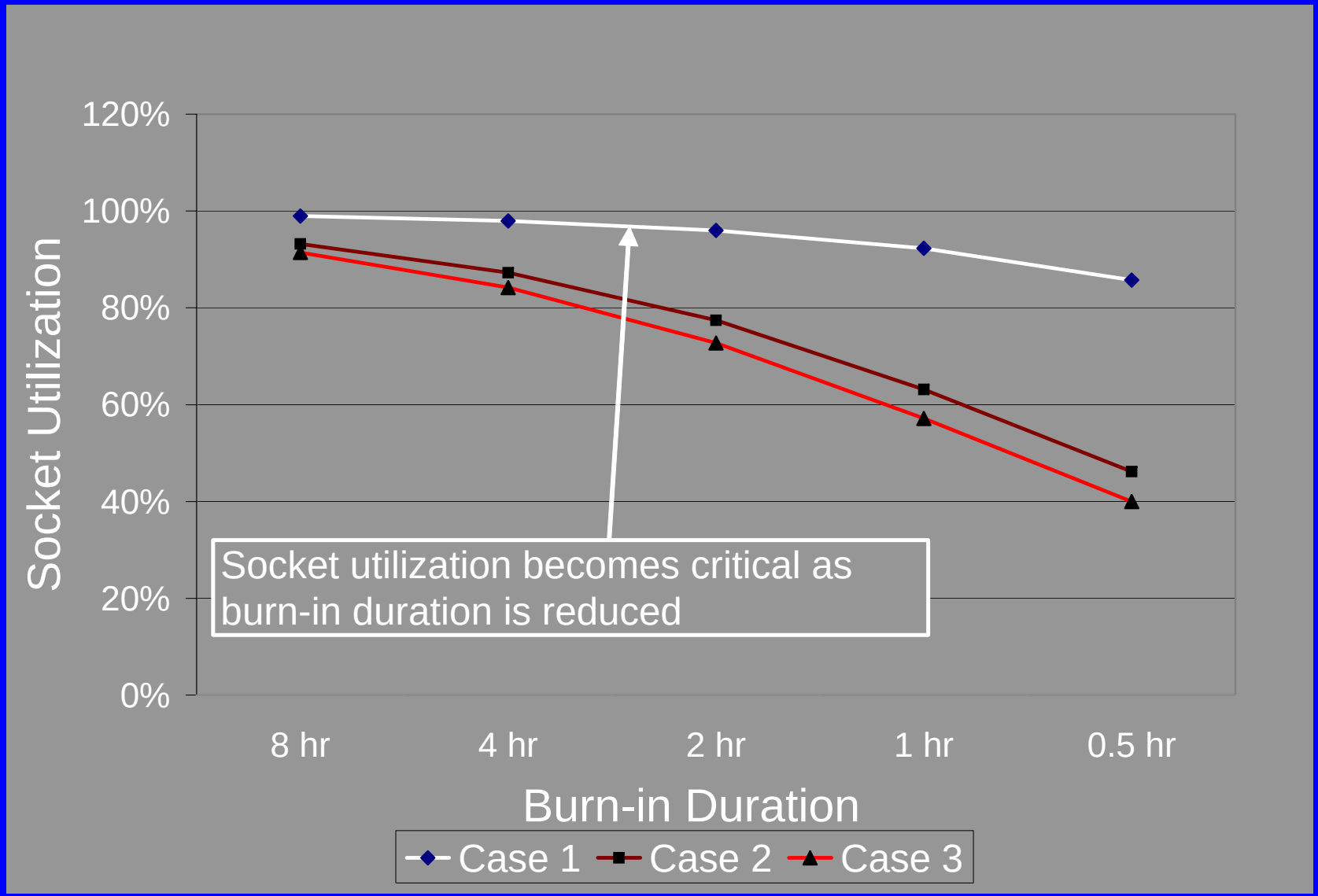
Case study conditions:

- Based on commercially available burn-in equipment
  - DUT power between 25W to 200W
  - Uses TCO model as basis for comparison..
    - Utilization, UPH, equipment cost, BIBs, handlers…
  - Does not factor in burn-in duration reduction

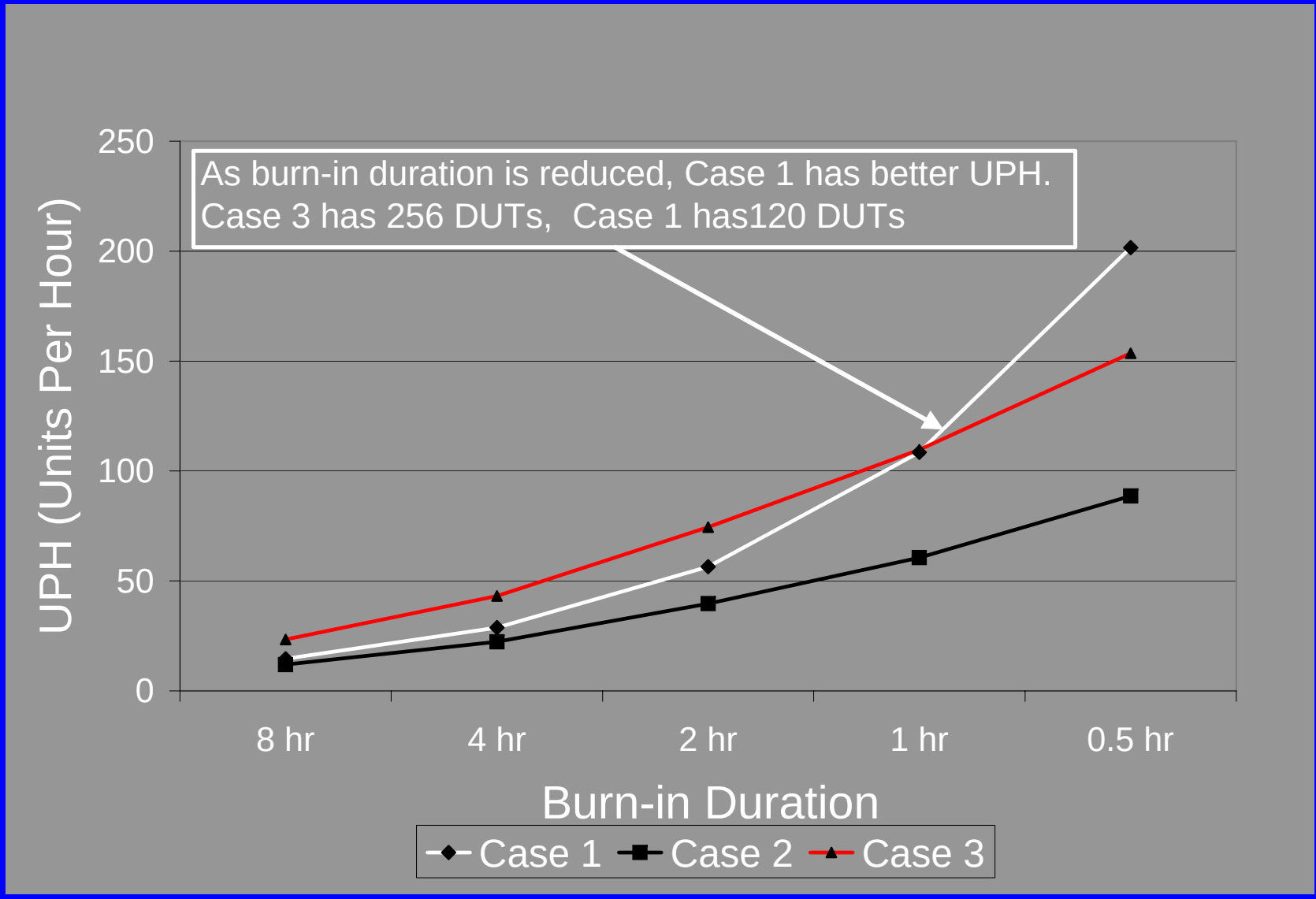
Case study
Optimized vs Traditional Burn-in

- Case 1 - Optimized burn-in
  - Fully automated burn-in integrated into the burn-in system
  - Continuous flow burn-in process
  - System socket capacity = 120 DUTS
- Case 2
  - Traditional burn-in – Manual loading
  - Batch burn-in process
  - System socket capacity = 128 DUTS
- Case 3
  - Traditional burn-in – Manual loading
  - Batch burn-in process
  - System socket capacity = 256 DUTS

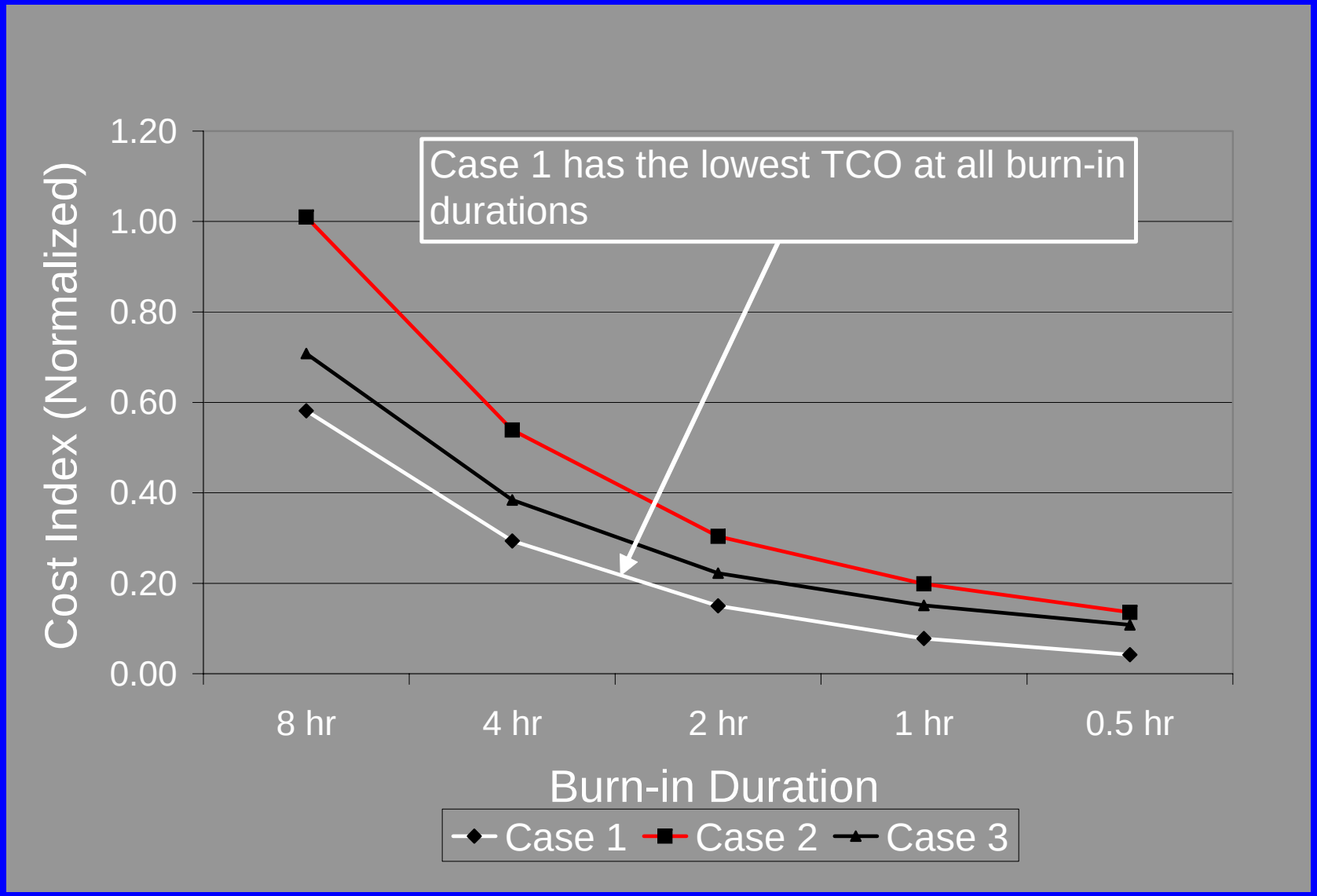
Burn-in Duration vs Socket Utilization



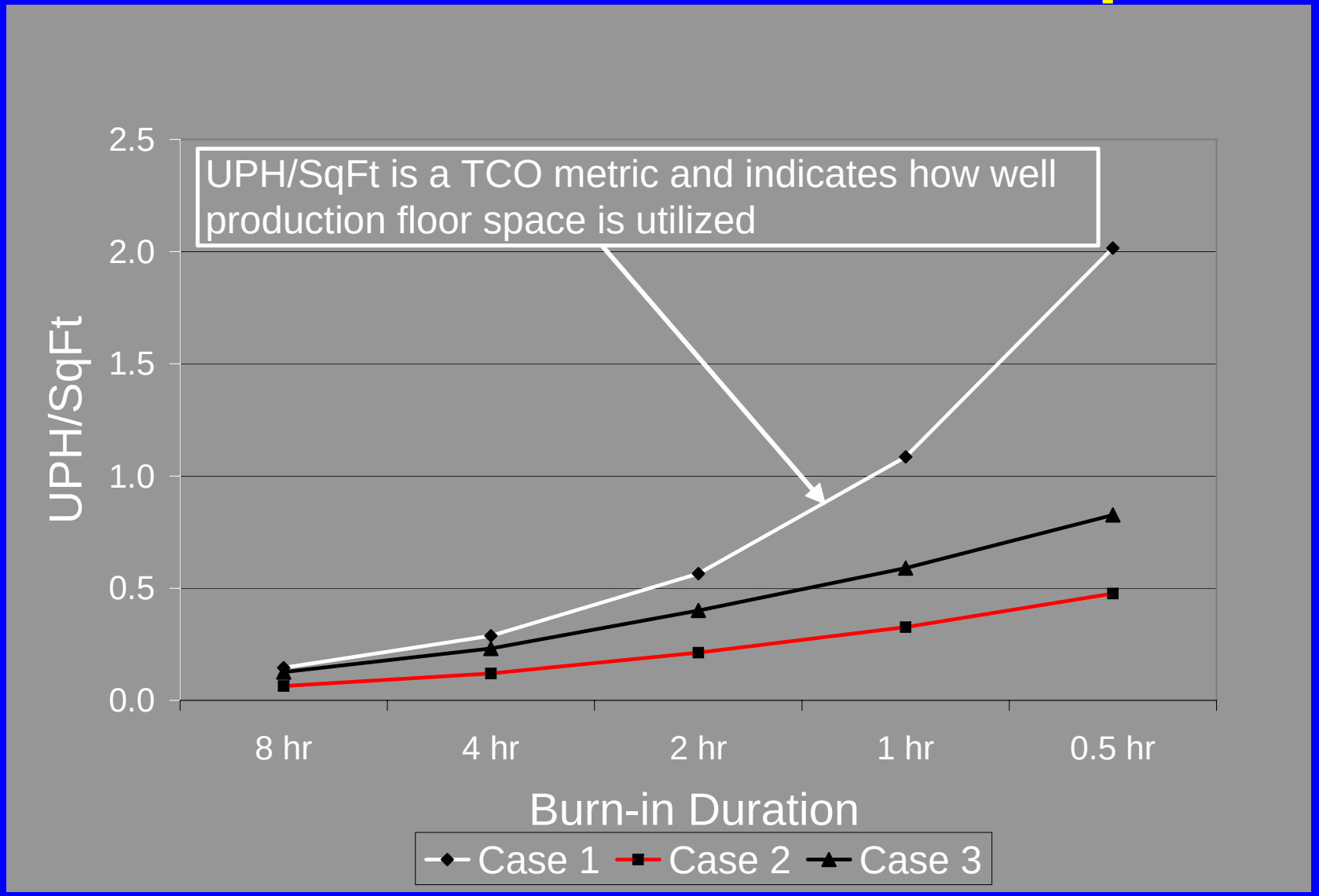
Burn-in Duration vs UPH



Burn-in Duration vs Cost/UPH



Burn-in Duration vs UPH/SqFt



Summary

- Optimizing burn-in temperature and voltage control can dramatically reduce burn-in durations
- Integrating “DUT level” automation into the burn-in system, “Burn-in in a Box”, can achieve 90% socket utilization even at short burn-in durations
- Managing the Total Cost of Ownership is the right way to reduce the cost of burn-in
  - Reducing burn-in duration dramatically reduces TCO
  - Automation is required as burn-in durations are reduced

Q & A

References

- ASIC Products Applications Note, Quality and Reliability, Revision 3, IBM, 1999.
- Knowledge Based Reliability Evaluation of New Package Technologies Utilizing Use Conditions, Intel, #245162-001, 1999.
- CMOS Quality Monitor Report, IBM, 1999.

Approaches and Methodologies for High Resolution Burn-In and Test Data Management

Tamás Kerekes
NplusT Semiconductor Application Center
Burn-in & Test Socket Workshop
March 6 – 9, 2005

Agenda

- Targets
- Difficulties
- New Methodologies
- Case Studies
- Conclusions

Burn-In

Monitoring

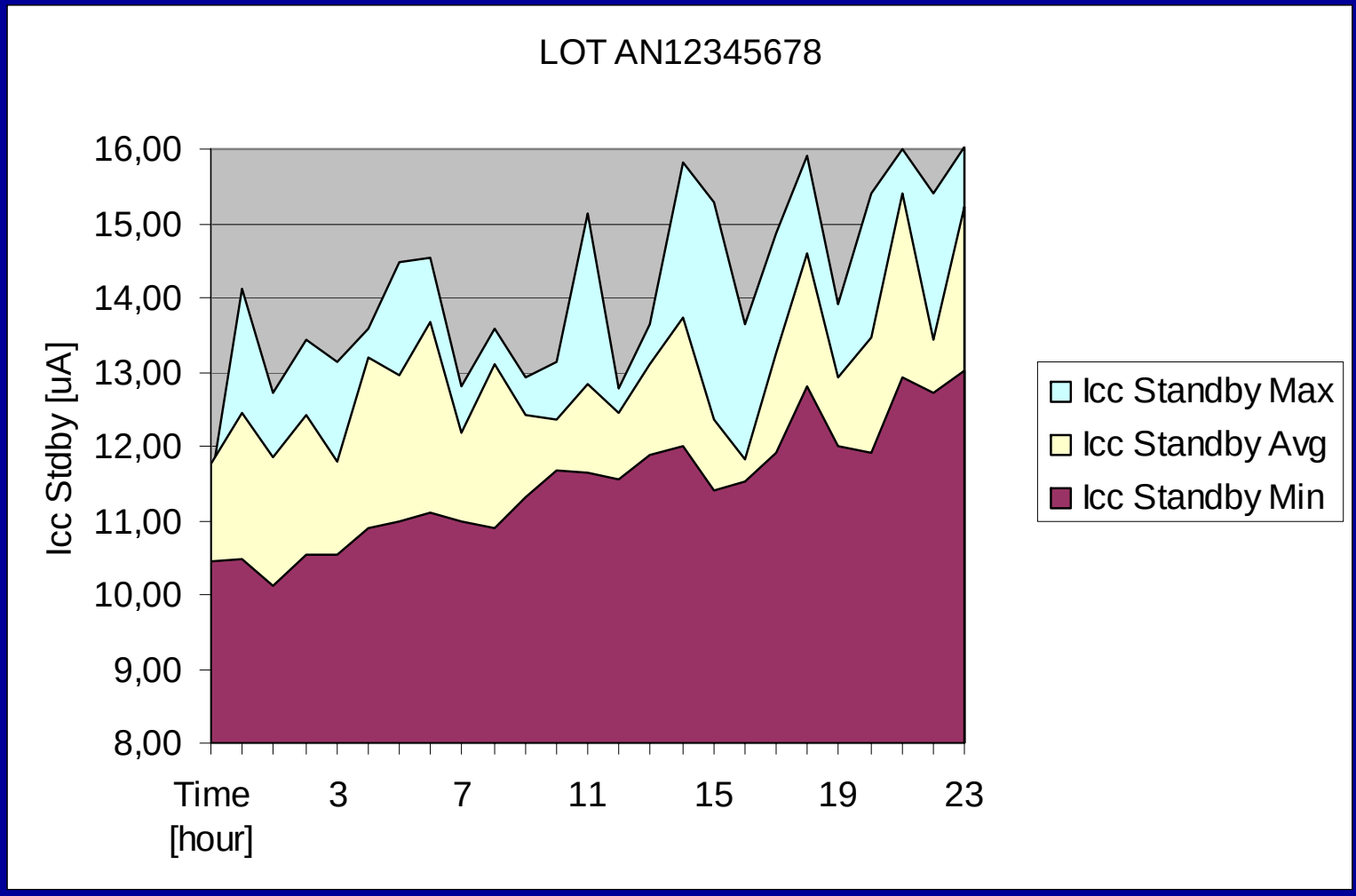
Data Collection is not new in Burn-In

Data Collection

Reporting

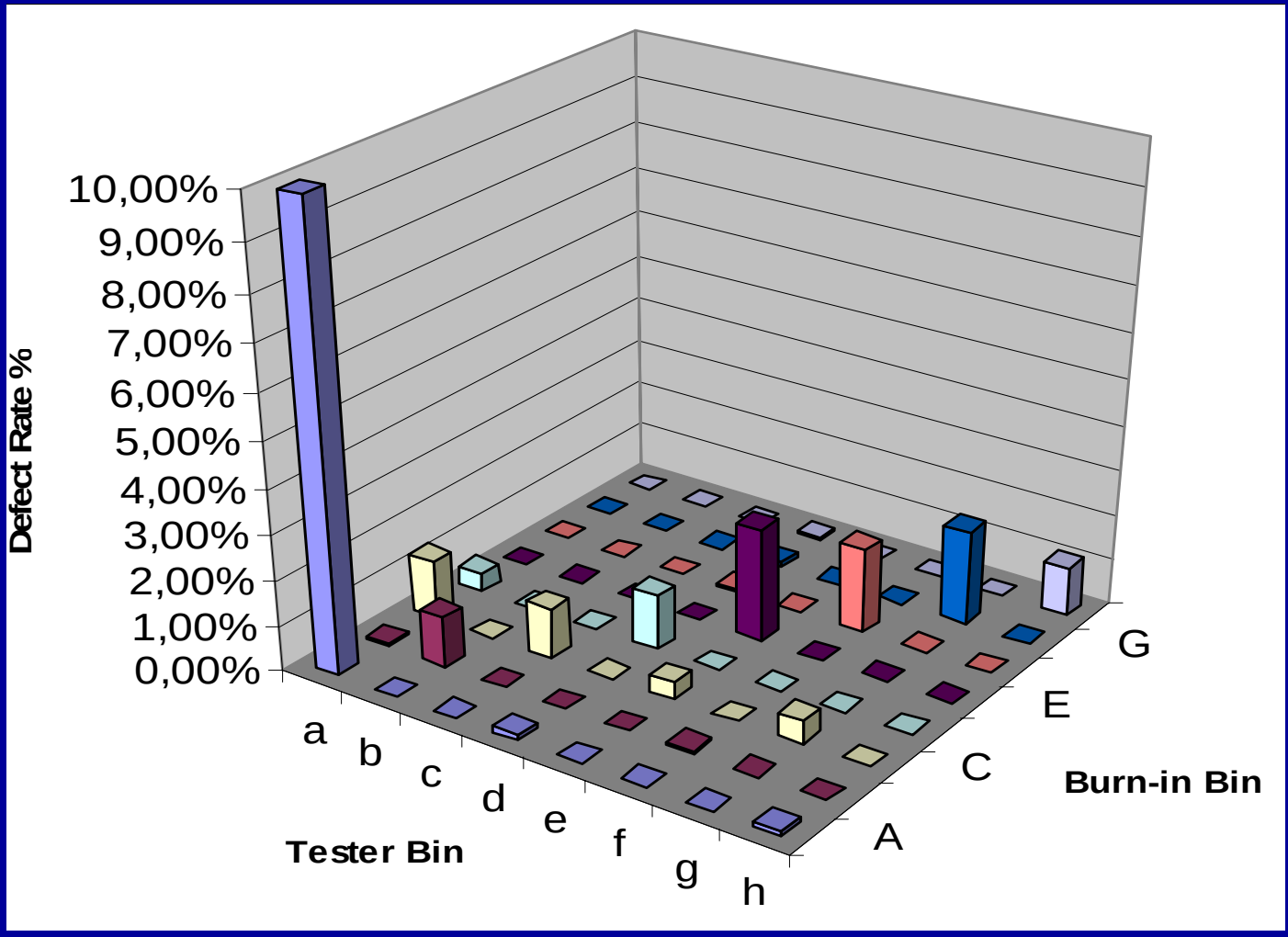
...but for certain tasks, high resolution data is needed

Parameter vs. Burn-in Time



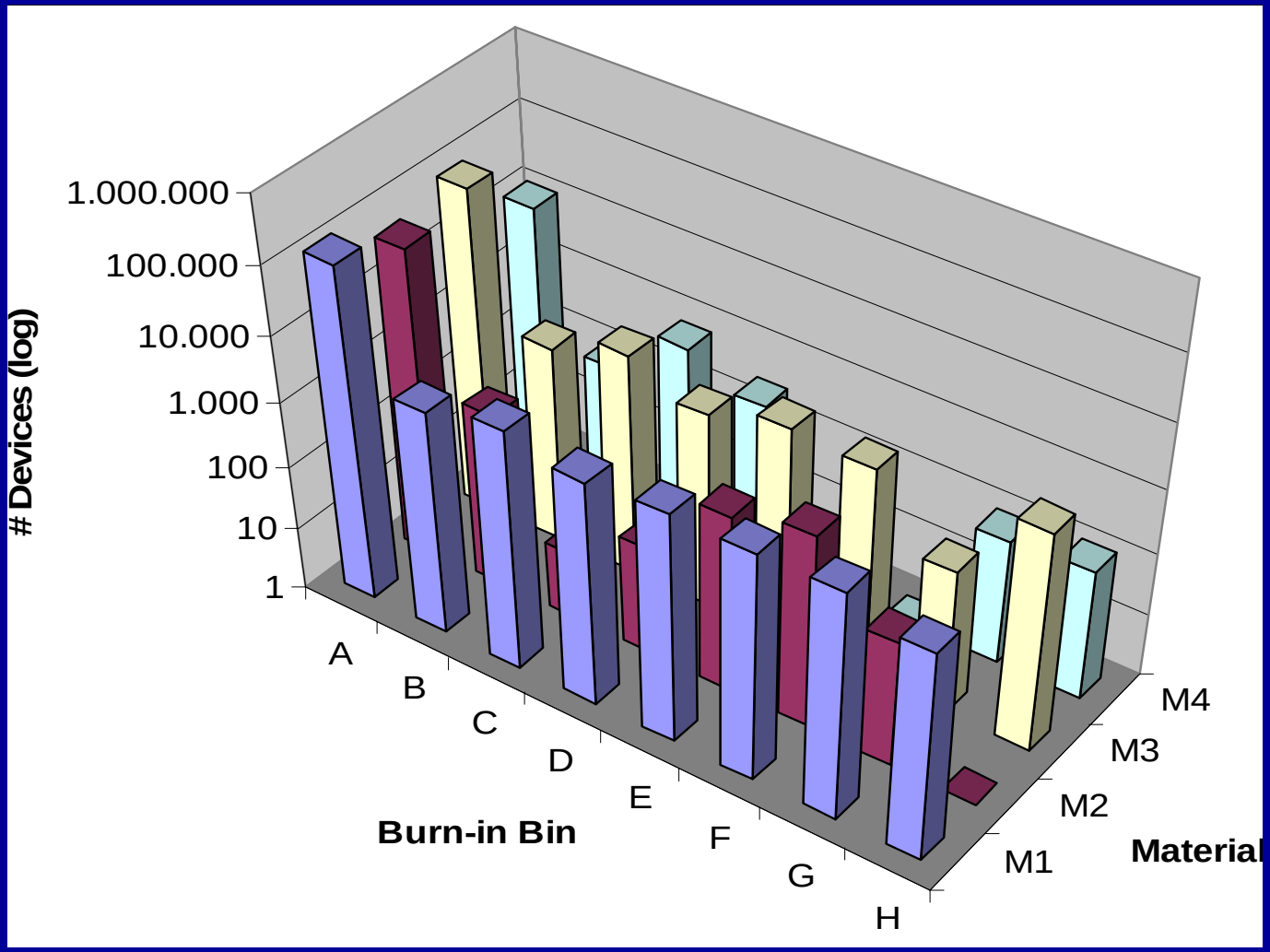
Values and charts prepared for demonstration

Correlation: Testing vs. Burn-in



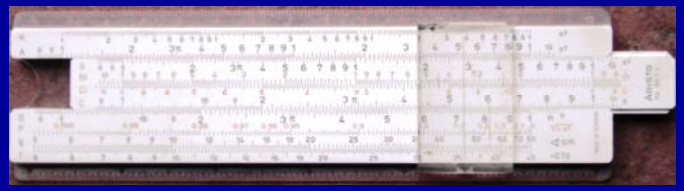
Values and charts prepared for demonstration

Material vs. Reliability

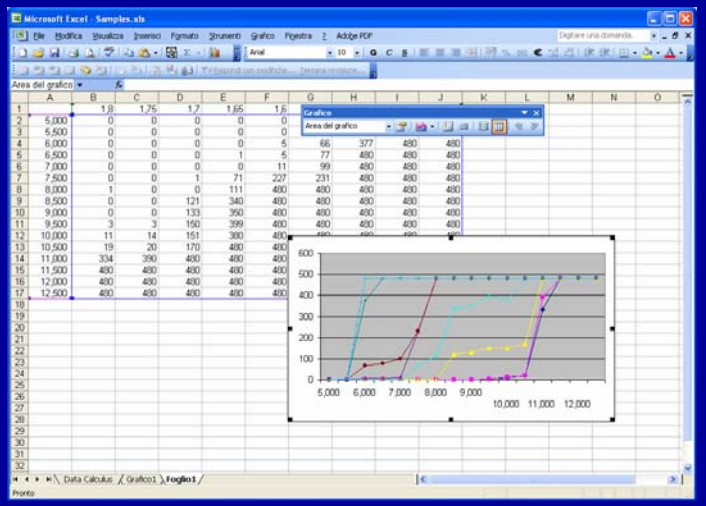


Values and charts prepared for demonstration

Flexible Data Access



Selected and preprocessed data available in spreadsheet programs for further custom processing



The preferred tools of the engineers are evolving fast ...

Area Management

- Summary Reporting
- Statistical Process Control
- Equipment and Board Utilization
- Socket Reliability Tracking
- STDF Output
- ...

Difficulties

- Good news: equipment are able to generate the necessary data
  - BI → TDBI → MDBI (Measurement During Burn-in)
- Bad news: too much data
  - High parallelism, high throughput
  - Time available for deep and hi-res measurements
- Practical alternatives
  - No or limited data generation
  - No or limited data processing

Case Study: Data Calculus

- Reference Case:
  - 10 equipment, 48 slots each, 200 dut / bib
  - 500 test steps, 10 bytes per test
  - 3 cycles per day
- Data per year:
  - > 50 Giga records
  - > 500 Gigabyte data

Technically feasible - but far beyond the usual infrastructure (investment and management costs)

Something new is required ...

Traditional database structures can not be applied because of the huge amount of data

Testing is simpler: test time optimization does not allow extensive data generation

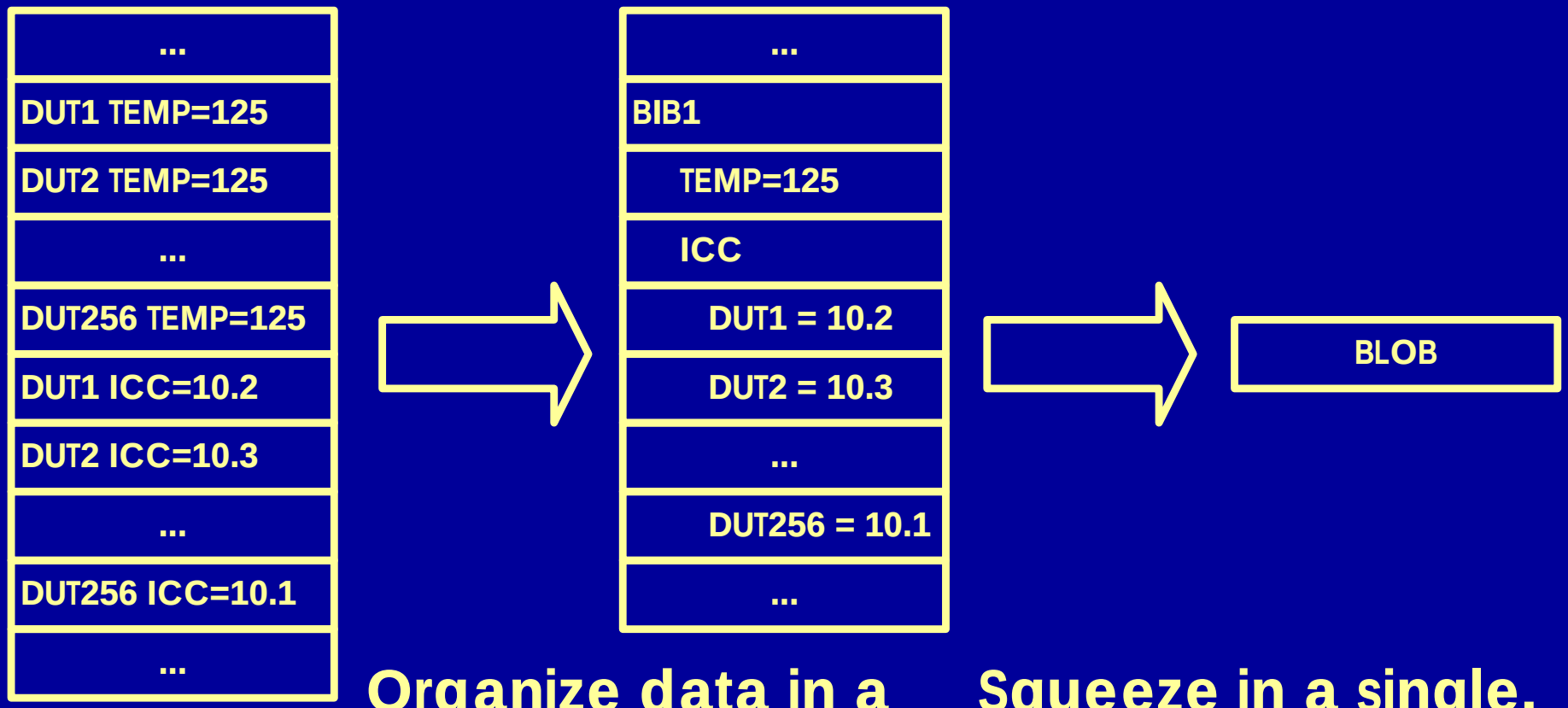
New Methodologies

- Data Organization
- Architecture

Avoiding “Record per Measurement”

- Hierarchic data storage
  - Measured values, common for every device on a board or in the equipment, are stored only once
- Measurement sequence is stored in a single, special structured record

Organization Example



Organize data in a hierarchic structure

Squeeze in a single, compressed record

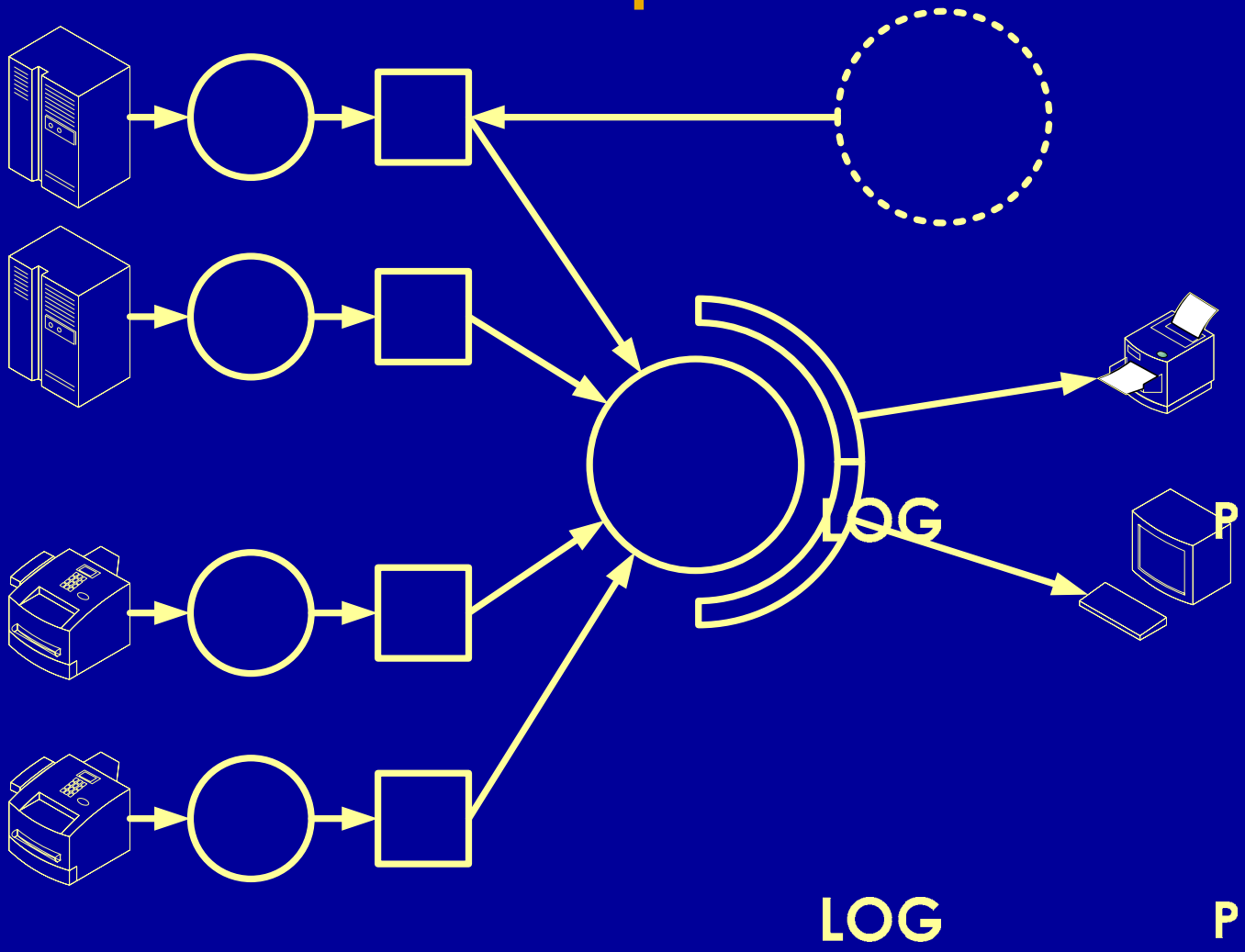
Organization Effects

- Drastically reduced record count
- Faster data transfer (lower data quantity)
- Search speeds changed
  - ☺Increased speed on standard look-ups
  - ☹Reduced speed on test data look-up (but not frequently used)

Avoiding Huge Data Sizes

- Compression of large size measurement data (bitmaps, memory images, ...)
- Compression of composite measurement structures

Architecture Proposal



Device Tracking

- By lot
  - Device level identification is possible while on board
- By single device
  - Serial number read from the device

Case Study 1: New Data Calculus

- Reference Case:
  - 10 equipment, 48 slots each, 200 dut / bib
  - 500 test steps, 10 bytes per test
  - 3 cycles per day
- Data per year:
  - > 50 Giga records ➔ < 250 Mega records
  - > 500 Gigabyte data ➔ < 60 Gigabyte

No feasibility problem with standard infrastructure

Case Study 2: Engineering Use

- Reference Case:
  - 4 equipment, 24 slots each, 200 dut / bib
  - 5,000 test steps, 100 bytes per test
  - 2 days per cycle
- Data per year:
  - 17 Giga records ➔ 7 Mega records
  - 1.7 Terabyte data ➔ 18 Gigabyte

Data organization makes feasible storage and processing

Conclusions

Maybe nothing special but ...

FEASIBLE

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