Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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BiTS Burn-in & Test Socket Workshop

Technical Program

Session 4
Tuesday 3/08/05 8:00AM

OPTIMIZING HIGH FREQUENCY PERFORMANCE

"Practical Techniques For Measuring High Bandwidth Electrical Models Of Test Sockets"

Eric Bogatin – Synergetix **Kevin DeFord** – Synergetix
Meena Nagappan – Synergetix

"3D AC Simulation Of Inter-Connector"

Jiachun (Frank) Zhou – Kulicke & Soffa
Uyen Nguyen – Kulicke & Soffa **Praba Prabakaran** – Kulicke & Soffa

"High Frequency Signal Integrity Issues In Semiconductor Test"

Ryan Satrom – Everett Charles Technologies
Jason Mroczkowski – Everett Charles Technologies

Practical Techniques For Measuring High Bandwidth Electrical Models of Test Sockets

Eric Bogatin, Kevin DeFord, Meena Nagappan
Synergetix, Kansas City, KS
www.synergetix.com

2005 Burn-in and Test Socket Workshop

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BiTS™ Burn-in & Test Socket Workshop

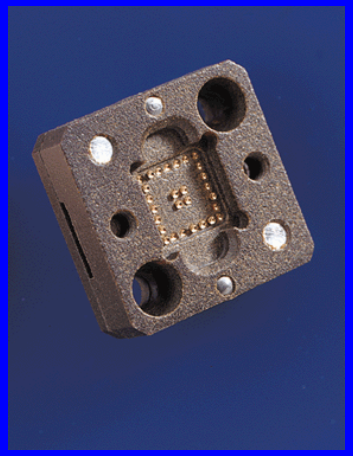
SYNERGETIX®

Agenda

- Features of the new method
- Technique/equipment
- Secrets revealed
- Example results
- Benefits

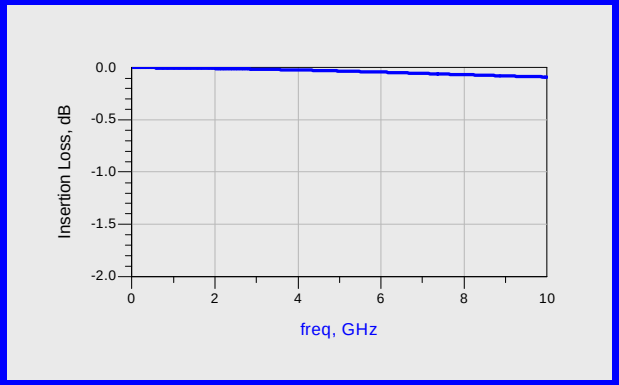
What is Electrical Characterization?

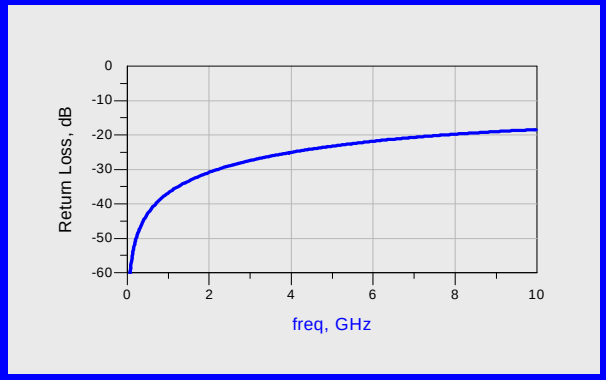
Physical world



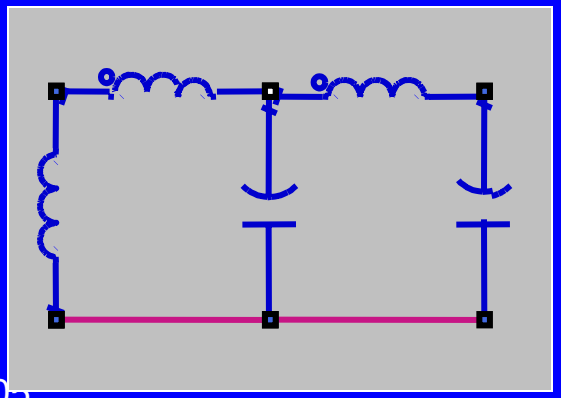
Electrical world

Behavior model: insertion loss, return loss





SPICE model: RLCT components



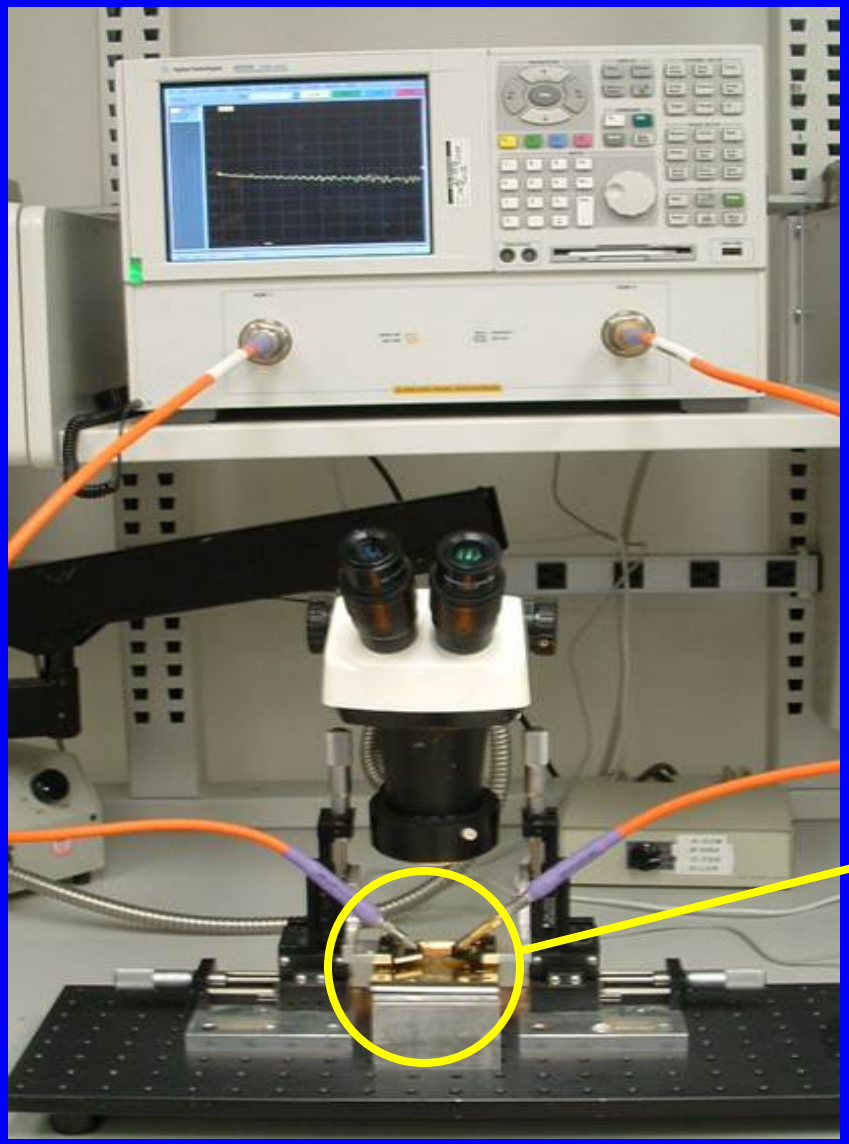
Problems and Opportunities

- Problems with current methods
  - Difficult to calibrate
  - Difficult to de-embed fixture effects
  - Published models missing key circuit elements
  - Insertion loss based on loop thru measurements with fixture included
- Goals for a new method
  - Simple, Robust, Reproducible
  - Unambiguously de-embed the fixturing
  - Non-proprietary
  - SPICE model with verified accuracy > 3 GHz
  - Evaluation of insertion and return loss

Synergetix Characterization Method

- Define specific return path configurations
- Measure fixture, fixture & socket, open/short
- Build SPICE model, fit to measurement, verify against measurement
- Interpret socket performance from the model

Elements of Synergetix System

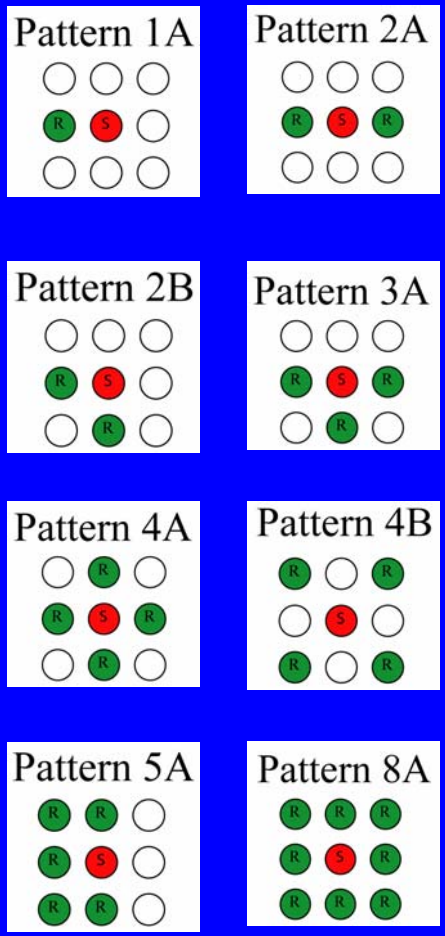


- Agilent E8363B VNA
- Megaphase high bandwidth cables
- ggb industries pico probes
- Synergetix custom test board
- Synergetix custom rf test socket

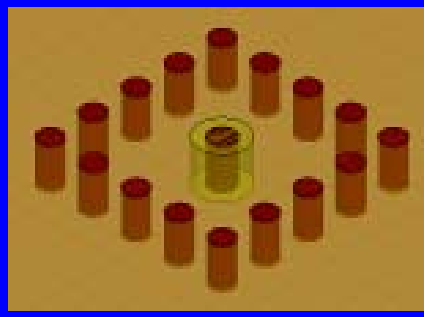
Secrets……Revealed!

1. Define specific return path pins
2. Simple fixture board
3. 2 port VNA for low Z
4. GSG probes to minimize common currents
5. Mode suppression pins to minimize socket resonances
6. Agilent ADS to build and optimize models to measurements
7. Model includes real losses (though tiny)
8. Comparison of T line and lumped models

 # 1 Return Path Patterns

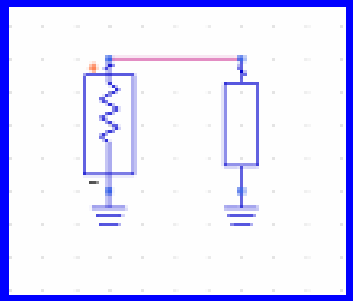


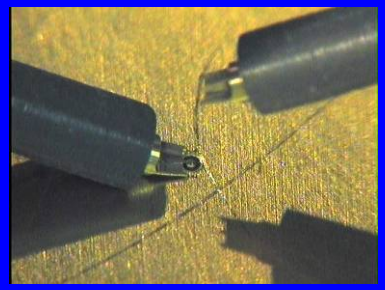
 # 2 rf Fixture Board

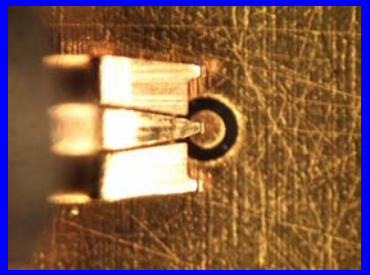


Secret #3: 2 port VNA for low Z measurement

1 port measurement of impedance



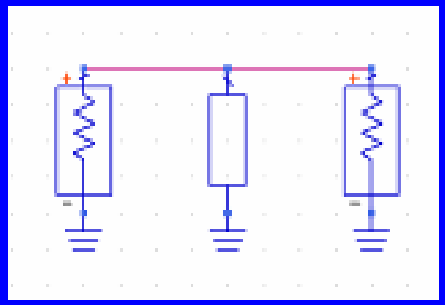


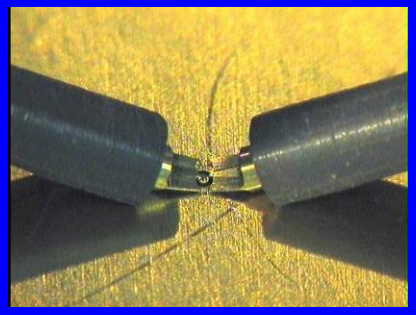


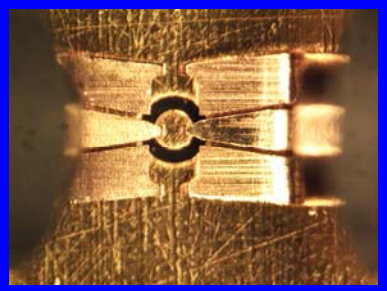
$$Z = 50\Omega \frac{1+S_{11}}{1-S_{11}}$$

Limitations: residual probe loop resistance, inductance

2 port measurement of impedance





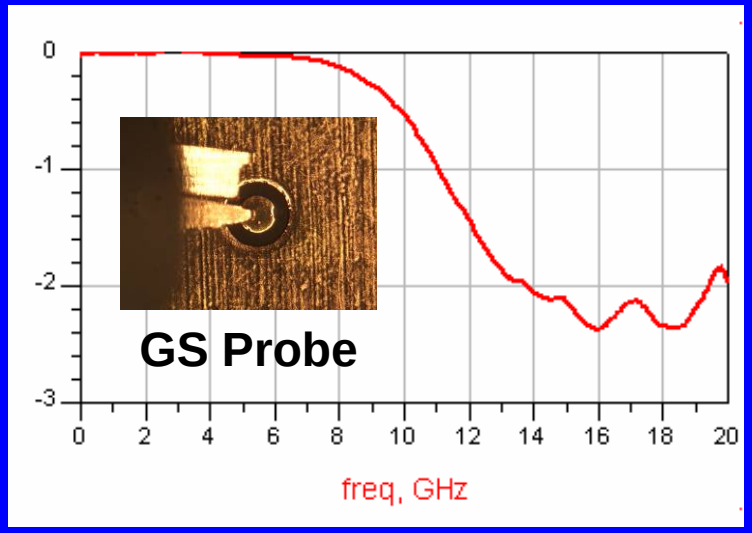


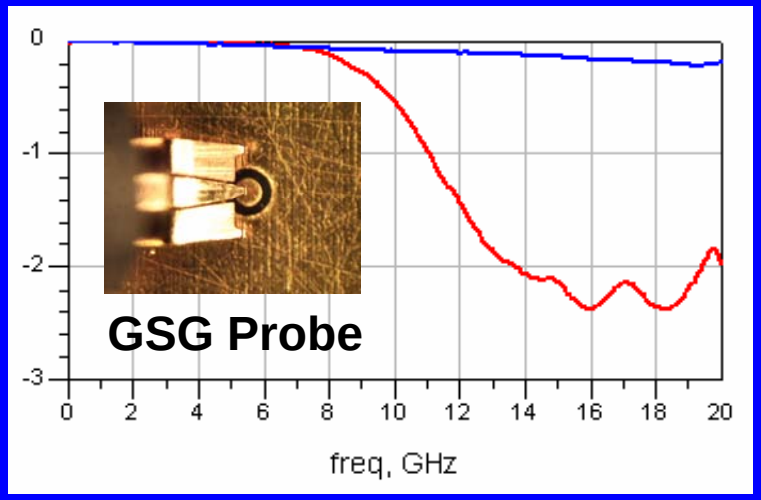
$$Z \sim 25\Omega \; x \; S_{21}$$

Capabilities of process: reproducible 1 mOhm, 1 pH

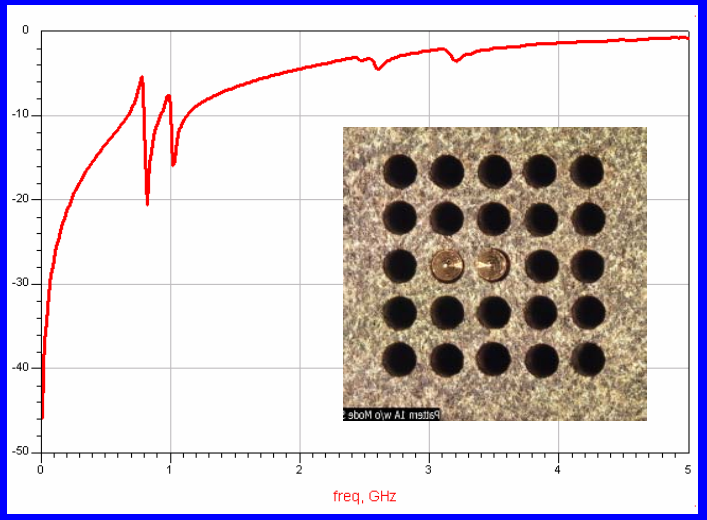
Secret #4, #5: Minimize Two Artifacts: common currents, mode suppression

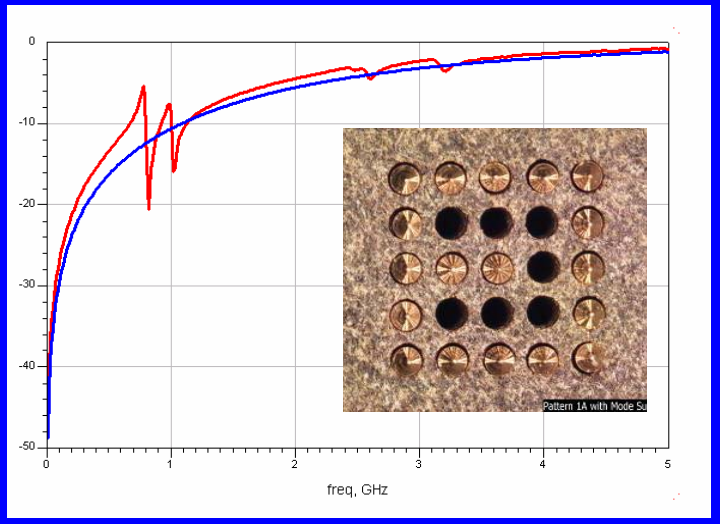
Fixture Open Termination





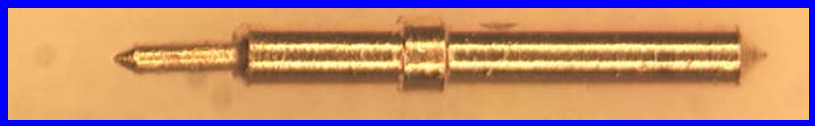
Socket Short Termination



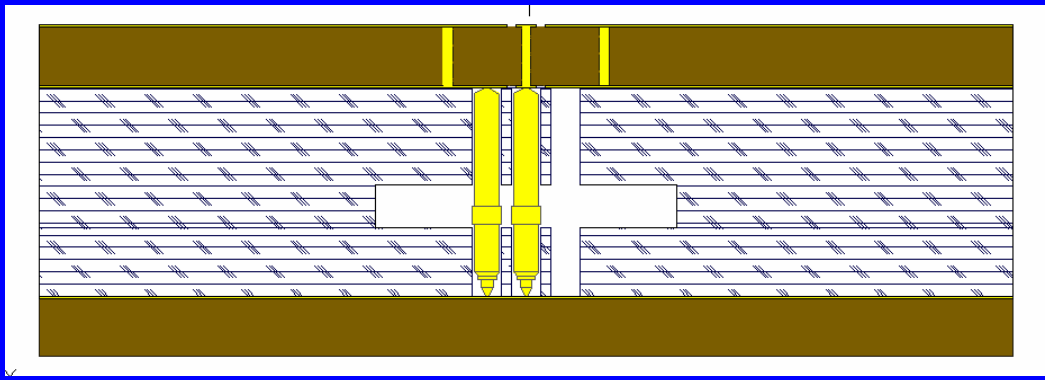


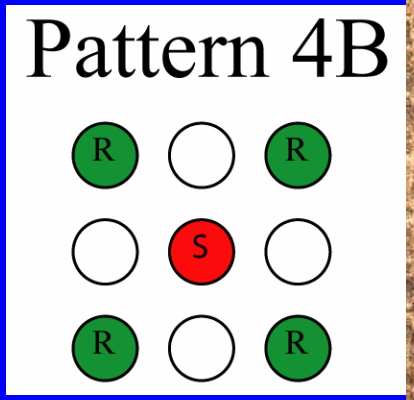
Synergetix 0.5 mm pitch Test Socket

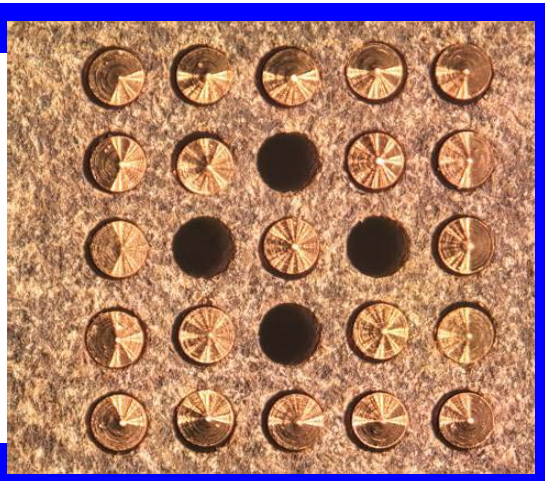
Synergetix 101267 probe



Cross section of rf test socket and fixture

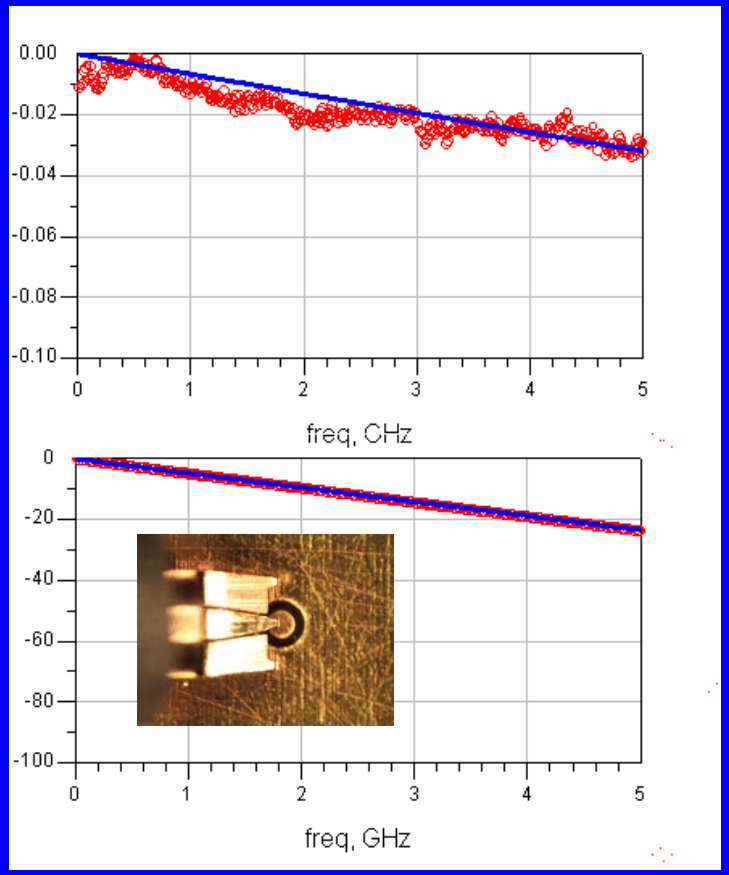




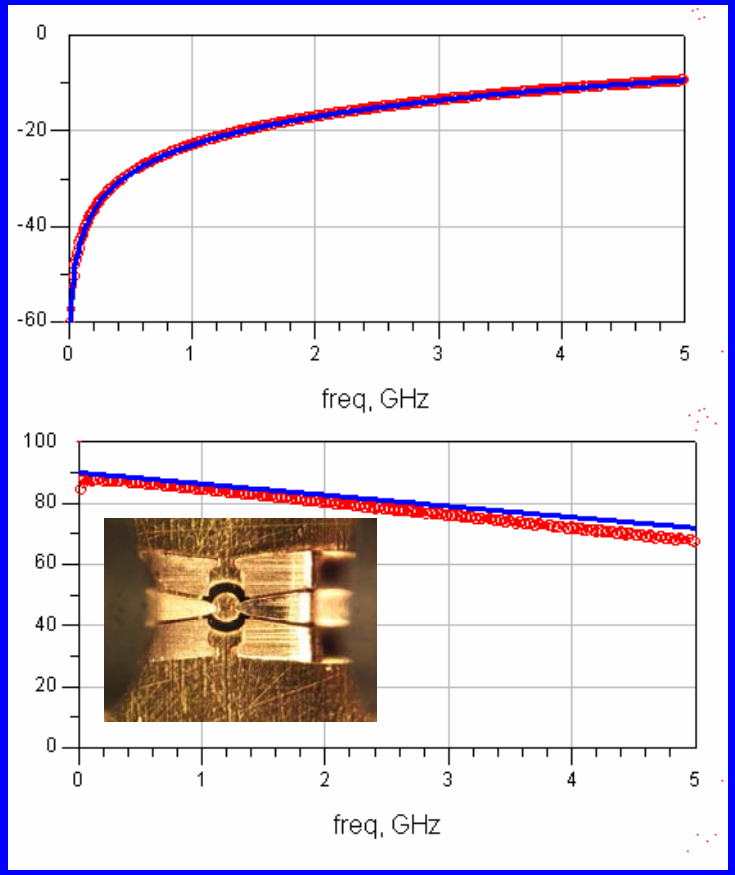


Secret #6: Build Model with ADS and Optimize to measurements: fixture only

Open termination

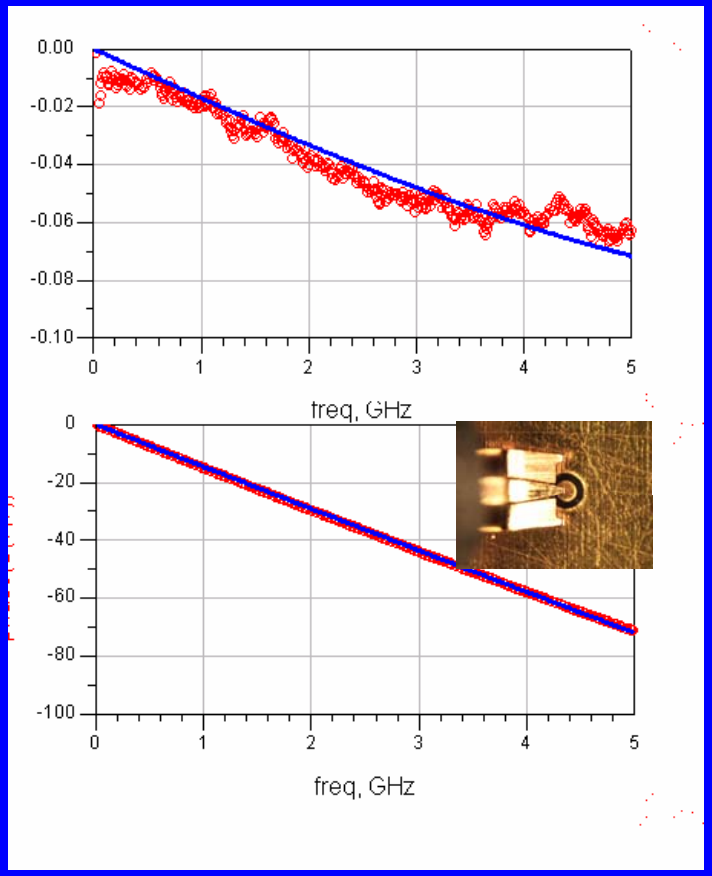


Short termination

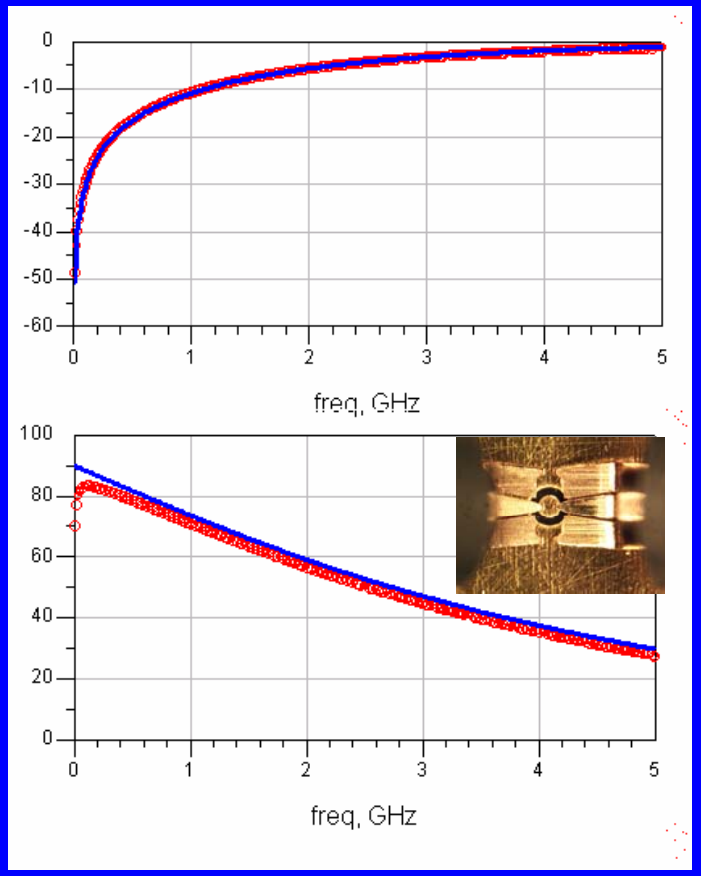


Secret #6: Build Model with ADS and Optimize to measurements: fixture & socket

Open termination

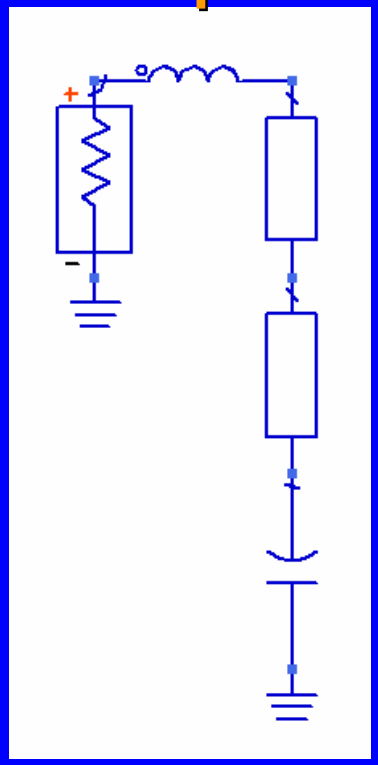


Short termination

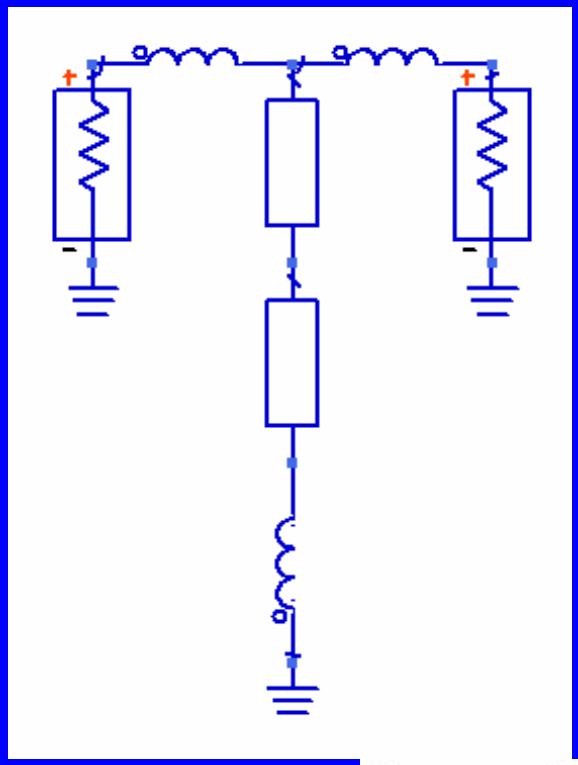


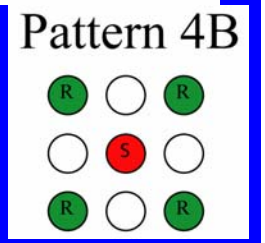
Secret #6, #7: Simple High Bandwidth Model Using Ideal Lossy Transmission Lines

Fixture & socket open



Fixture & socket short





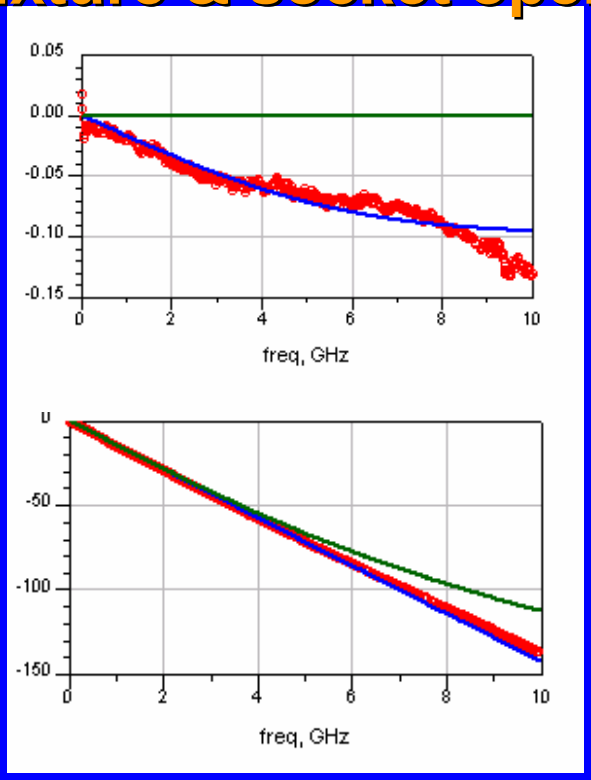
- Elements:
  - Residual probe inductance
  - Ideal lossy T line model of fixture
  - Ideal lossy T line model of socket pins
  - C of socket open
  - L of socket short

Parameters	Fixture	Socket
Z_0 (Ohms)	45	58
TD (psec)	4.4	16
tan(δ)	0.01	0.007

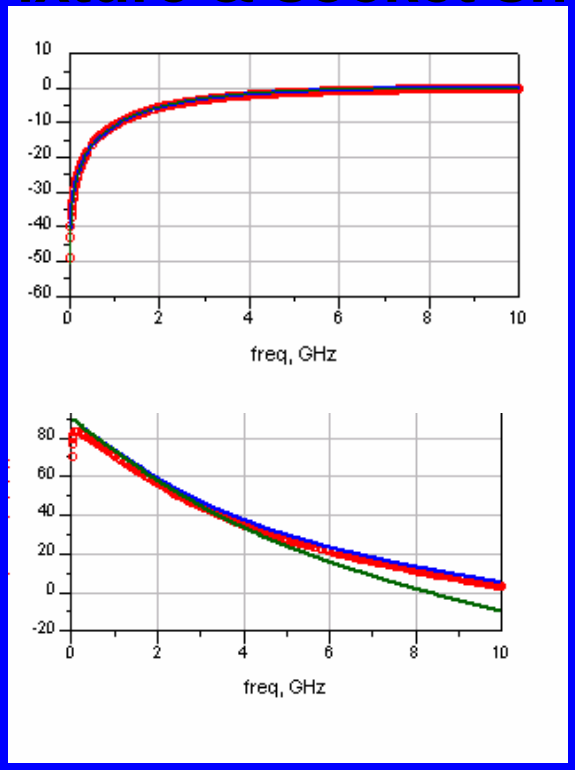
Secret #7: Single Section Lumped Circuit Model has limited bandwidth

Simple rule of thumb: $$BW \sim \frac{1}{10}\ x\ \frac{1}{TD} \sim \frac{1}{200\,p\,\mathrm{sec}} \sim 5\,GHz$$

Fixture & socket open

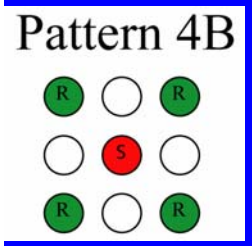


Fixture & socket short

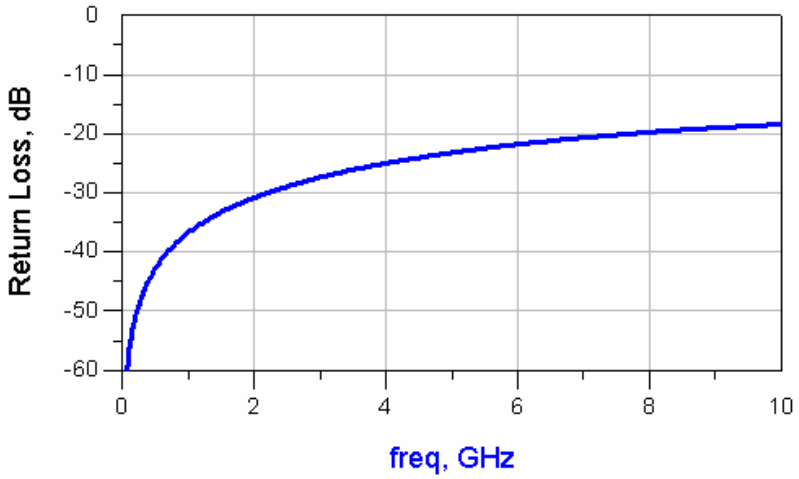


BW of T line model ~ 10 GHz
BW of LC model ~ 5 GHz

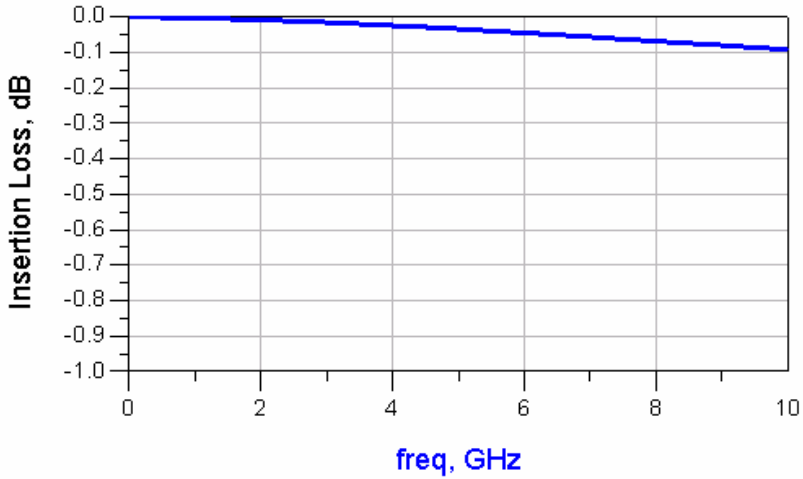
Simulated Insertion and Return Loss of just the Socket Model, de-embedded from the fixturing



Return Loss



Insertion Loss



Conclusions

- Synergetix Characterization Method is:
  - Simple, robust, reproducible
  - Non-proprietary
  - Accurate to > 5 GHz
  - Minimal and controllable artifacts
  - Output is SPICE compatible model
  - Direct measurement of model bandwidth
  - Accurate simulation of insertion loss
  - Extendable to differential impedance characterization, cross talk, > 5 GHz bandwidth
  - GigaTest Labs will offer Synergetix characterization method as a service

3D AC Simulation of Inter-Connector

Jiachun Zhou (Frank), presenter
Uyen Nguyen, presenter
Praba Prabakaran

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Hayward, CA 94545
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BiTS
BURN-IN & TEST SOCKET WORKSHOP

Overview

Introduction & Objective

Methodology

Simulation Validation

Applications and Results

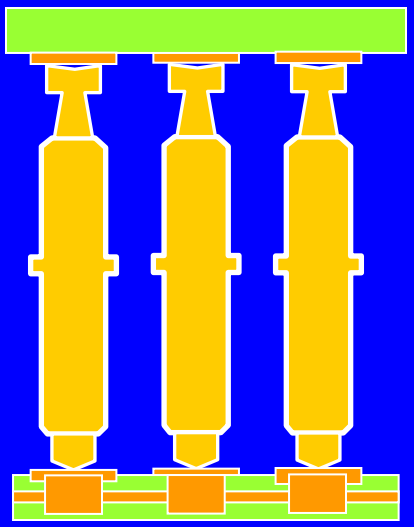
Summary

Introduction

Inter-connector

Testing at high frequency what is:

- **Inductance**
- **Capacitance**
- **Bandwidth**
- **Cross talk**



Technical Challenges in determining AC Performance

- How to determine AC performance in contactor design
- Measurement has high cost and not feasible for different sockets
- Theoretical calculation needs assumptions and is at acceptable accuracy level.

Objectives

Investigate the feasibility and reliability of employing 3-D HF electromagnetic simulation model/software.

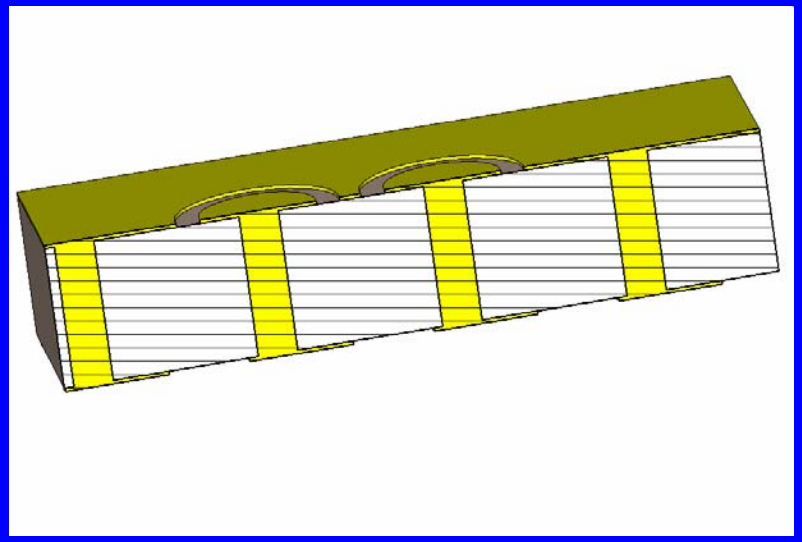
Methodology

- Use CST Microware Studio to perform all electromagnetic simulations
- Verification of simulation results on PCB and inter-connectors with measurements
- Investigate AC performance of inter-connector when varying its dimensions, material and other parameters using electromagnetic simulator

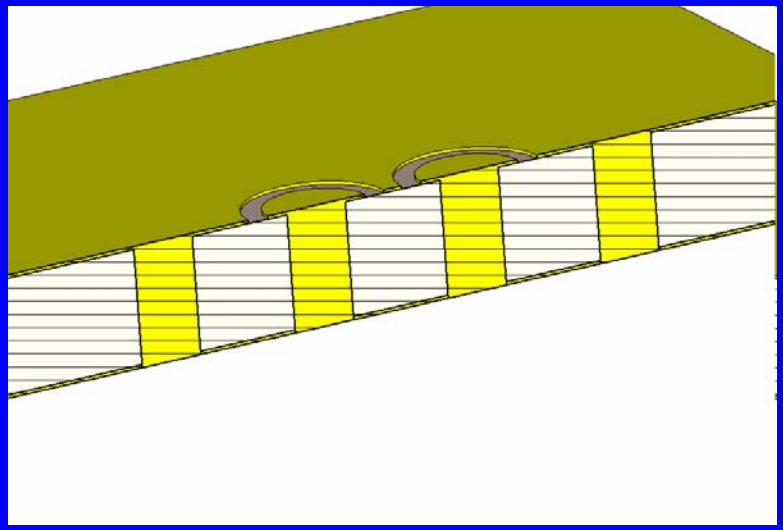
Calibration

Use Open Calibration Board and Short Calibration Board to verify simulation results with measurements.

Open Calibration Board

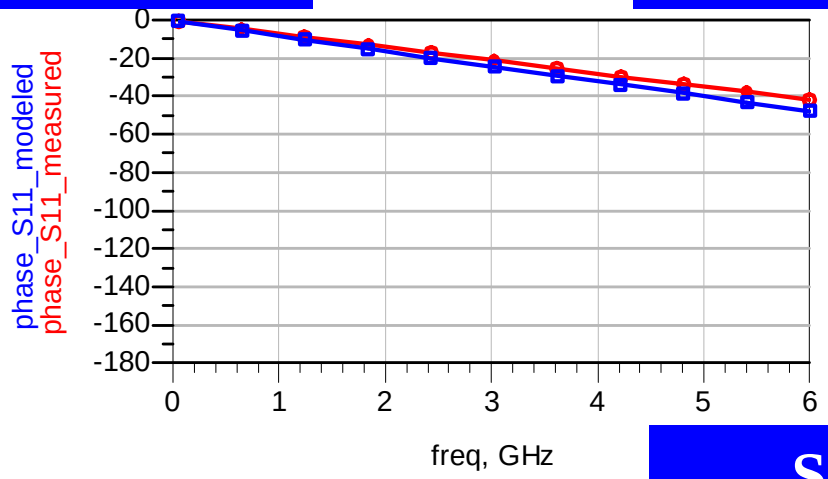


Short Calibration Board



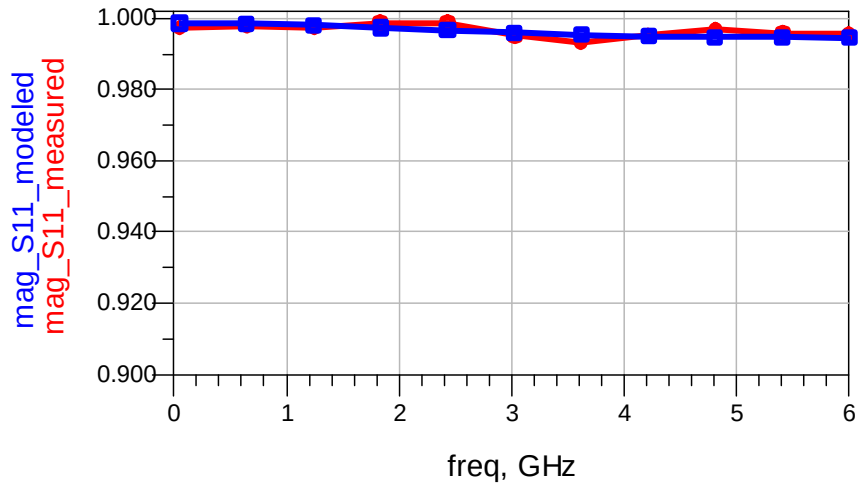
Verification – Modeled vs Measured

S11 Phase



Open Calibration Board

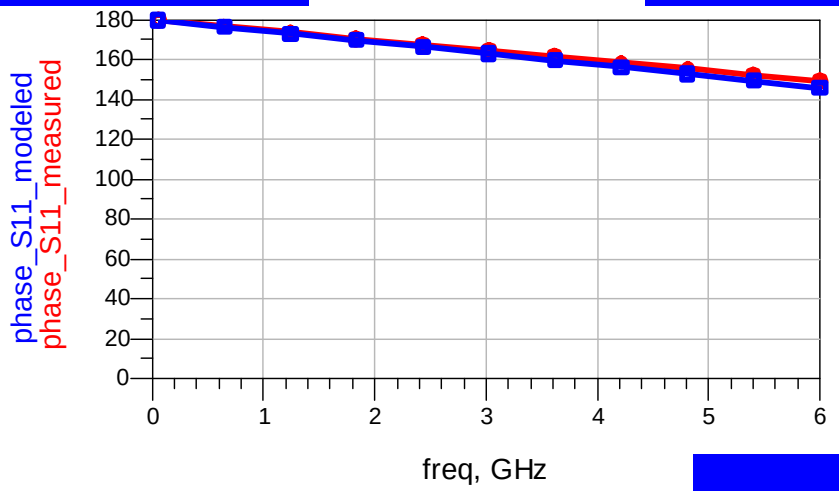
S11 Magnitude



Measured (red)
Modeled (blue)

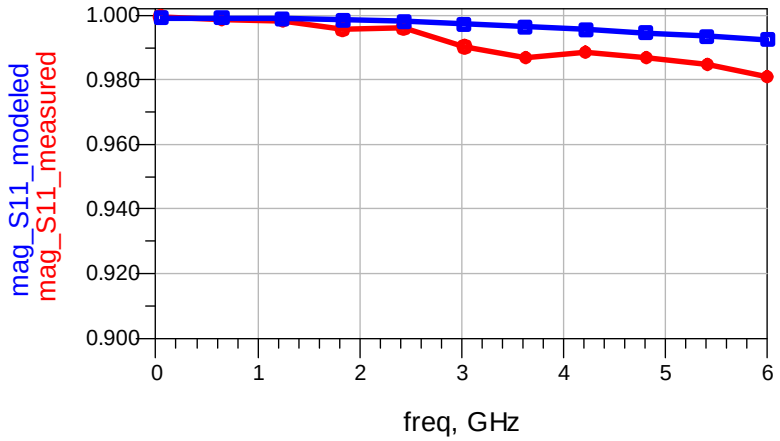
Verification – Modeled vs Measured

S11 Phase



Short Calibration Board

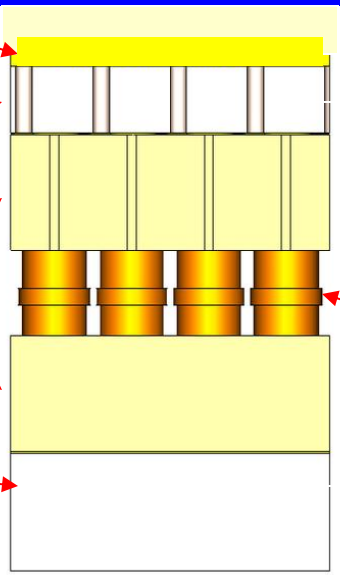
S11 Magnitude



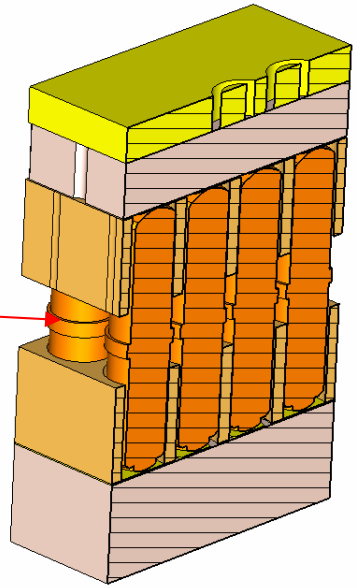
Measured (red)
Modeled (blue)

Spring Probe Contactor – Model

Fixture Side View

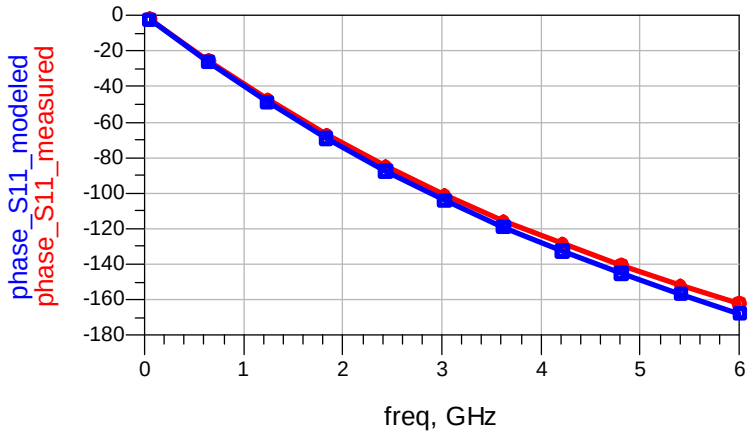


Fixture Cross Section



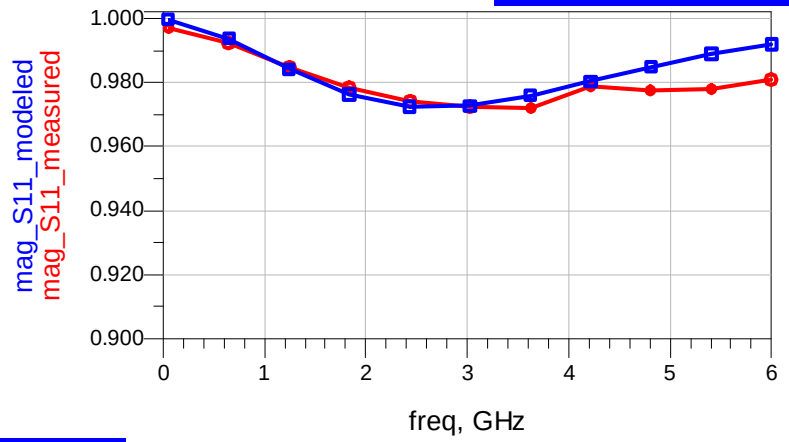
Spring Probe Contactor – Open

Phase

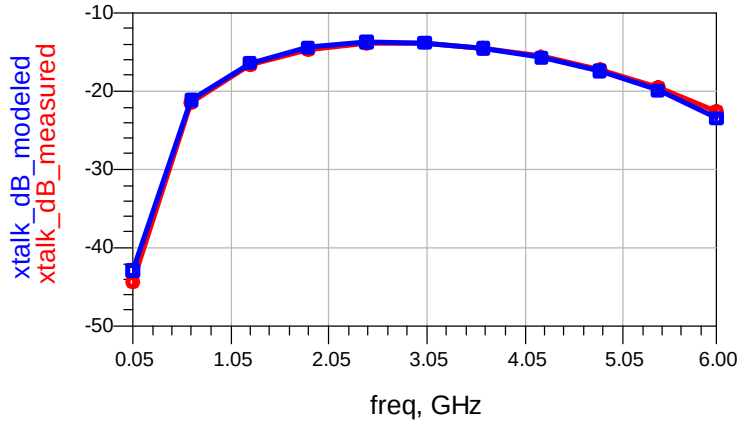


S11

Magnitude



Cross Talk

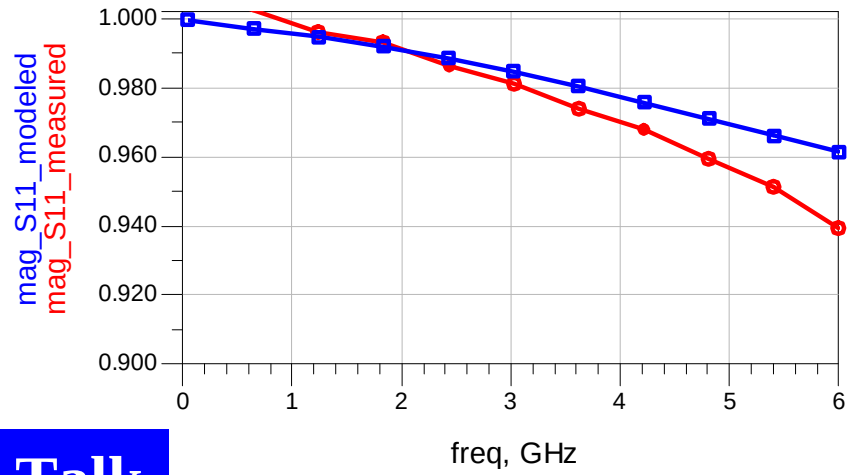


Measured (red)
Modeled (blue)

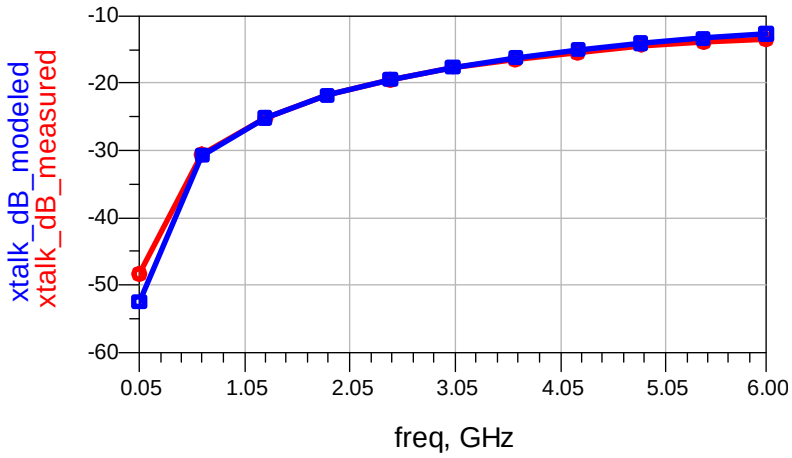
Spring Probe Contactor – Short

Phase

S11 Magnitude



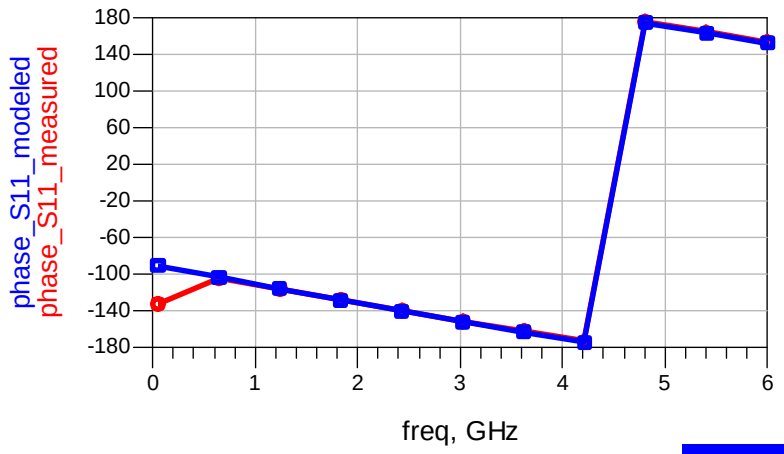
Cross Talk



Measured (red)
Modeled (blue)

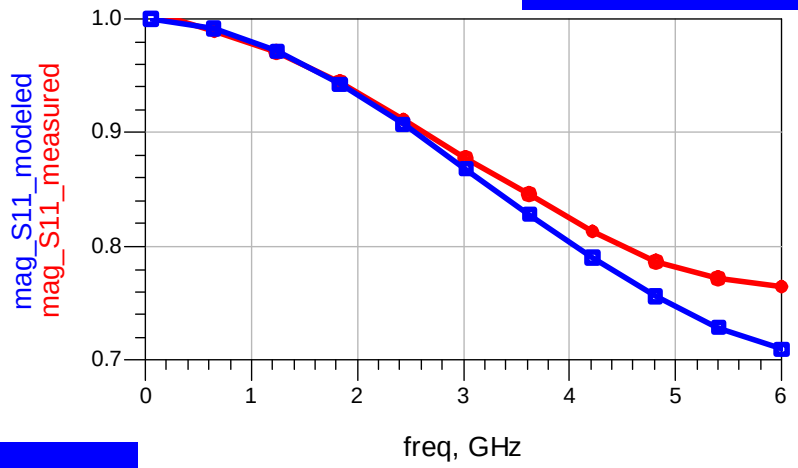
Spring Probe Contactor – Through

Phase

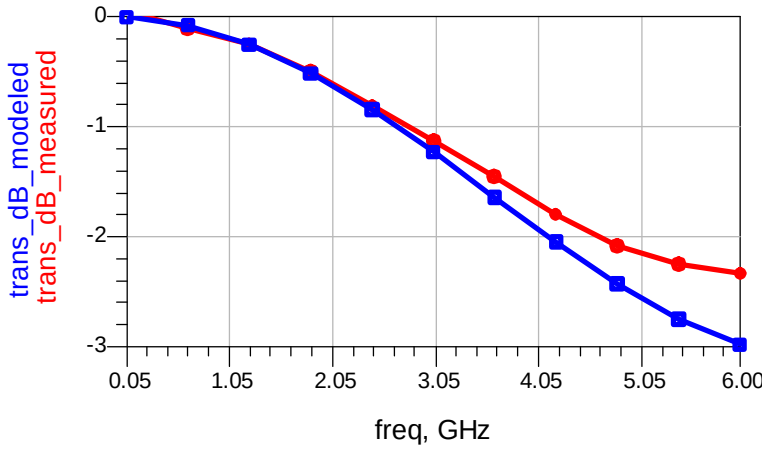


S11

Magnitude



Cross Talk



Measured (red)
Modeled (blue)

Verification Summary

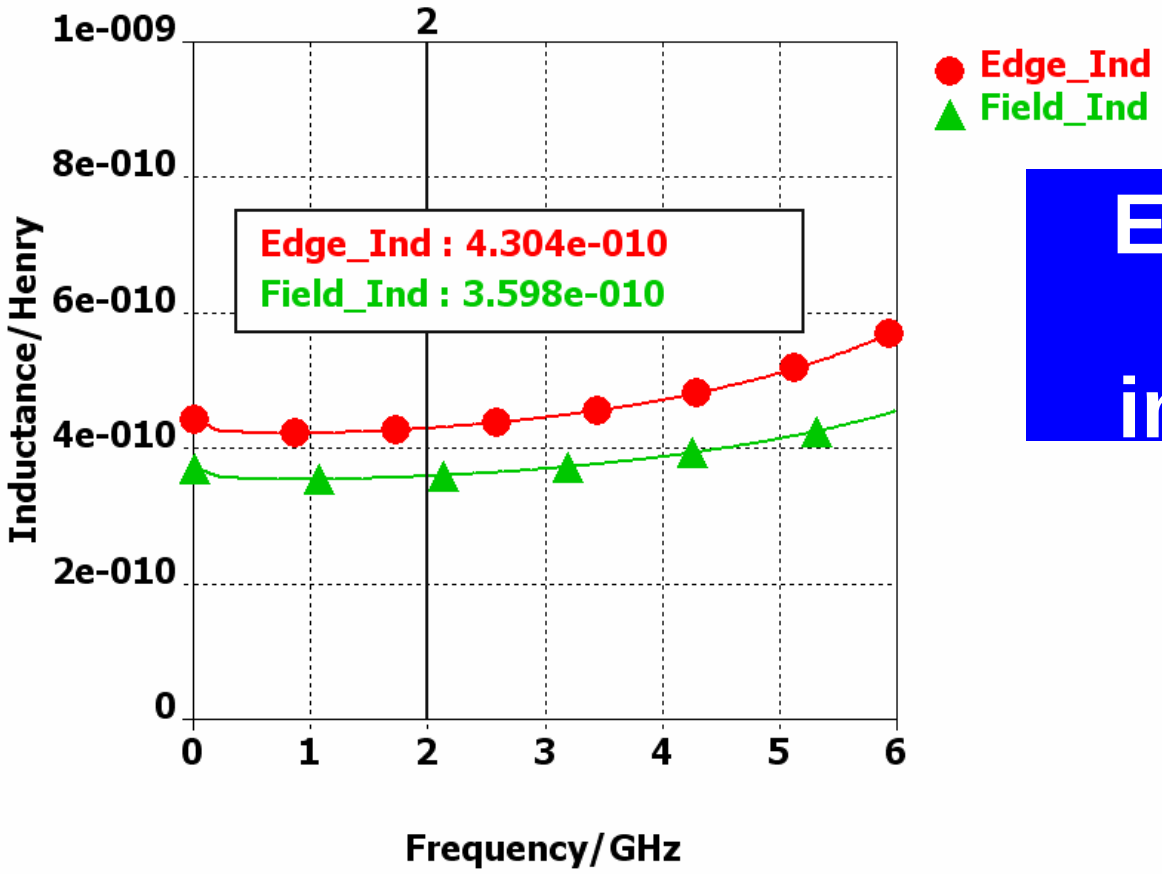
All simulations agree well with Measurements.

Simulations vs measurements: < 10% differences.

As frequency increases, this difference increases.
All data fit well when 0.5 ~ 6 GHz.

Applications – Field vs. Edge

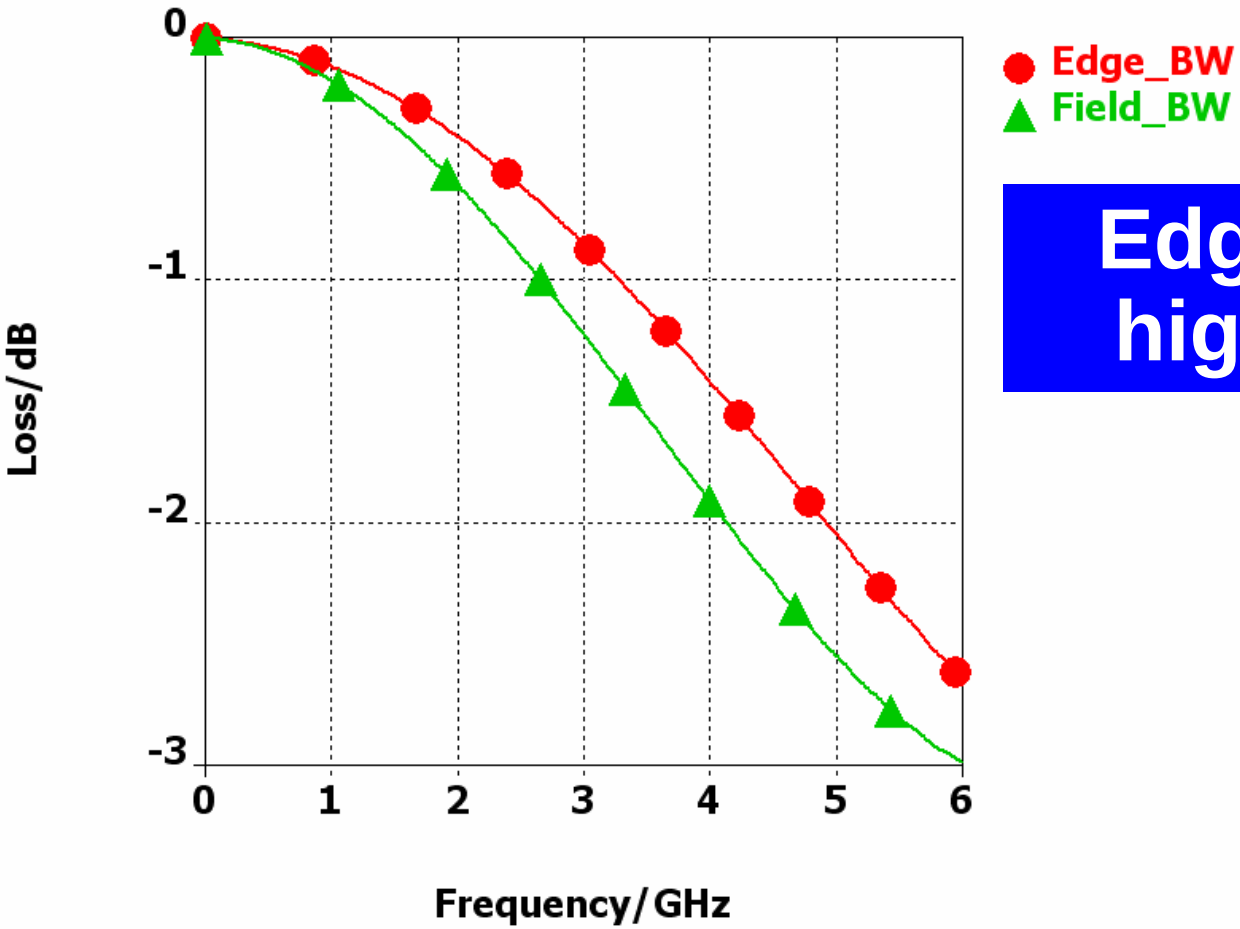
Field vs Edge Adjacent Inductance



Edge pin-higher inductance

Applications – Field vs. Edge

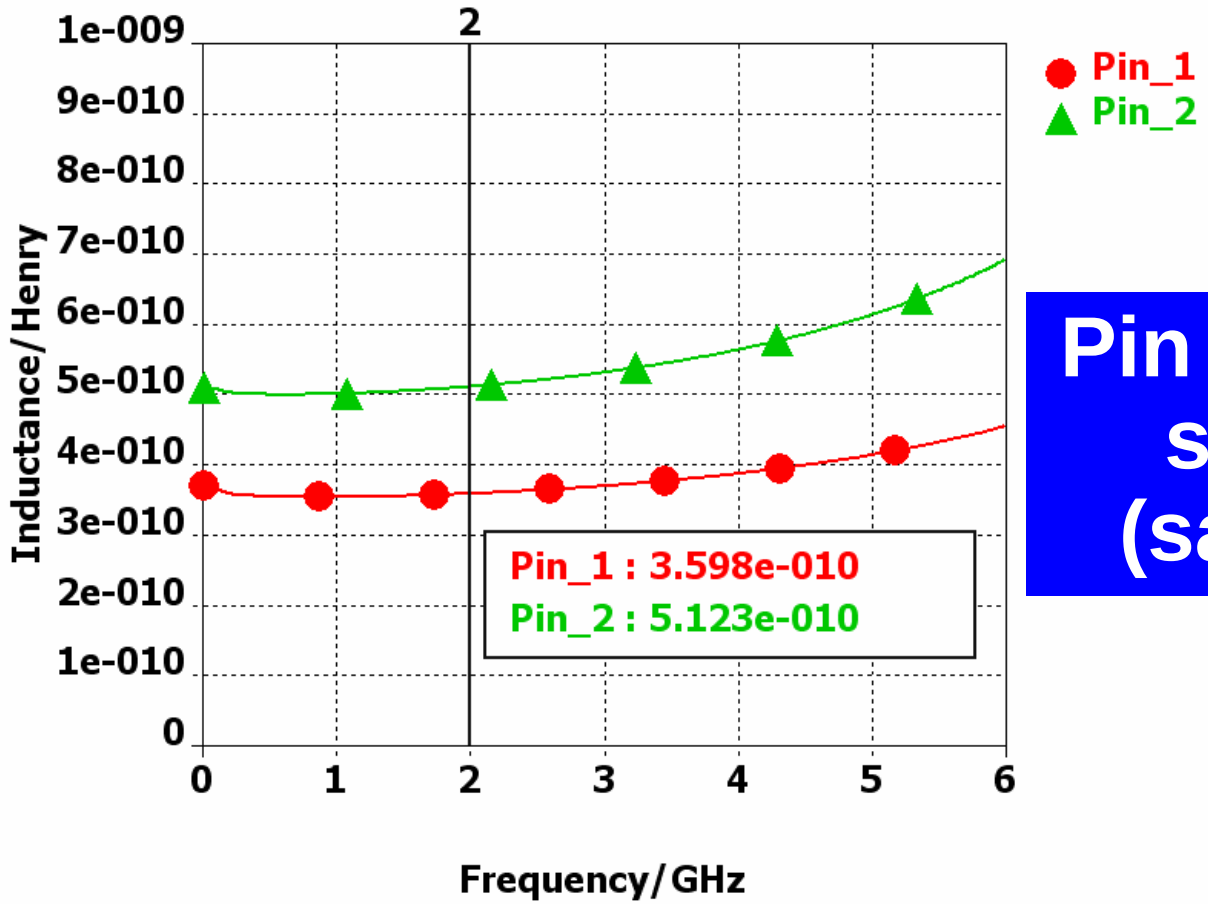
Field vs Edge Adjacent BW



Edge pin-higher BW

Applications – Pin 1 vs. Pin 2

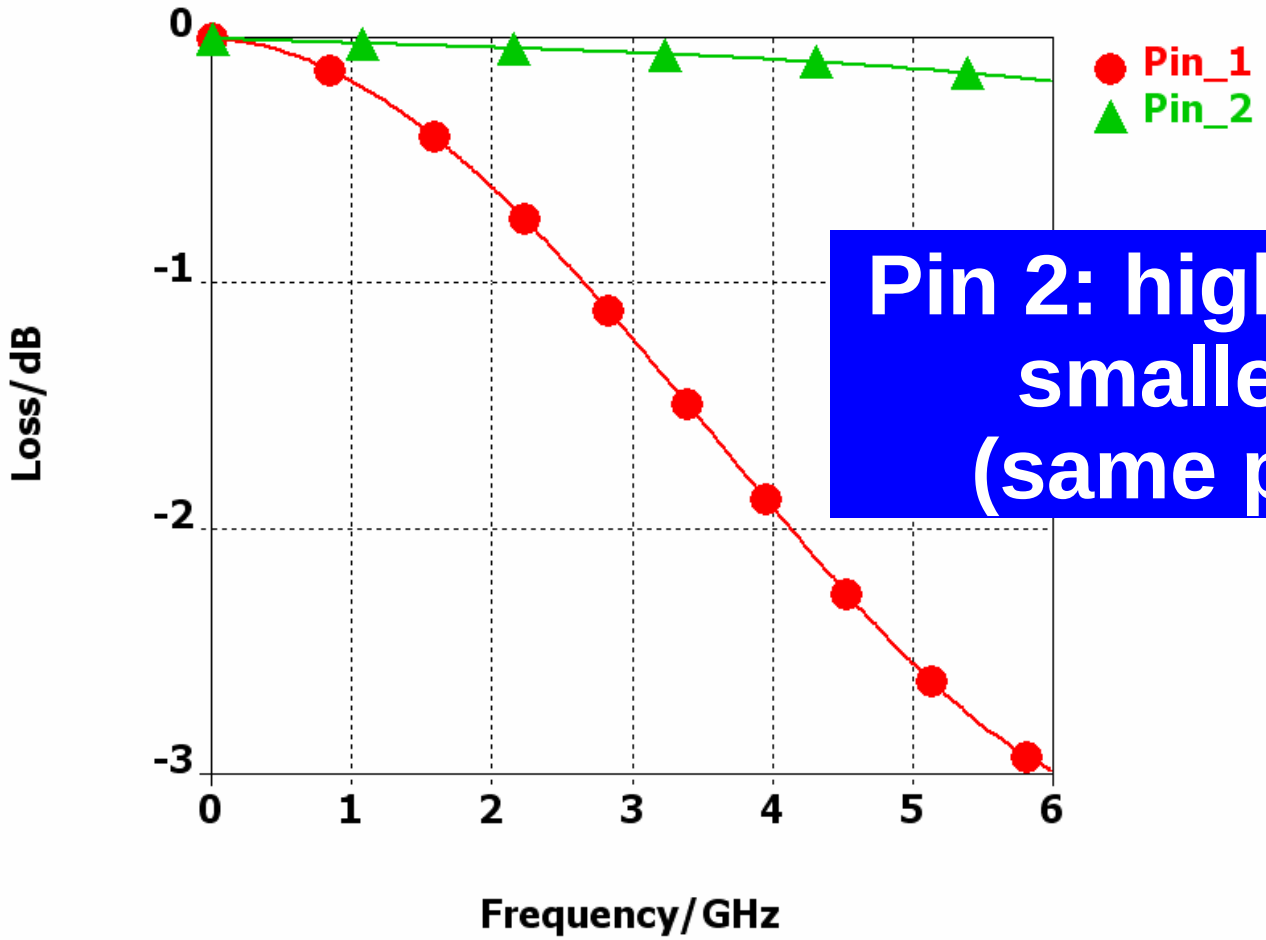
Pin 1 vs Pin 2, Adjacent Inductance



Pin 2: higher L; smaller size (same pitch)

Applications – Pin 1 vs. Pin 2

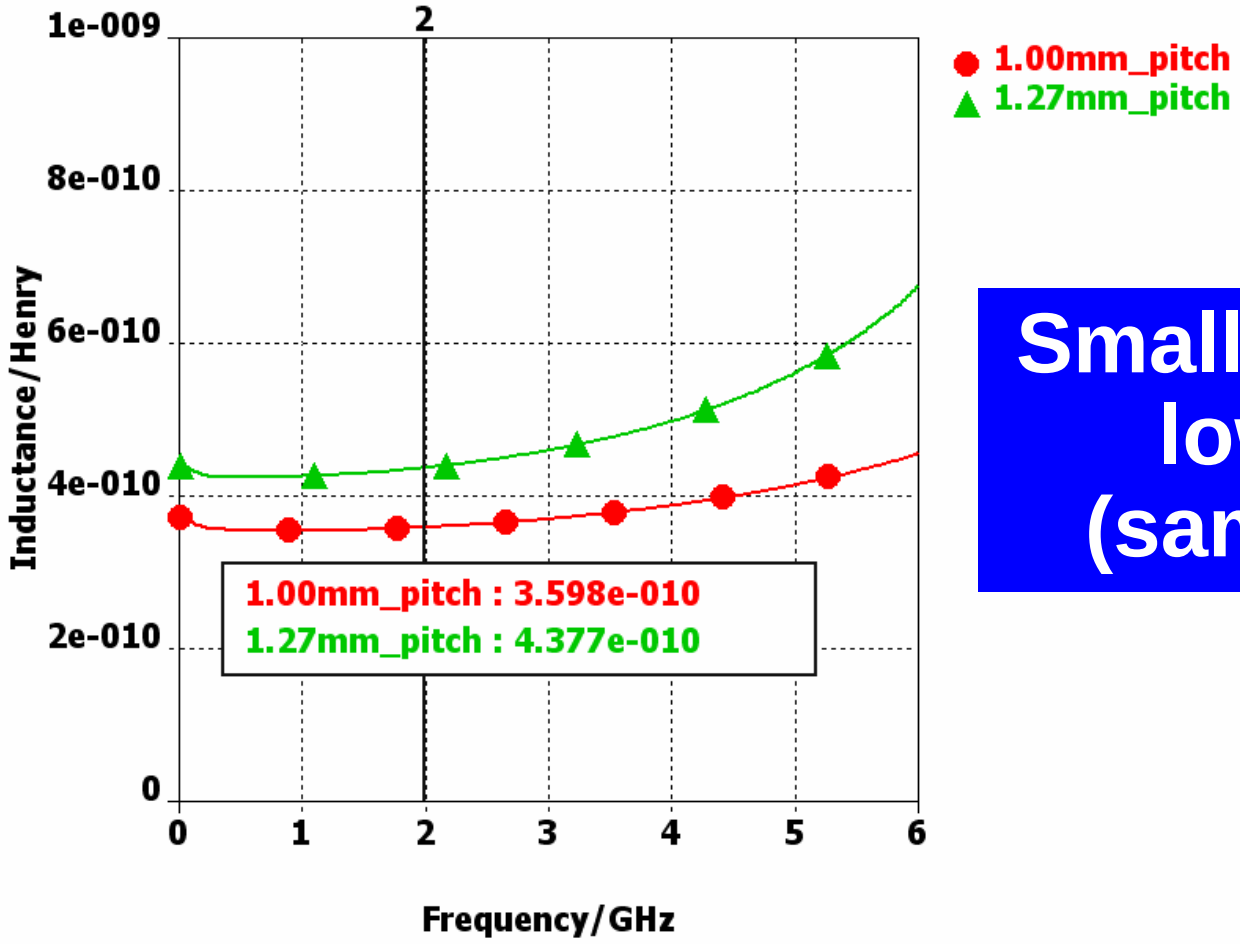
Pin 1 vs Pin 2, Adjacent Inductance



Pin 2: higher BW; smaller size (same pitch)

Applications – 1.0mm vs 1.27mm Pitch

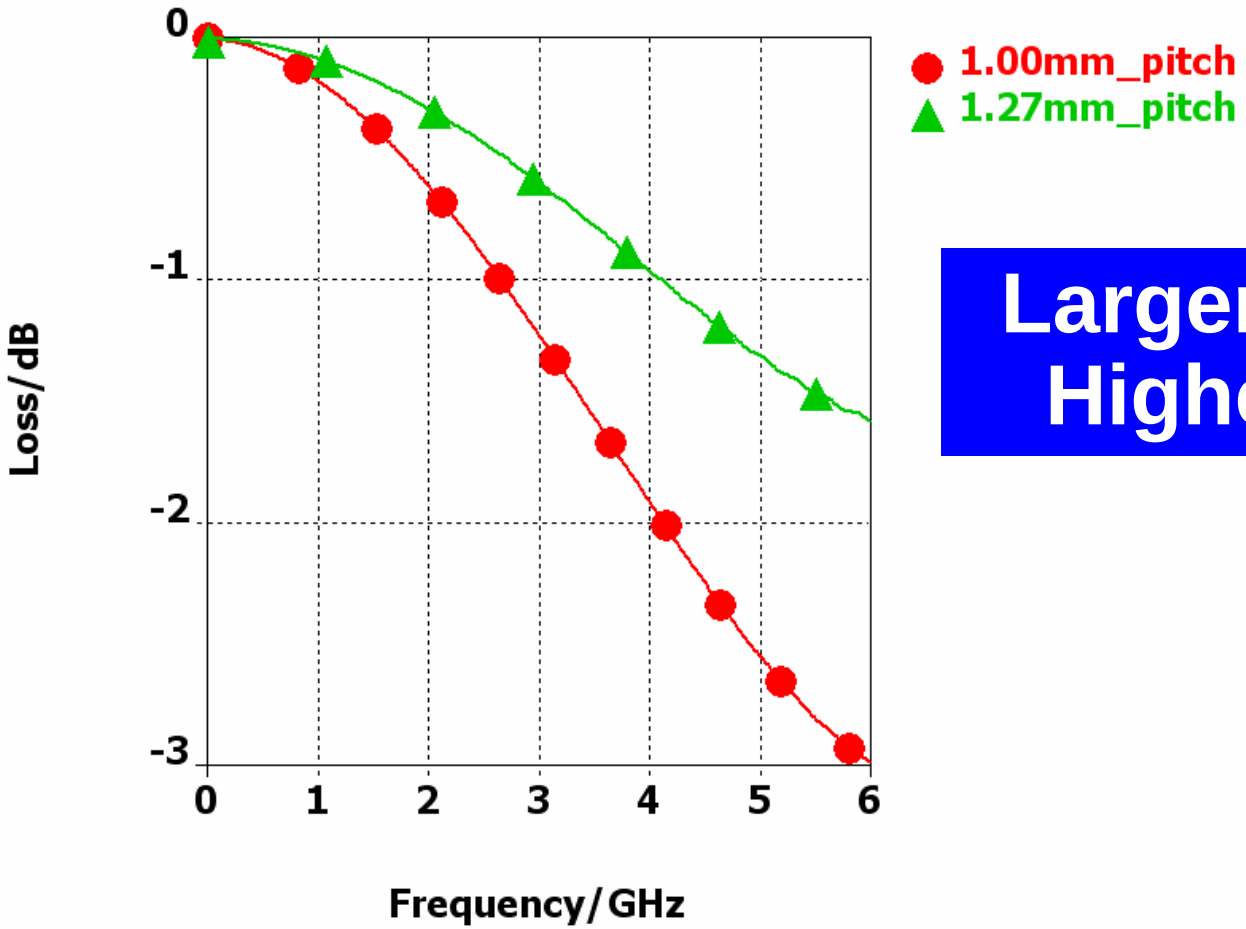
1.0 vs 1.27mm Pitch, Inductance



Smaller pitch; lower nL (same pin)

Applications – 1.0mm vs 1.27mm Pitch

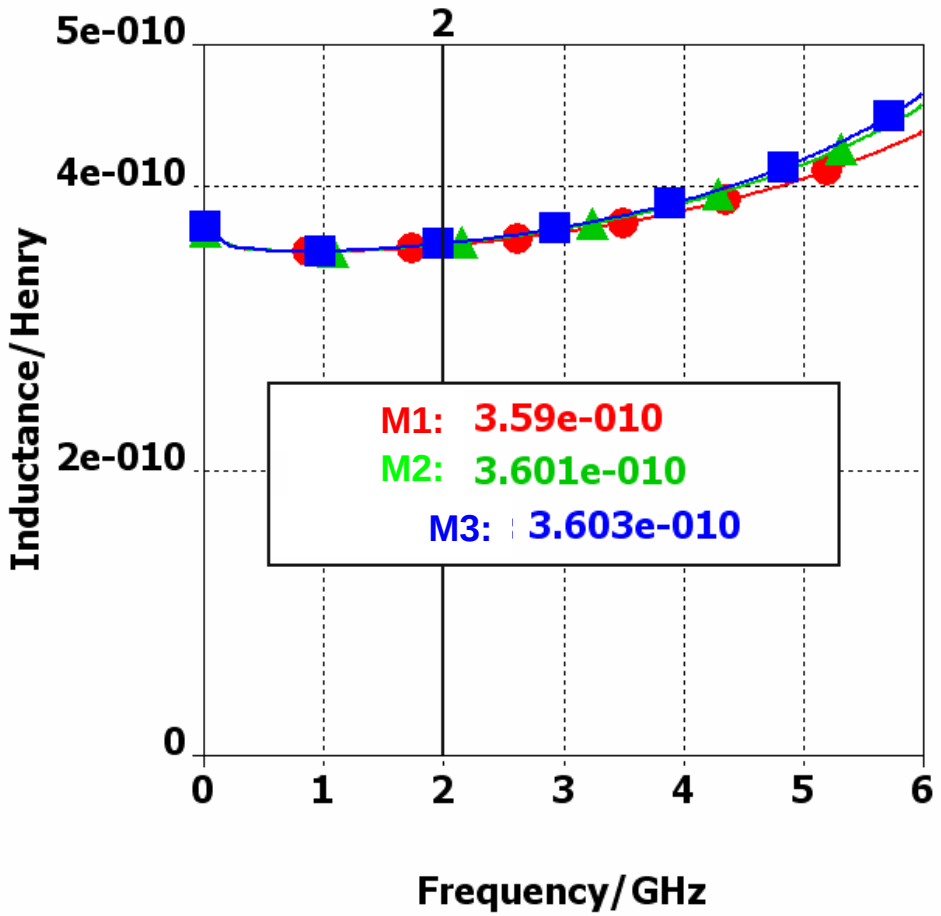
1.0 vs 1.27mm Pitch, BW



Larger pitch; Higher BW

Applications – Socket Material

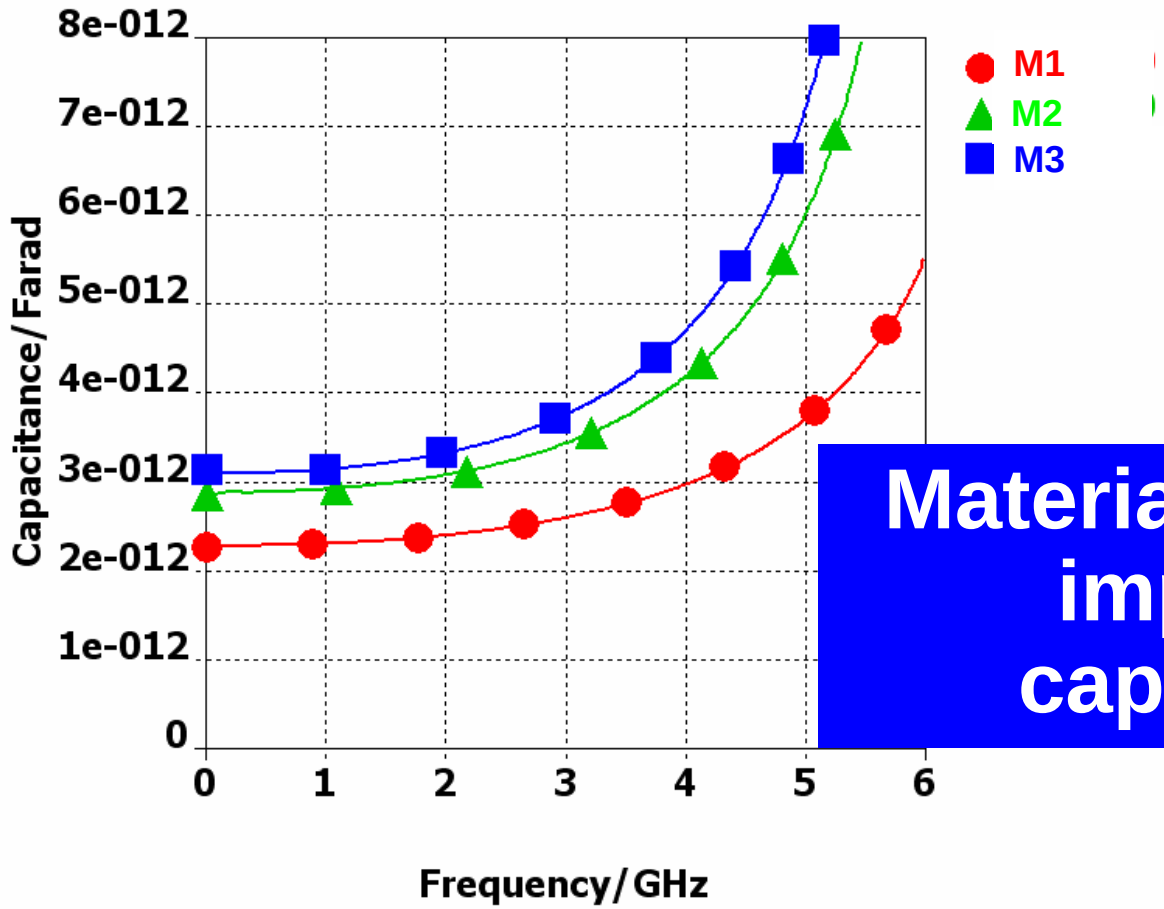
3 Material Inductance (same pin)



Material: little impact on Inductance

Applications – Socket Material

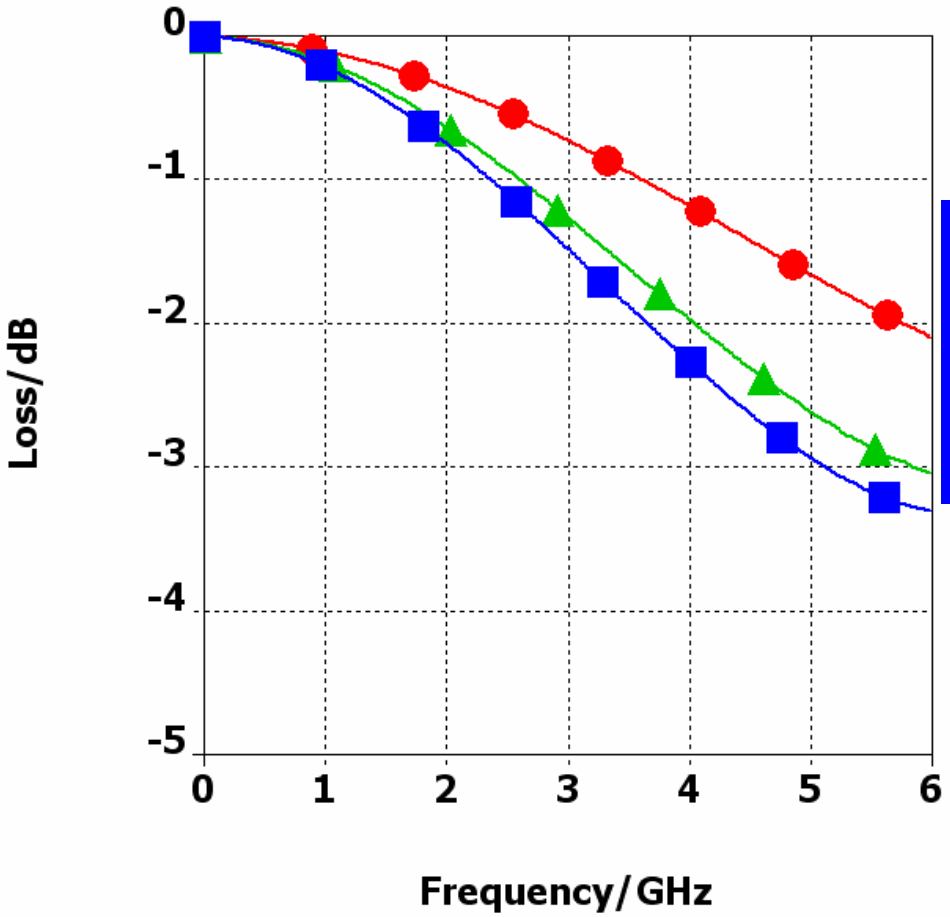
3 Material Capacitance (same pin)



Material: obvious impact on capacitance

Applications – Socket Material

3 Material Bandwidth (same pin)



Material: greater difference at higher frequency

Summary

3D electromagnetic simulation models and software become suitable tools for socket/pin design.

Technical barrier of using simulation is the verification of its accuracy due to technical limitation on measurements.

Applications of this model has provided more understandings of factors that impact AC performance of socket/pin system.

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High Frequency Signal Integrity Issues in Semiconductor Test

Ryan Satrom
RF Engineer, ECT-MN
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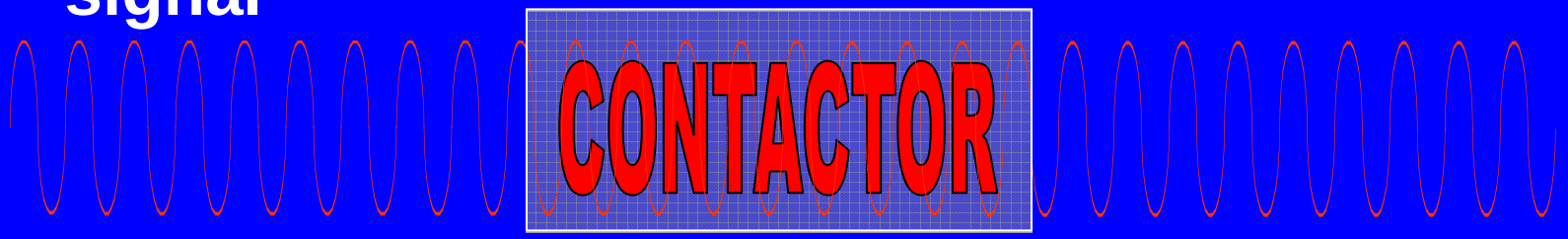
EVERETT CHARLES TECHNOLOGIES
Testing the Limits

BiTS
BURN-IN & TEST SOCKET WORKSHOP

High Speed Challenges

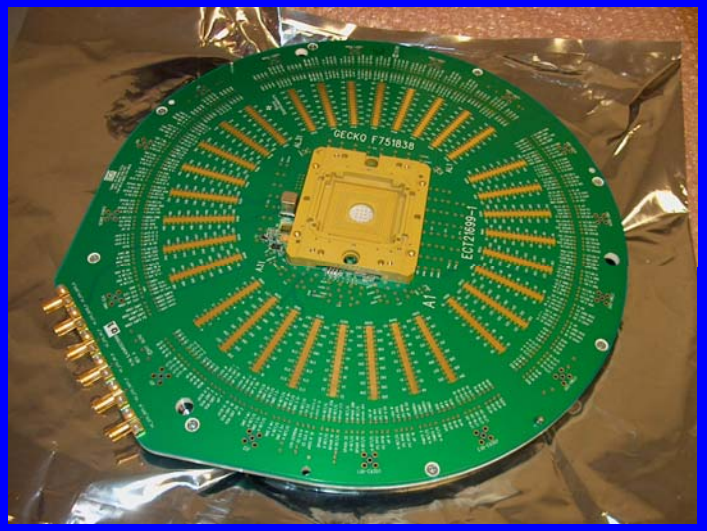
- At high frequencies, characteristic impedance must be matched for clean transmission of signal



- Transmission line theory must be understood and properly used to achieve good signal integrity
- The techniques outlined in this presentation can be applied to all transmission line models

The Transmission Path

- **Signal: Tester cables - to - Loadboard - to - contactor - to - DUT. This presentation will focus on the Loadboard-Contactor section.**
- **Each transition may create reflections and further degrade the signal quality.**



The Transmission Path

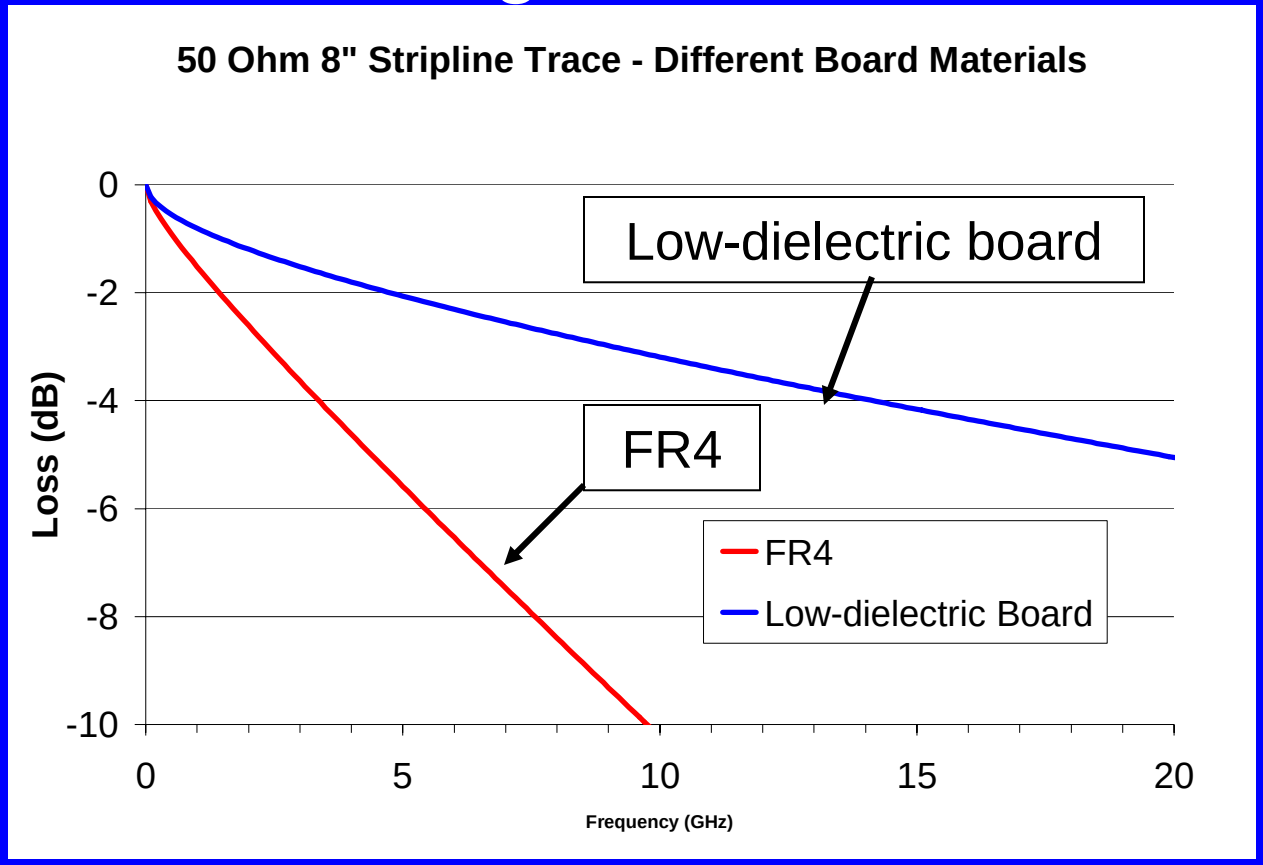
- **Goal: Create an electrically transparent interconnect between tester and DUT to optimize integrity of each signal to achieve $V_{INPUT\text{-}DUT} = V_{OUTPUT\text{-}TESTER}$**
- **In the real world, there will always be some signal loss and distortion.**
- **Main causes:**
  - **Conductor loss, Dielectric loss**
  - **Impedance discontinuities cause reflections and loss**
- **It is possible to minimize their effects in order to maximize performance.**

Transmission Path - Key Issues

- Board Material
- Trace Length
- Vias
  - Stub Length
  - Antipad size
  - Power, ground path location
- Pad Structures
- Probe Geometry

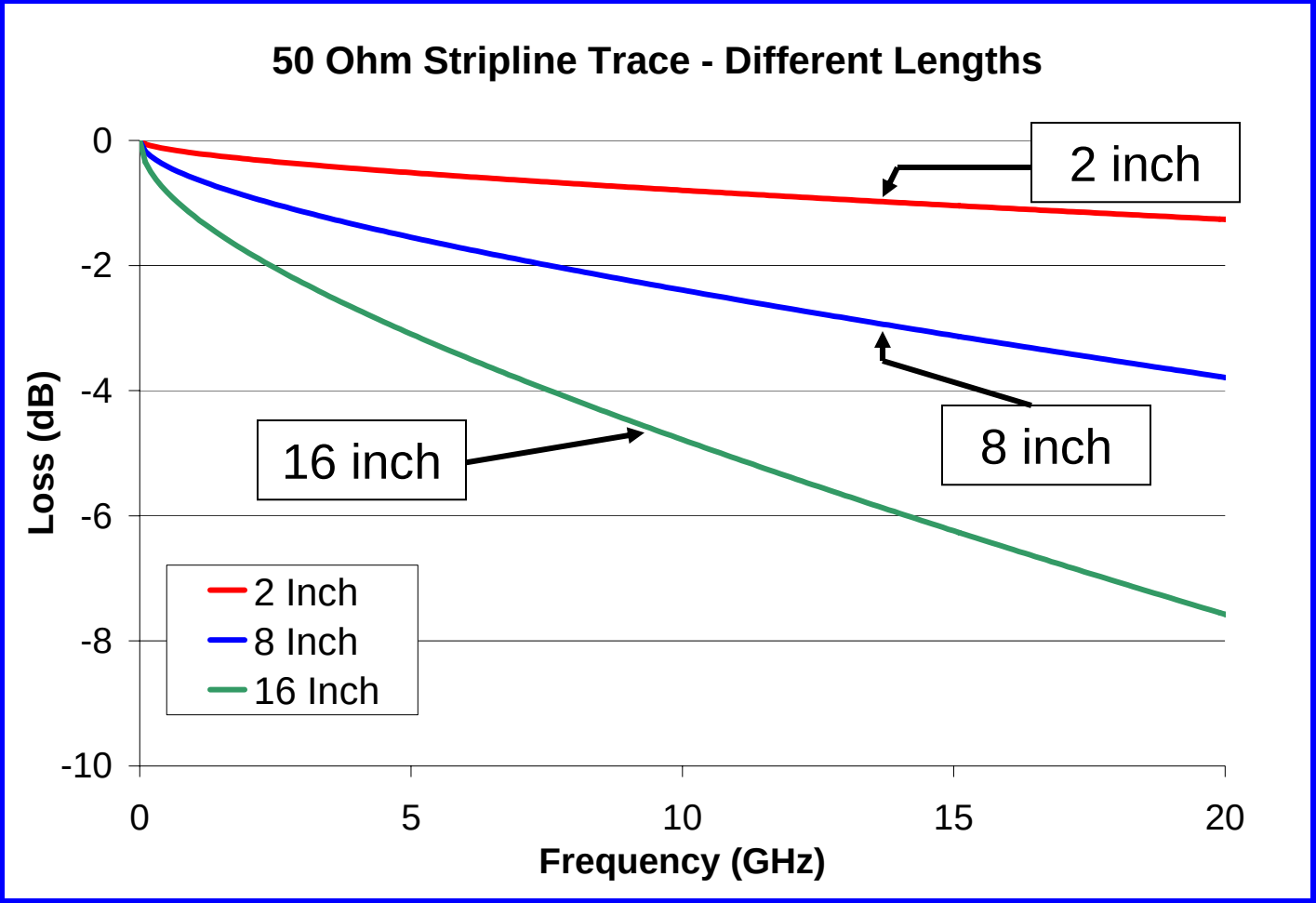
Transmission Path - Board Material

- Low-dielectric board materials are preferred for high-frequency applications. However, these laminates are more expensive and have lower routing densities



Transmission Path - Trace Length

- **Example: 2”, 8”, 16”**

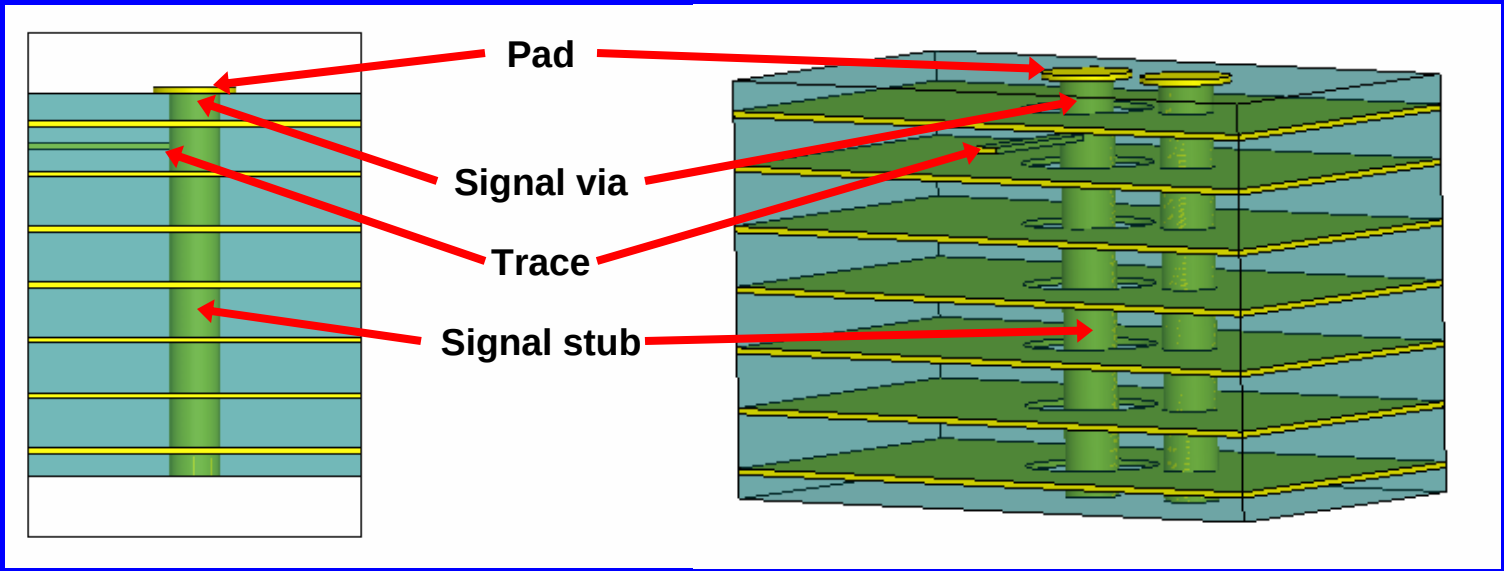


Via-Pad Structure

- The pad and the via are not independent. Changing the geometry of one will affect the electrical characteristics of the other.
- Decreasing the antipad diameter will increase the capacitance
- Increasing the diameter of the pad will increase the capacitance
- Significant source of loss, reflections, and resonances.
- However, if understood, most negative effects can be minimized.

Via-Pad Structure

- A closer look
  - Signal stub creates a capacitance to ground plane
  - Signal via causes increased inductance
  - Pad creates capacitance to ground plane
  - Creates excessive impedance mismatch



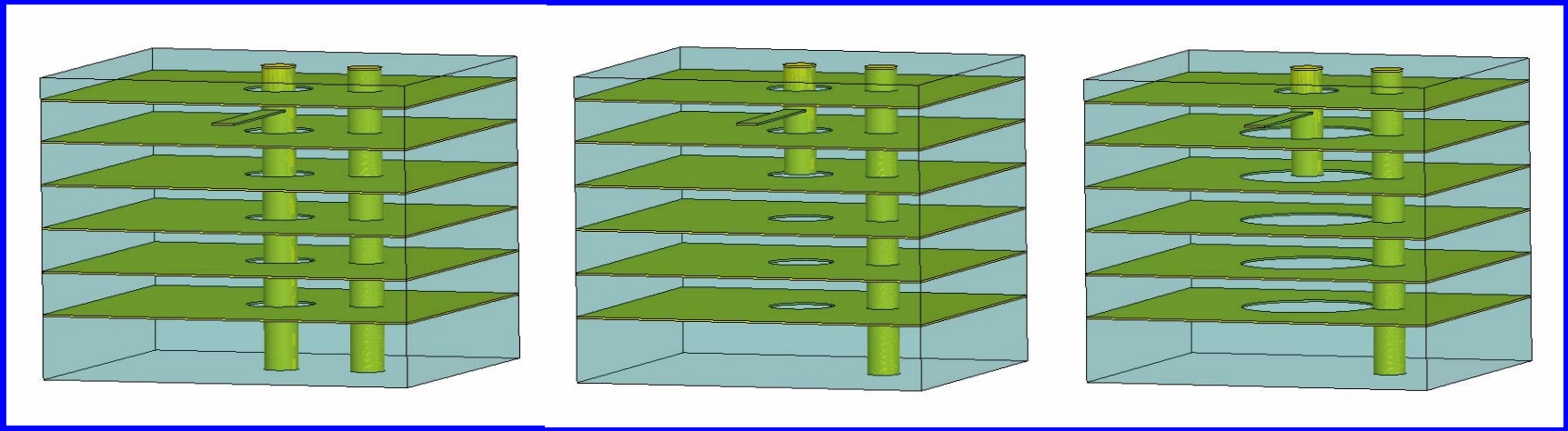
Via-Pad Structure

- **Must look at via as a transmission line, and try and match impedance to 50 ohms**
  - **Inductance is mainly a function of via length and distance to ground vias, which are both fixed.**
  - **Must modify capacitance to get characteristic impedance close to 50 ohms**
  - **To achieve optimal performance, capacitance must be distributed equally throughout via**

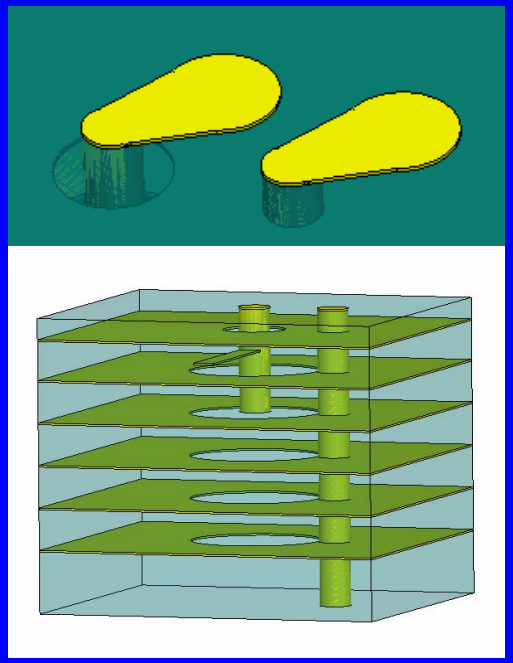
$$Z_0 = \sqrt{\frac{L}{C}}$$

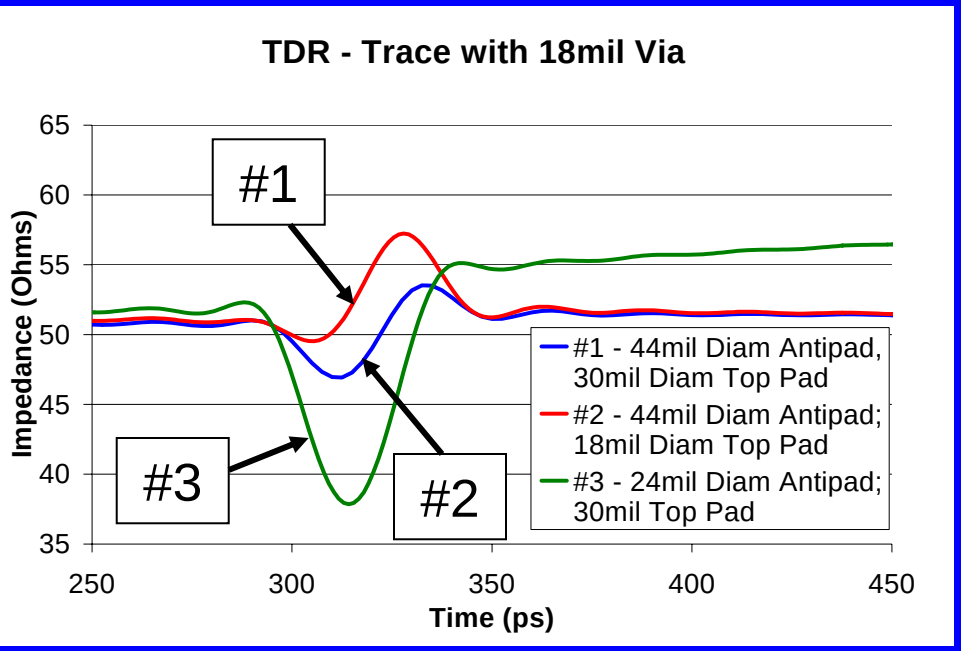
Via-Pad Structure

- How can we modify capacitance?
  - Reduce/remove stub from signal via
  - Increase diameter of antipad to decrease capacitance between signal via and ground planes
  - Decrease diameter of antipad to increase capacitance between signal via and ground planes



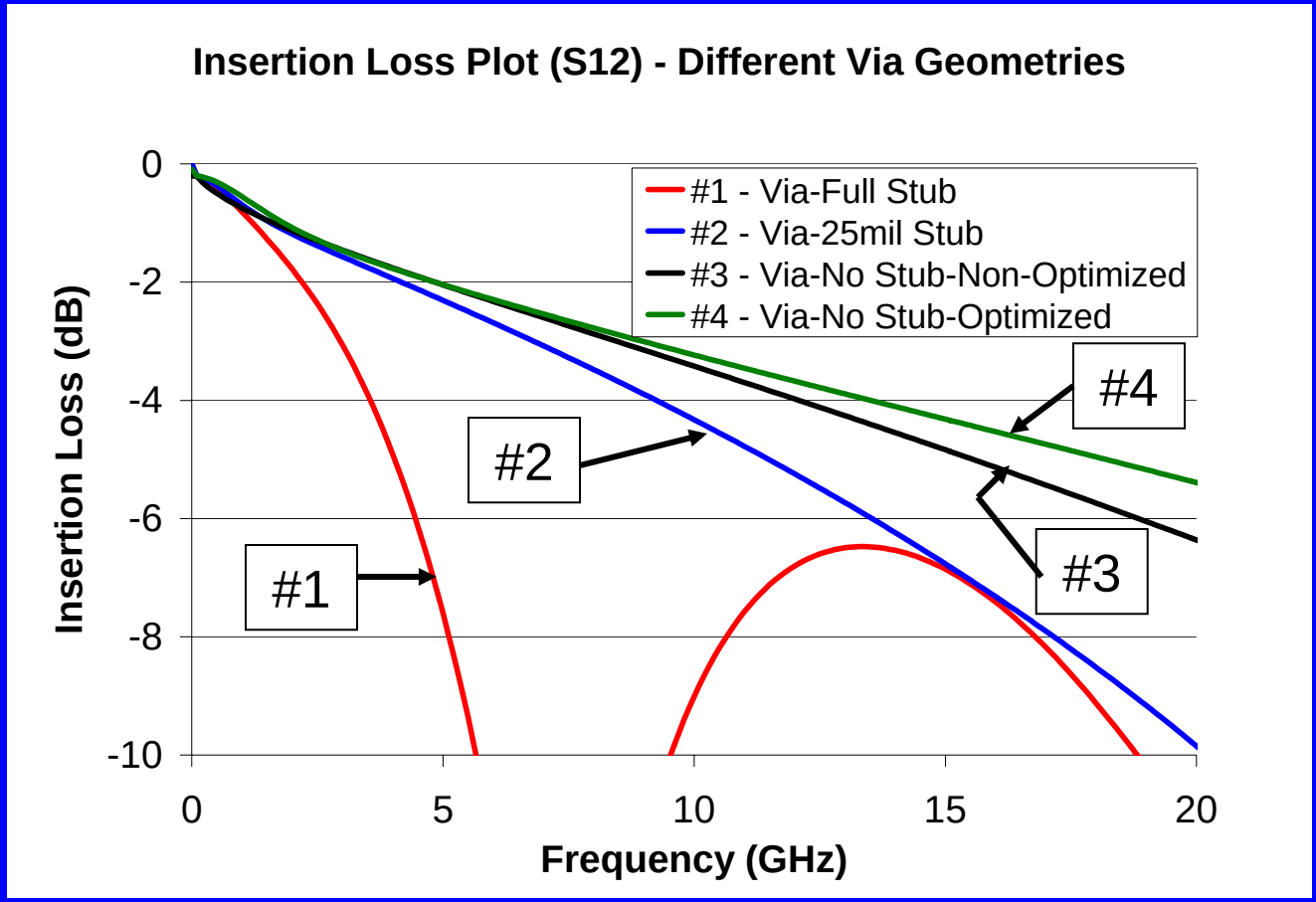
Via-Pad Structure





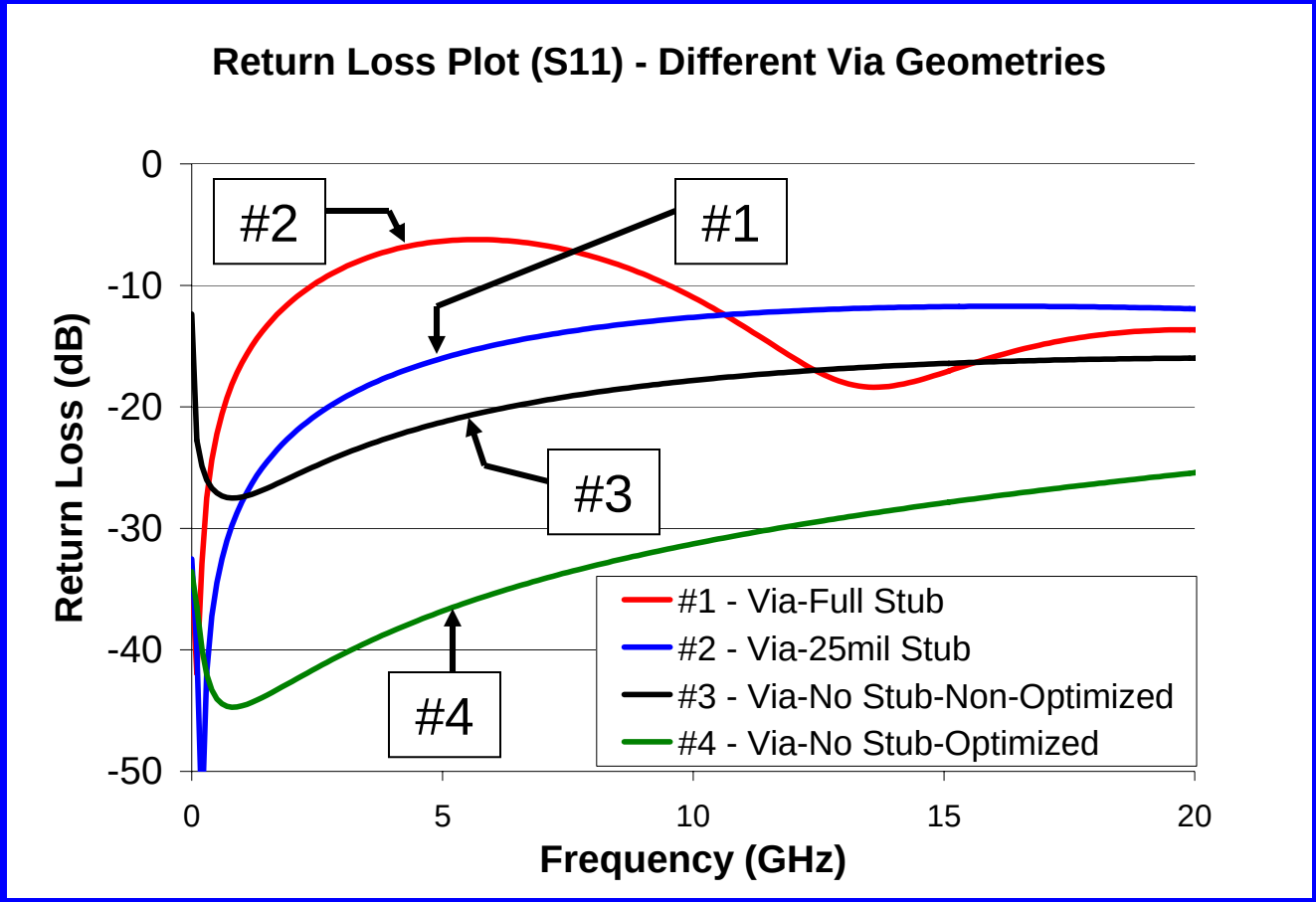
- **Green: Antipad too small, too much capacitance on via**
- **Red: Top pad too small, not enough capacitance between pad and ground plane**
- **Blue: Capacitance distributed well between antipad and top pad**

Results - Insertion Loss



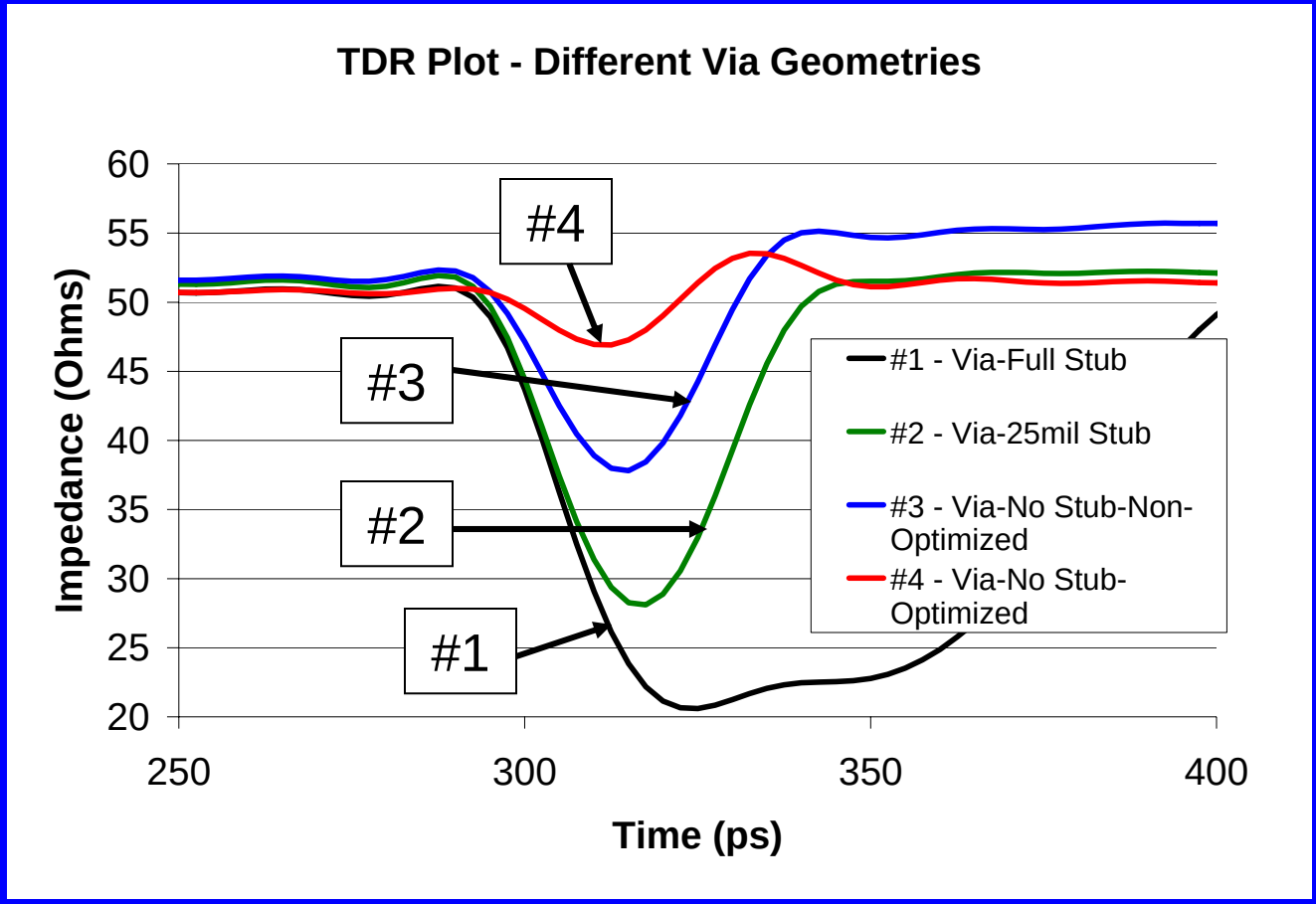
- However, insertion loss alone is not sufficient to fully characterize the system

Results - Return Loss



- **Optimized geometry shows lowest return loss and therefore the least amount of reflections**

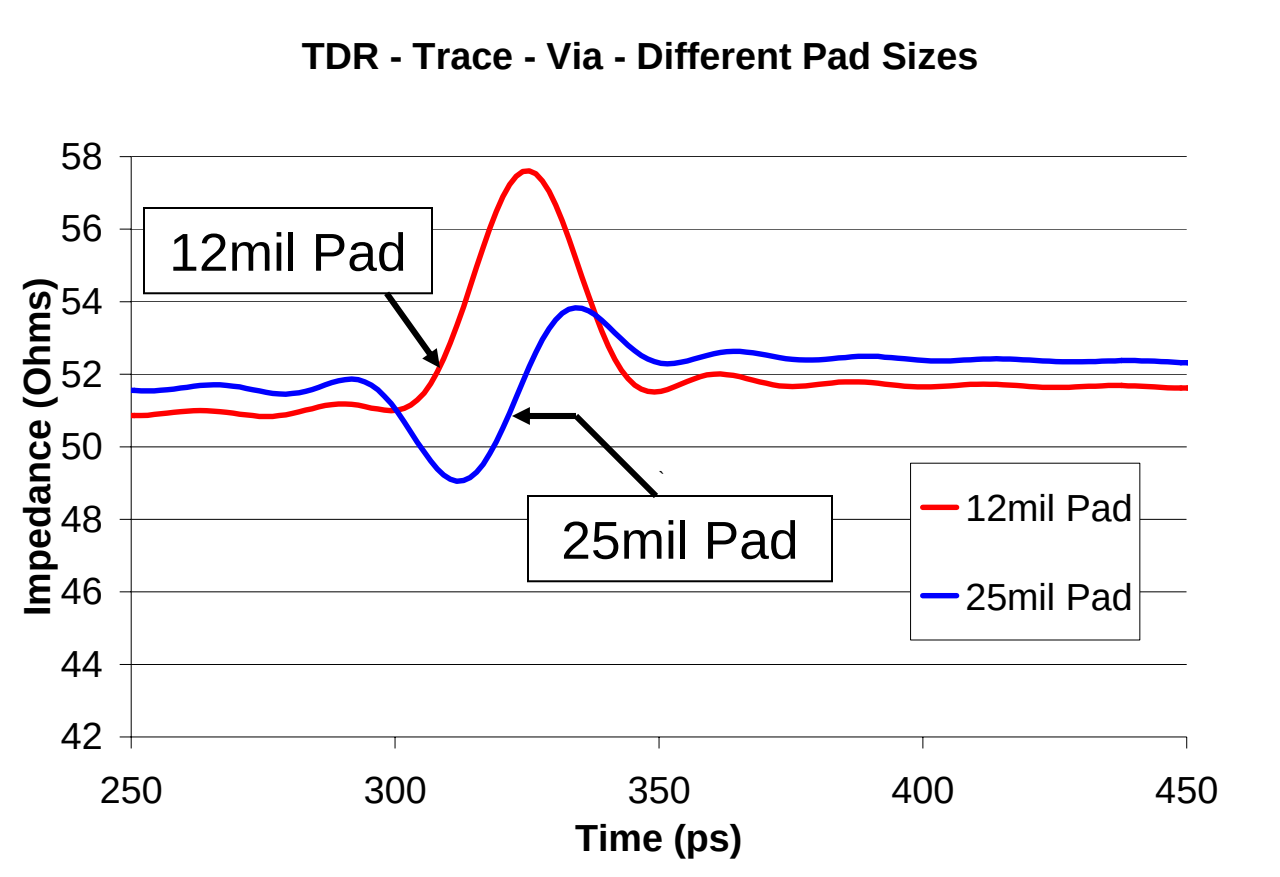
Results - Impedance



- **The goal is for a 50-ohm impedance through the via to reduce reflections**

Transmission Path - Pads

- If via has high inductance, pad can offset this to create impedance much closer to 50 ohms



Results - Via-Pad Structure

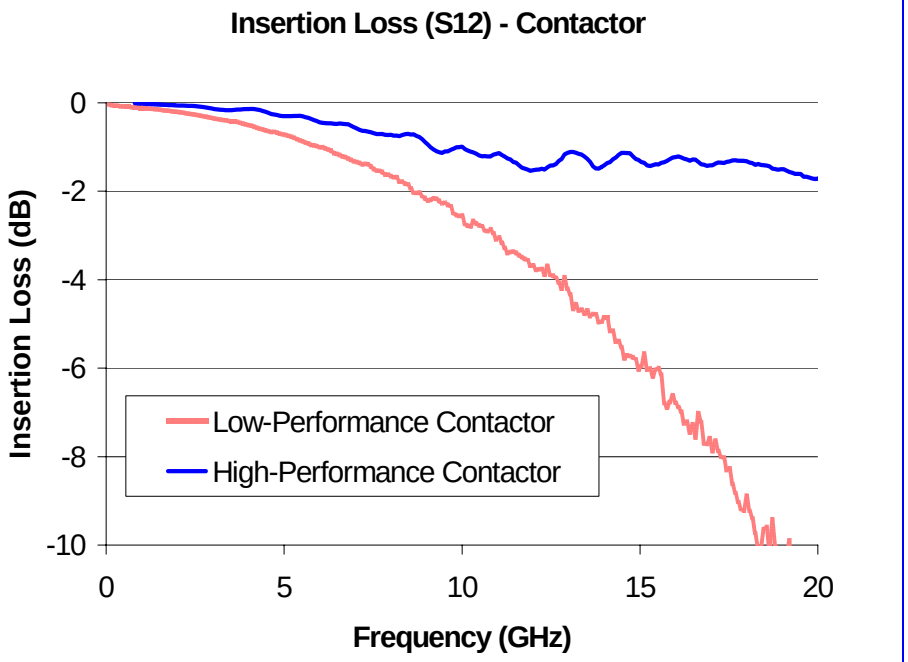
- Vias will always cause reflections. The goal is to minimize them.
- The stub creates a huge capacitance and should be removed/minimized whenever possible
- If any stub remains, use a large antipad to decrease capacitance
- Modify antipad size and/or pad size to match 50-ohm impedance as close as possible

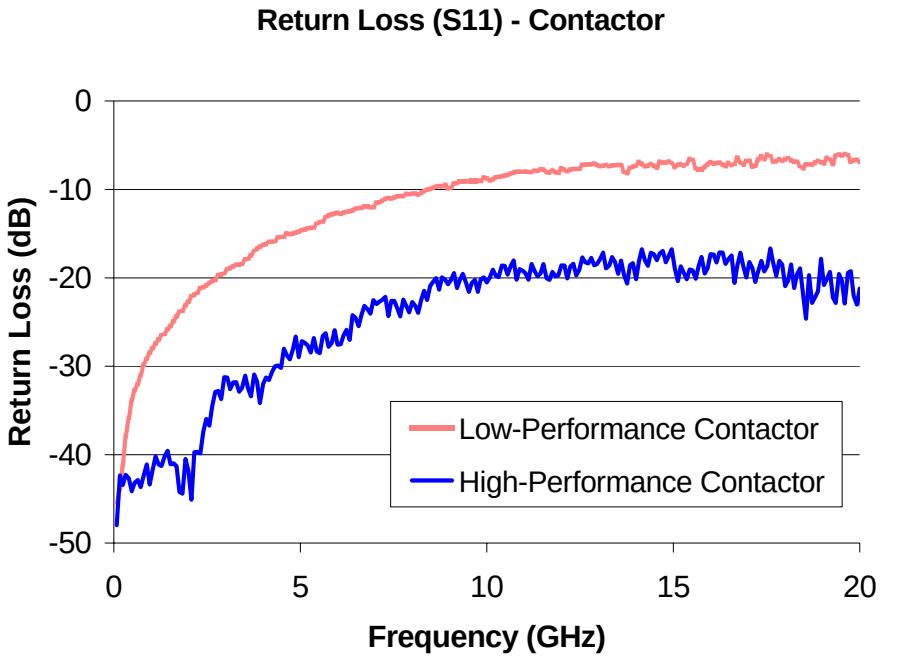
Transmission Path - Contactor

- Typically more loss through board (~8”) than through contactor (~0.100”-0.250”)
- However, a low-performance contactor will cause significant return loss and may compromise test yields.
- Ultra-short path lengths and controlled impedance contactors yield -1dB bandwidth of 30 GHz and beyond.

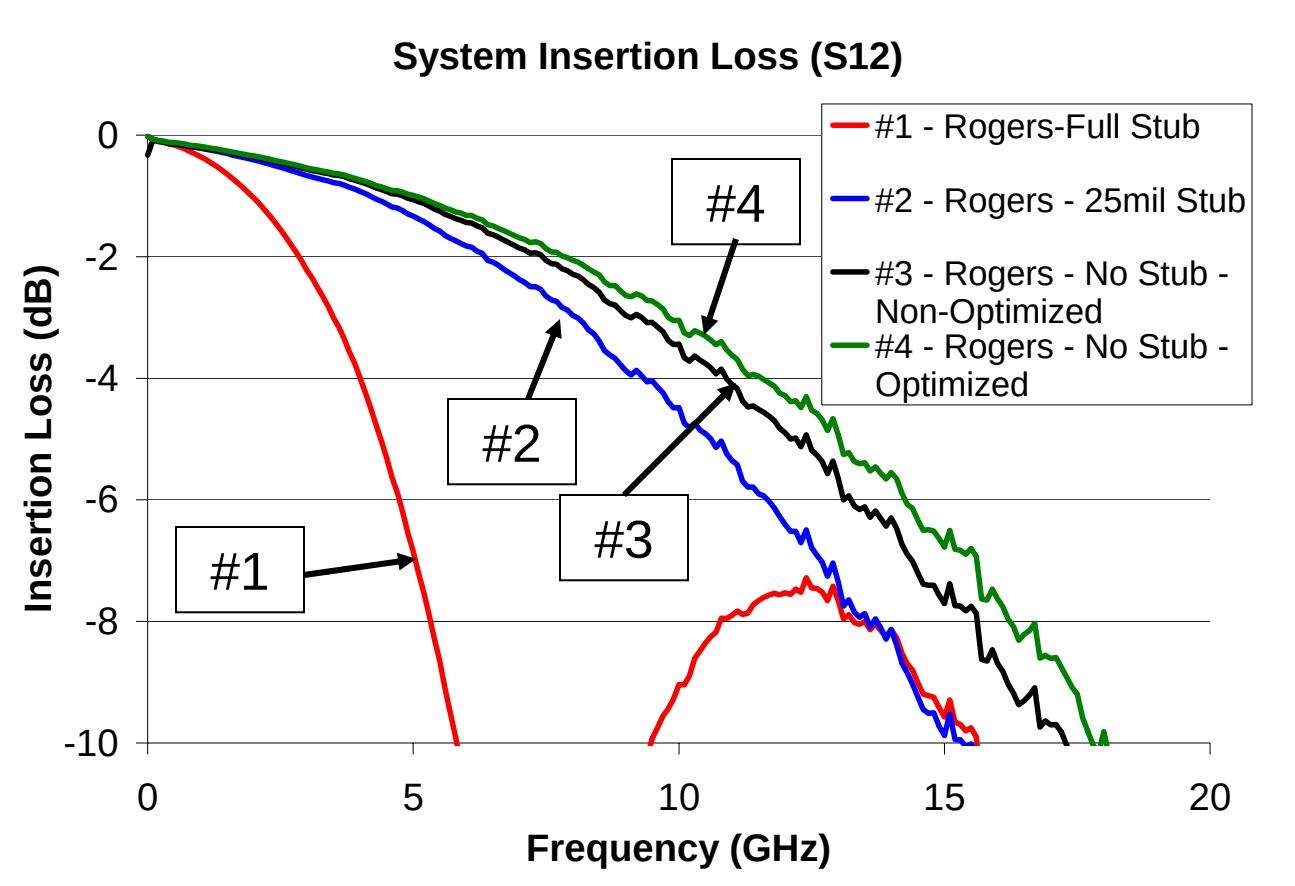
Transmission Path - Contactor

- **Small differences in conductor geometries can significantly increase bandwidth and reduce return loss**



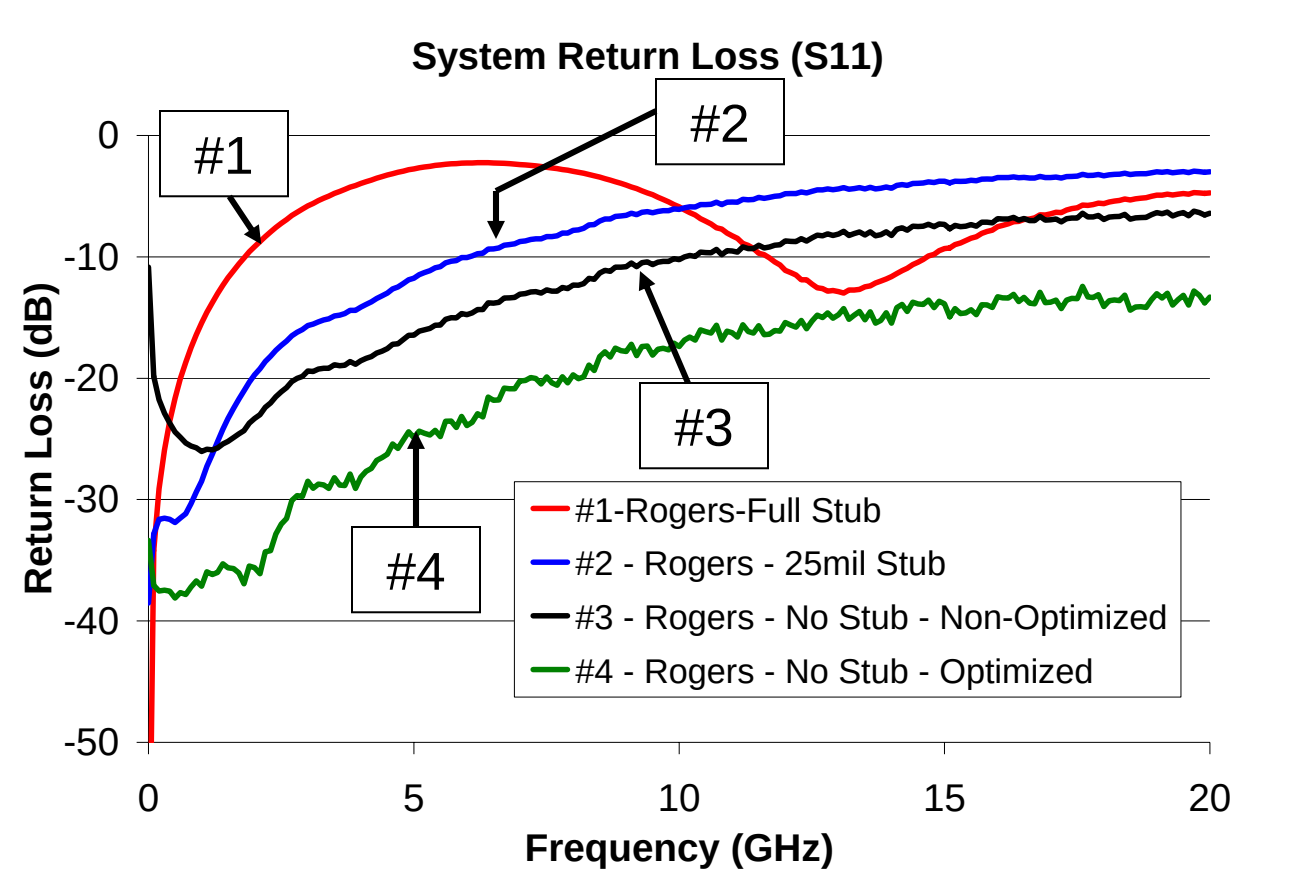


Transmission Path - System Bandwidth



- **-3dB bandwidth of board/contactor system can be increased to ~8GHz**

Transmission Path - System Return Loss



- **By reducing the return loss, the performance of the system has been optimized**

Conclusion

- High frequency performance can be optimized through matching the impedance throughout the system to reduce reflections and increase transmission of signal.
- These issues must be taken considered for good performance in high frequency applications
- The techniques described in this presentation can be applied to all transmission lines.

Special Thanks to...

- Co-author, research partner - Jason Mroczkowski, ECT-Semiconductor Test Group
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