Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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BiTS tm Burn-in & Test Socket Workshop

Technical Program

Session 3
Monday 3/07/05 1:00PM

PRINTED CIRCUIT BOARD DESIGN

"ATE And DUT Socket Demands On PCB Transmission Lines"
Zaven Tashjian – Circuit Spectrum **Martin Mullaney** – Circuit Spectrum

"Trace/Grid Power Plane Design For Fine Pitch Printed Circuit Board"
Anthony Wong Yeh Chiing – Intel TTO **Cher-Shyong (CS) Low** – Intel TTO

"Leakage As The Filaments And Dendrites Form In PWB"
Sungalingam Kumaran – Trio-Tech International Pte Ltd

"Challenges In High Current PCB Power Delivery"
Hon Lee Kon – Intel TTO **Anthony Wong Yeh Chiing** – Intel TTO

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ATE and DUT Socket Demands on PCB Transmission Lines

by

Zaven Tashjian

and

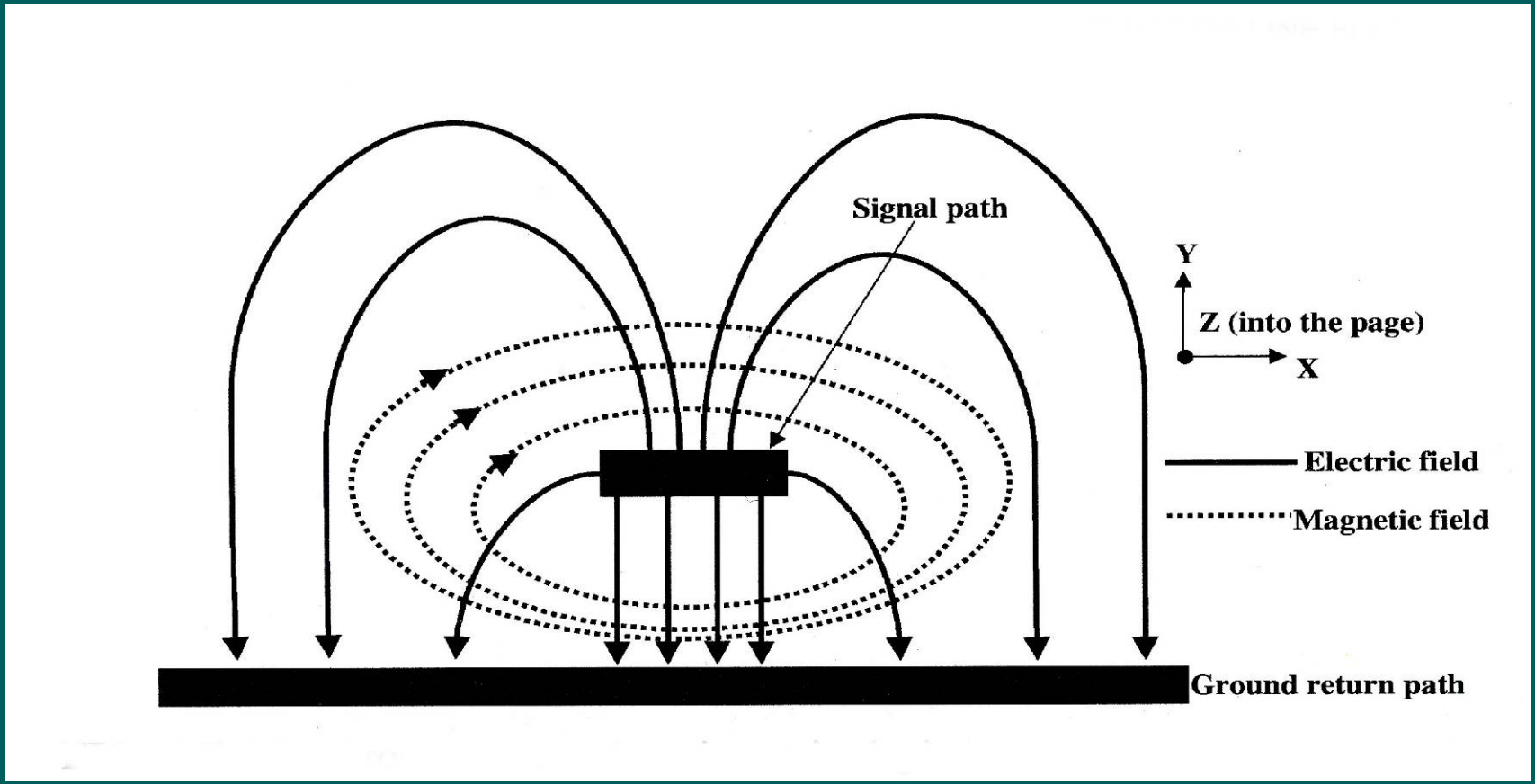
Martin Mullaney

Methodology

- Signal interconnects as a series of inductors, capacitors, etc.
- Modeling of single-ended, LVDS and via structures in different dielectric media
- Signal losses (or rise-time degradation) predicted by models
- Mitigating undesirable parasitic effects at vias and surface pads

Electromagnetic Fields

- Voltage on a conductor creates an electric field
- Current through a conductor creates a magnetic field

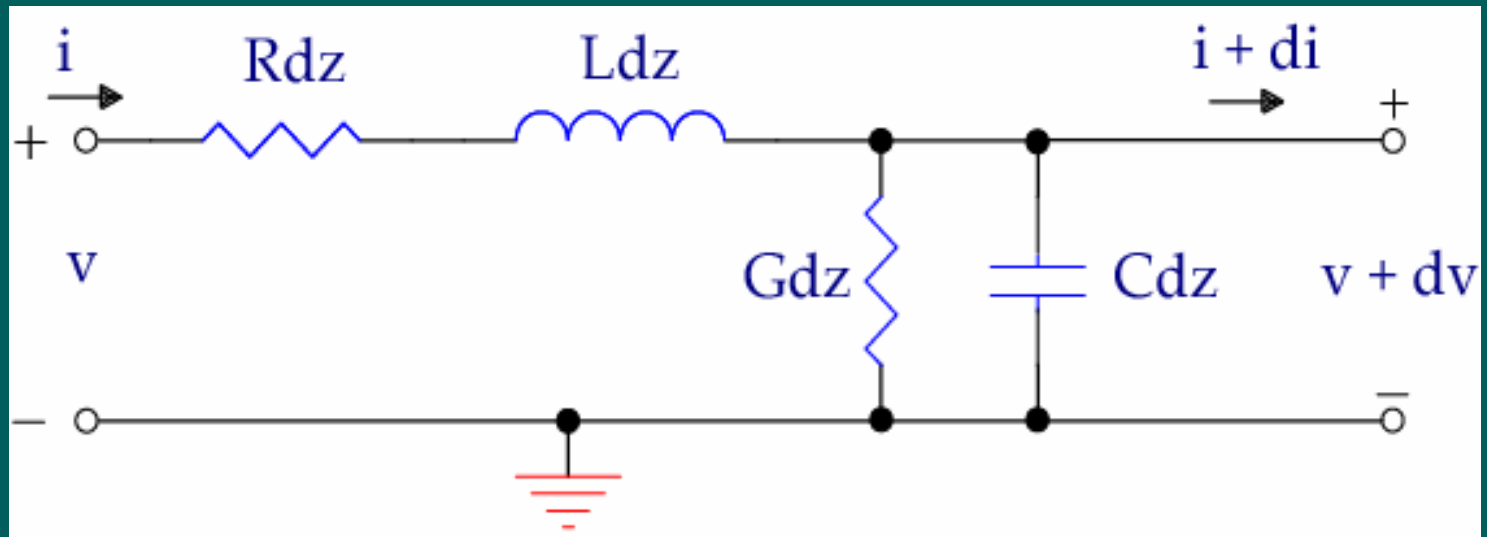


Electric field due to voltage on signal path with respect to ground

Magnetic field due to current flow in signal path

Equivalent Circuits

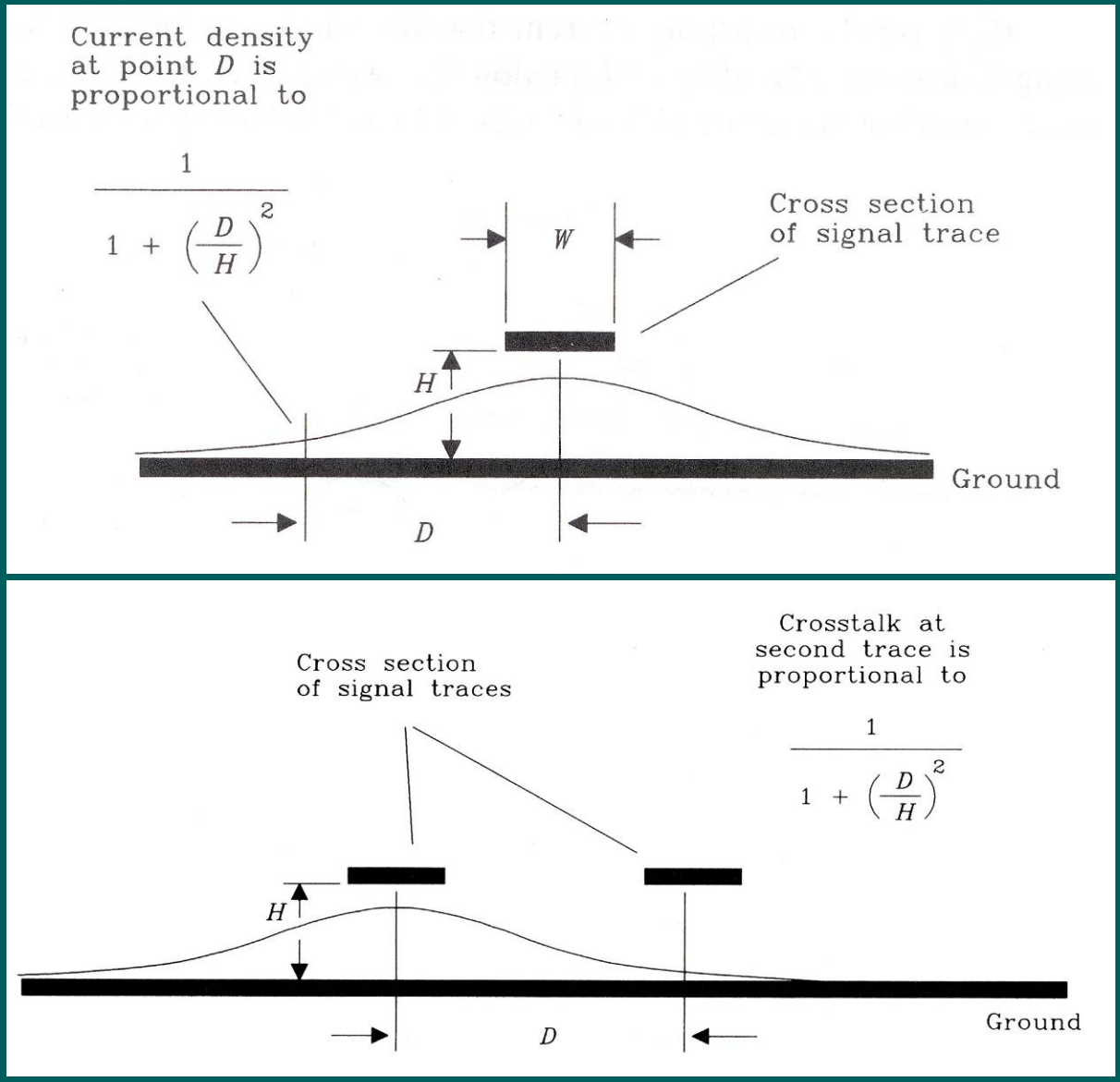
- Field equations lead to the derivation of RLGC equivalent circuit per unit length of conductor with equation for the voltage-current relationship
- Adjacent conductors also develop mutual capacitance and inductance



$$\frac{dv}{dz} = -L\frac{di}{dt} - Ri$$

$$\frac{di}{dz} = -C\frac{dv}{dt} - Gv$$

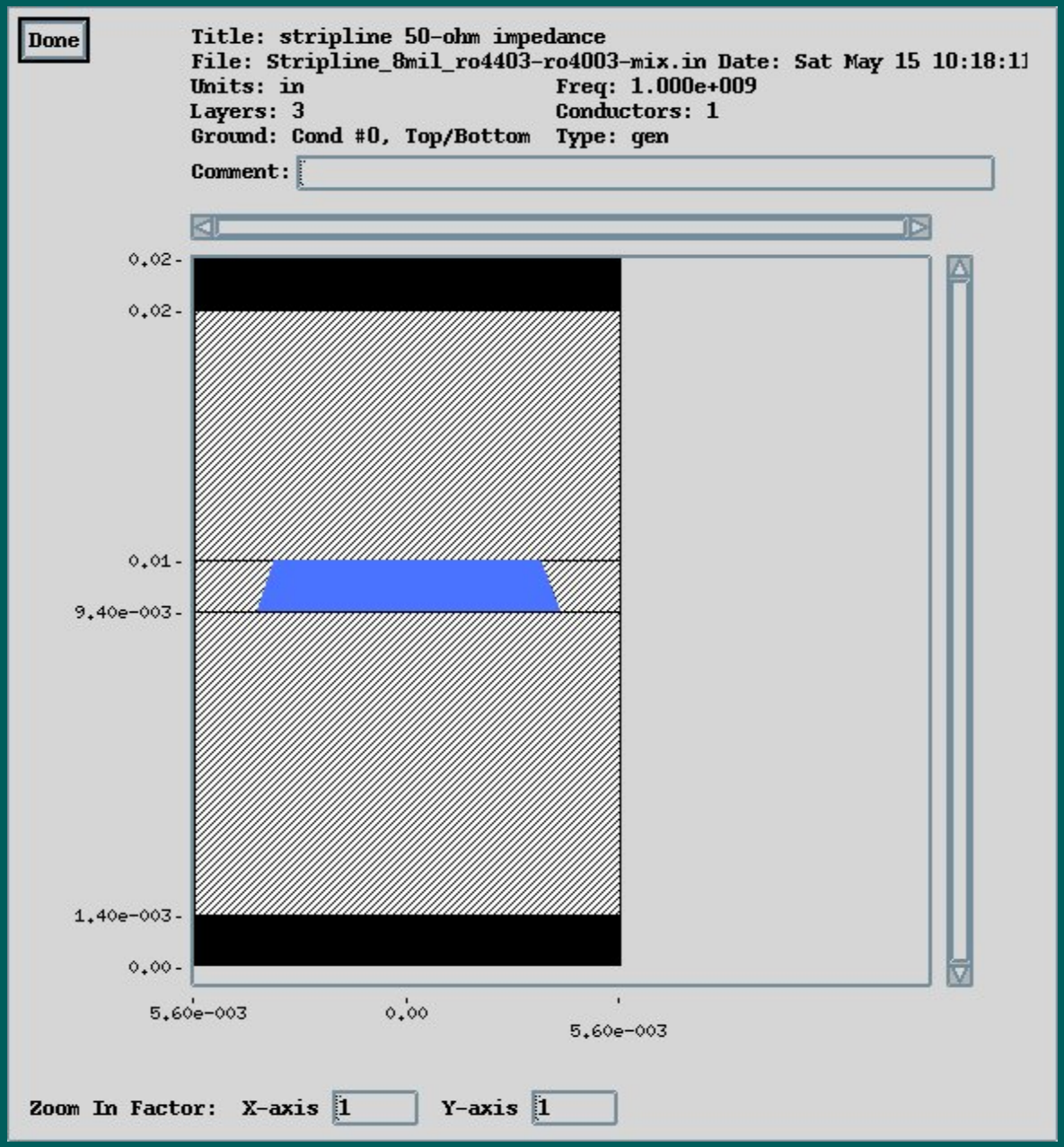
RLGC equivalent circuit for a single conductor of incremental length dz



Current density profiles in signal return paths

Modeling with 2-D Tool (RLGC)

- Derives all four circuit element values per unit length defined by user
- Derives mutual element values
- Calculates equivalent circuit elements for a via
- Output file formats are compatible with simulation tools



Modeling setup for stripline

```
                RLGC MATRICES FOR GENERAL CONFIGURATION

*title: stripline Rogers 4003/4403, 50-ohm impedance

Frequency = 1.000e+009 Units = in

Method used = 1 (default is 1)
```

```
epsr1 = 3.170e+000 tand1 = 5.000e-003 height1 = 6.600e-003
epsr2 = 3.170e+000 tand2 = 5.000e-003 height2 = 1.400e-003
epsr3 = 3.380e+000 tand3 = 3.700e-003 height3 = 8.000e-003
```

Model Stackup

```
    Number of traces in conductor 1 = 1
layer1 = 2, widthBottom1 = 8.000e-003, widthTop1 = 7.000e-003,
     xcord1 = 0.000e+000, sigma1 = 5.800e+007
```

Trace Width

```
CMATRIX (F/in) =
3.151e-012

CMATRIXAIR (F/in) =
9.656e-013
```

Capacitance per unit length

```
LMATRIX (H/in) =
7.434e-009
```

Inductance per unit length

```
GMATRIX calculated at a frequency of 1.000e+009

GMATRIX (S/in) =
7.795e-005
```

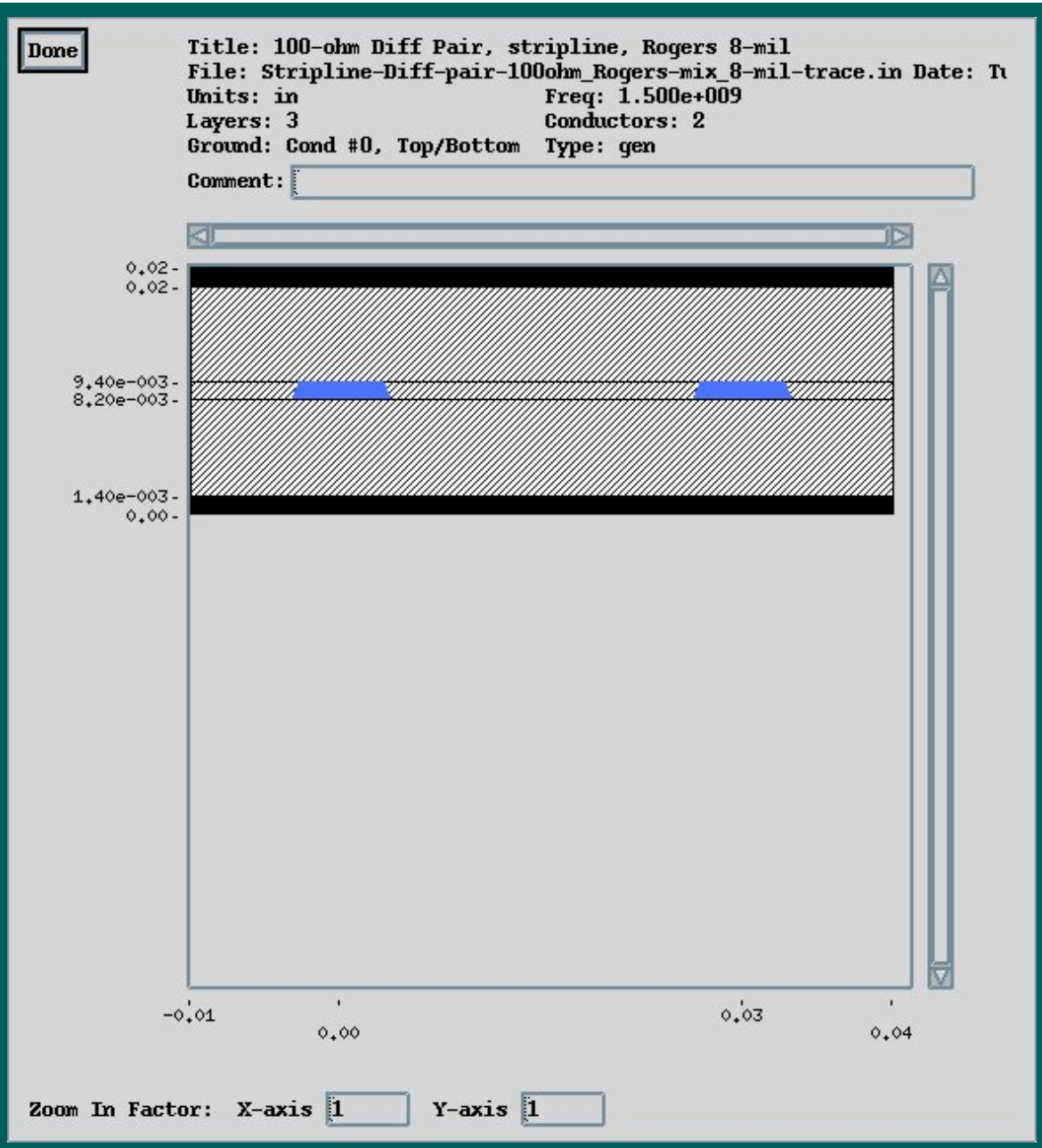
Conductance per unit length

```
RMATRIX calculated at a frequency of 1.000e+009

RMATRIX (ohm/in) =
7.035e-001
```

Resistance per unit length

```
CHARACTERISTICS OF VARIOUS MODES

 Mode #       Z0          Effective Relative    Attenuation
            (ohms)        Dielectric Constant     (dB/in)

    1      48.57-j0.27           3.26            7.934e-002
```

Model output data for stripline



Modeling setup for stripline differential pair

```
RLGC MATRICES FOR GENERAL CONFIGURATION

*title: 100-ohm Diff Pair, stripline, Rogers 8-mil
Frequency = 1.500e+009 Units = in
Method used = 1 (default is 1)
```

```
epsr1 = 3.480e+000 tand1 = 4.000e-003 height1 = 6.600e-003
epsr2 = 3.170e+000 tand2 = 5.000e-003 height2 = 1.200e-003
epsr3 = 3.170e+000 tand3 = 5.000e-003 height3 = 6.800e-003
```

Model Stackup

```
    Number of traces in conductor 1 = 1
layer1 = 2, widthBottom1 = 7.000e-003, widthTop1 = 6.000e-003,
     xcord1 = 0.000e+000, sigma1 = 5.800e+007

    Number of traces in conductor 2 = 1
layer1 = 2, widthBottom1 = 7.000e-003, widthTop1 = 6.000e-003,
     xcord1 = 2.800e-002, sigma1 = 5.800e+007
```

Trace Widths

```
CMATRIX (F/in) =
3.079e-012 -1.174e-014
-1.174e-014 3.079e-012

CMATRIXAIR (F/in) =
9.305e-013 -3.661e-015
-3.661e-015 9.305e-013
```

Capacitance per unit length

```
LMATRIX (H/in) =
7.715e-009 3.036e-011
3.036e-011 7.715e-009
```

Inductance per unit length

```
GMATRIX calculated at a frequency of 1.500e+009

GMATRIX (S/in) =
1.314e-004 -5.387e-007
-5.387e-007 1.314e-004
```

Conductance per unit length

```
RMATRIX calculated at a frequency of 1.500e+009

RMATRIX (ohm/in) =
9.986e-001 2.328e-002
2.328e-002 9.986e-001
```

Resistance per unit length

Model output data for stripline differential pair

```
CHARACTERISTICS OF VARIOUS MODES

 Mode #        Z0              Effective Relative     Attenuation
              (ohms)           Dielectric Constant      (dB/in)

    1       49.87-j0.22              3.31              1.135e-001
    2       50.25-j0.24              3.31              1.169e-001

For two identical conductors symmetric with respect to ground,
the differential and common mode impedances are defined.

Differential impedance (assuming condition above) =  99.73 ohms
Common mode impedance (assuming condition above) =  25.13 ohms
```

Differential Impedance

```
FORWARD CROSSTALK COEFFICIENT MATRIX (ns/in):

Real part  =
1.541e-001 9.480e-006
9.480e-006 1.541e-001

Imaginary part  =
-1.407e-003 -2.049e-005
-2.049e-005 -1.407e-003

BACKWARD CROSSTALK COEFFICIENT MATRIX :

Real part  =
1.000e+000 1.938e-003
1.938e-003 1.000e+000

Imaginary part  =
0.000e+000 -6.685e-005
-6.685e-005 0.000e+000

The forward and backward crosstalk matrices can be used to get
approximate crosstalk information. See manual for details.
```

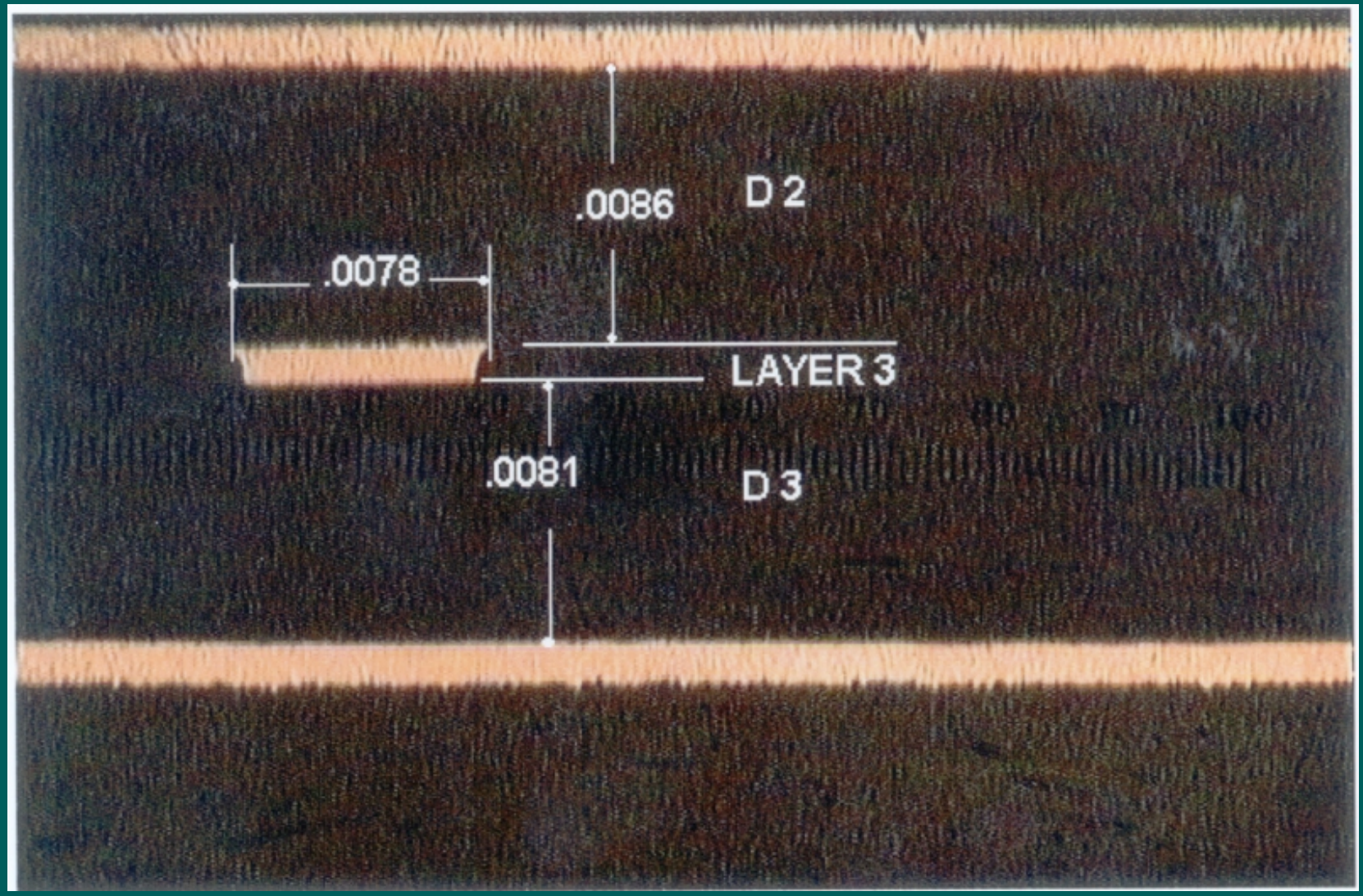
Crosstalk Calculations

```
CHARACTERISTICS OF INDIVIDUAL LINES FROM DIAGONAL ELEMENTS OF RLGC
MATRICES.
COUPLING IS NEGLECTED IN THE INFORMATION GIVEN BELOW

 Line #        Characteristic Impedance      Delay       Attenuation
                      (ohms)                (ns/in)       (dB/in)

    1               50.06-j0.23           1.541e-001     1.152e-001
    2               50.06-j0.23           1.541e-001     1.152e-001
```

Impedance

Propagation delay

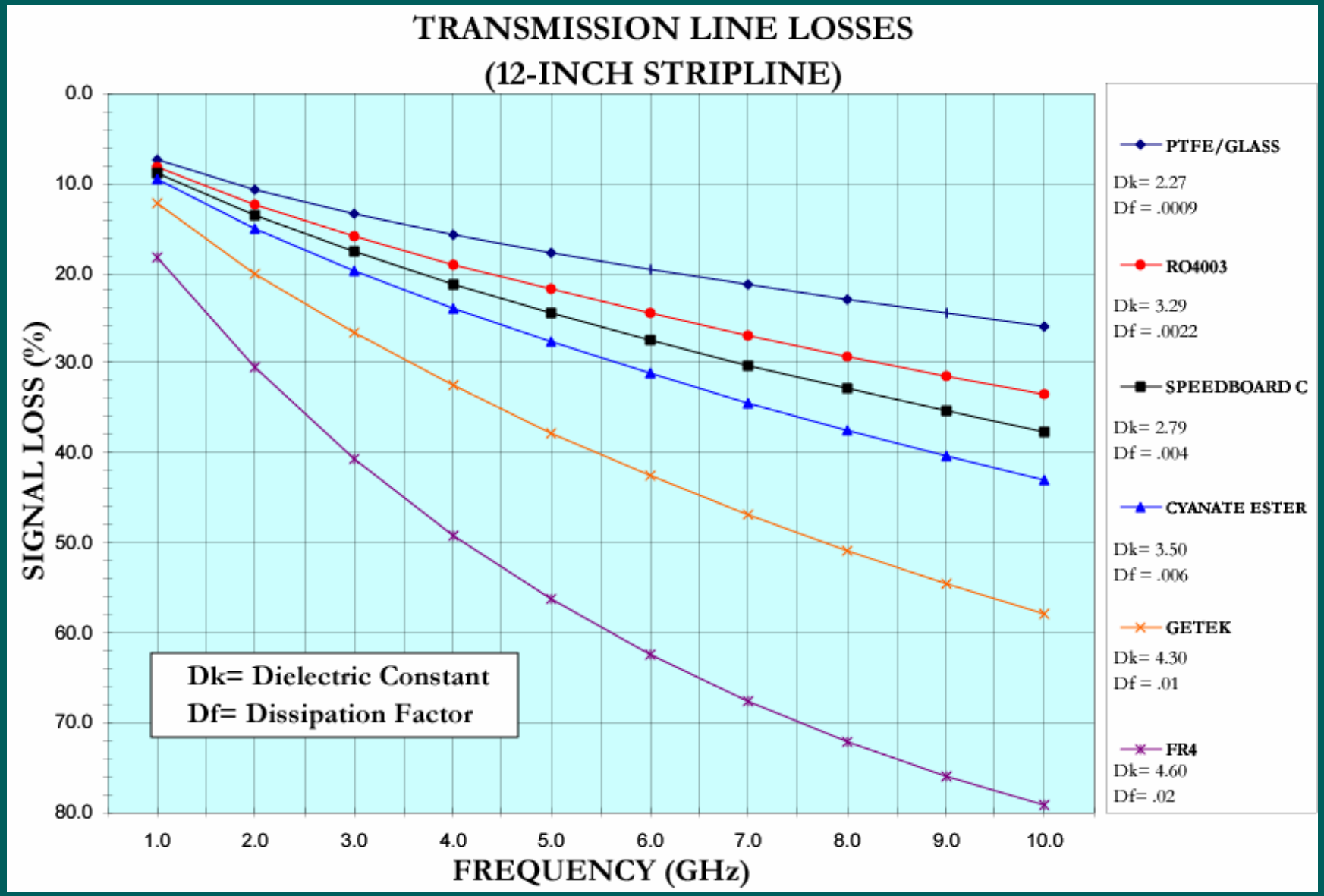
Model output data for stripline differential pair



Micro-section photo for stripline

Signal Losses and Rise-Time Degradation

- The models and output files show signal losses as a function of line length and frequency
- The electrical properties of the dielectric material are characterized by the values of the dielectric constant and loss tangent
- In the digital world losses as a function of frequency translate to rise-time degradation


TRANSMISSION LINE LOSSES
(12-INCH STRIPLINE)
SIGNAL LOSS (%)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
FREQUENCY (GHz)
Dk= Dielectric Constant
Df= Dissipation Factor
PTFE/GLASS
Dk= 2.27
Df = .0009
RO4003
Dk= 3.29
Df = .0022
SPEEDBOARD C
Dk= 2.79
Df = .004
CYANATE ESTER
Dk= 3.50
Df = .006
GETEK
Dk= 4.30
Df = .01
FR4
Dk= 4.60
Df= .02

$$t3db = \frac{.350}{f3db}$$

$$ti = \text{input risetime}$$

$$td = \sqrt{ti^2 + t3db^2}$$

	F3db (GHZ)			T3db (PS)			Ti	Td (PS)		
	FR4	GETEK	RO4003	FR4	GETEK	RO4003	INPUT	FR4	GETEK	RO4003
STRIPLINE	1.9	3.1	8.9	184	113	39	50 PS	191	124	63
MICROSTRIP	2.4	3.8	10.1	146	92	35		154	105	61
STRIPLINE	1.9	3.1	8.9	184	113	39	100 PS	209	151	107
MICROSTRIP	2.4	3.8	10.1	146	92	35		177	136	106
STRIPLINE	1.9	3.1	8.9	184	113	39	200 PS	272	230	204
MICROSTRIP	2.4	3.8	10.1	146	92	35		248	220	203
STRIPLINE	1.9	3.1	8.9	184	113	39	400 PS	440	416	402
MICROSTRIP	2.4	3.8	10.1	146	92	35		426	410	402

Rise time degradation for 12-inch lines

Unwanted Parasitics

- Removing unwanted parasitic effects
  - Plate capacitance
  - Impedance discontinuity at via
  - Via stub drilling

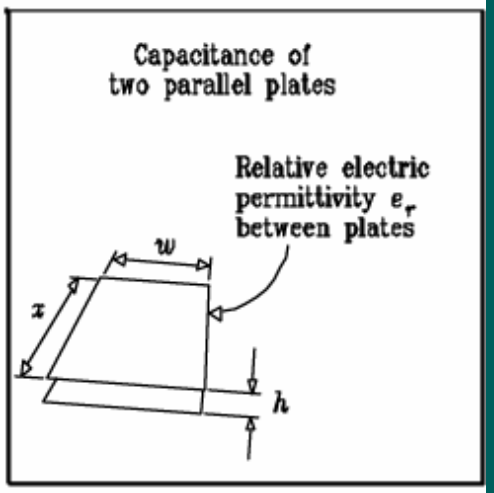
CAPACITANCE OF TWO PARALLEL PLATES file: capac.mcd

Formulas included in this spreadsheet:

Capacitance of two plates	CPLATE()
Impedance magnitude of capacitor at one frequency	XCF()
Impedance magnitude of capacitor as seen by rising edge	XCR()

Variables used:

w	Width of plate overlap (in.)
x	Length of plate overlap (in.)
h	Height of one plate above the other (in.)
er	Relative dielectric constant of material between plates



Capacitance of two plates (F):

$$CPLATE(w,x,h,er) := 2.249 \cdot 10^{-13} \cdot \frac{er \cdot x \cdot w}{h}$$

A power and ground plane separated by 0.010 in. of FR-4 dielectric (er = 4.5) share a capacitance of 100 pF/in.\253

Halving the separation doubles the capacitance.

Impedance magnitude of capacitor at frequency f (

c	Capacitance (F)
f	Frequency (Hz)

The impedance, at 100 MHz, of a 100-pF capacitor is 16

$$XC(c,f) := \frac{1}{2 \cdot f \cdot c}$$

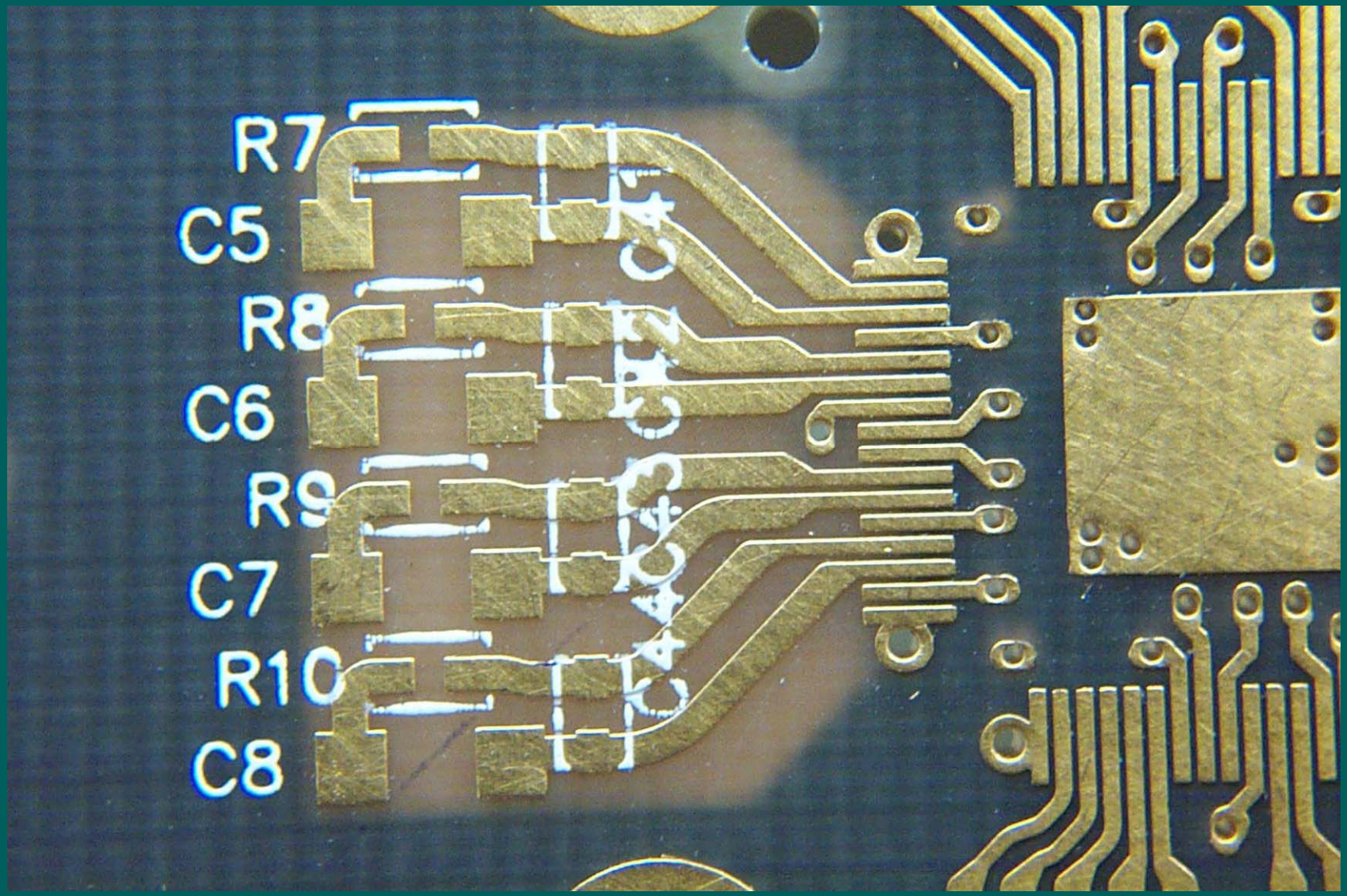
Impedance magnitude of capacitor as seen by rising edge

c	Capacitance (F)
tr	10-90% rise time (s)

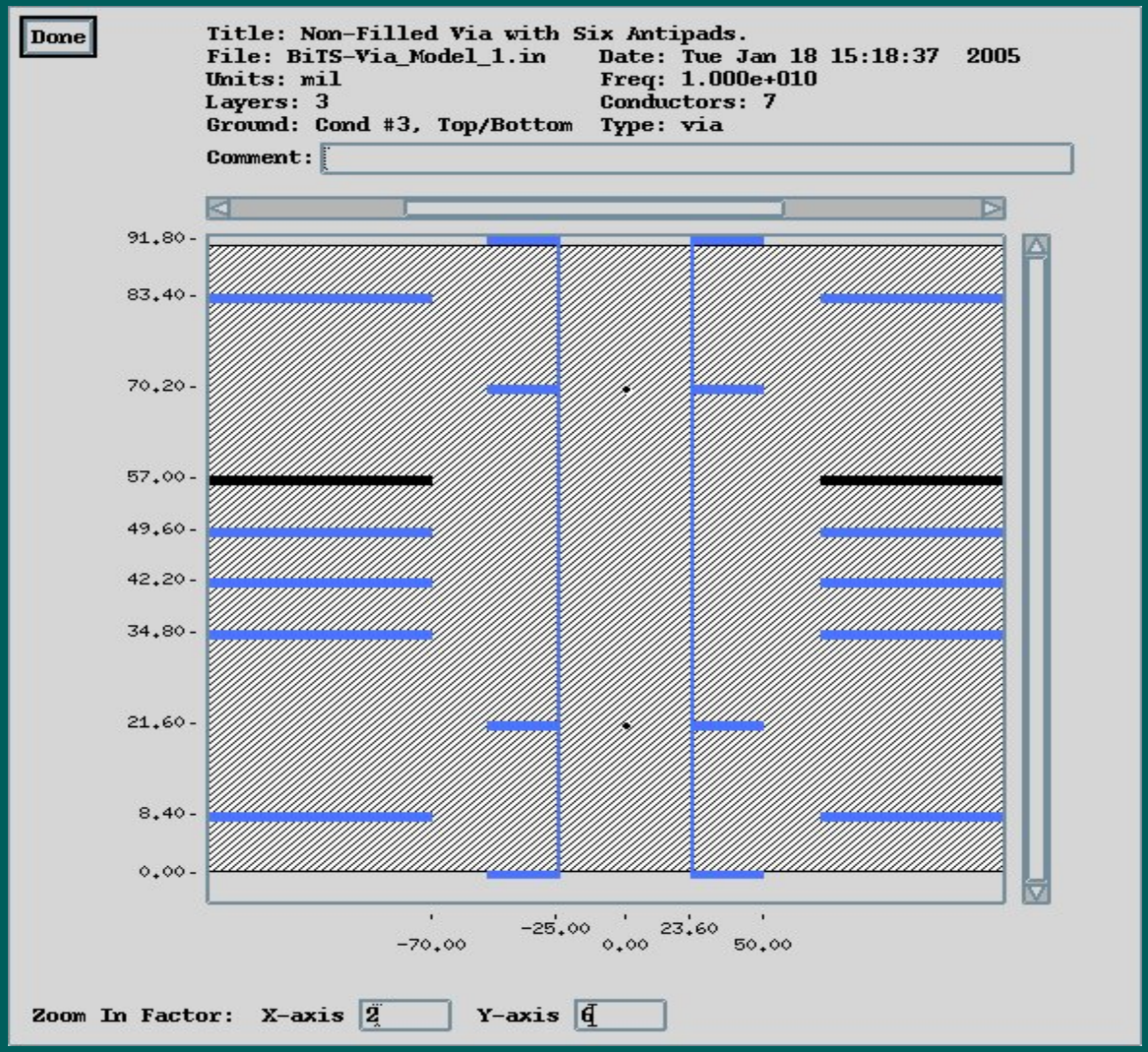
The impedance, as seen by a 5-ns rising edge of a 100-pF capacitor is 16

$$XC(c,tr) := \frac{tr}{c}$$

Plate capacitance calculation



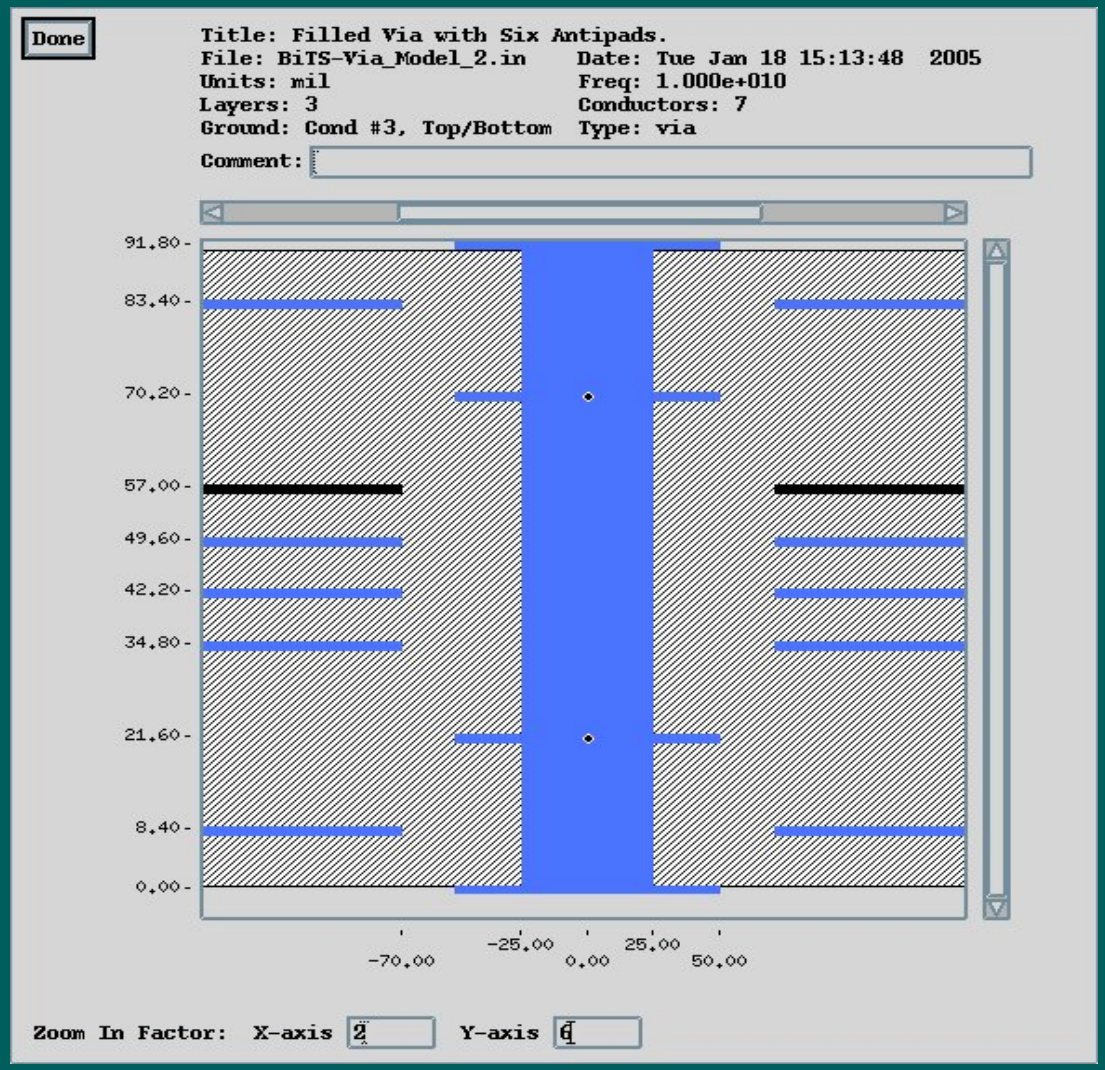
Voided ground plane beneath circuit



Standard via model

Output data for standard via model

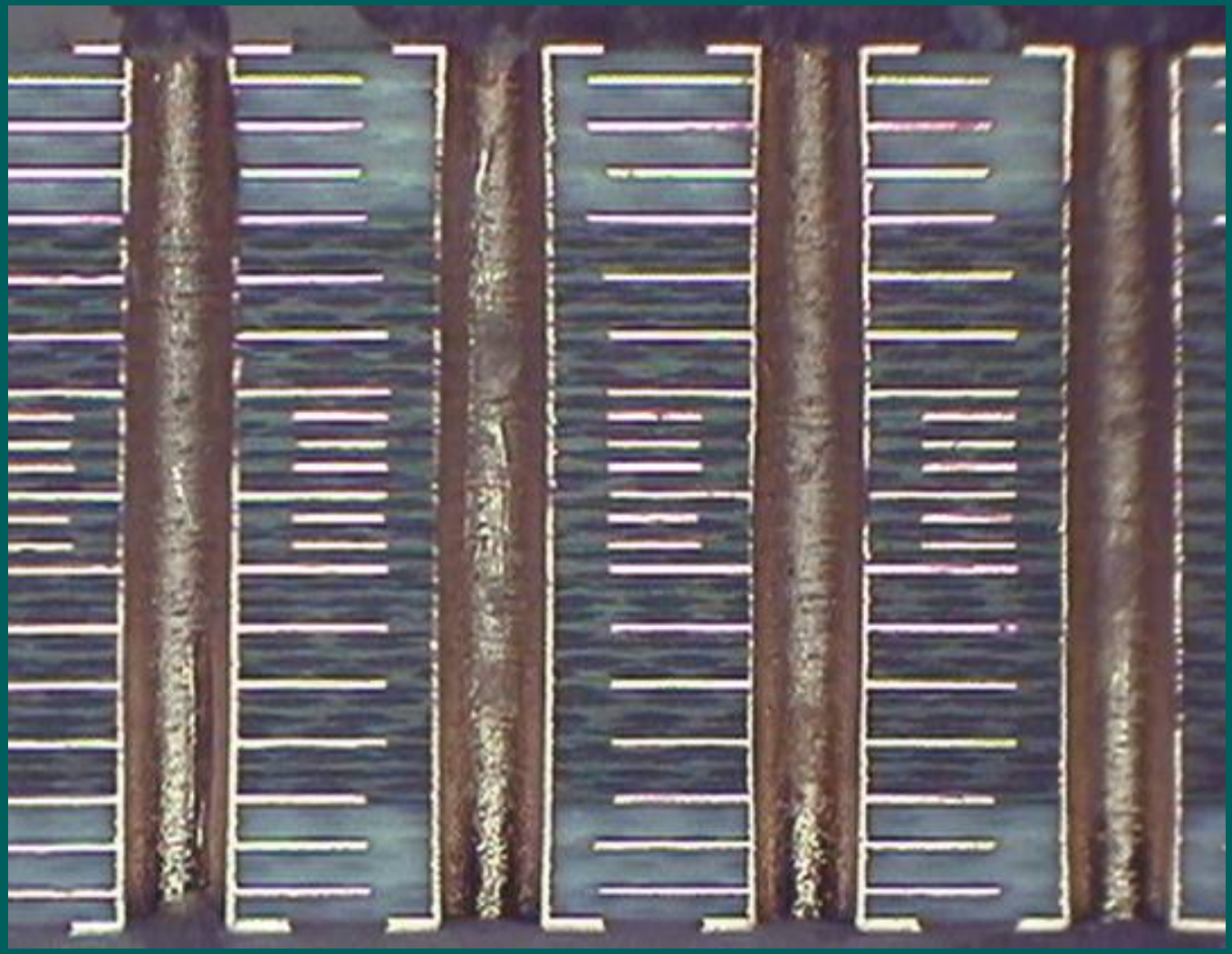
- Ltop top node1r 1.007e-012H
- Rtop node1r node1 1.512e-003
- L1 node1 inr 2.920e-012H
- R1 inr in 2.194e-003
- L2 in node2r 2.920e-012H
- R2 node2r noade2 2.194e-003
- L3 node2 node3r 1.559e-013H
- R3 node3r node3 1.230e-003
- L4 node3 node4r 1.559e-013H
- R4 node4r node4 1.230e-003
- L5 node4 node5r 1.559e-013H
- R5 node5r node5 1.230e-003
- L6 node5 outr 2.920e-012H
- R6 outr out 2.194e-003
- L7 out node6r 2.920e-012H
- R7 node6r node6 2.194e-003
- Lbot node6 botr 1.007e-012H
- Rbot botr bot 1.512e-003
- Ctop top p2 9.596e-014
- C2 node1 p2 1.392e-013
- C3 node2 ref 1.378e-013
- C4 node3 p4 5.931e-014
- C5 node4 p5 5.920e-014
- C6 node5 p6 1.387e-013
- C7 node6 p7 1.410e-013
- Cbot bot p7 9.723e-014



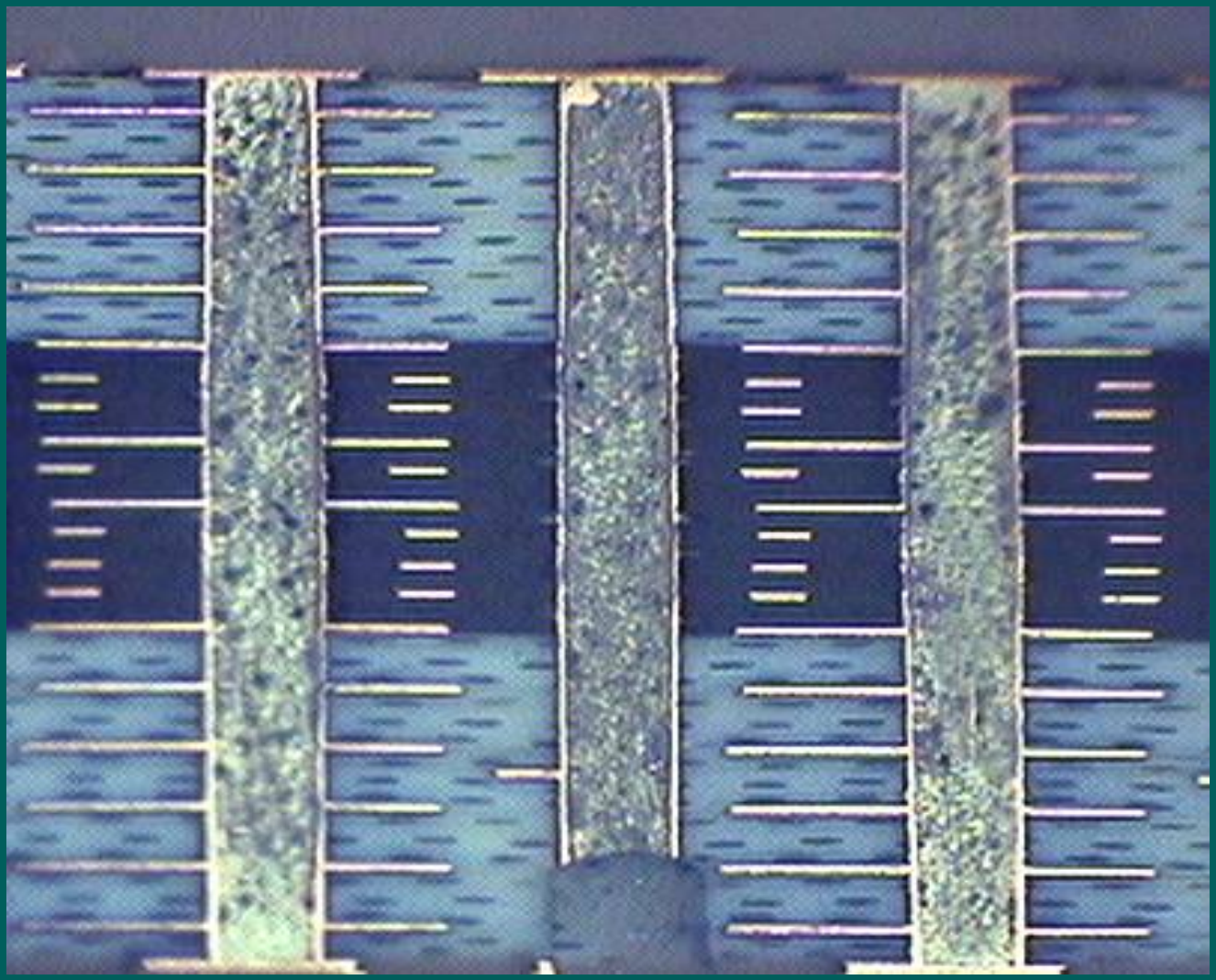
Filled via model

Output data for filled via model

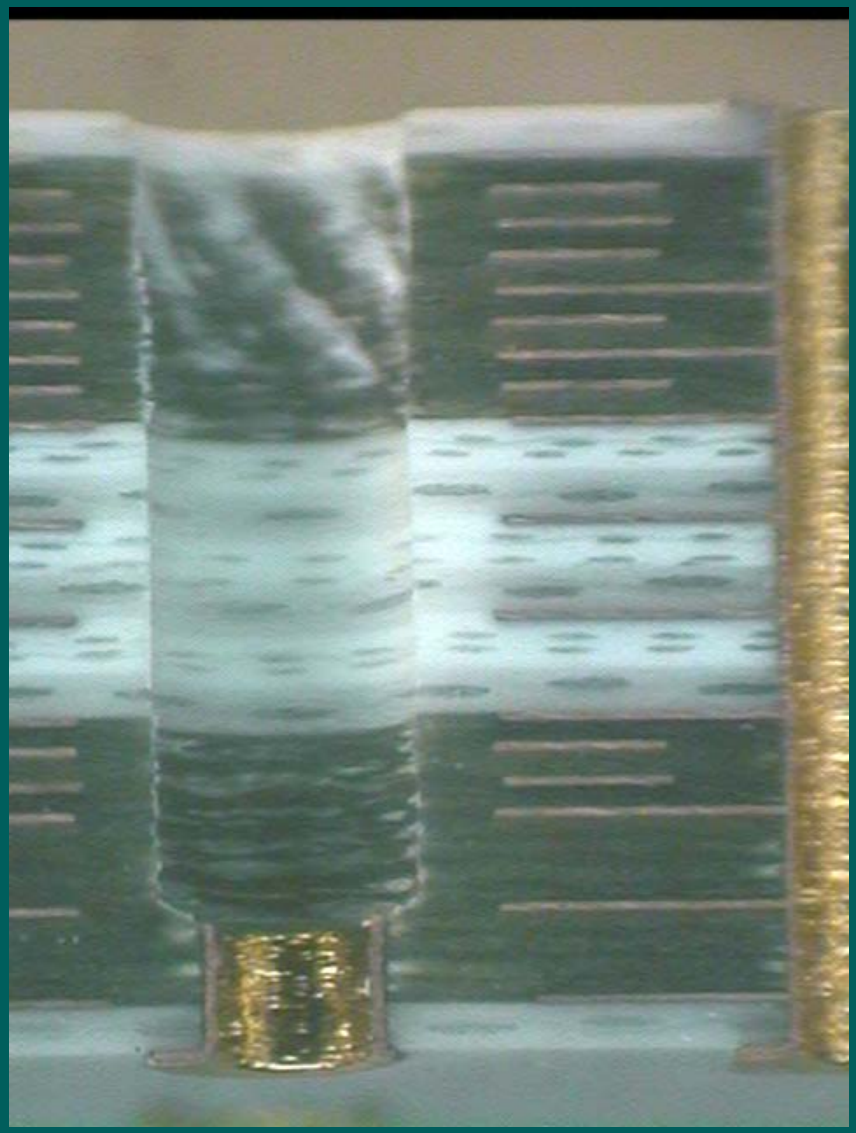
- Ltop top node1r 1.007e-012H
- Rtop node1r node1 1.512e-003
- L1 node1 inr 2.920e-012H
- R1 inr in 2.194e-003
- L2 in node2r 2.920e-012H
- R2 node2r node2 2.194e-003
- L3 node2 node3r 1.559e-013H
- R3 node3r node3 1.230e-003
- L4 node3 node4r 1.559e-013H
- R4 node4r node4 1.230e-003
- L5 node4 node5r 1.559e-013H
- R5 node5r node5 1.230e-003
- L6 node5 outr 2.920e-012H
- R6 outr out 2.194e-003
- L7 out node6r 2.920e-012H
- R7 node6r node6 2.194e-003
- Lbot node6 botr 1.007e-012H
- Rbot botr bot 1.512e-003
- Ctop top p2 9.453e-014
- C2 node1 p2 1.371e-013
- C3 node2 ref 1.353e-013
- C4 node3 p4 5.823e-014
- C5 node4 p5 5.815e-014
- C6 node5 p6 1.361e-013
- C7 node6 p7 1.389e-013
- Cbot bot p7 9.578e-014



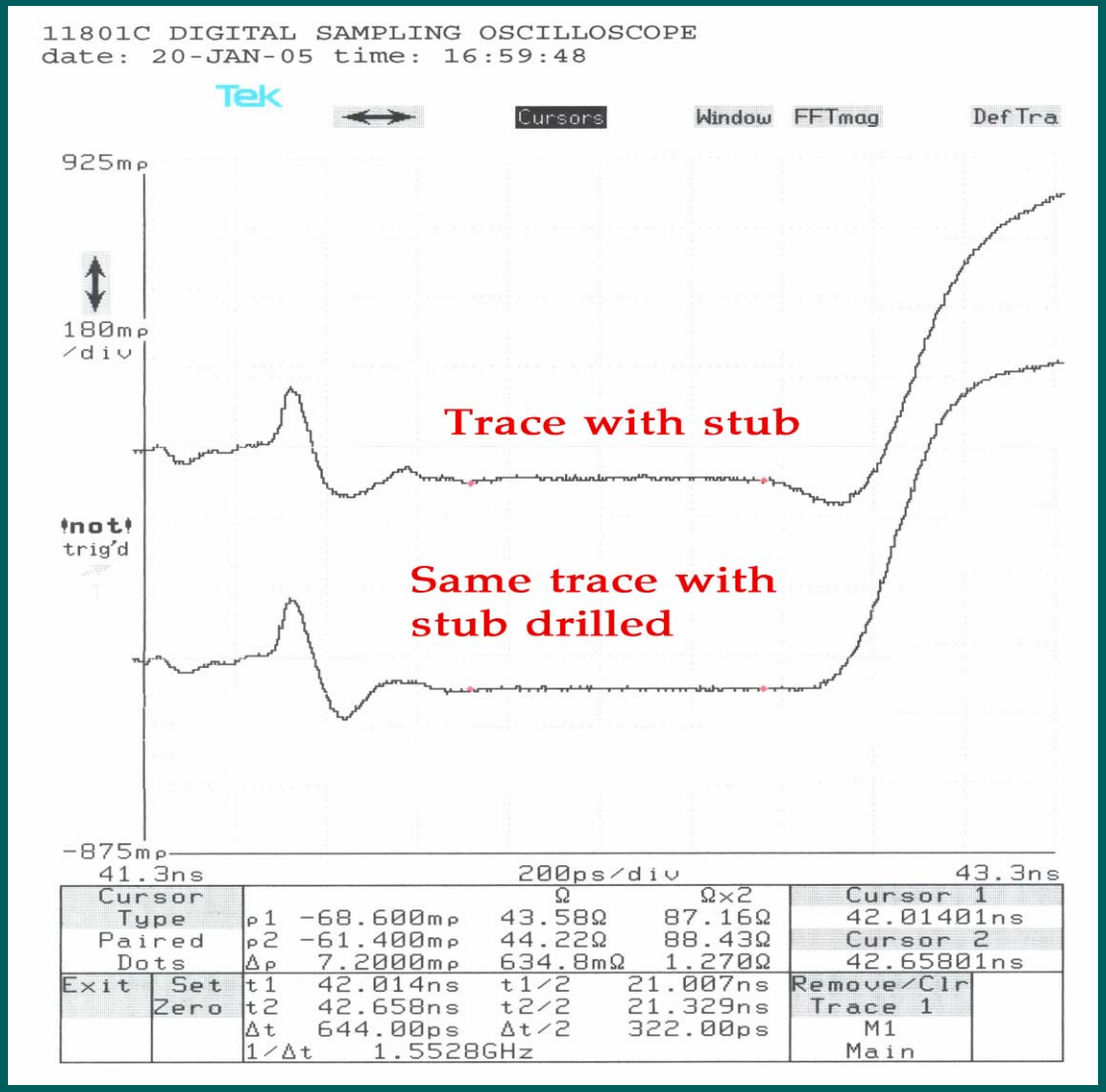
Via micro-section



Stub-drilled via micro-section 1



Stub-drilled via micro-section 2



Effect of via stub drilling

Conclusion

Printed circuit board implementation of signal delivery from ATE to DUT in a production environment may be laden with features that have detrimental effects on signal fidelity. Fortunately, construction and metallization geometry techniques are available to minimize their impact.

Trace/Grid Power Plane Design for Fine Pitch Printed Circuit Board

Anthony Wong Yeh Chiing
Cher-Shyong (CS) Low
Intel Test Tooling Operations

BiTS™
Burn-in & Test
Socket Workshop

Agenda

- Today's World of Electronics
- Industrial Package Pin Pitch Trend
- Conventional Fine Pitch Power Plane Design
- Area of Concerns / Challenges
- Common Method
- Trace/Grid Design Method
- Conclusion

Today's World of Electronic

- Electronic gadgets such as cell phone, pager, personal digital assistance, digital camera, digital camcorder, GPS systems and personal PC have become a daily necessary for everybody.
- Continuously shrinking in size due to consumers' needs of smaller, light weight, mobile, powerful and best of all – All In One.

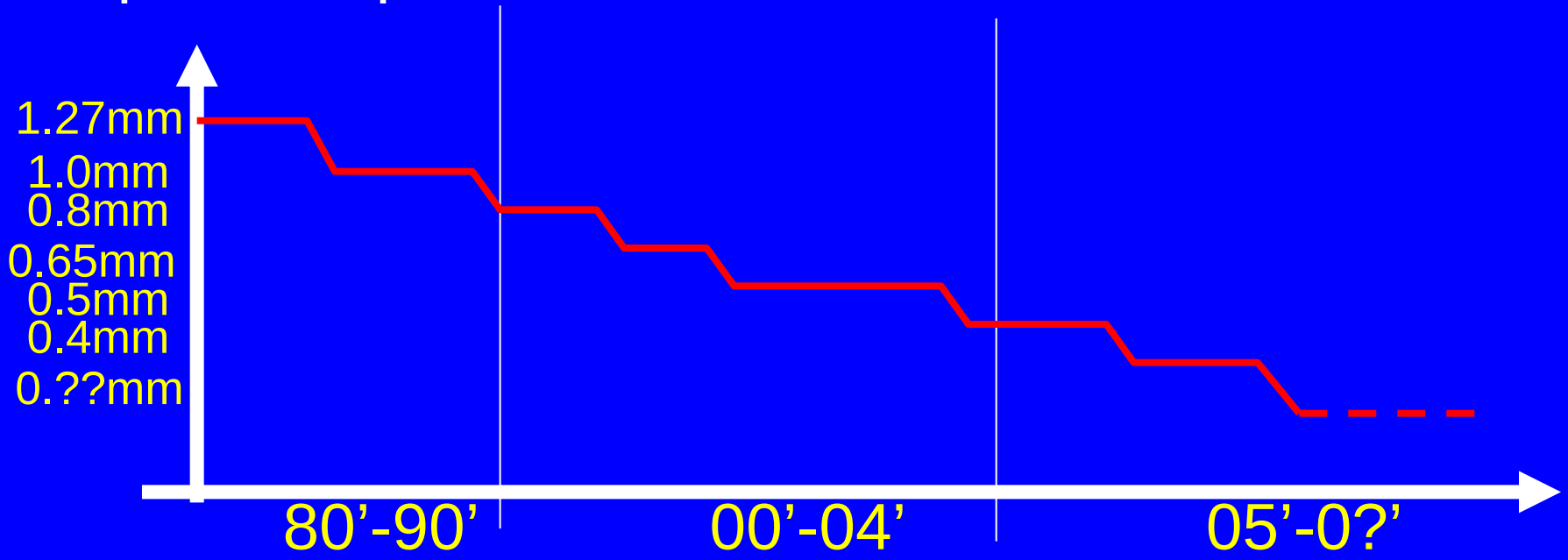
80s-90s
Big and Bulky

Late 90s
Size reduction

Future ?
All in One

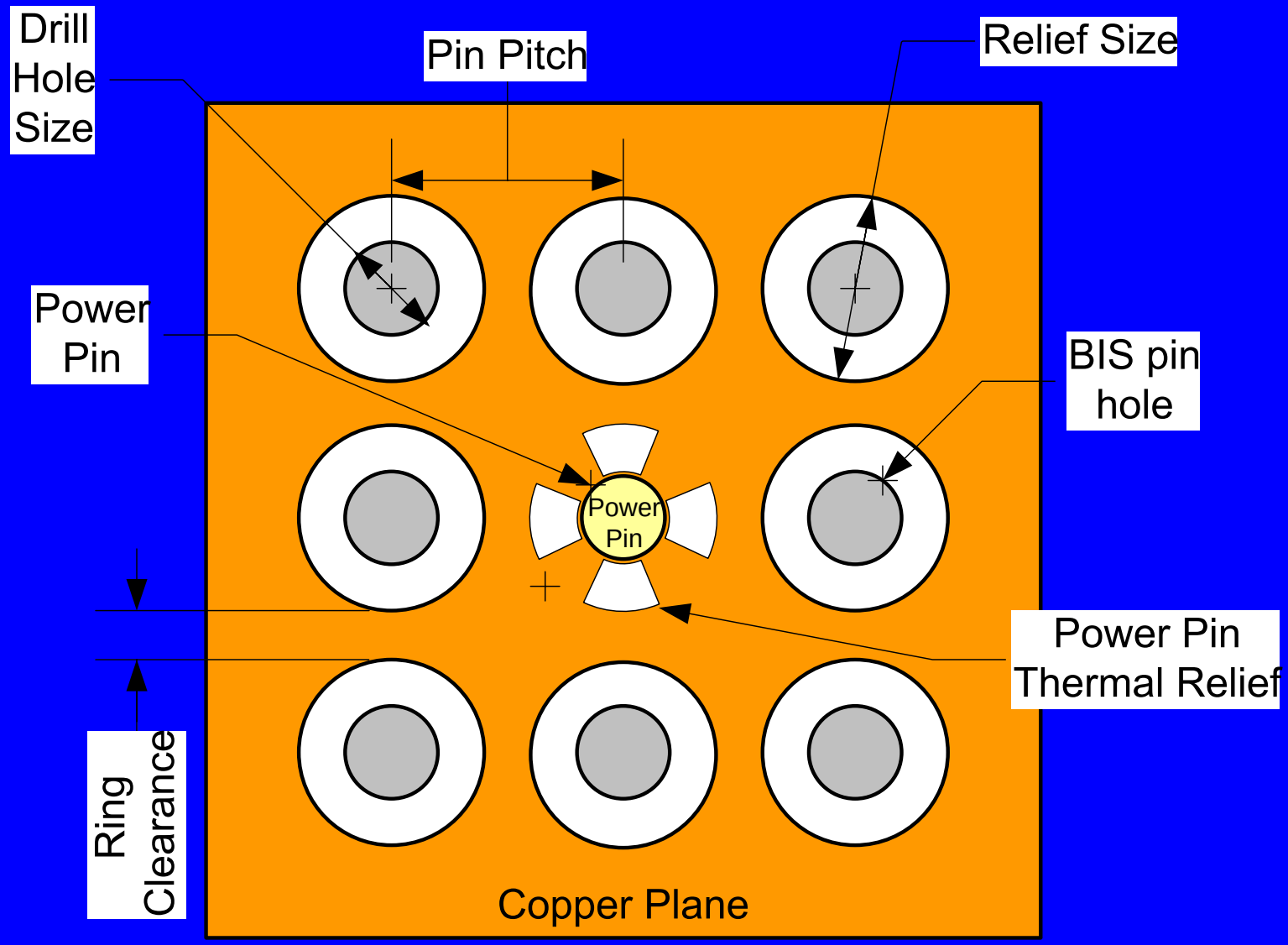
Industrial Package Pin Pitch Trend

- Technology companies are pursuing smaller and better products to suit consumers' needs.
- Available spaces for devices are shrinking.
- Required smaller package, finer pitch device to optimize space utilization



- Pitch shrinkage post a challenge to conventional PCB design and manufacturing.

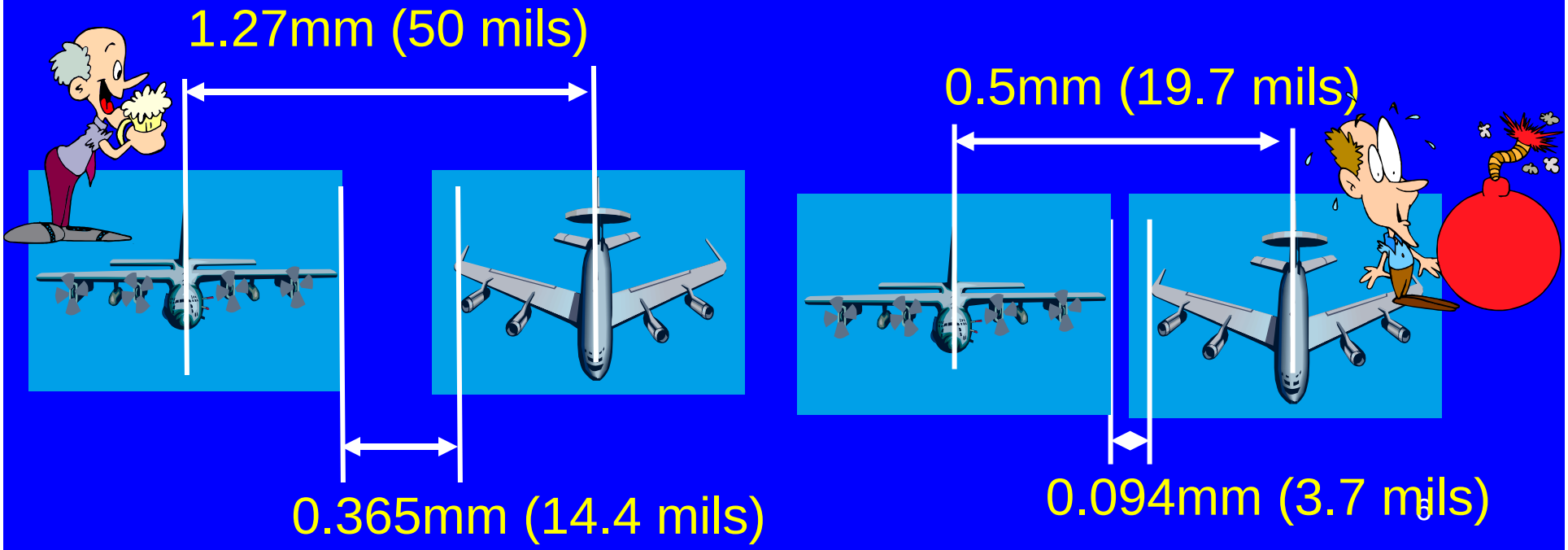
Conventional Fine Pitch Power Plane Design



Ring Clearance Calculation Examples

	Case I	Case II
Pin Pitch	1.27mm (50 mils)	0.50mm (19.7 mils)
BIS Hole Size	0.6mm (23.6 mils)	0.203mm (8.0 mils)
Relief Ring Size	0.905mm (35.6 mils)	0.406mm (16.0 mils)
Contact Width	0.365mm (14.4 mils)	0. 094mm (3.7 mils)

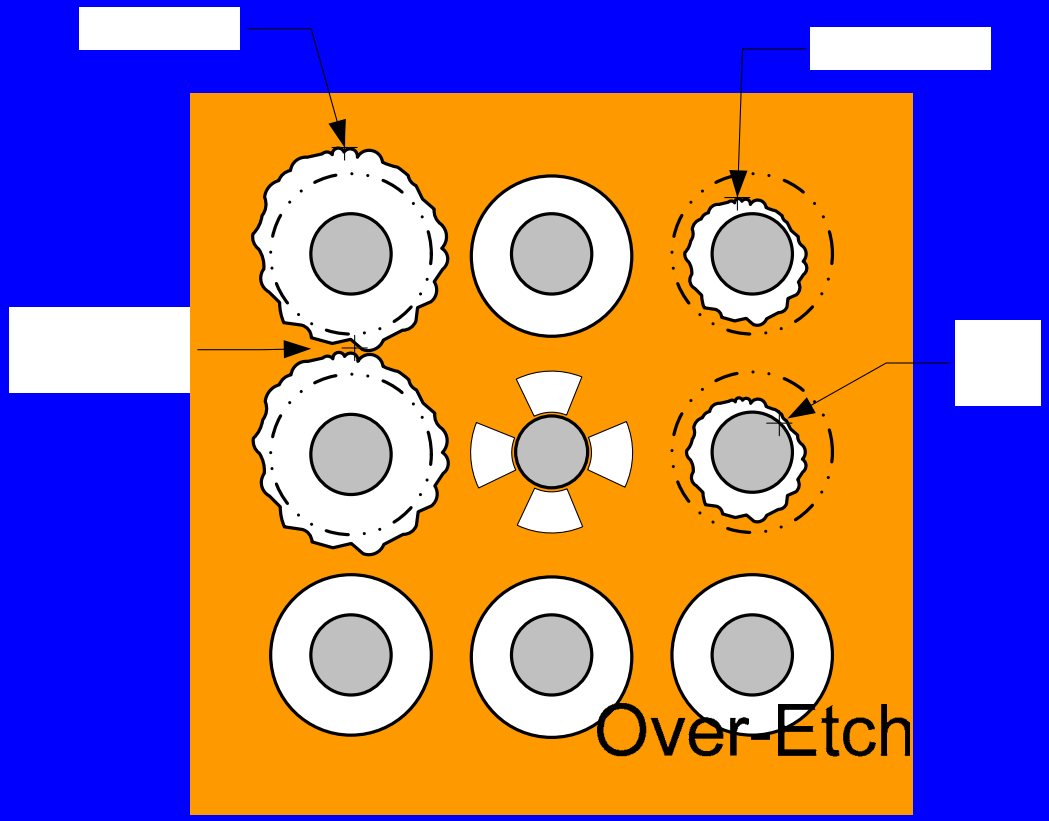
74% Reduction



Area of Concern 1

Etching Process

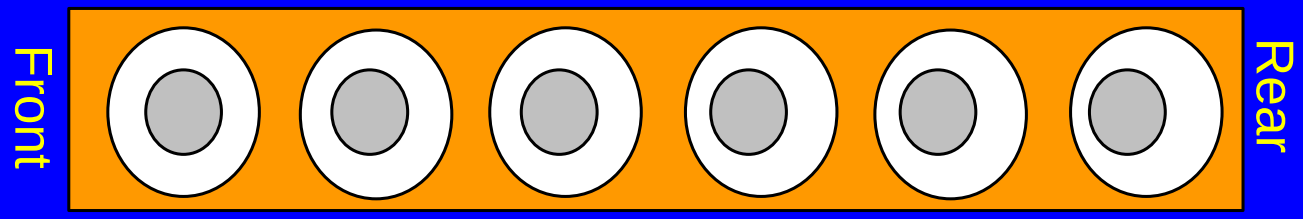
1. Over-etch/under-etch of smaller relief: < 5 mils
   - Broken connection
   - Poor isolation for non-power pin

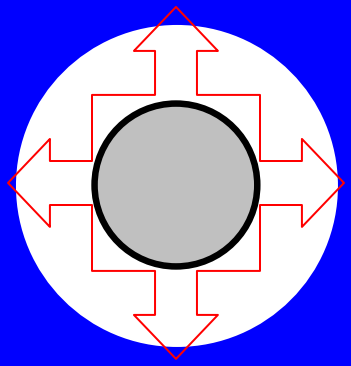


Area of Concern 2

Drilling Process

1. Registry/Alignment over a big size board.
   - Position tolerance – Drill wandering
   - Progressive Error
2. High yield loss during PCB drilling



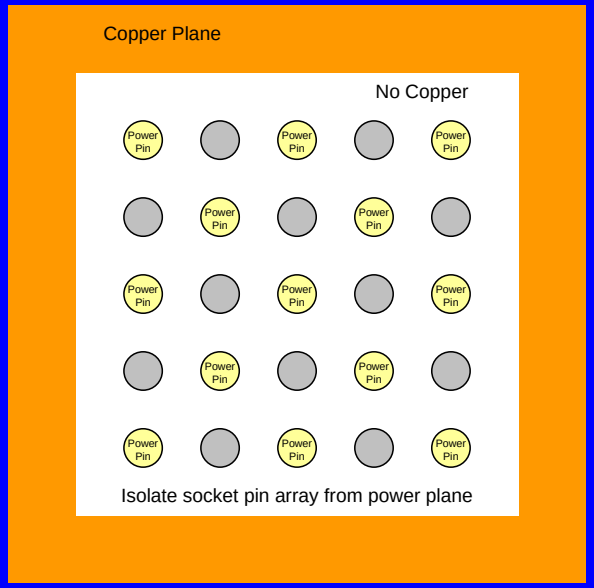


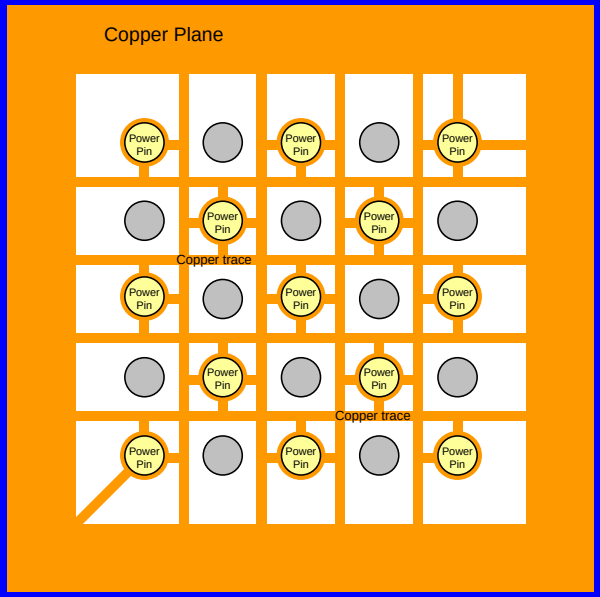
Common Method

1. Slow down machine run rate and close monitoring
2. Frequent Machine calibration and maintenance
3. Machine upgrade
   - Better etching
   - Finer and more accurate drilling
   - Laser Drilling option
4. We need an innovative way!

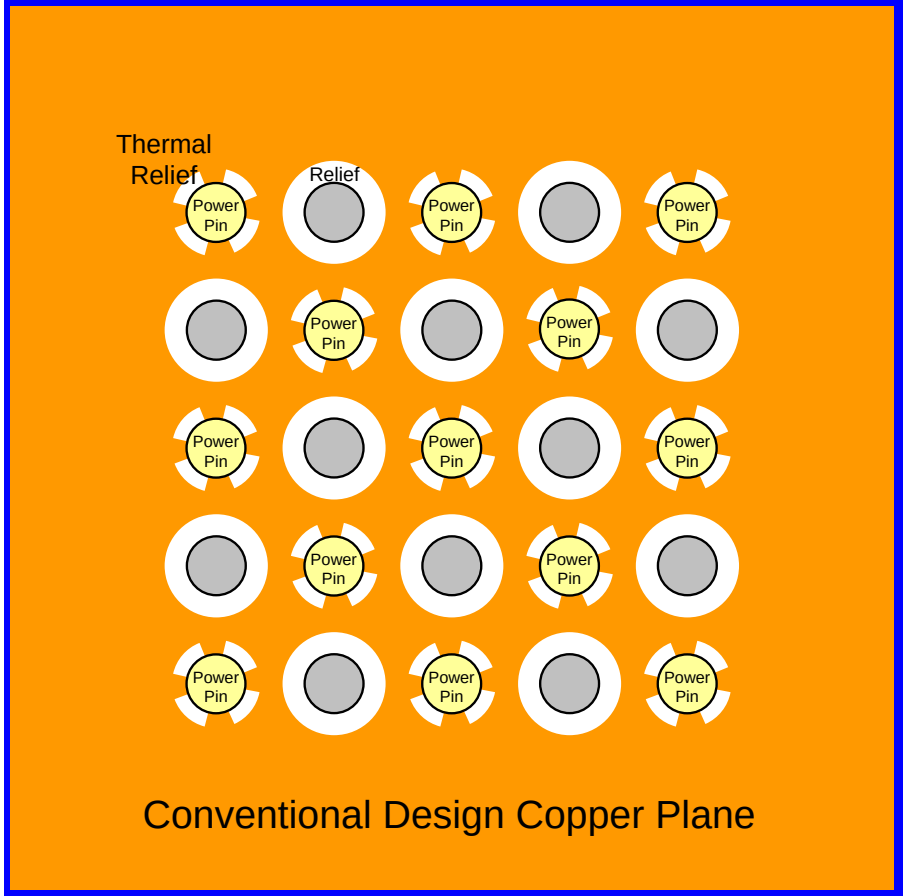
Trace/Grid Design Method

- Innovative power plane design method
  - Improve PCB manufacturing yield
  - Zero additional cost
- Isolate socket pin array from power plane
- Use traces to connect power pin (GND / VCC) to power plane
- Non-power pins will be left isolated.
- Provides wider isolation / relief from power plane.

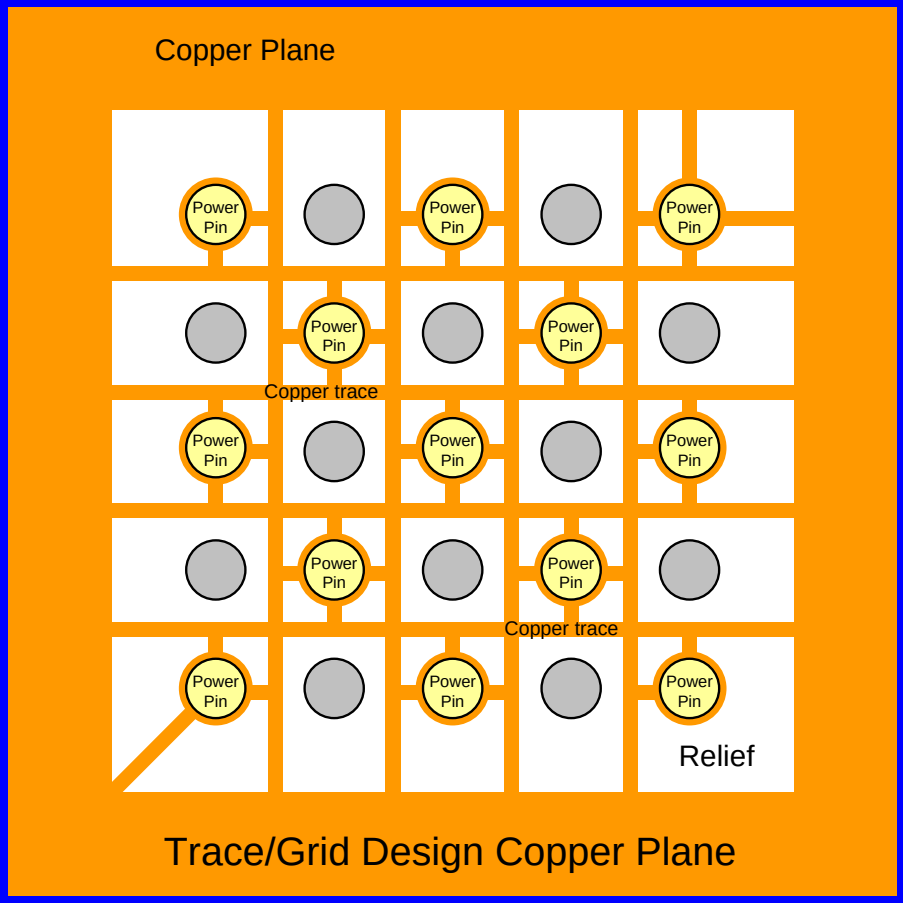




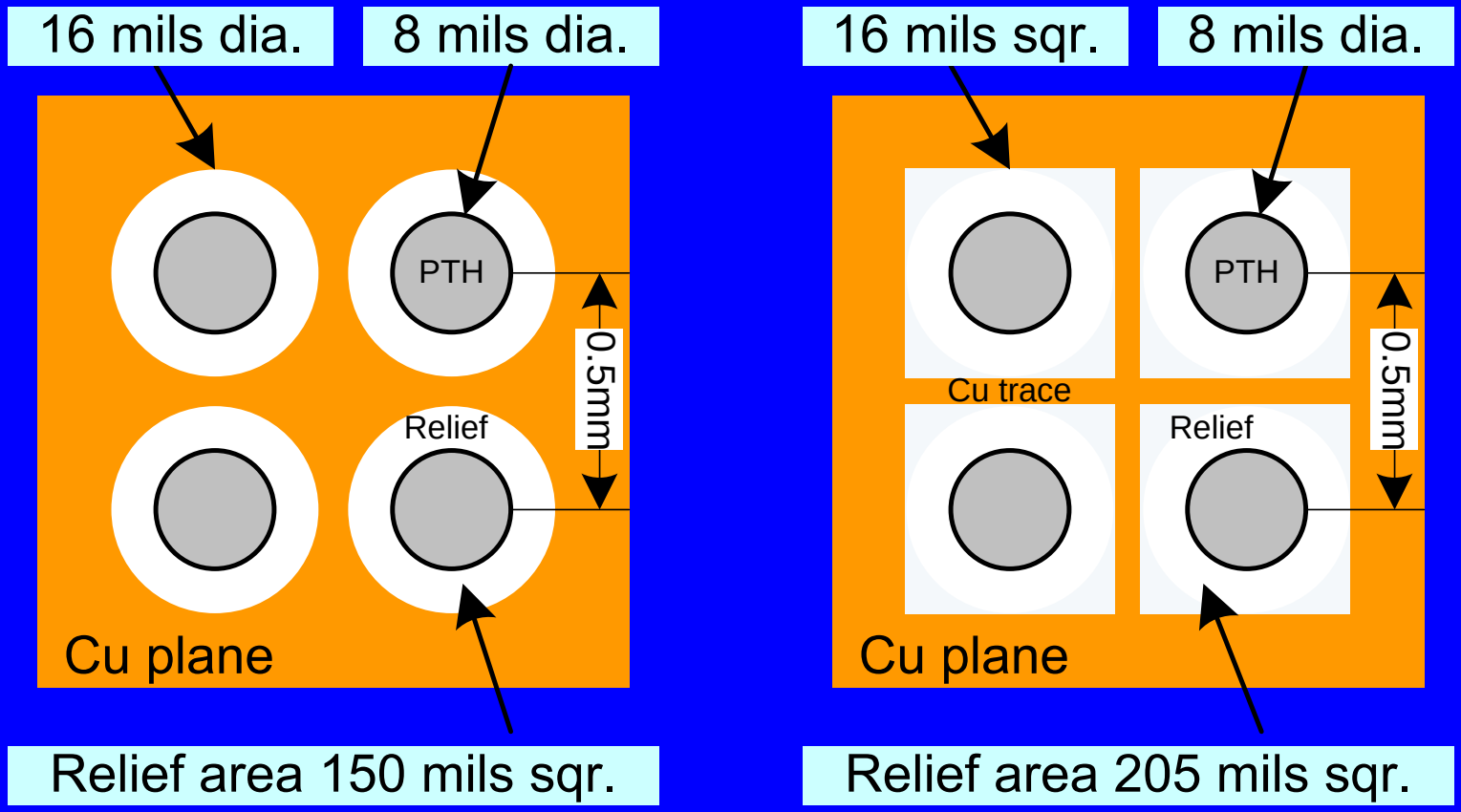
- Small relief ring isolate Non-power pins from power plane.



vs

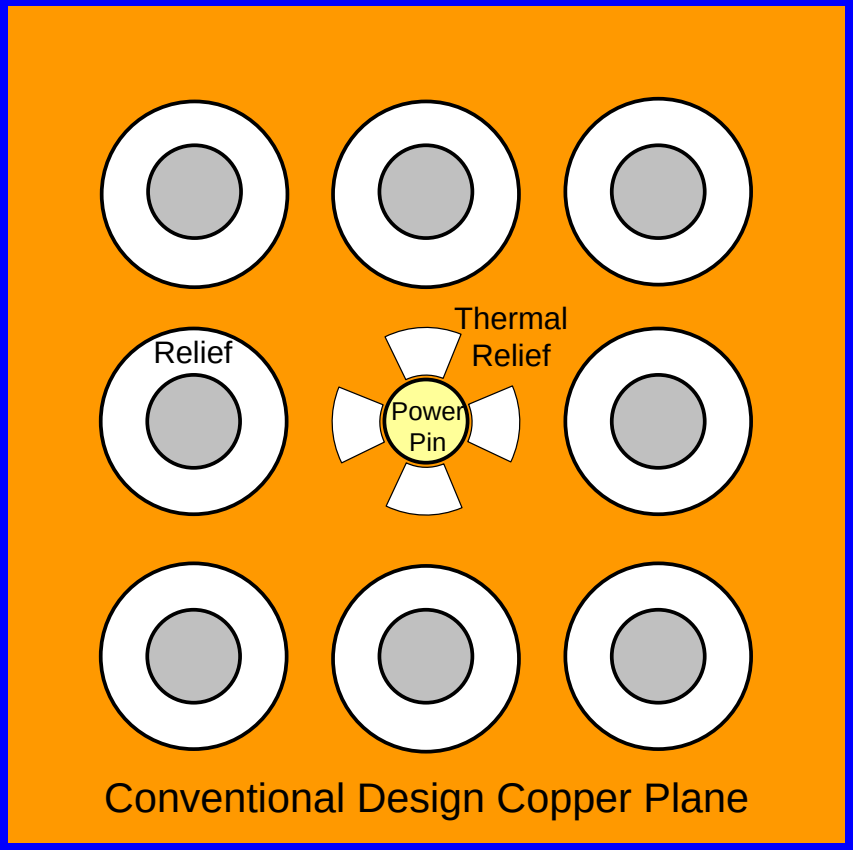


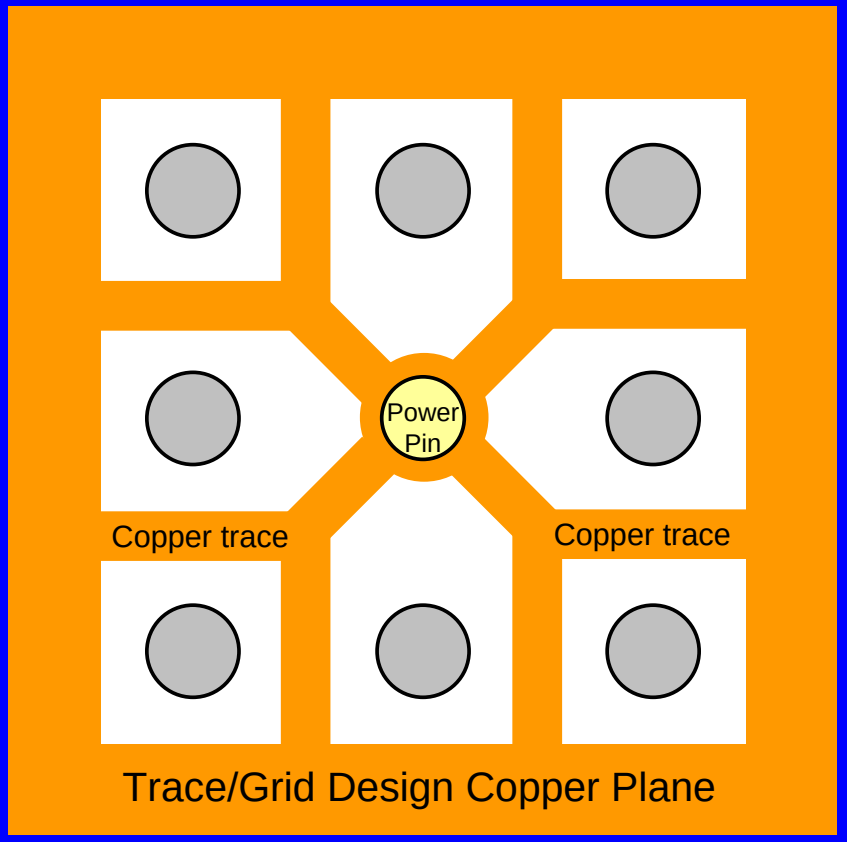
- Wider isolation / relief from power plane.



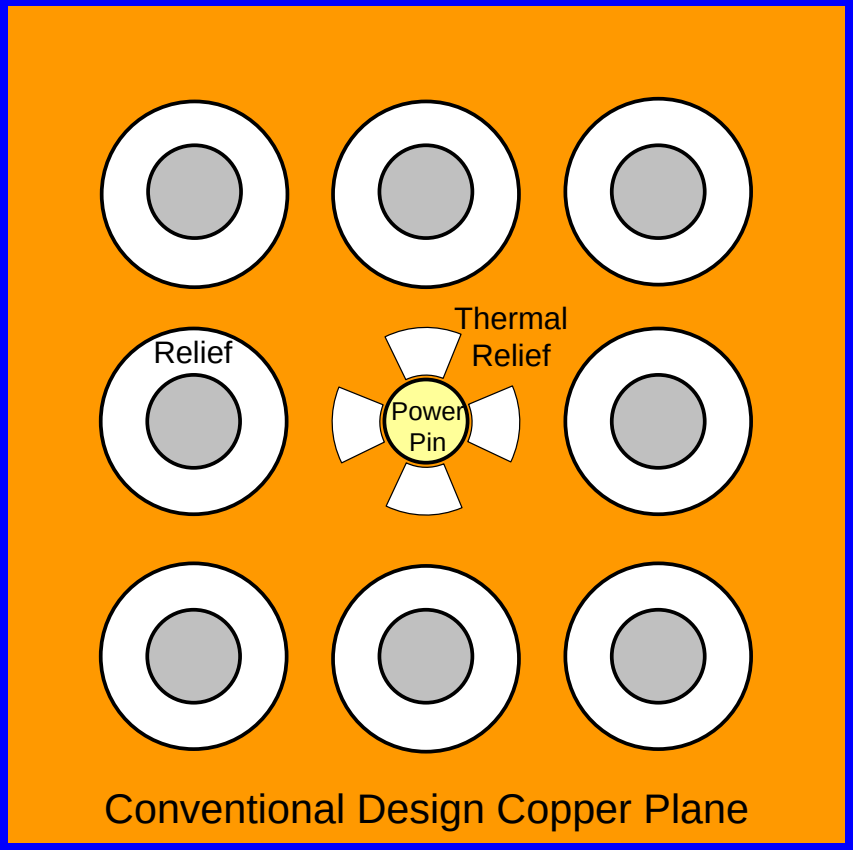
- Relief area improved by >36%.
- Provides better tolerance for etching and drilling process.

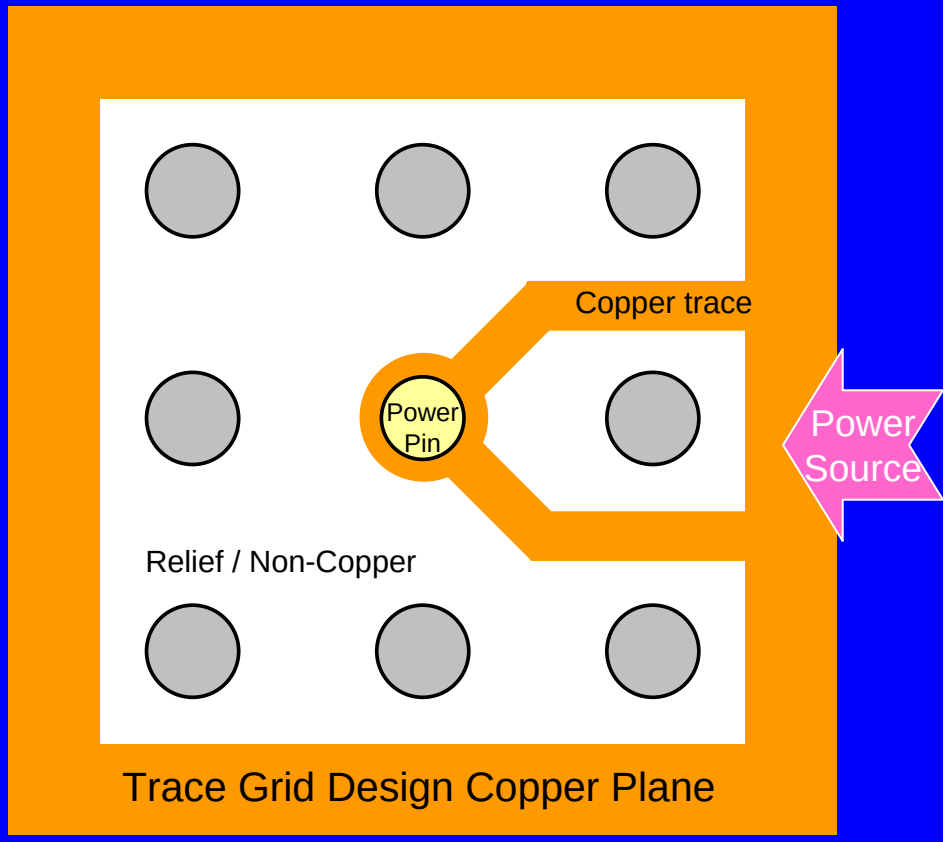
Different Ways of Trace/Grid Power Plane Design



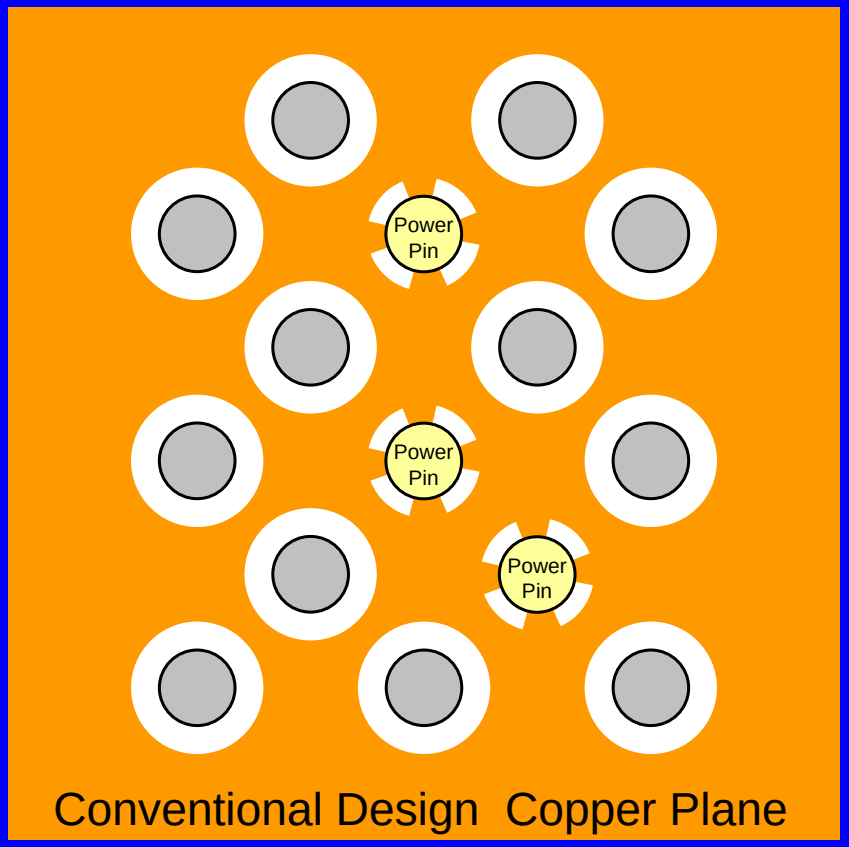


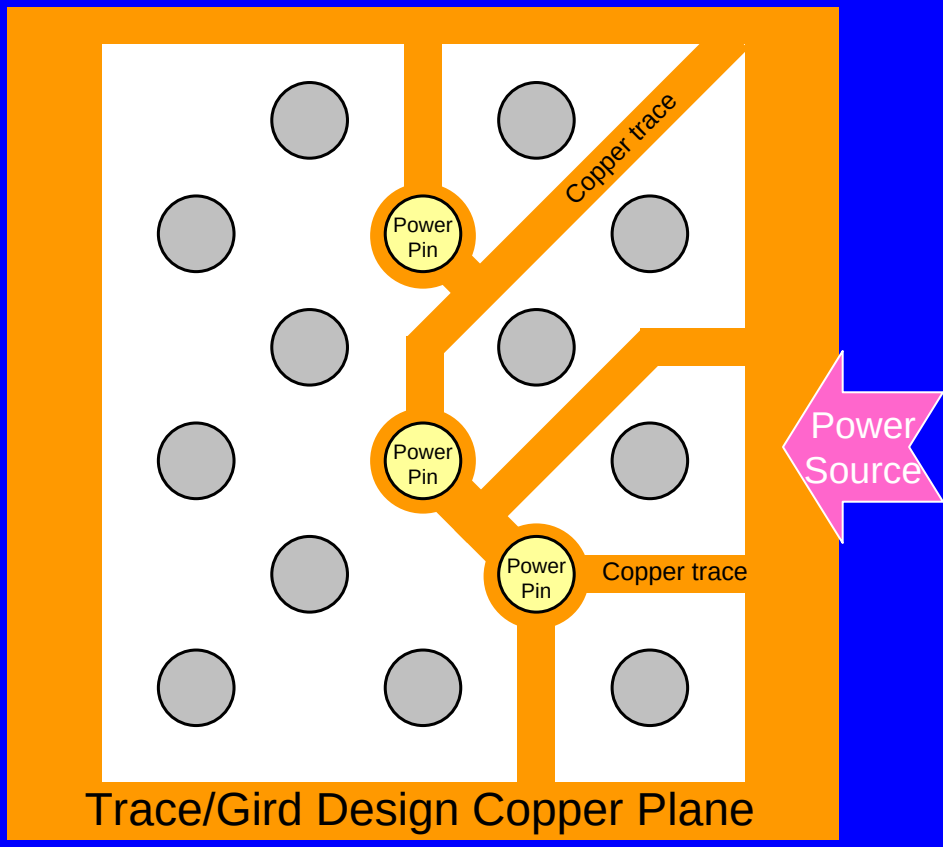
- Power pin at center of grid.
- Route traces from all directions.



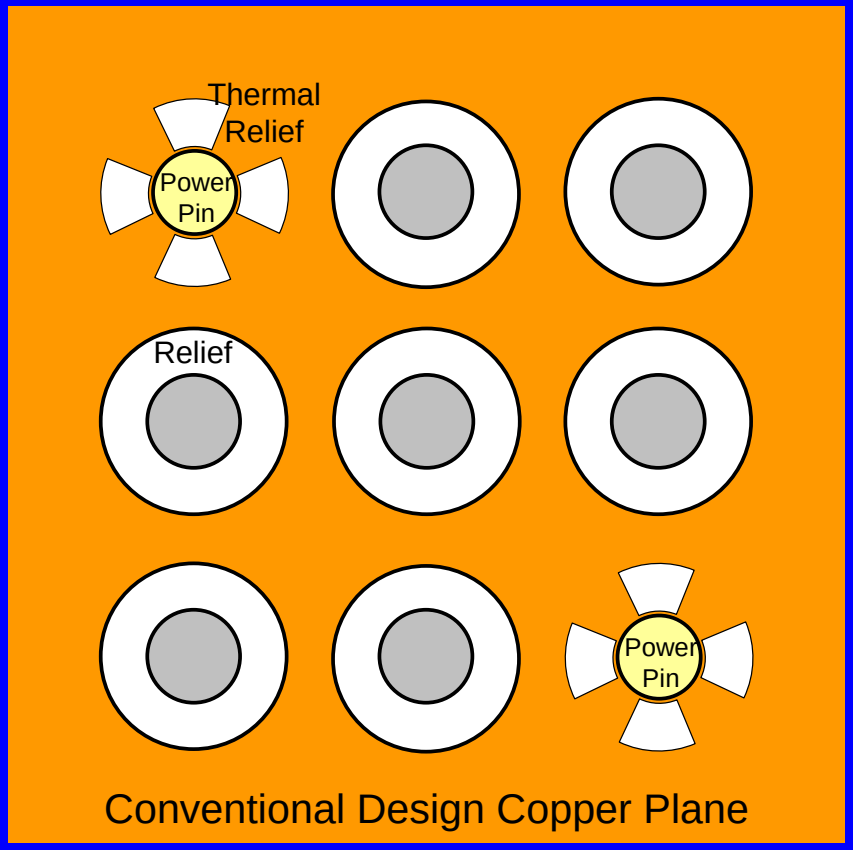


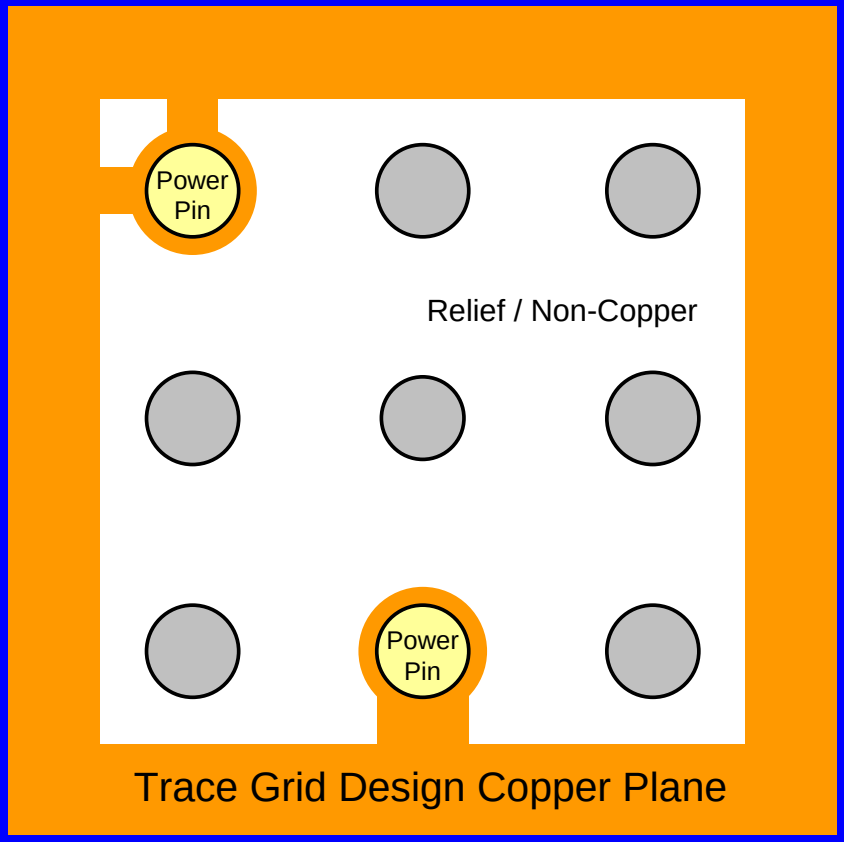
- Power pin at center of grid.
- Route traces from power source direction.



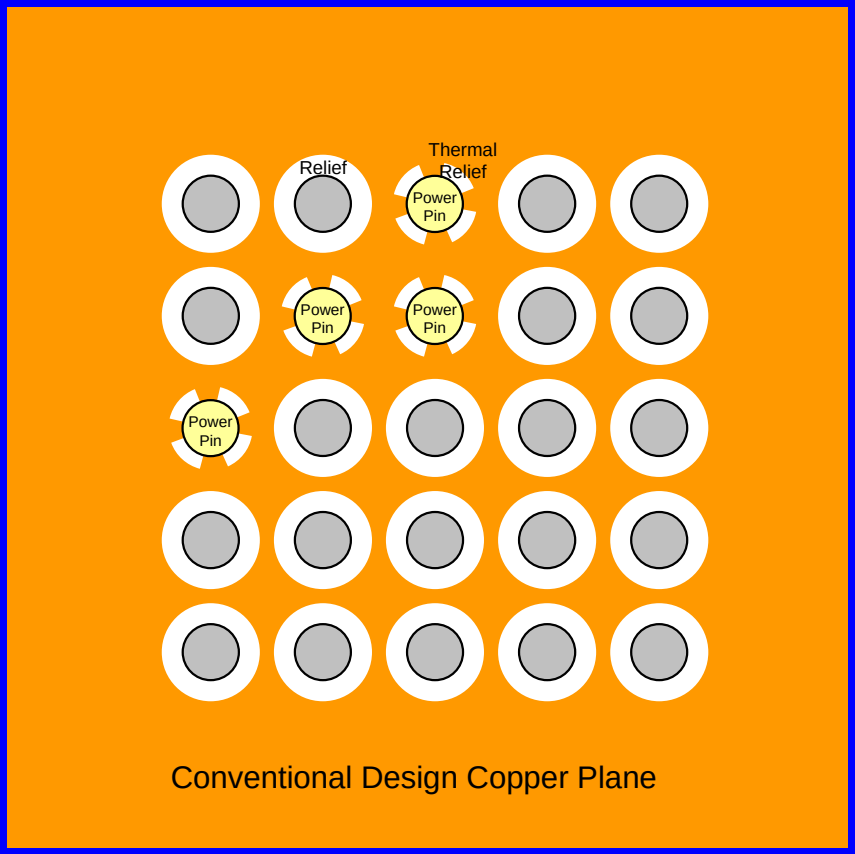


- Staggered grid array.
- Route traces in 45º to power pin.
- Route traces from power source.

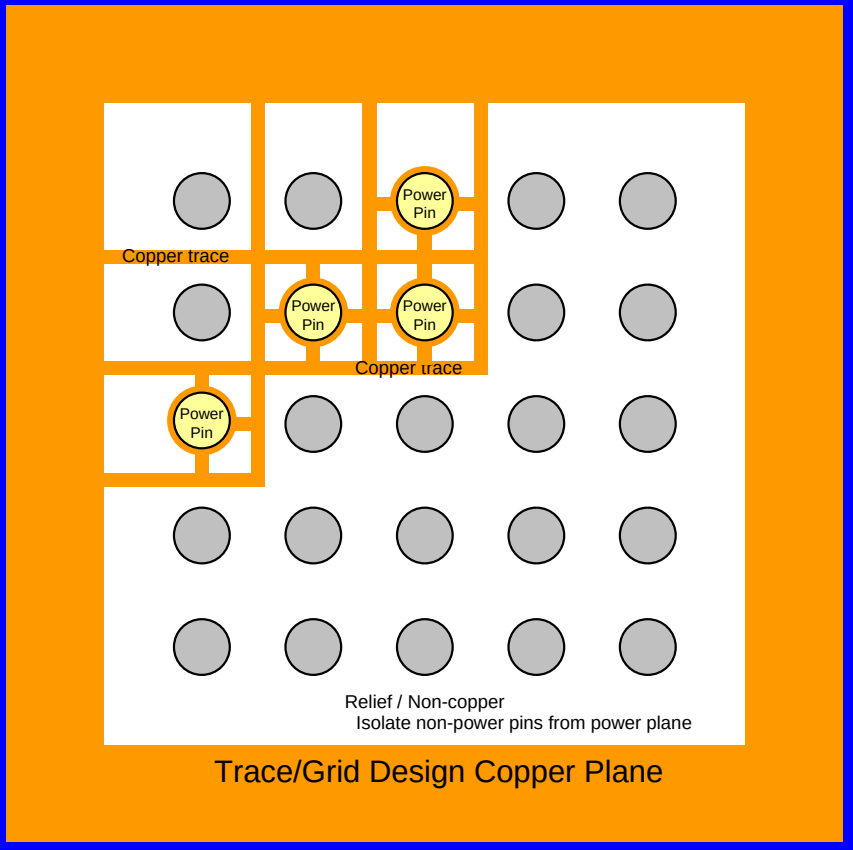




- Power pin at edge of grid array.
- Use wide trace or multiple traces.



Conventional Design Copper Plane



Trace/Grid Design Copper Plane

- Power pin at corner of grid array.
- Route traces from corner to power pins.
- The rest of the area/non-power pins can be isolated.

Power Delivery Performance

- Assumption:
  - 1 oz copper, 250mils trace length, 3.7 mils trace width.
  - 80mA per power pin

	Conventional	Trace/Grid
Resistance	30mΩ	32mΩ
Voltage drop	2.4mV	2.6mV
Current Carrying Capacity	1.32A	1.31A

Conclusions

1. Trace/grid method improved non-power pin relief / isolation by >36%
2. Improved PCB manufacturing yield without additional cost
   - Wider etching and drilling margin tolerance
   - Improve machine run rate
3. Minimal impact to power delivery performance
   - Short power traces
4. More fun in fine pitch power plane design
   - Designer's creativity in power trace routing

TRIO-TECH INTERNATIONAL

2005 Burn-In & Test Socket Workshop

Leakage as the Filaments and Dendrites Form in PWB

Sungalingam Kumaran (Engineering Manager)

BiTS
BURN-IN & TEST SOCKET WORKSHOP

We are certified QS9000

Outline

1) Objective
2) Introduction
3) Electrochemical Migration (ECM)
4) Dendrites Formation
5) Conductive Anodic Filament Formation
6) MTF Modeling for CAF
7) Dendrites vs Filament
8) Variable influencing CAF and ECM
9) Technology
10) Summary

1) Objective

- To present the cause for leakages
- The formation of filament and dendrites
- Predictive tool to project PWB's CAF susceptibility
- Process influence in leakages
- Ways to minimize the menance

2) Introduction

- Continuing miniaturization process is threaten by Leakage caused by Electrochemical Migration in PWB severely affect PCB lifespan.

- With circuit density ever increasing, the condition of this failure mode is becoming more prevalent

- Electrochemical Migration is a condition, that emerge in PCBs that passed all electrical test when leaving factory but can fail in field

- Reliable PCB may be achieved by controlling design material and manufacturing process.

3) Electrochemical Migration (ECM)

- Electrochemical migration is defined as the growth of conductive metal filaments on PCB under the influence of DC bias voltage. This often occurs on surface of board

- Another type of an electrochemical phenomenon is CAF growth, which occurs inside the material surface.

3) Electrochemical Migration (ECM)

- ECM occur on PCB that are exposed to moisture and electrical field:-

- Electrochemical reaction at anode are
  - $H_2O \rightarrow ½O_2 + 2H^+ + 2e^-$
  - $Cu \rightarrow Cu^+ + e^-$
  - $Cu \rightarrow Cu^{2+} + 2e^-$
  - $Sn \rightarrow Sn^{2+} + 2e^-$
  - $Sn \rightarrow Sn^{4+} + 4e^-$

3) Electrochemical Migration (ECM)

- Electrochemical reaction at cathode are

  - $O_2 + 2H_20 + 4e- \rightarrow 4OH^-$
  - $2H_2O + 2e^- \rightarrow 2OH^- + H_2$
  - $Cu^{2+} + 2e^- \rightarrow Cu$
  - $Cu^+ + e^- \rightarrow Cu$
  - $Sn^{2+} + 2e \rightarrow Sn$
  - $Sn^{4+} + 4e^- \rightarrow Sn$

4) Dendrites Growth

- **One form of ECM is Dendritic growth where electrolytic dissolution of the metal occurs at the anode and reduction of the metal ions occurs at the cathode**

- **As the surface dendrites grows, their effect on the insulation resistance is minimal until they are very close to the anode**

Fig 1:-Surface PCB dendrites as a result of contamination[5]

5) Conductive Anodic Filament(CAF)

- Another form ECM is Conductive Anodic Filament Formation

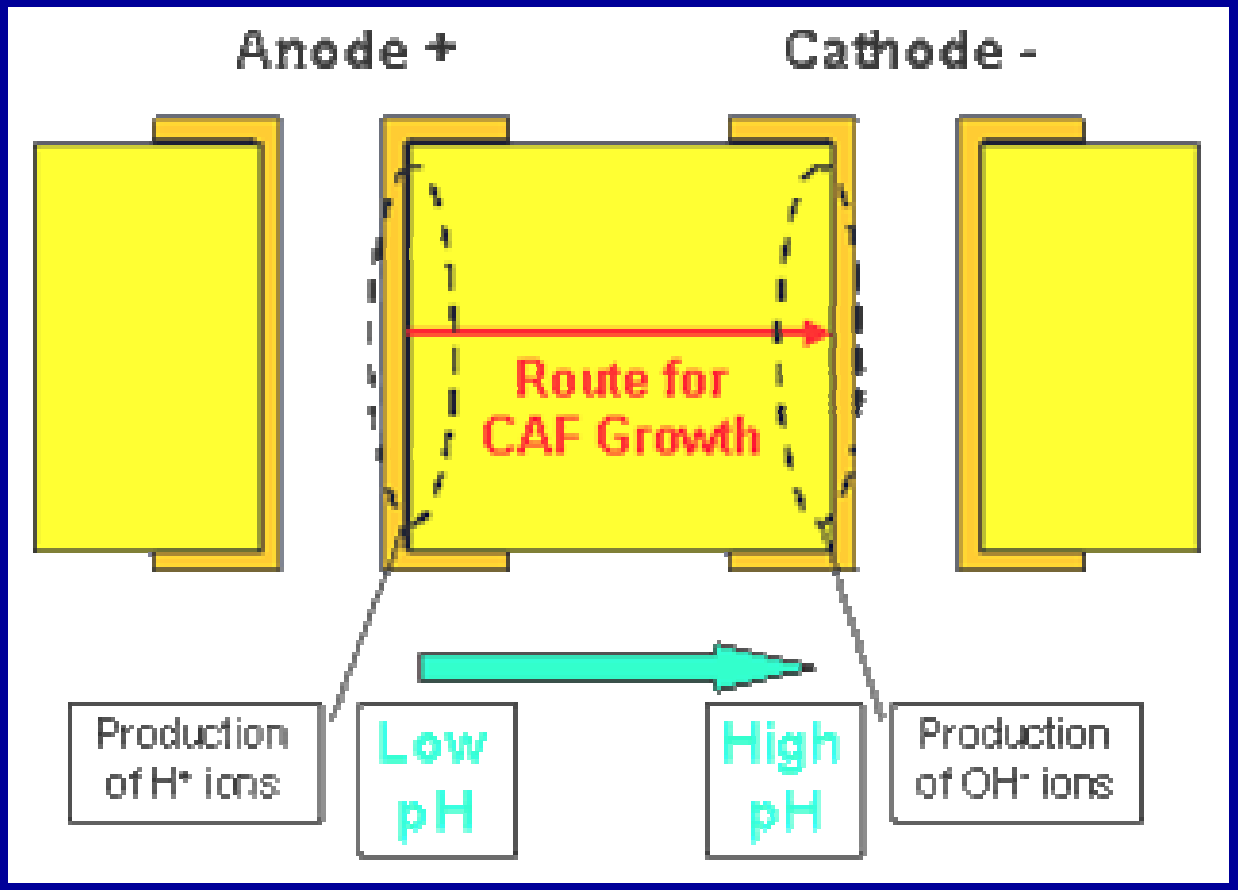
- This Failure mode is characterized by an abrupt, unpredictable loss of Insulation Resistance between conductors held at a potential difference.

- This is result of ECM process that initiates at the anode and proceeds along separated fiber/epoxy interface

- Punch-thru is a similar to CAF, except the filament grows between circuit layers rather than along a fiber.

5) Conductive Anodic Filament(CAF)

Schematic of CAF growth between two vias via glass fibre



6 CAF Formation Model for PCB

- The Failure model for CAF composed of factor shown to affect MTF for CAF
- CAF failure modelled can be simplified as[1]

$$MTF = AV^{-m}KL^{n}(RH)^{-b}\exp(Ea/kT)$$

Where; Ea is the activation energy
k is Boltzmann's constant
T is absolute temperature
RH is relative humidity
V is voltage
L is the gap separation
K is a conductor shape factor
m is voltage factor
n is gap size factor
b is humidity factor
A is constant factor

7) Dendrites vs Filament (CAF)

- Dendrites growth is easily differentiated from CAF

- In Dendrites growth, metal ions go into solution at the anode but plate out at the cathode
- In contrast, CAF growth from the anode via a fiber/epoxy interface

- Dendrites contains pure metal and is a surface phenomenon
- Wherelse CAF contains copper halide ions and is a subsurface phenomenon

8) Variables influencing CAF and ECM

- In dense multi-layer PCBs this can often occur at the PTH wall where the plating has ingress into the glass reinforcement fibre

- Initial weakness introduce by drilling

- Subsequence plating solution ingressing during plating of vias

- Application of and electric field and humidity, ion transports proceeds along the weaken fiber.

8) Variables influencing CAF and ECM

- **Process variables that can affect CAF:-**
  - PCB Material
  - Hole Wall quality & Drilling
  - Ionic impurities in PWB fabrication
  - Environment
  - Polyglycol
  - Washing Process
  - Conductor Spacing
  - Operating Voltage

8.1 PCB Material

- Of the material tested by investigator[2], the BT and Polymide material is more resistance to CAF formation.

- Lately several supplier are coming up with CAF laminates and some has been proven to be CAF resistance.

- The susceptibility of the material is detailed in table[2]

Laminate Material	Susceptibility to CAF
FR4	Moderate
G10	Low
Polyimide	Very Low
BT	Very low

Note:-There New CAF resistance material in the market to be investigated
E.g.:- DICY free Resin material[4]
Non-Woven Glass

8.1 PCB Material

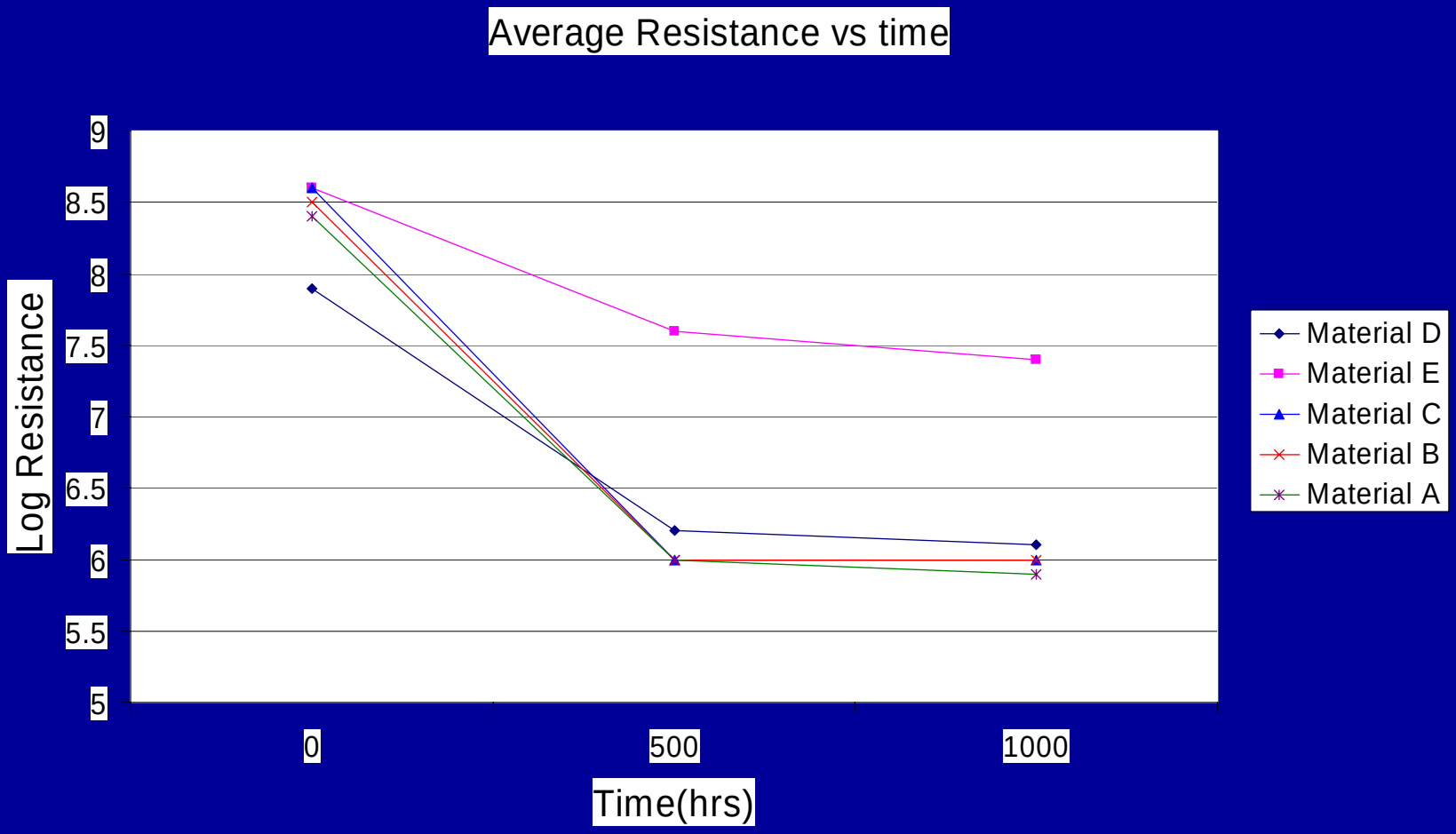


Figure :- Average insulation resistance versus time, hole to hole spacing [3]

8.2 Drilling & Hole Wall Quality

- Current understanding propose that drilling can introduced further weakness.
- Where the fibre end get damaged
- Subsequent plating of the vias results in plating solution ingressing some way along the fibres
- Laser drilling will not lead to this susceptibility
- Problem can be reduced by controlling the drill hits and speed.

8.3 Ionic impurities in PWB

- Ionic impurities present and chemical used during the fabrication of inner and outer layers assist in creation of ECM between conductors

- Improved DI water rinsing and rinse water resistively monitoring is needed.

- Fabrication material shall be stored and handled in a manner minimising ionic impurities being transfer onto PWB material.

8.4 Environments

- High level of moisture could lead to serious reliability concerns and field study shows that conformal coating does not substantially improve HAST board electrical performance.[4]

- Moisture leads to metal migration, delamination and poorer electrical performance

- Moisture is absorbed during storage and transportation. Hence board should be baked or keep in dry environment before supplying power to reduce the occurrence electrochemical migration

- Extreme temperature exposure is potentially harmful to PWB's CAF performance

8.5 Polyglycol and WSF

- Studies[4] has correlated the presents of some ionic contamination to polyglycol diffusing into the PWB

- Research by Alpha Metal showed that Surface Insulation resistance is affected by:-

Degree of Flux absorption

Hygroscopicity of flux

Effectiveness of cleaning process

Humidity

Presence of water soluble ions on the PCB surface

Temperature

8.5 Polyglycol and WSF

• Study has shown that choice of Flux and Temperature influence CAF formation[4]

Flux Type	SIR (ohm) 201^0C Reflow	SIR (ohm) 241^0C Reflow	# CAF at 201^0C Reflow	# CAF at 241^0C Reflow
PEG	$<10^6$	$<10^6$	90	55
PEG/HBr	$<10^6$	High 10^8	None	None
PPG	$>10^{10}$	$>10^{10}$	None	455
PPG/HBr	$>10^{10}$	$>10^{10}$	1	423
GLY	$>10^{10}$	High 10^9	None	56
GLY/HBr	$>10^{10}$	High 10^9	3	104

Table 2:- Comparison of SIR levels and number of CAF associated with different flux and temperature[4]

8.6 Washing

- Board Fabrication House need to minimise ionic residue on board
- WSF have gain widespread favour among manufacture. Whichever method is chosen, it is essential that all flux residue be removed from PCB
- Cleaning is more difficult when the PCB has components with a small standoff
- If flux or other ionic residue are allowed to remain on the PWB, then ECM, corrosion and hence electrical malfunction could occur.

8.7 Conductor spacing and voltage

- Another critical factor used in determining CAF susceptibility is the voltage gradient. Minimising voltage gradient in PCB design is essential to reduce CAF formation
- Minimising Adjacent PTH aligned with the glass fibres as CAF grows along fibre
- Minimising via hole
- Minimising PTH Diameter
- Maximising PTH to PTH/trace distance

9. Technology

New material and technology need to be proven using standaderdise CAF test board (IPC-TM-650 CAF resistance test)

a) **Woven and Nonwoven reinforcements in PCB**

b) **Resin system based solution[3]**

c) **Inorganic filler with high affinity for metal ions[7]**

d) **Laser and Mechanical Drilling**

e) **Etching and Rinsing**

f) **Layer registration and Image transfer**

10. Summary

In conclusion:

- **Awareness of CAF mechanism and implementation of prudent design practices in susceptible application will minimise the likelihood of CAF becoming a future PCB limiting life constrain.**
- **MTF model discussed can contribute to certainty in future MTF prediction.**
- **CAF issues need to be collectively address as an industry since CAF often results from process and material interactions**

11. References

[1] Lando,D.J.;J.P.Mitchell and T.L. Welsher."Conductive Filaments Reinforced Polymeric Dielectric: Formation and Prevention," 17th Annual Proceedings Reliability Physics.

[2] Mitchell, J.P and Welsher, T.L "CAF growth in Printed Circuit Material." Proceedings of Printed Circuit World Convention II, pp 80-93 (1981).

[3] Erik J.Bergum CAF "Resistance of NON-DICY FR4" PC FAB, September 2002.

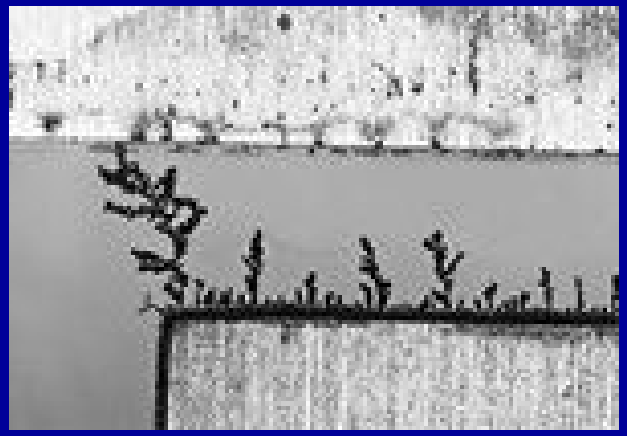
[4]Laura J.Turbini and Stuart R.Stock "Evaluating the effect of conformal coating in reducing the rate of CAF formation", Geogia Tech project E18-T43.

[5]Alan Brewin, Ling Zou & Christopher Hunt, "Susceptibility of Glass-Reinforced Epoxy Laminates to CAF", National Physical Laboratory, UK Report, Jan 2004

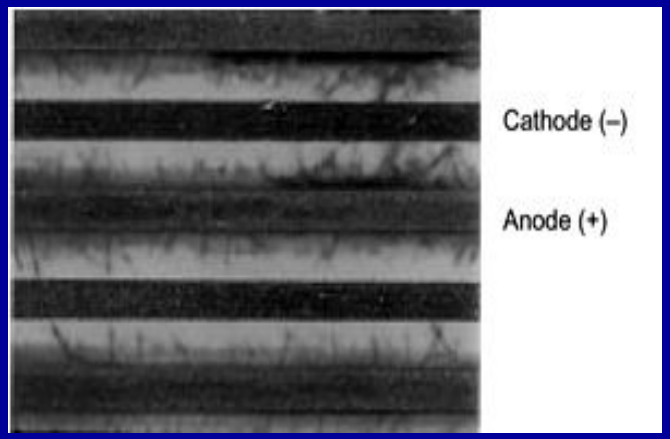
[6] Shigeharu Yamamoto, Hiroko Katayanagi, Hirokazu Tanaka and Yuichi Aoki, "The effects of absorbed water on PCB and the process of ionic migration" ESPEC Technology report, April 2002

[7]Velpari, Vedagiri."Electronic support methods and apparatus", US Patent Application 200200888 Kind Code A1, Jul 2002

12. Questions



Dendrites



CAF

WHY CAF:-

PWB Material

FAB Process

Geometries...

Challenges In High Current PCB Power Delivery

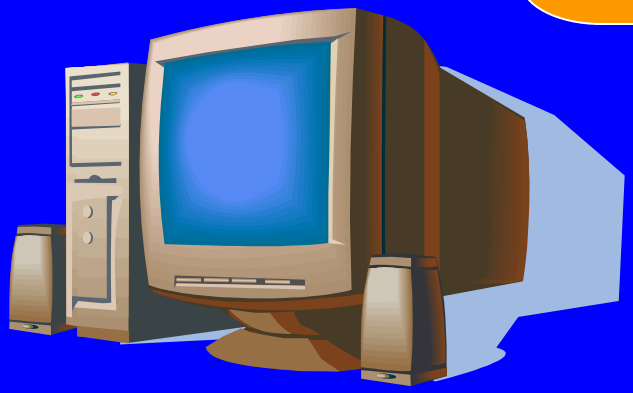
Hon Lee Kon
Anthony Wong Yeh Chiing
Intel Test Tooling Operations

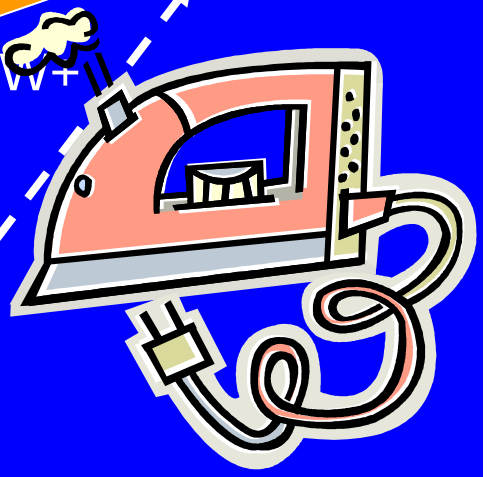
BiTS™
Burn-in & Test
Socket Workshop

Agenda

- Microprocessor Power Trend
- Burn-In Requirements
- Problem Statement
- Design Challenges
- Power Delivery Solutions & Limitations.
- Technical Challenges

Microprocessor Power Trend



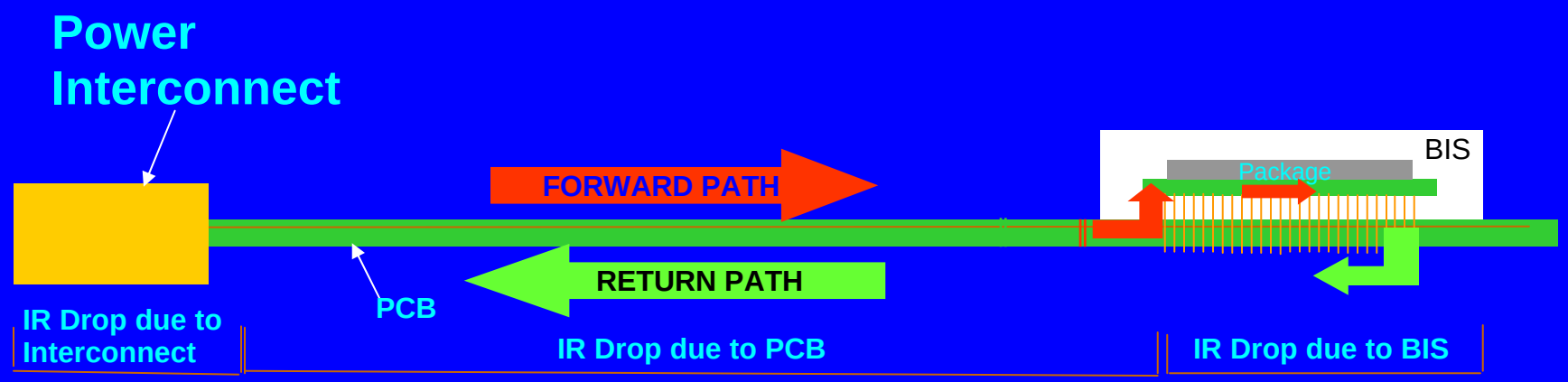


Future Burn-In Requirements

- Microprocessor Speed ↑
- Burn-in power ↑
- Current consumption ↑
- Burn-in voltage ↓
- Dynamic stress duration ↓
- Device thermal dissipation requirement ↑
- Power delivery performance ↑

Problem Statement

- **Excessive voltage drop along power delivery path during high current flow.**
- **Understanding of Current Carrying Capacity (CCC) is becoming more important**
  - Power Interconnect
  - Forward & Return PCB Path
  - BIS Pins

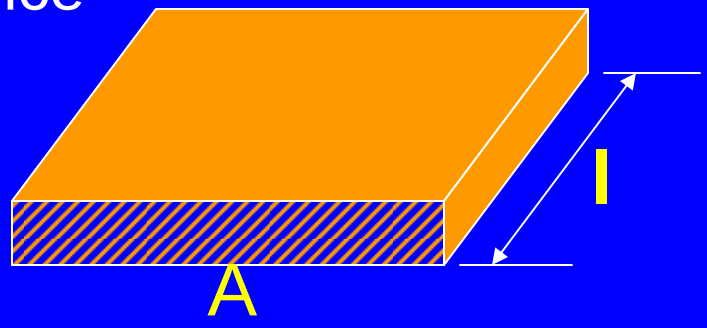


Design Challenges

- **Minimum voltage drop**
  - Minimal Conductive Path resistance

$$R = \frac{\rho(T)\, l}{A} \text{ ohms}$$

R = Conductor resistance
ρ(T) = Material Resistivity
l = Conductor length
A = Conductor X-section area



Resistivity, ρ
Cu 1.7 x 10^{-8} Ωm
Al 2.6 x 10^{-8} Ωm

- **Resistance of an electrical conductor depends on:**
  - Length of the conductor, **l**
  - Cross-sectioned area, A
  - Type of material – Resistivity value
  - Material operating temperature

Design Challenges

- **High current delivery >100 Amps per device**
  - Current Carrying Capability

$$I = k * \triangle T^{\beta 1} * W^{\beta 2} * Th^{\beta 3}$$

Equation source: Douglas Brooks, UltraCAD Design Inc

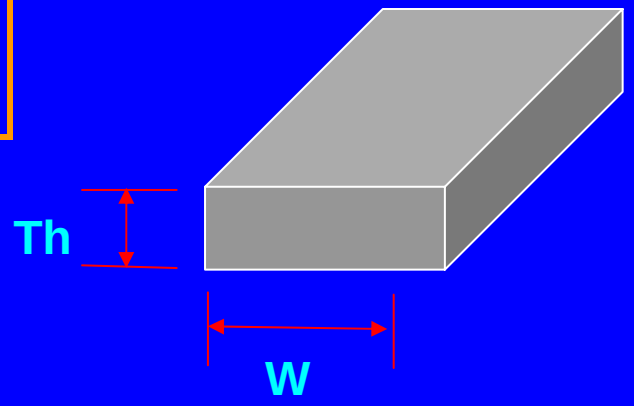
I = Current (A)

△T = Temperature rise (°C)

W = Conductor width (mils)

Th = Conductor thickness (mils)

K, β1, β2, β3 = constant



- **CCC depends on:**
  - Cross-sectioned area, A (W x Th)
  - Type of material – Material operating temperature
  - Acceptable amount of heat rise

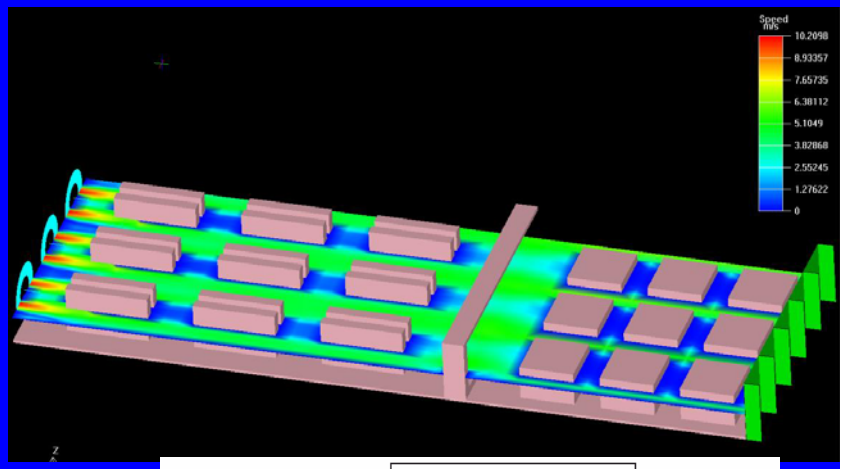
Design Challenges

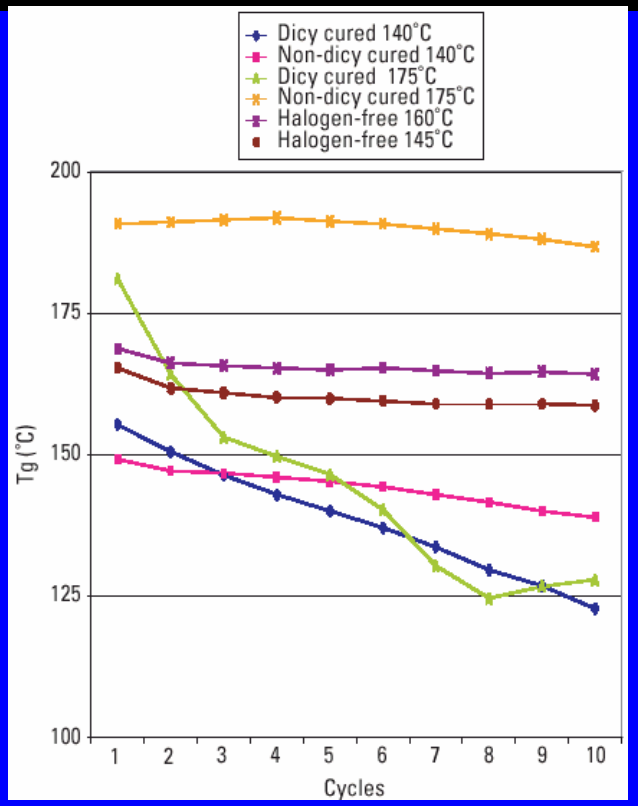
- **Thermal challenge**
  - Joule heating of power planes
  - Components temperature rise
  - Power connector heating
  - Interconnect heating

$$\triangle T = I * R^2 / \sqrt{W}$$

Equation source: Douglas Brooks, UltraCAD Design Inc

△T = Temperature rise (oC)
I = Current (A)
R = Conductor resistance (ohms)
W = Conductor width (mils)



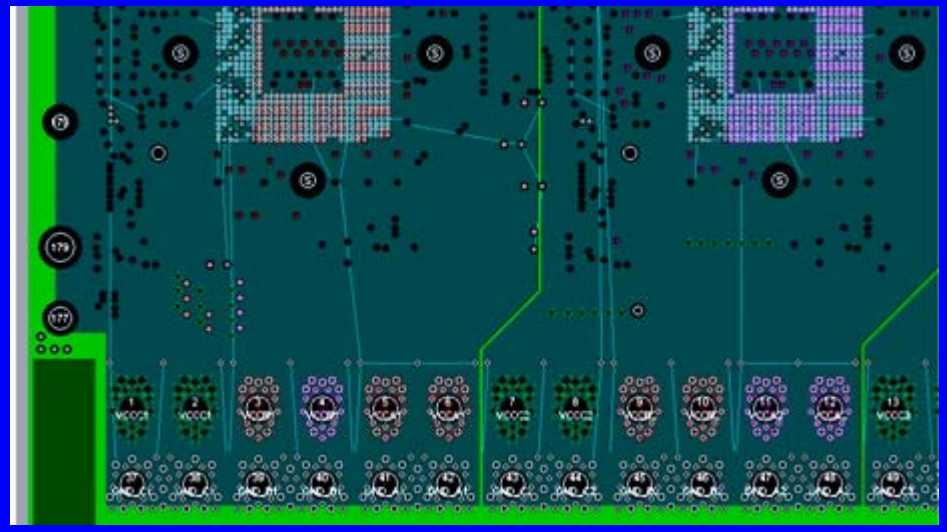


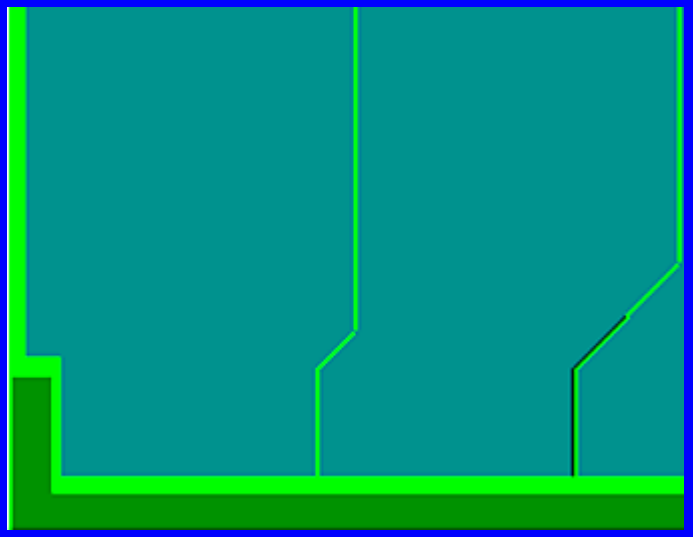
Source : Printed Circuit Design and Manufacture, Sept 2003

- **Temperature rise depends on:**
  - Power loss (IR^2) along the conductor
  - Conductor width

Design Challenges

- **Thermal Modeling & Simulation**
  - **Model construction accuracy**
    - **Correlation using IR thermal imaging**
  - **CAD layout format conversion**
    - **Design layout information loss**
  - **Limited capability**
    - **Plot thermal dissipation and IR drop for every layer**





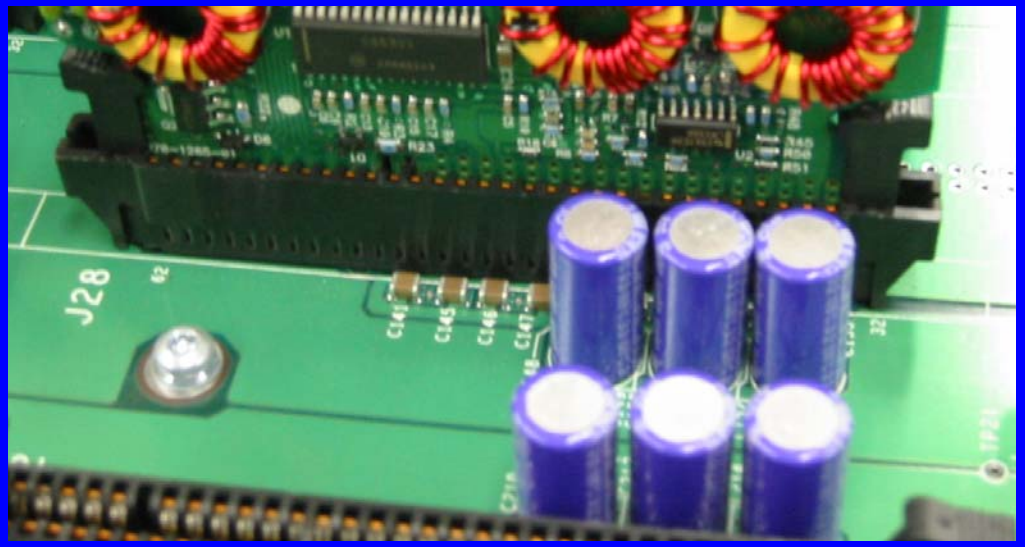
Design Challenges

- **What's needed to overcome the challenges?**
  - Bigger conductor X-section area
    - Thicker and wider conductor
  - Better conductor material resistivity
    - Copper @ **1.7 x 10 -8 Ωm**
    - Aluminum @ **2.6 x 10 -8 Ωm**
  - Higher laminate operation temperature
  - More intuitive thermal modeling capability

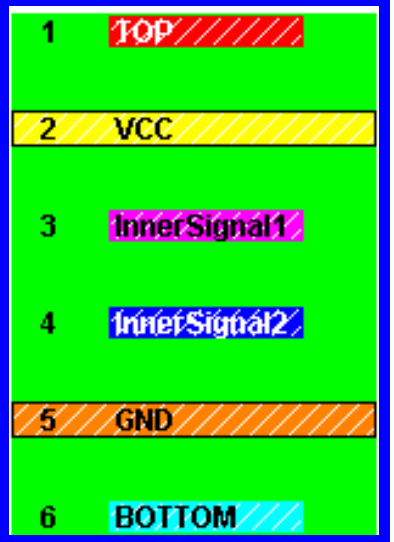
Power Delivery Options & Limitations

1. Copper Clad Printed Circuit Board

- De facto standard for delivering power to device through single or multiple power planes
- Provide good source of reference for signal integrity.
- Enable miniaturization for small form factor devices eg. Cell phone, PDAs and is easily implemented
- CCC is determined by power plane cross-section

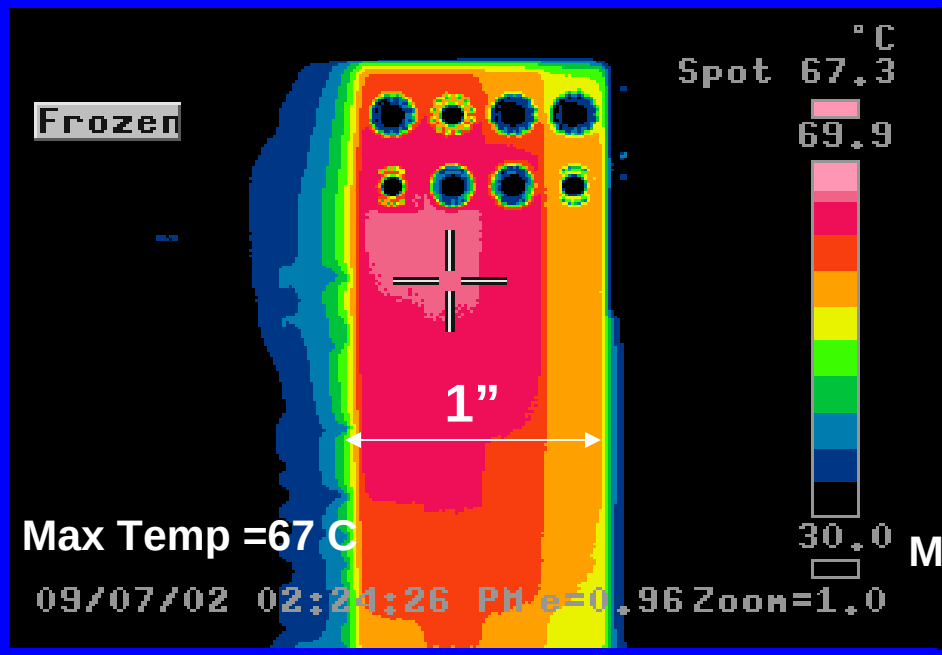


Power Delivery Options & Limitations



- **Limitations in copper clad PCB**
  a) PCB thickness
    - Total layer counts
      - ~12 layers max for .062” (1oz & 2oz Cu)
      - ~18 layers max for .120” (1oz & 2oz Cu)
    - Power plane and inner layers stackup
      - Signal trace routing and component placement
      - Controlled impedance traces
      - Current carrying capacity
      - Thermal performance
    - Thru-hole components pin length
      - Mostly available in 0.062” and 0.120”

Temperature Rise Experiment on Copper Clad PCB



Stackup A, 2 oz Cu at 70 A, 300 LFM

Stackup B, 2 oz Cu at 70 A, 300 LFM

PCB Stackup do affect thermal dissipation

Power Delivery Options & Limitations

- **Limitations in copper clad PCB**
  - b) Thicker Cu plane >2oz
    - Limited manufacturing capability – mostly for R&D
    - increased manufacturing complexity and throughput time
      - Longer learning curve, requires more test boards / run
    - High yield loss
    - 1.5X increase in manufacturing cost due to yield lost
    - Long leadtime and high cost of thick copper clad laminates (> 2oz)
  - c) High temperature PCB laminate
    - Limited high operating temperature material
      - ~ 170-250C
  - d) Conductor material
    - Copper – any better material than this?
    - Affordable cost

Power Delivery Options & Limitations

2. Buss Bar Technology

- Used primarily in military, computing and communication segment for power delivery.
- Rigid bus-bars made of high conductivity copper preformed to shape
- Provides better efficiency and thermal cooling to the end application.
- Current Carrying Capacity can easily reached 1000 watt per unit length.

Power Delivery Solutions & Limitations

- **Limitations in Buss Bar**
  a) Customization
     - BIB and socket location dependent
     - High cost
     - Additional processes
  b) Interconnect resistance to PCB
     - Contact resistance
  c) Interference with system and mechanical structure
     - Limit buss bar size and shape
  d) Insulation to prevent unwanted short
     - PCB surface & components

Conclusion

- **Standardization needed for cost-effective, stable and capable solutions to enable**
  - **Low cost >2 oz laminate**
    - Stable Manufacturing process with consistent PCB yield
  - **Reliable modeling tool to verify thermal concern**
    - Need layer by layer thermal modeling capability
    - IR drop modeling capability
  - **Buss bar interconnect solution and availability**
- **Need to explore other viable & cost effective solutions.**

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