



Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

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Technical Program

Panel Discussion

Sunday 3/06/05 8:00PM

“Thermal Issues Related To Devices Of Today And Tomorrow, What Can We Expect Moving Forward?”

Moderator:

Fred Taber

IBM Microelectronics (ret.)

Panel Members:

Ken Heiman

Micro Control Company

Chris Lopez

Wells-CTI

Mike Noel

Freescale

Steve Steps

AEHR Test Systems

Mike Ramsey

Plastronics

Dave Gardell

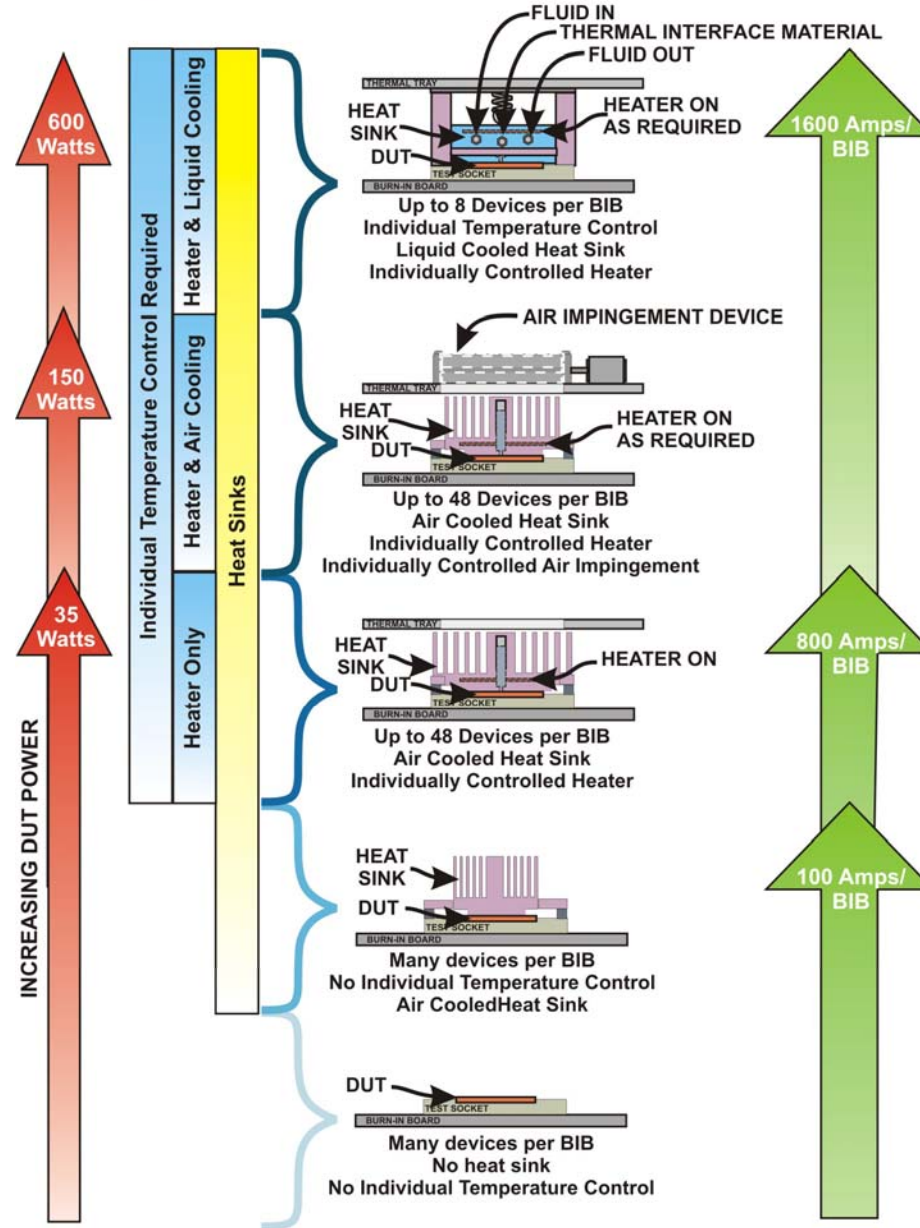
IBM Microelectronics

Jim Rhodes

Unisys

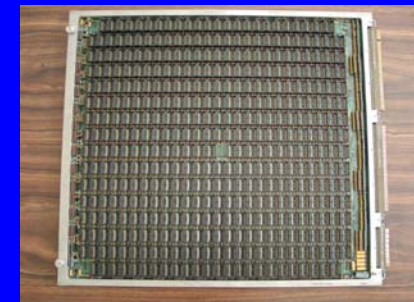


High Power Burn-In 2005



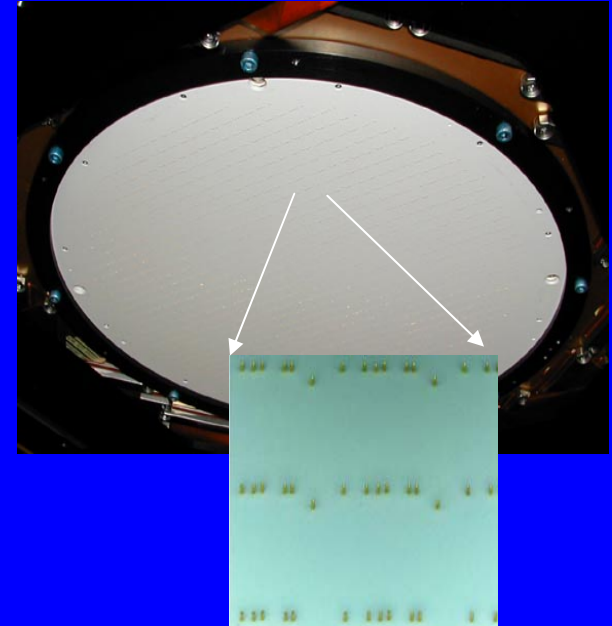
Packaged Part Burn-In Challenges

- **Upward trend in Burn-In Power**
 - Voltage dropping
 - Significantly higher currents
- **Power is becoming leakage related versus frequency related**
- **Individual temperature control**
 - Helps control part to part temperature variation
 - Total oven thermal load is the sum of all part maximums
- **Summary: solutions will involve all parts of the system**



Wafer Level Burn-In Challenges

- Same issues as packaged parts, plus...
- Single dimensional heat removal
- For high performance IC processes
 - Total wafer wattage is fixed
 - Issue is heat density (W/m^2)
- Most wafers: trivial
- High performance: Should be possible, but not trivial



Contact Temperature Rise

- $\Delta T = I^2 L^2 / 2 \nu \kappa A^2$
 - ΔT = Temperature Rise
 - I = Current
 - L = Contact Length
 - A = Cross Sectional Area
 - ν = Electrical Conductivity
 - κ = Thermal Conductivity

High-Power Test -> Point-Counterpoint

> Customer Expectation on Capital cost

P Always lower capital costs

C Increase functionality

> Thermal Control - Mechanical

P Power levels increasing

C Die or lid size decreasing

> Power Delivery Demand

P Technology– lower voltage, higher current, same delivery path

C High density, moveable BIBs still the demand

> Total Cost of Ownership

P Automation centric solutions are ripe for lowering TCO

C Customers unwilling to make the conceptual change