Burn-in & Test Socket Workshop

March 6-9, 2005
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop

TM

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Technical Program

Keynote Address
Tuesday 3/08/05 8:00PM

“Processor Packaging Trends and the Impact on Test”

Eric Tosaya
Director Packaging Engineering
Advanced Micro Devices

AMD

Processor Packaging Trends and the Impact on Test

J. Kwon, S. Singh & E. Tosaya*

* presenter

Processor Roadmaps

AMD

- The roadmaps were created using information collected from various sources:
  - Tom's Hardware: www4.tomshardware.com
  - X-bit Labs: www.xbitlabs.com
  - PC Watch: //pc.watch.impress.co.jp
  - Intel: www.Intel.com
  - SUN Microsystems: www.sun.com
  - Transmeta: www.transmeta.com
  - nVIDIA: www.nvidia.com
  - ATI: www.ati.com
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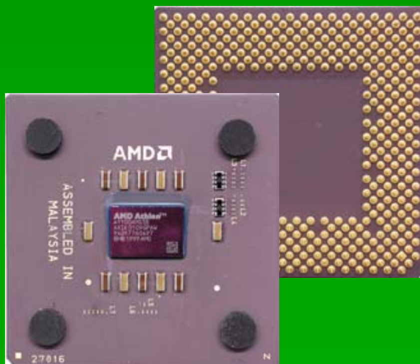
AMD Desktop: K7

AMD

Athlon

Thunderbird

~72 W

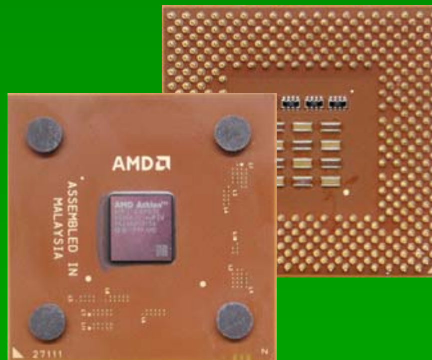


50mm / CPGA
Socket 462 / 2.54 Pitch

Athlon XP

Palomino

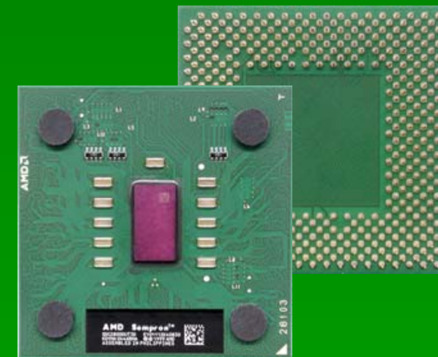
~72 W



50mm / OPGA
Socket 462 / 2.54 Pitch

T-Bred/Barton

~76 W



50mm / OPGA
Socket 462 / 2.54 Pitch

2000 — 2001 — 2002

AMD Desktop: K8

New Castle

~89 W

40mm / uOPGA
Socket 939 / 1.27 Pitch

ClawHammer

~89 W

40mm / uOPGA
Socket 754 / 1.27 Pitch

SledgeHammer

~89 W

40mm / uCPGA
Socket 940 / 1.27 Pitch

2003 2004

AMD Mobile

K8

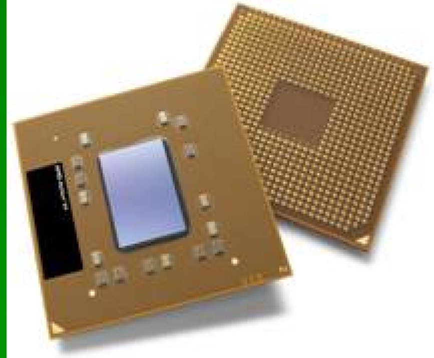
Hammer

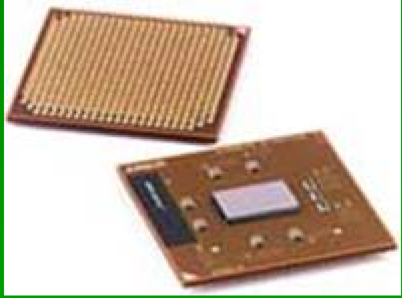
~ 35 W

K7

T-Bred/Barton

~ 25 W

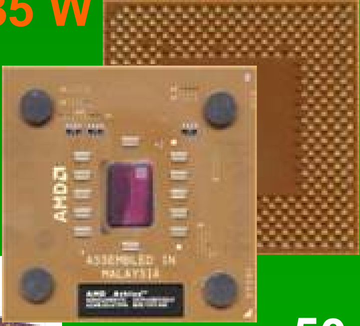




40mm / uOPGA
Socket 754 / 1.27 Pitch

T-Bred/Barton

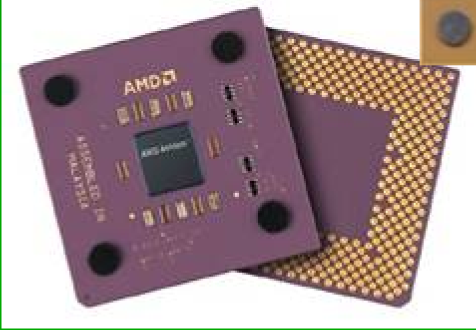
~ 35 W



33mm / uOPGA
Socket 563 / 1.27 Pitch

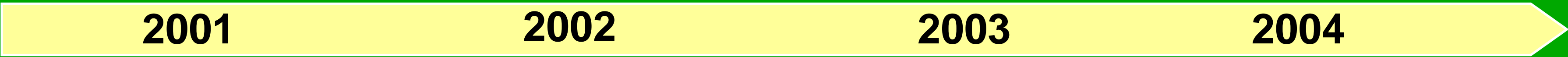
Palomino

~ 35 W



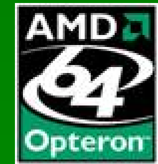
50mm / OPGA
Socket 462 / 2.54 Pitch

50mm / CPGA
Socket 462 / 2.54 Pitch



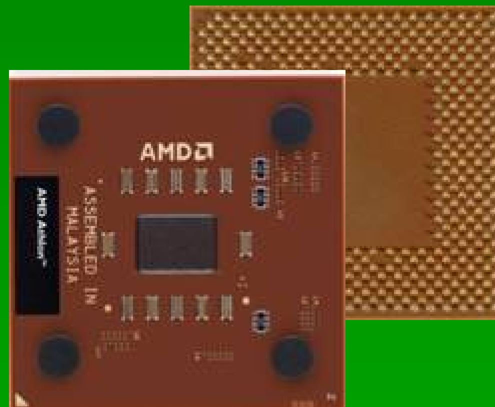
AMD Server

K8 ~ 89 W



K7

~ 66 W



~ 66 W

40mm / uCPGA
Socket 940 / 1.27 Pitch

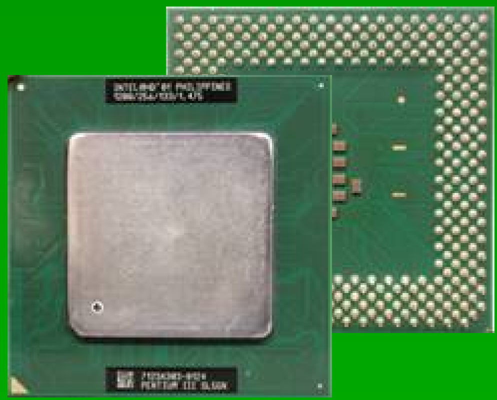
50mm / OPGA
Socket 462 / 2.54 Pitch

50mm / CPGA
Socket 462 / 2.54 Pitch

Intel Desktop

P3

Tualatin
~ 33W



50mm / PGA
Socket 370 / 2.54 Pitch

P4

Willamette
~ 71W

50mm / PGA
Socket 423 / 2.54 Pitch

Northwood /Prescott
~ 103W

35mm / uPGA
Socket 478 / 1.27 Pitch

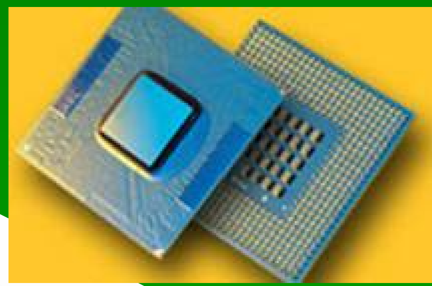
Prescott
~ 115W

37.5mm / LGA
Socket 775
1.09 X 1.17 Pitch

Intel Mobile

P4

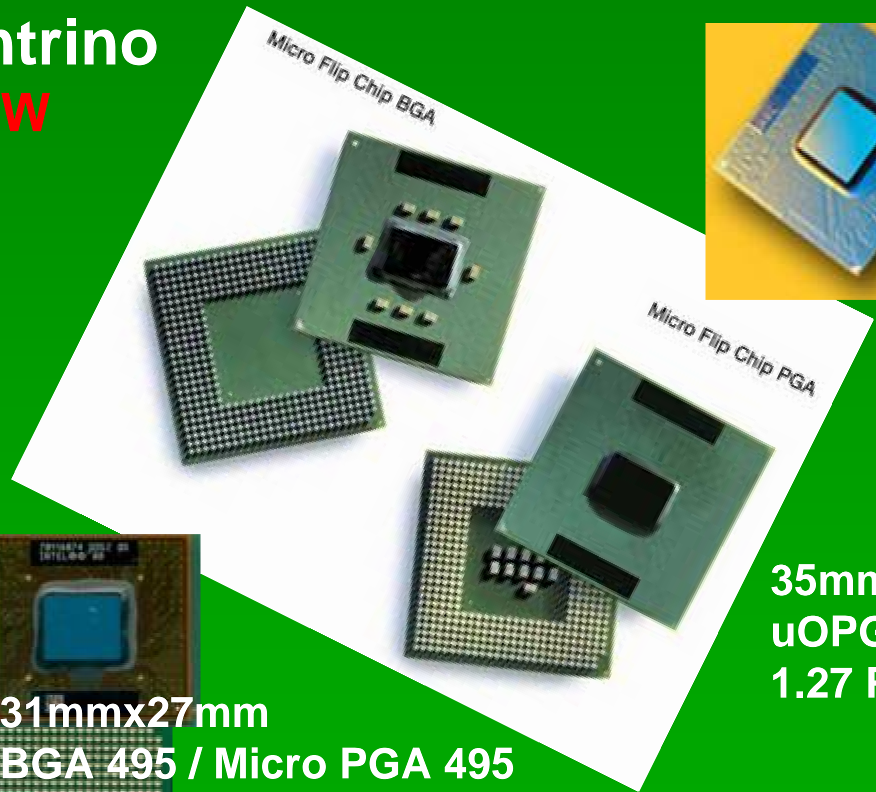
~ 35 W



37.5mm / LGA
Socket 775 ,
1.09X1.17 Pitch

Centrino

~ 25W



35mm / uOPGA
Socket 478
1.27 Pitch

P3

~ 7 W

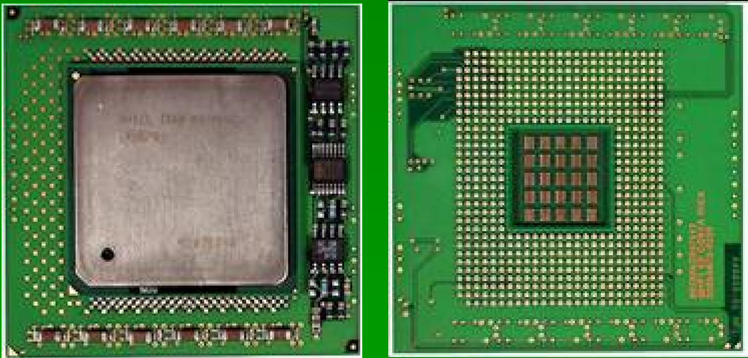
35mm
uOPGA / BGA 478
1.27 Pitch

31mmx27mm
BGA 495 / Micro PGA 495
1.27 Pitch

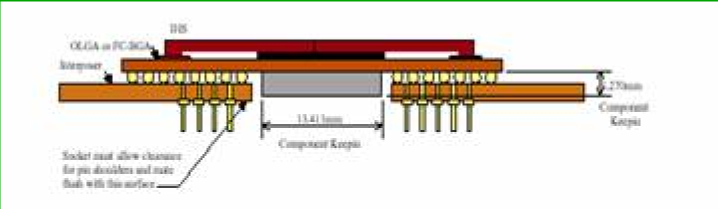
AMD

Intel Xeon

Gallatin ~ 80 W

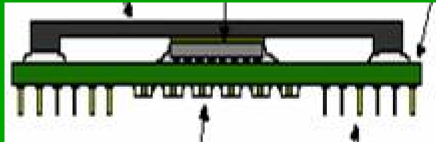


53.34mm Interposer
35mm x 35mm OBGA
Socket 603 / 1.27 Pitch



Nocona ~ 103 W

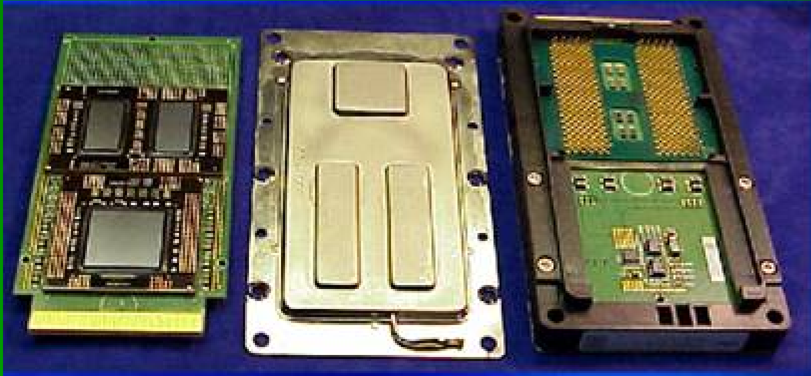
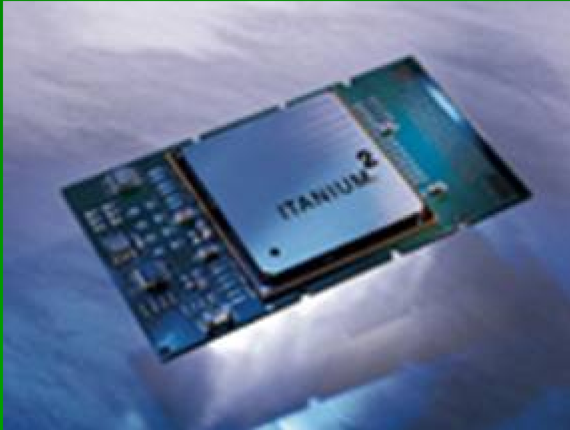
42.5mmX42.5mm
uOPGA
Socket 604 / 1.27 Pitch



2002 → 2004

AMD

Intel Itanium

Itanium 1	*Itanium 2*
	
PCB with OBGA **Socket : PAC 418**	**PCB with OBGA** **Socket PAC 611**
~ 130 W	**~ 130 W**
2001	**2002**

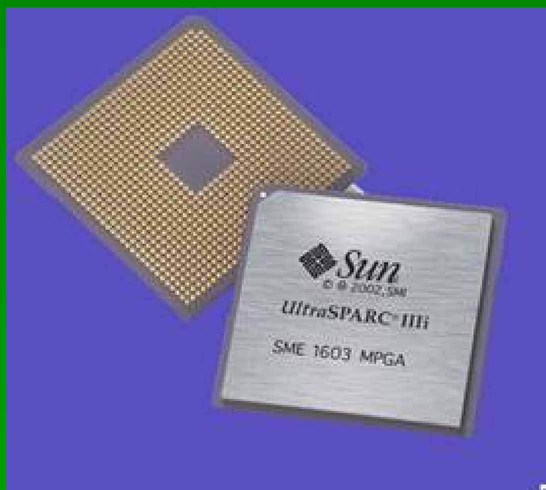
Ultra SPARC : SUN

II	IIe	IIi
35mm X 35mm Ceramic 787 LGA 1.0mm Pitch	50mm X 50mm Ceramic 370 PGA 2.54mm Pitch	37.5mm X 37.5mm Ceramic 587 LGA 1.27mm Pitch

Ultra SPARC : SUN

AMD

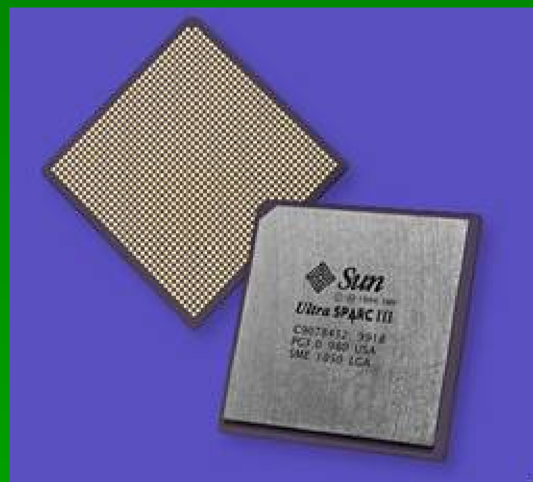
IIIi



45mmX 45mm
Ceramic 959 uPGA
1.27 Pitch

~ 52W

III



45mm X 45mm
Ceramic 1368 LGA
1.12mm Pitch

~ 50W

IV

45mm X 45mm
Ceramic 1368 LGA
1.12mm Pitch

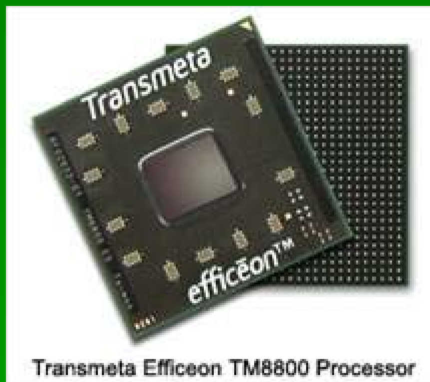
~ 108W

Transmeta Crusoe

5.7 ~ 7.3 W	5.1 ~ 9 W	5 ~ 9.5 W
474-pin **Ceramic BGA** **32.5mm x 25mm**	**474-pin** **Ceramic BGA** **32.5mm x 25mm**	**399-contact** **FC-OBGA** **21mm x 21mm**

Image captions: Crusoe TM5600/TM5400 Processor; Crusoe TM5800/TM5500 Processor; Crusoe TM5700/TM5900 21mm x 21mm

Transmeta Efficeon



Transmeta Efficeon TM8800 Processor

Efficeon TM8620 Processor

Transmeta Efficeon TM8600 Processor

783-pin
FC-OBGA
29mm x 29mm
1.0mm Pitch

592-pin
FC-OBGA
21mm X 21mm
0.8mm Pitch

783-pin
FC-OBGA
29mm x 29mm
1.0mm Pitch

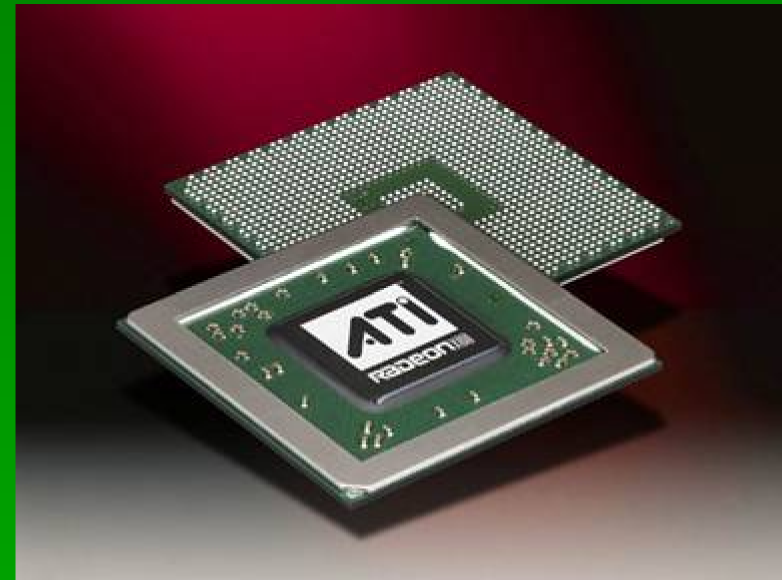
AMD

GPU : nVidia

FC OBGA with Stiffener

AMD

GPU : ATI



w/Stiffener
42.5mm X 42.5mm
1265 Pin FC OBGA

What does the crystal ball say?

AMD

- Platform infrastructure sets the electrical, thermal & mechanical requirement of processor design:
  - data rates (Gbps)
  - power (100W - 130W)
  - 2nd level interconnect (*sli*)
- Tomorrow's platform definition is driving multicore processors (MCP), new signaling technology for 5Gbps and beyond, core level hot spot cooling technology, improved socket & PCB technology to support better *sli*.

What does the crystal ball say?

AMD

- In 2004, > 100M X86 single core processors (SCP) were shipped, the vast majority with organic substrate technology.
  - uOPGA: can we drive the pitch down w/ acceptable cost?
  - OLGA: will LGA sockets reach the cost curve of PGA ZIF w/ the same manufacturability & reliability?
  - BGA is the mainstream for handheld mobile

What does the crystal ball say?

AMD

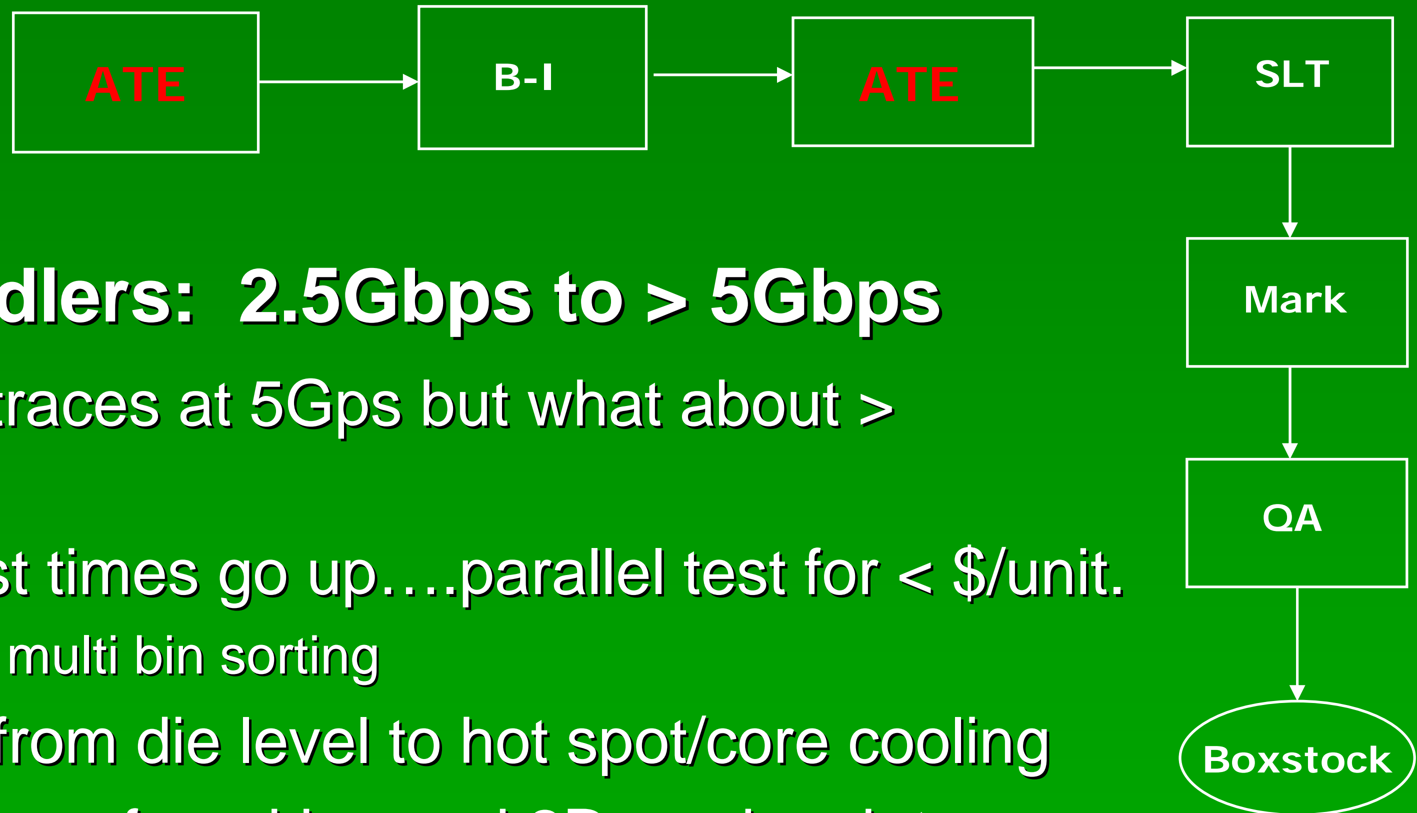
- Typical 1st level interconnect (*fli*) for high volume manufactured (*hvm*) 130nm – 65nm product is solder alloy based w/ a pitch of 150um – 200um.
  - Low-K dielectric w/ short stack-ups are pervasive
- Future 45nm product will use a Pb-free *fli*.
  - Low-K dielectric w/ taller stack-ups are the goal.
    - Organic: New underfills and/or creative substrate constructions
    - Ceramic (LTCC): $$$ = some niche applications?
  - *fli* pitch will be driven by SCP mobile (low pwr) architecture

What does the crystal ball say?

AMD

- *fli* will drive new wafer sort technology
  - What kind of *fli* will it be…bumped, bumpless, post, optical or some combination?
  - How long will physical contact last?
    - Probe pitch and density limits
    - Data rate limits
- Platform economics drives the use of sockets today. At 10Gbps and beyond will this model breakdown due to performance limitations?
  - What happens to ATE?
  - What happens to Burn-in
  - What happens to SLT?

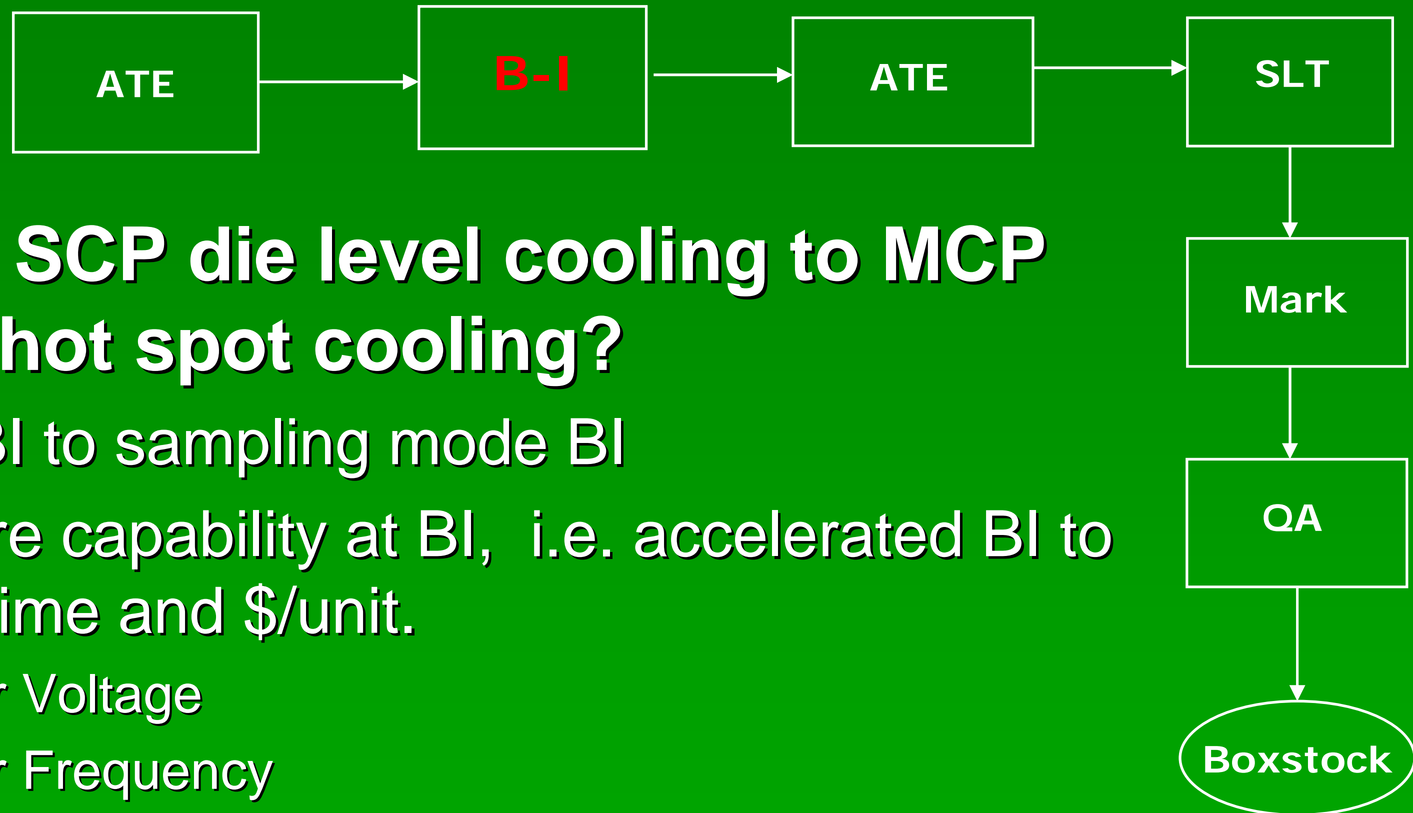
What does the crystal ball say?



- **ATE/Handlers: 2.5Gbps to > 5Gbps**
  - Still Cu traces at 5Gps but what about > 5Gbps?
  - MCP test times go up….parallel test for < $/unit.
    - offline multi bin sorting
  - Moving from die level to hot spot/core cooling
  - Integration of marking and 2D readers into

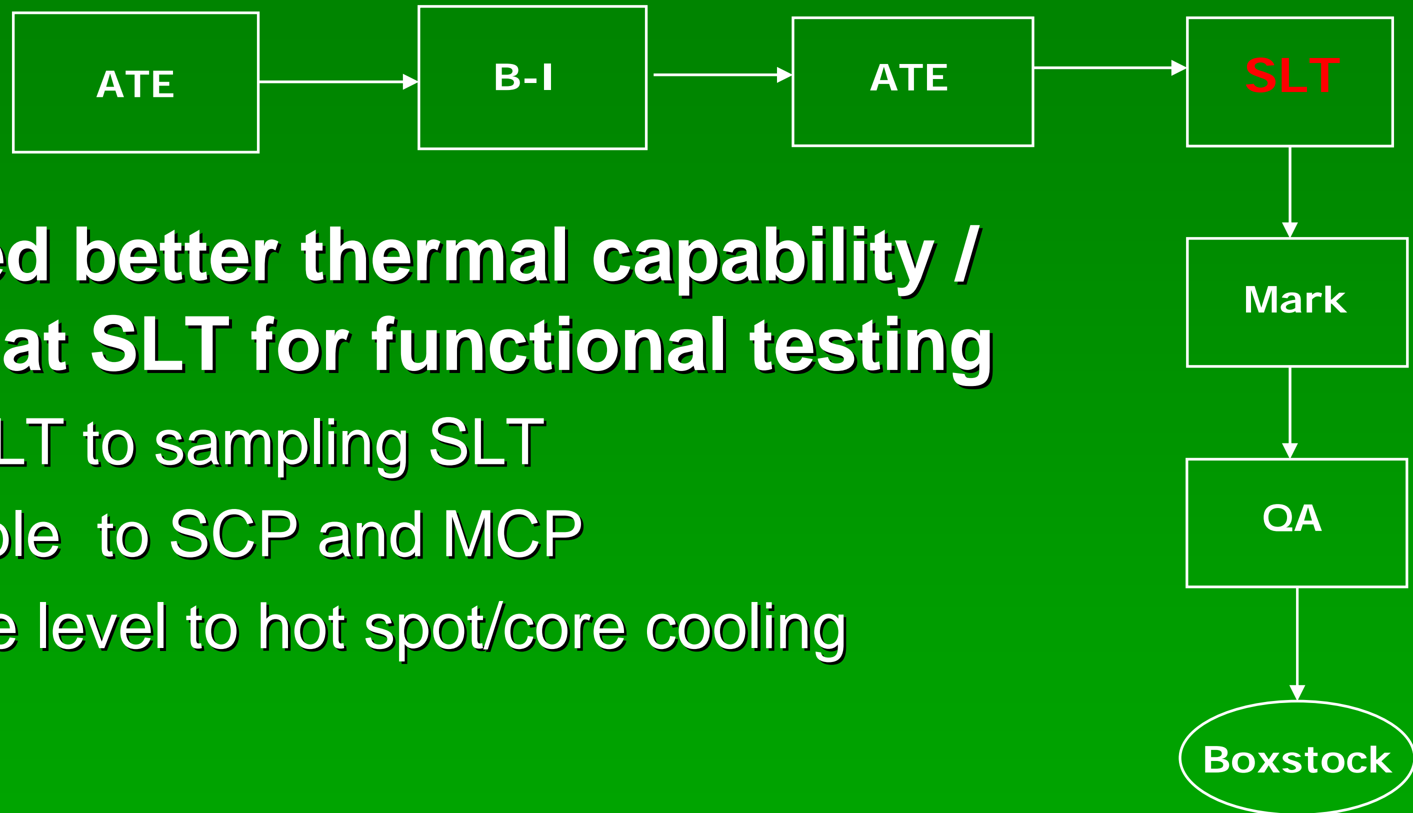
    handlers or offline binners

What does the crystal ball say?



- **Burn-In : SCP die level cooling to MCP per core hot spot cooling?**
  - 100% BI to sampling mode BI
  - Add more capability at BI, i.e. accelerated BI to reduce time and $/unit.
    - Higher Voltage
    - Higher Frequency

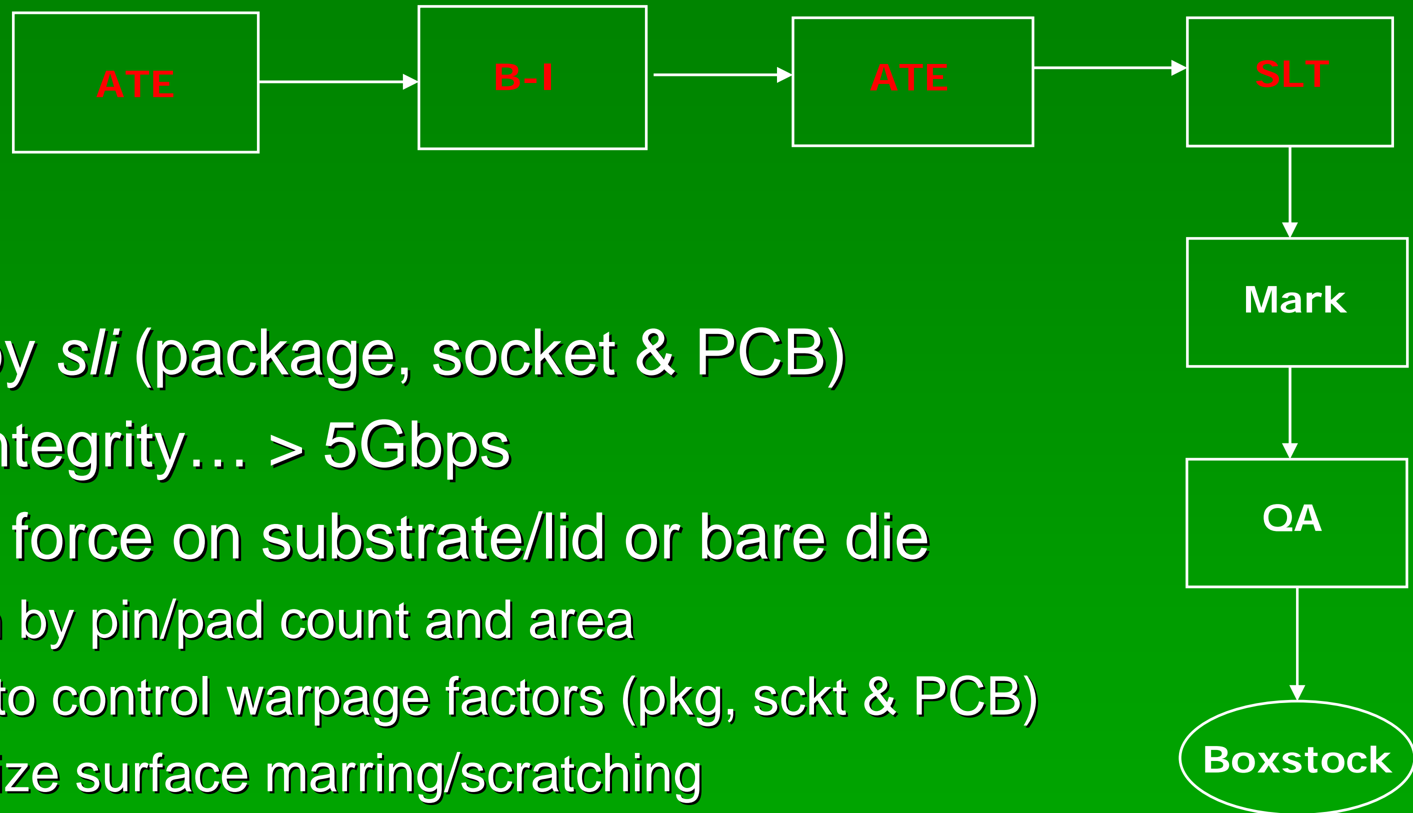
What does the crystal ball say?



- **SLT: Need better thermal capability / capacity at SLT for functional testing**
  - 100% SLT to sampling SLT
  - Applicable to SCP and MCP
  - From die level to hot spot/core cooling

What does the crystal ball say?

AMD



- **Sockets**
  - Driven by *sli* (package, socket & PCB)
  - Signal integrity… > 5Gbps
  - Loading force on substrate/lid or bare die
    - Driven by pin/pad count and area
    - Need to control warpage factors (pkg, sckt & PCB)
    - Minimize surface marring/scratching
  - Tighter *sli* pitch impacts pin integrity and bending

SUMMARY

AMD

- Platform infrastructure limits rate of change and defines processor boundaries
- Mainstream substrates technology will continue to be organic uPGA, LGA & BGA
- How far beyond 5Gbps will Cu interconnect go?
  - Sockets may not be far behind as a bottleneck
- MCPs will drive development of active hot spot cooling for BI & SLT
- ATE moving to parallel processor testing
  - Offline binning more cost effective