Burn-in & Test Socket Workshop

March 7 - 10, 2004
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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BiTS Burn-in & Test Socket Workshop

Technical Program

Session 5
Tuesday 3/09/04 10:30AM

MANAGING HIGH FREQUENCY REQUIREMENTS

"Transmission Line Effects Of Nickel Plating In Contactor Applications"

Jon Diller – Synergetix **Kevin DeFord** – Synergetix

"Understanding The Effects Of Signal Path Bandwidth On Semiconductor Test"

Jason Mroczkowski – Everett Charles Technologies

"A Method For Contactor Characterization To 25 GHz"

Tim Swettlen – Intel Corporation **Orlando Bell** – GigaTest Labs
Gary Otonari – GigaTest Labs **Eric Bogatin** – Synergetix

Transmission Line Effects of Nickel Plating in Contactor Applications

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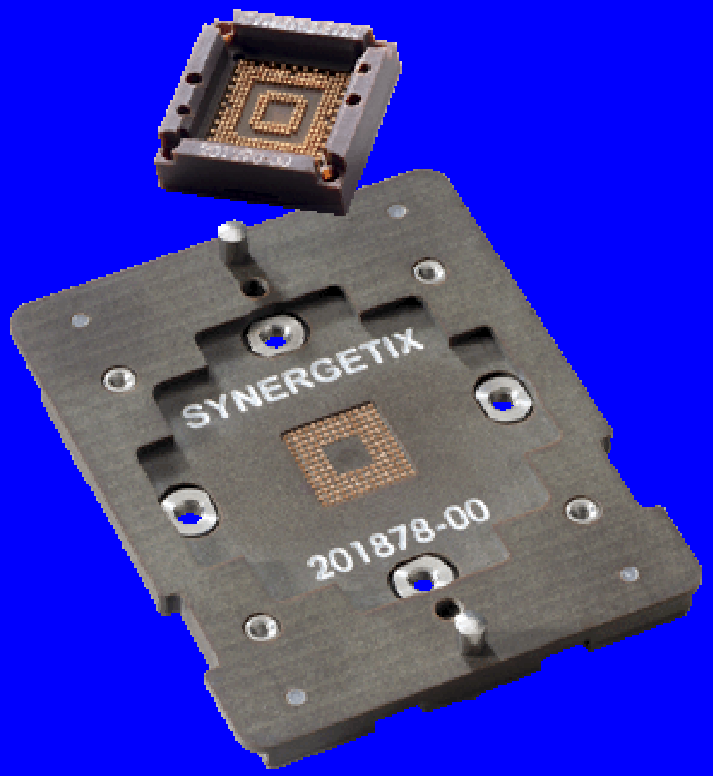
Jon Diller and Kevin DeFord
Synergetix

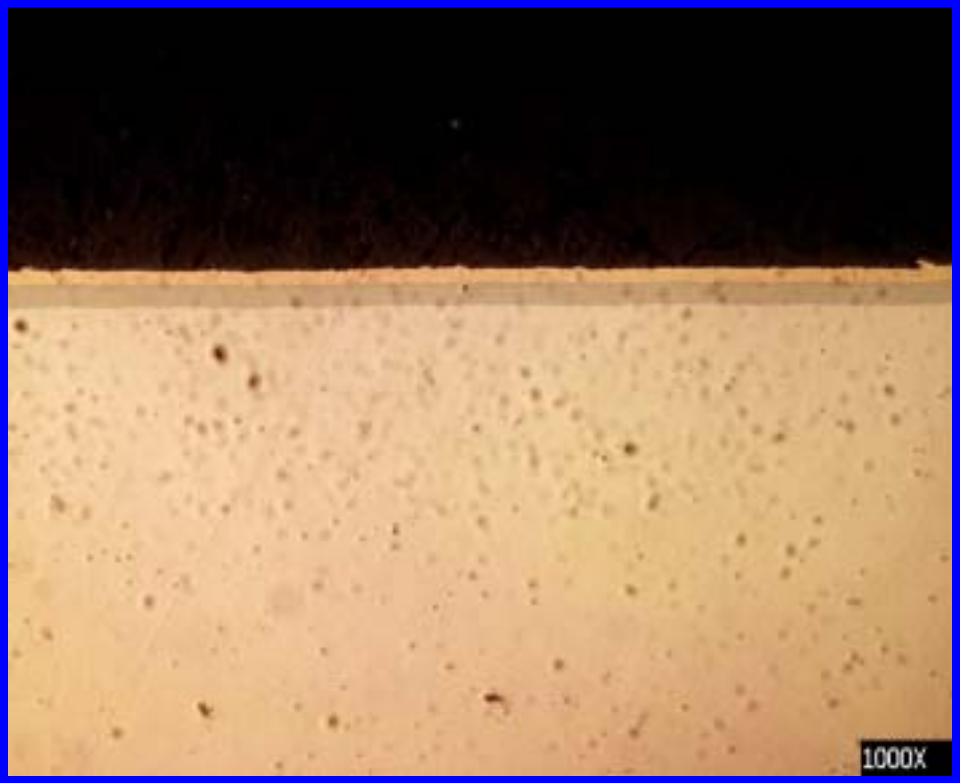
Introduction

- **Synergetix: Leading-edge since 1994**
- **Spring Contact Probe-based sockets**
- **RF expertise leads to Ni concerns**



Concerns Regarding Nickel

- **High permeability and resistivity**
  - **Thin skin depth at high frequency**
  - **Higher insertion loss**
- **Necessary as barrier layer and for hardness**

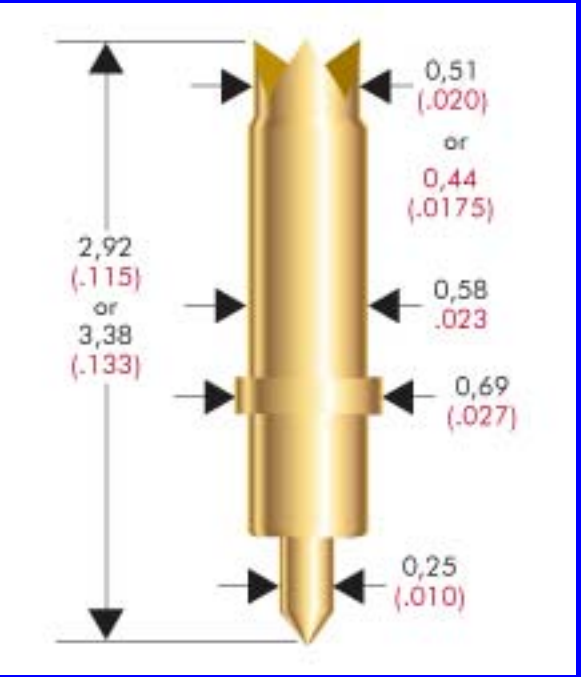


Predicted Response

- **Best case (no Ni) @ 9 GHz**
  - **R_L ~ 2.5 Ω / cm**
  - **α_L ~ 0.25 dB / cm**
  - **Total α ~ 0.06 dB**
- **Worst case, all current through thin flash (7 µ”) Au, α ~ 0.25 dB**

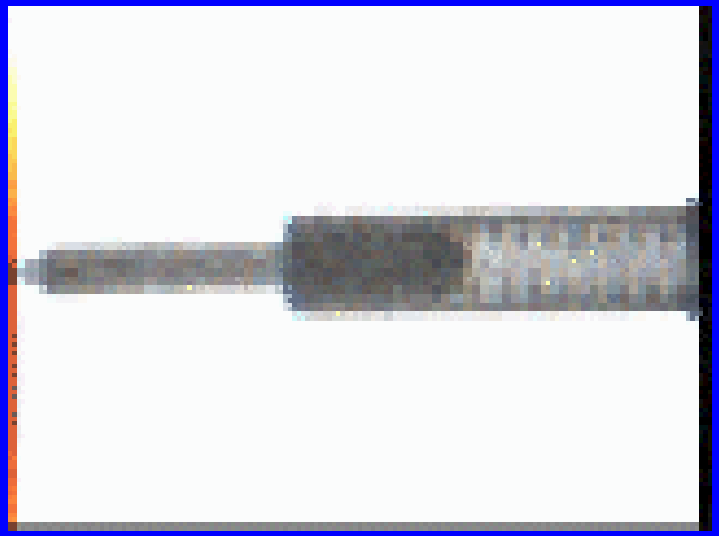
Test Subject

- **Probe: Ultra Micro Pitch (101052)**
  - **Moderate BW at 1 mm pitch**
  - **Good DC & life performance**
  - **In use at concerned customer**



Test Subject

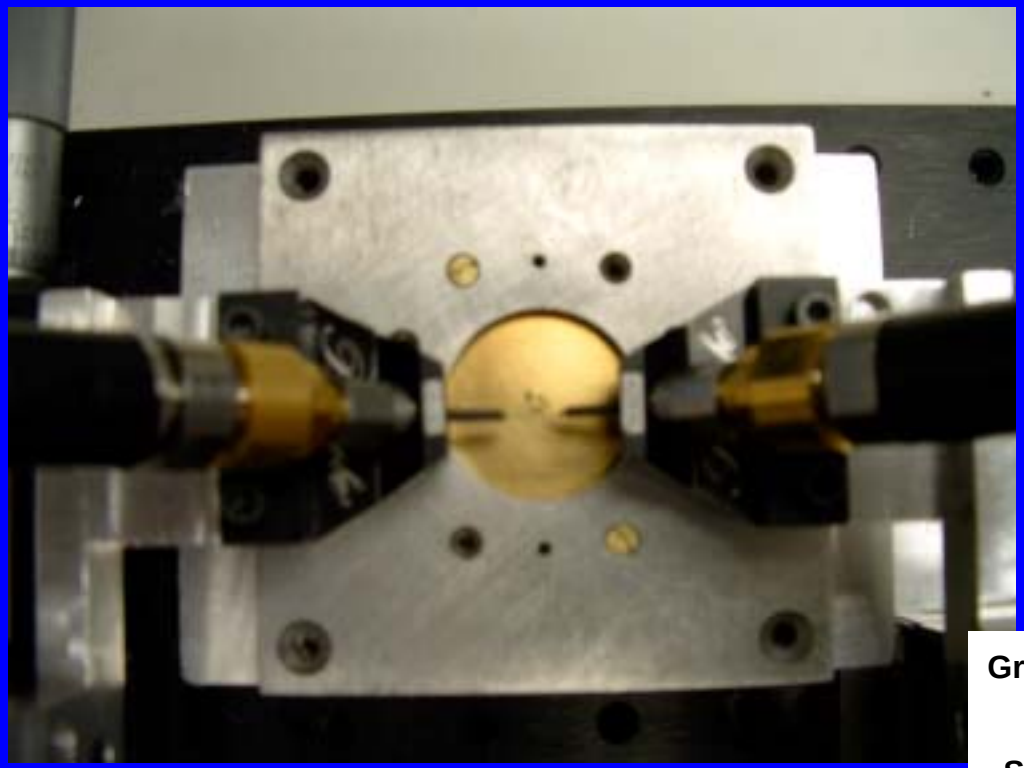
- Three-piece design
- Floats in test socket
- Plunger-barrel electrical path

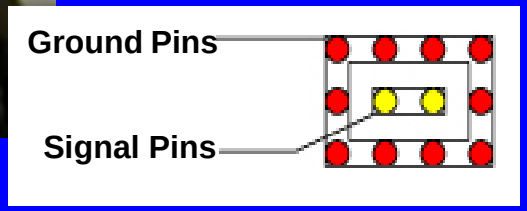


Test Concept

- Probes with various platings
- Measure S21 with HP8719 VNA
- Agilent ADS
- Measure repeatability
- Compare platings

Test Setup

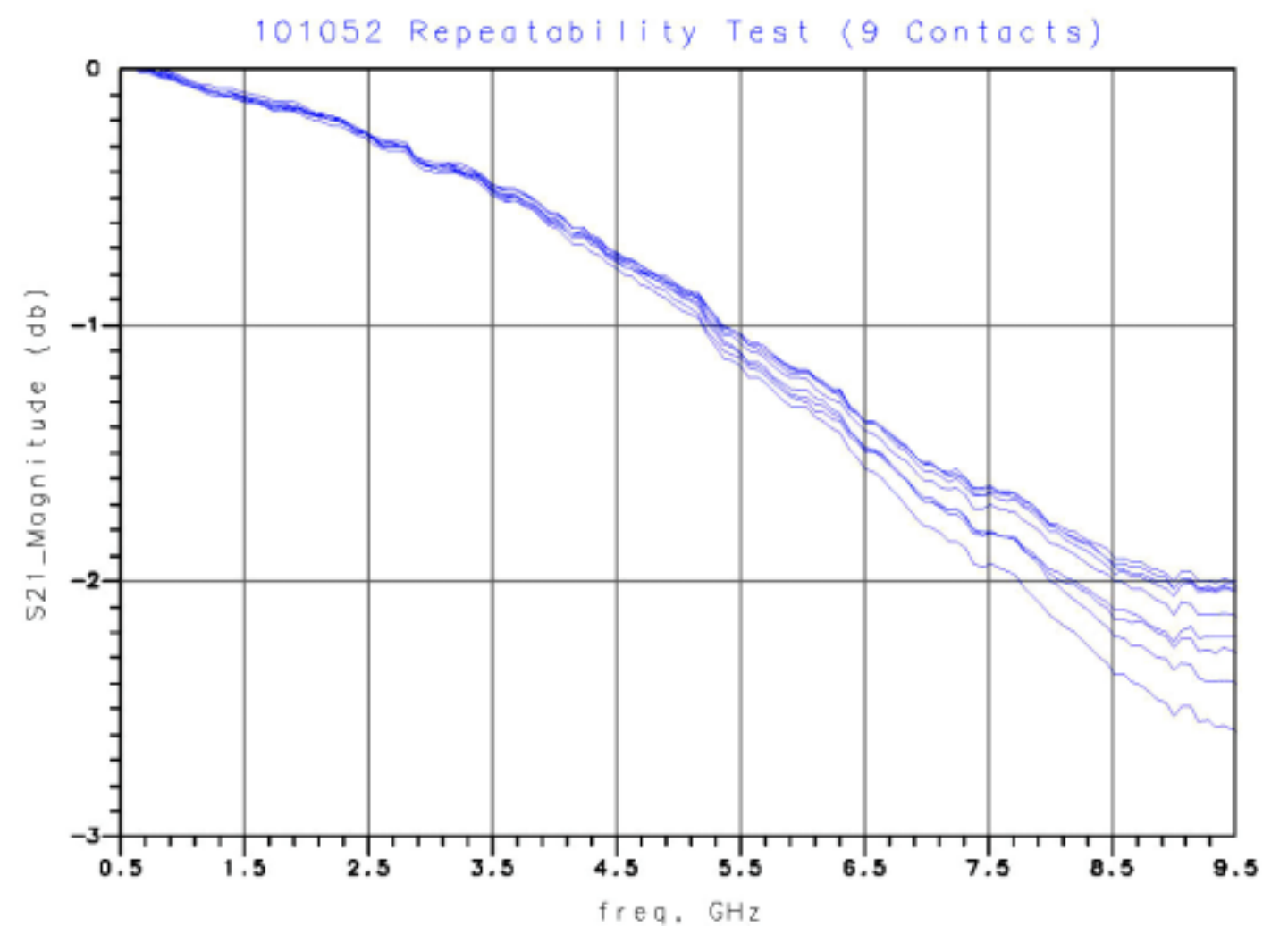




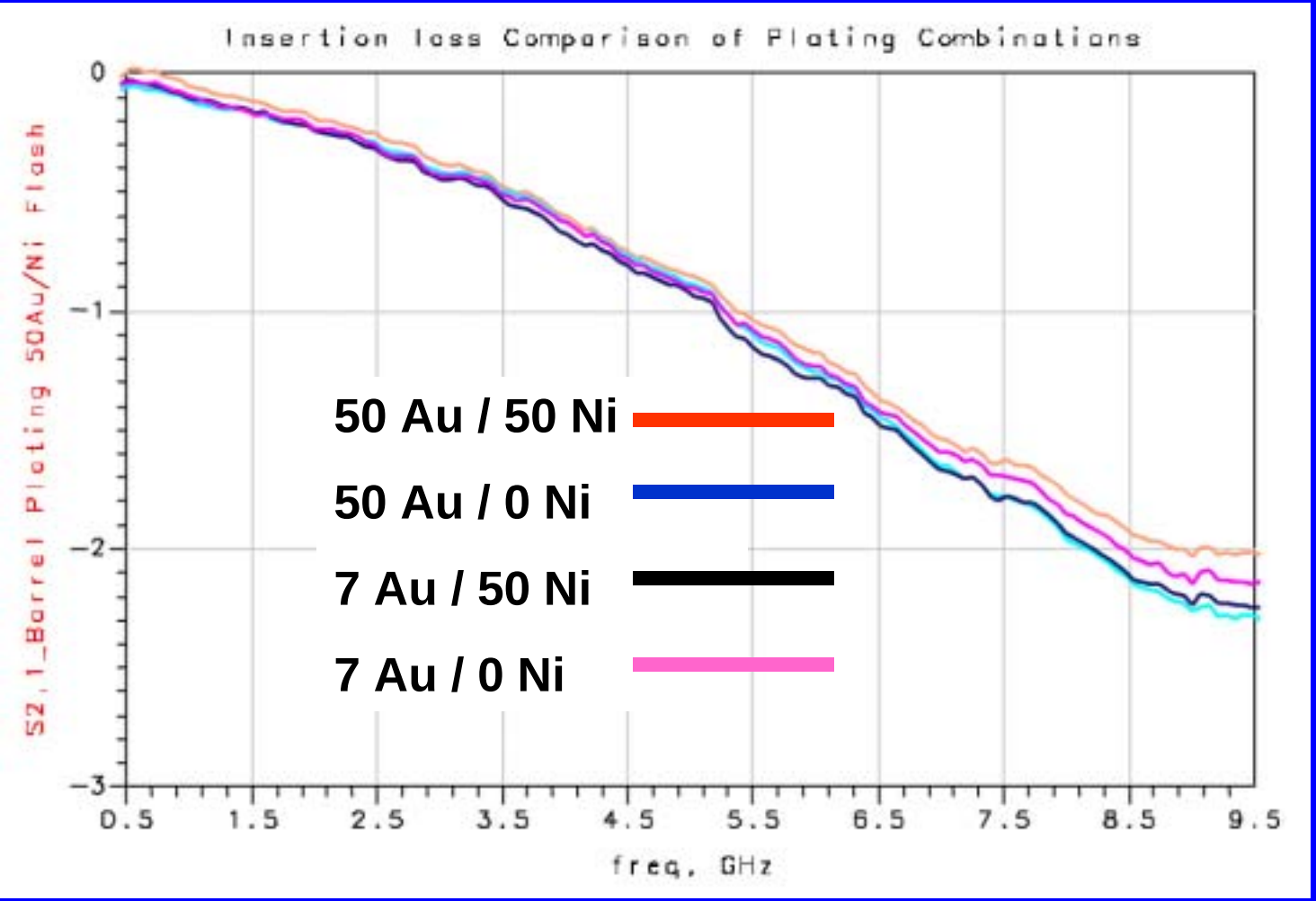
Probe Configurations

Pin	Au Thickness	Ni Thickness
1	50 µ” (1.3 µm)	50 µ” (1.3 µm)
2	50 µ” (1.3 µm)	None
3	7 µ” (0.1 µm)	50 µ” (1.3 µm)
4	7 µ” (0.1 µm)	None

Repeatability

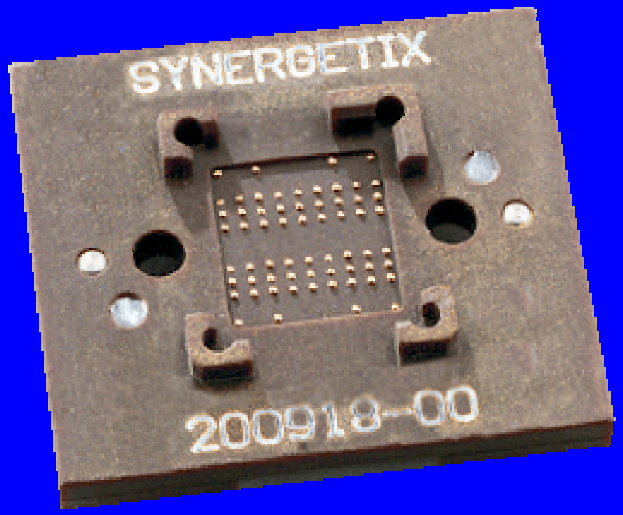


Results


Insertion loss Comparison of Plating Combinations
S2,1_Barrel Plating 50Au/Ni Flash
0
-1
-2
-3
0.5
1.5
2.5
3.5
4.5
5.5
6.5
7.5
8.5
9.5
freq, GHz
50 Au / 50 Ni
50 Au / 0 Ni
7 Au / 50 Ni
7 Au / 0 Ni

Conclusion

- Nickel content has no significant effect on TL behavior
- Gold thickness variations also not significant
- Testing very repeatable



EVERETT CHARLES TECHNOLOGIES
Testing the Limits

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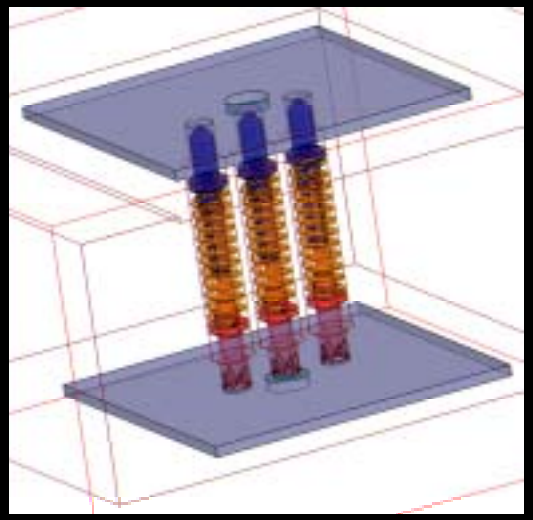
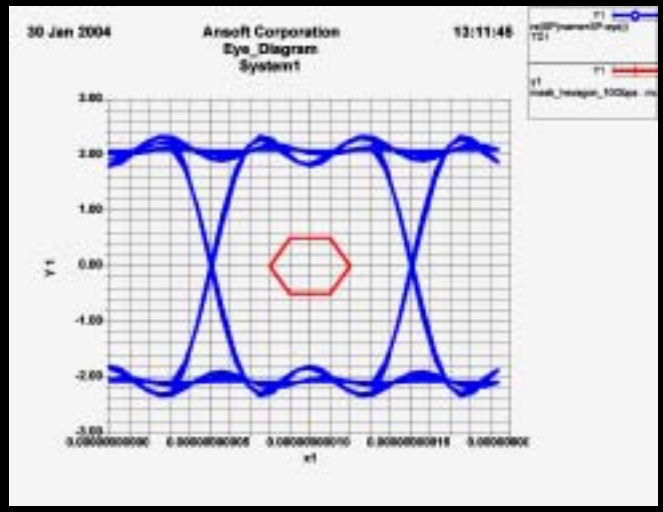
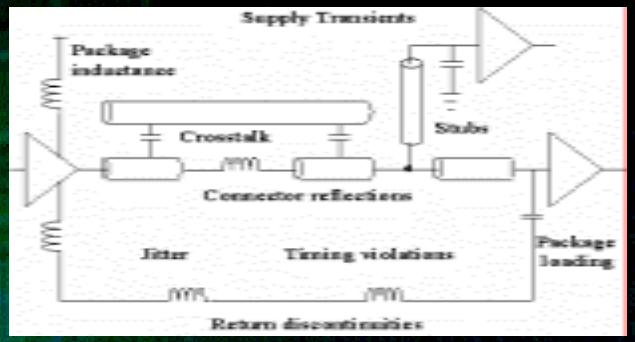






Understanding the effects of signal path bandwidth on semiconductor test

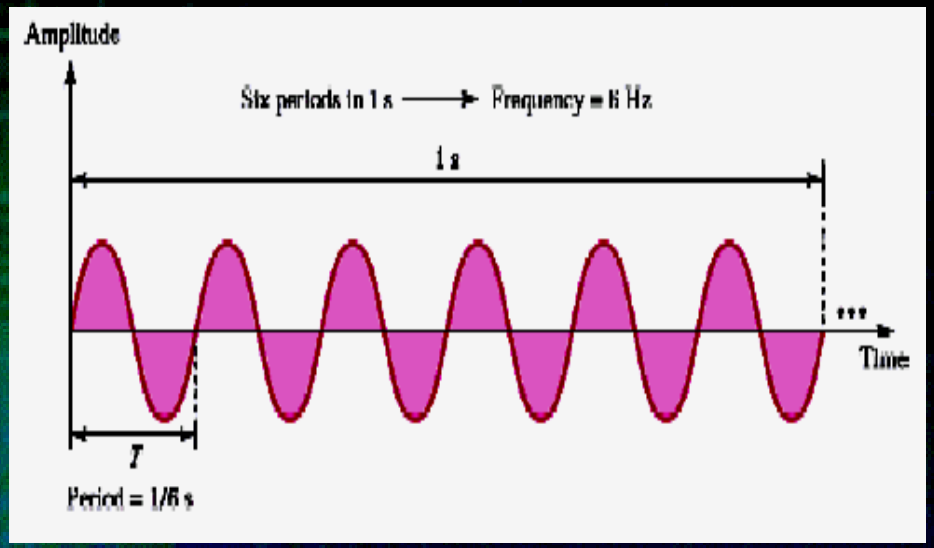
Jason Mroczkowski
ECT-Semiconductor Test Group - MN

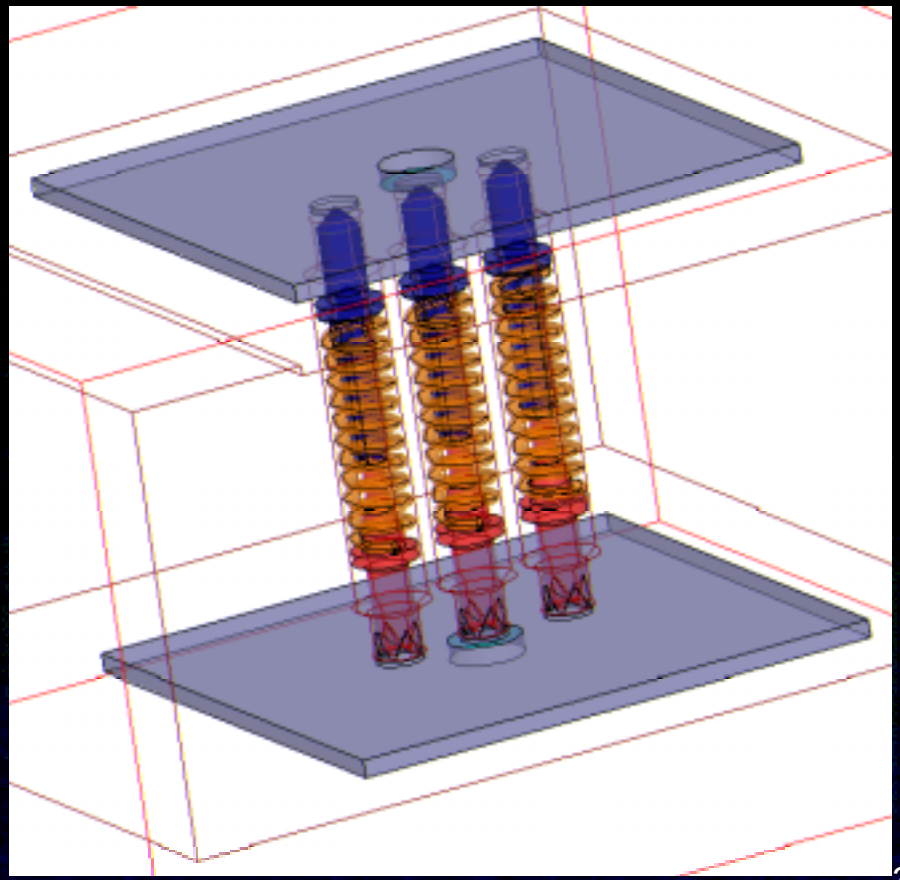
Presentation Topics

- Bandwidth Definition
- Bandwidth limitations
- Digital signal transmission
- Noise effects
- Jitter

Bandwidth

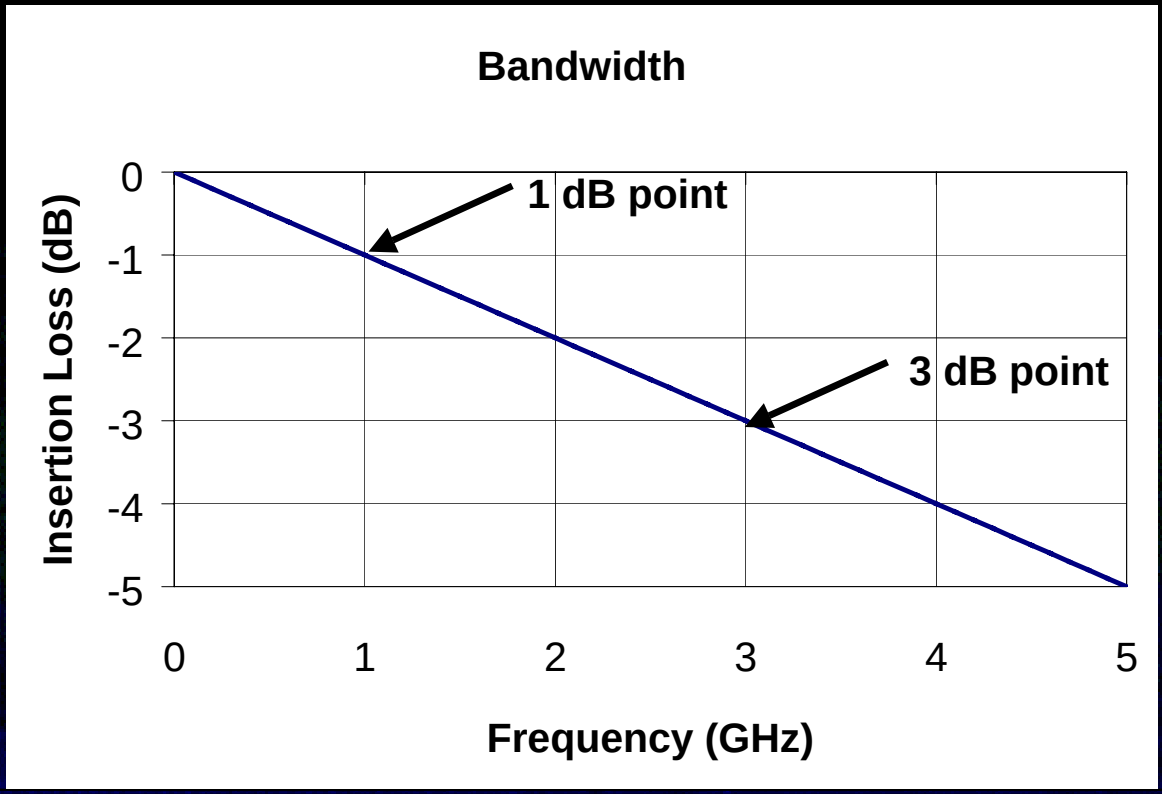
- The range of frequencies that can pass through a conductor without significant degradation
- The higher the bandwidth the greater the capacity in BPS.





Bandwidth

- 3 dB point
  - point at which power output is half the power input
  - point at which output voltage is 70% of input voltage
- 1 dB point
  - point at which output voltage is 90% of input voltage

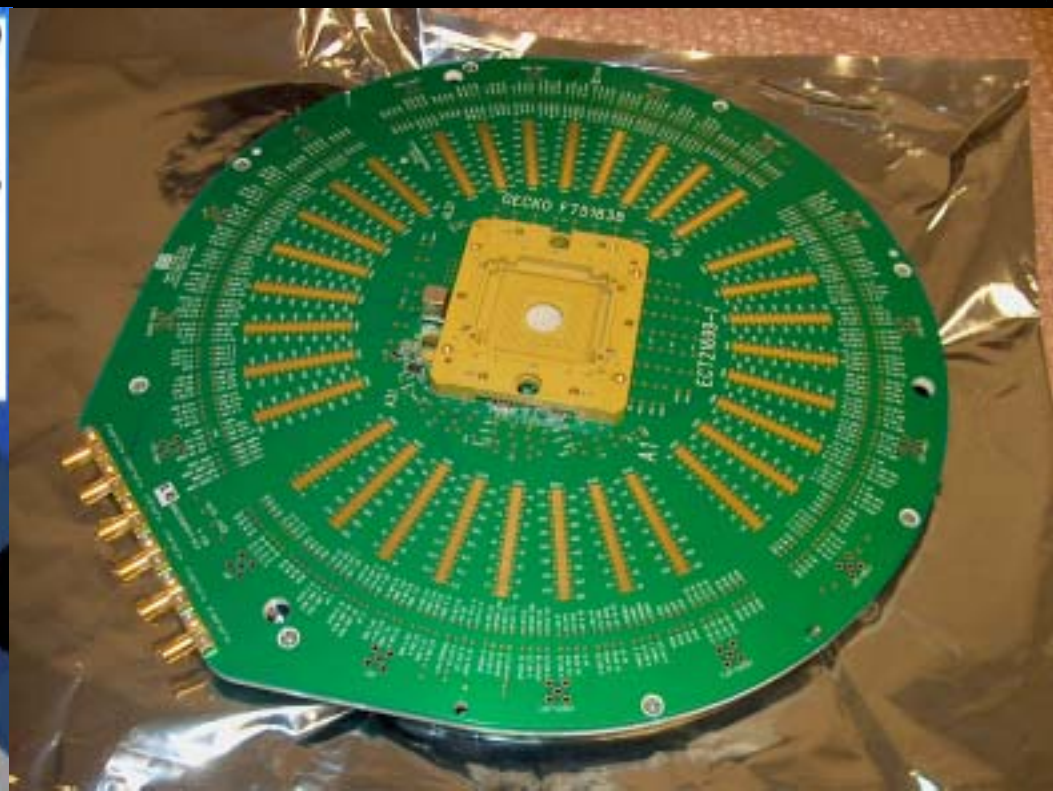


Bandwidth limitations

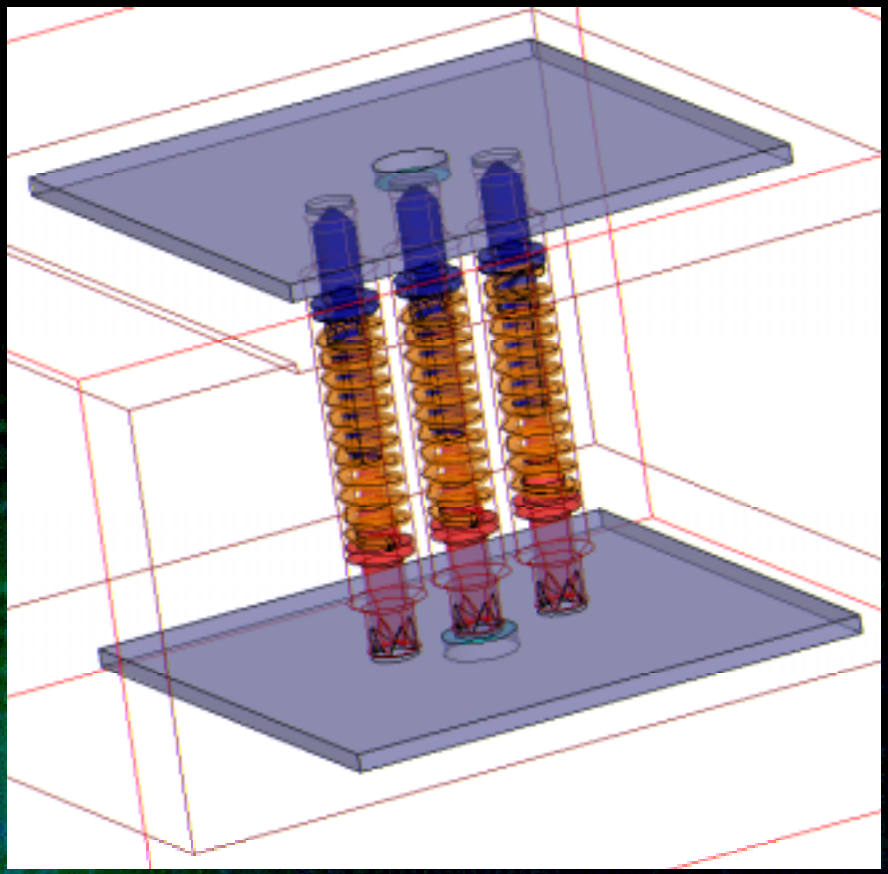
- What causes bandwidth degradation
  - inductance, capacitance, dielectric losses, skin effect, etc.
- PCB effects
  - Dielectric constant of PCB
  - Trace size
  - trace layout
- Contactor effects
  - Dielectric constant of Contactor body
  - Pitch of device
  - quality of contact element (spring probe)

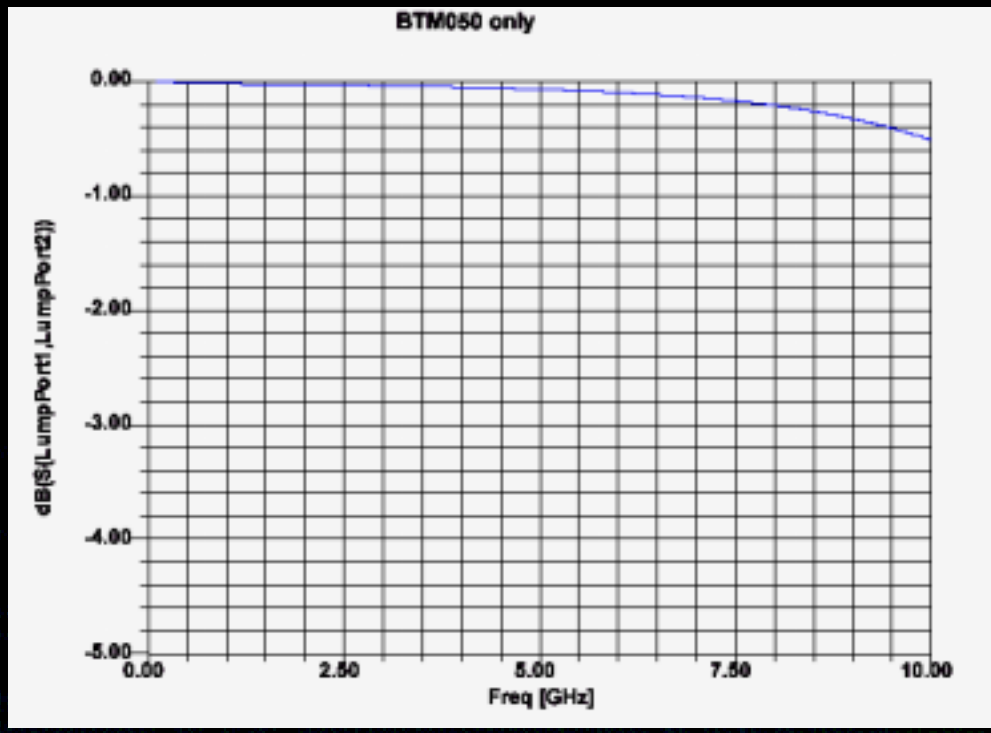
System Bandwidth in Semiconductor test

- At high frequencies, the board and contactor electrical performance interact.
  - reflections at connectors
  - 90 degree transition to contactor

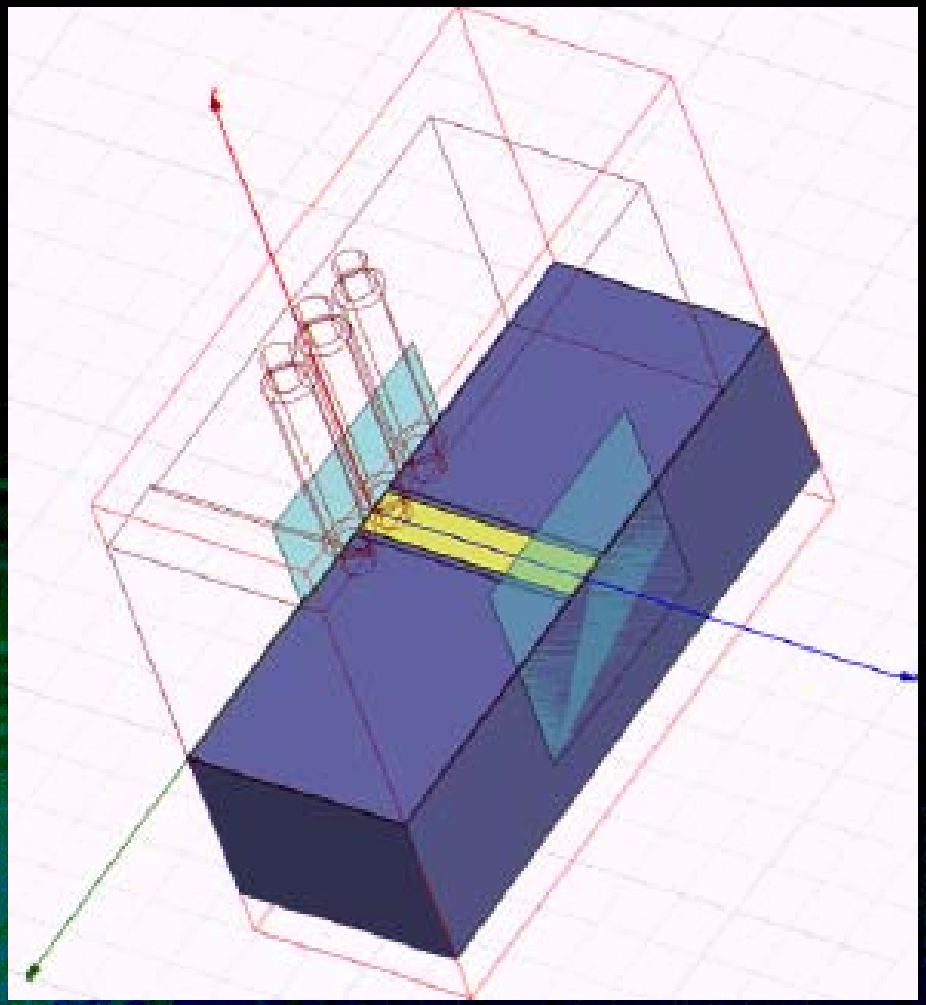


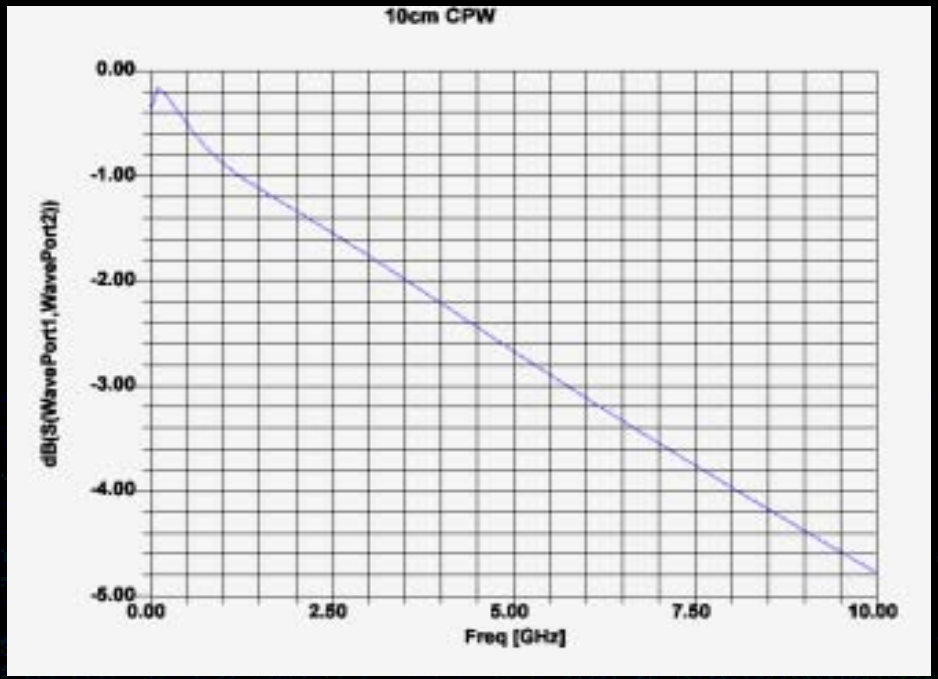
Insertion loss of contactor alone



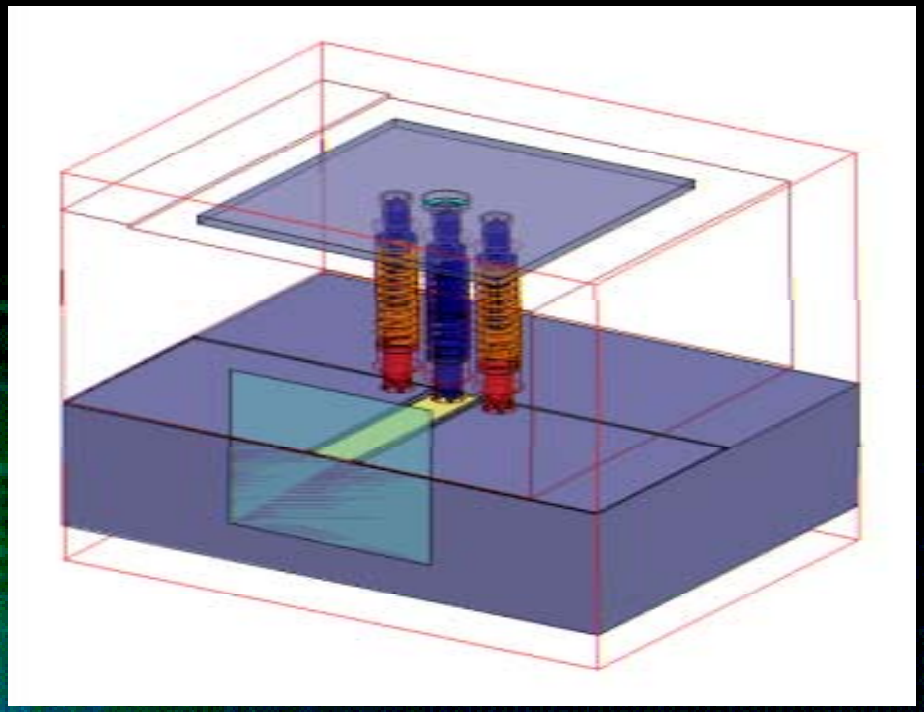


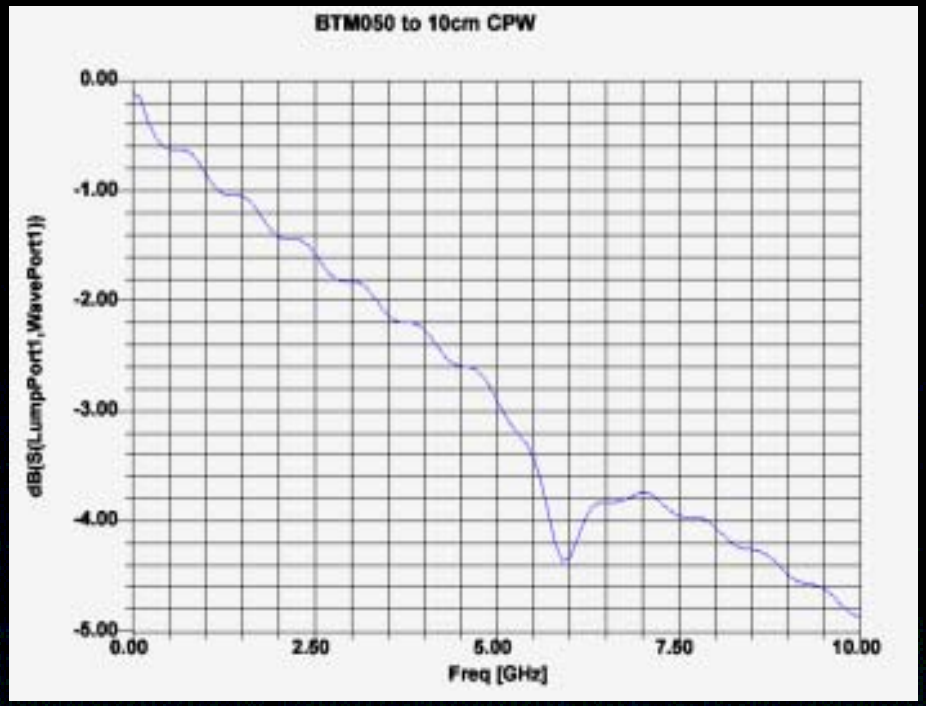
Insertion loss of 25cm PCB alone





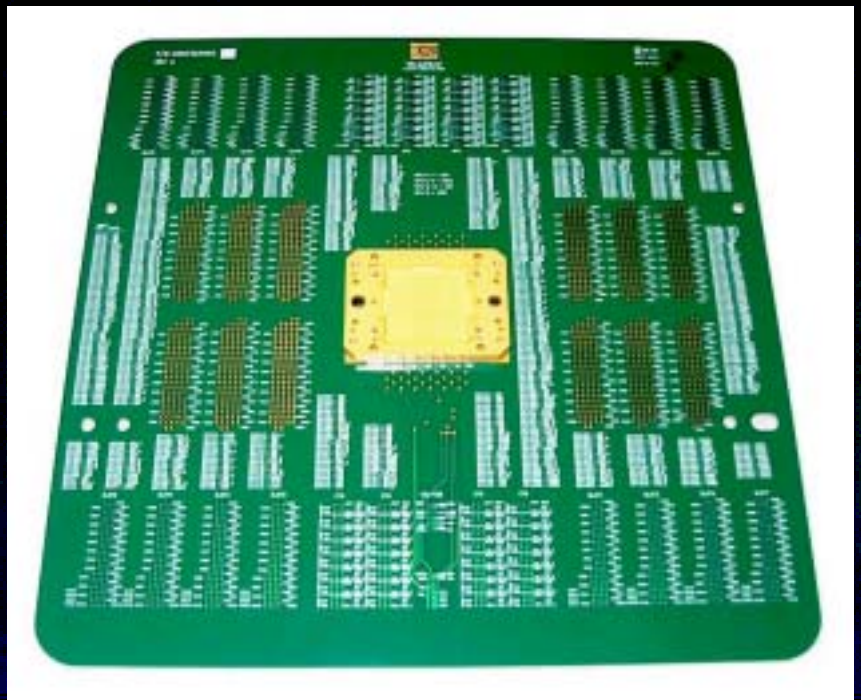
Insertion loss of contactor and PCB together





Bandwidth

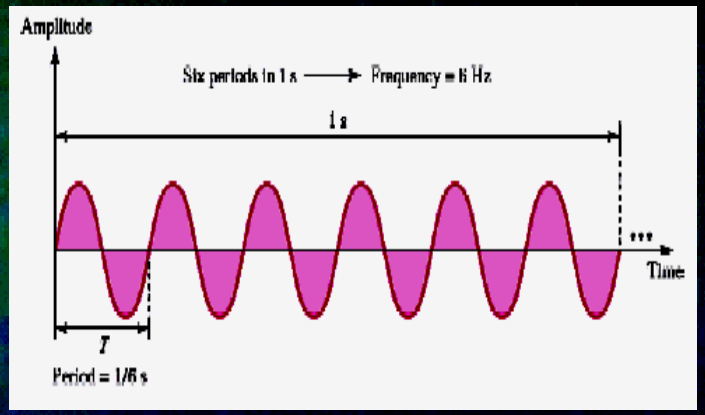
- compare board bandwidth to contactor bandwidth
  - ↗ contactor - 2.54-6 mm
  - ↗ board - 5-15 inches
  - ↗ more loss through board



Digital Signals

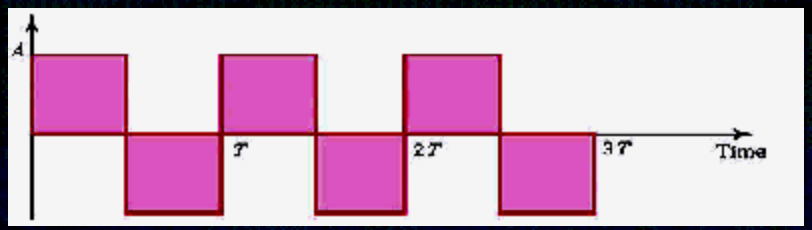
Analog signal

- A continuous signal that varies over time
- Sine wave represents an Analog signal
- Units of Hertz



Digital signal

- A sequence that has discrete values over time
- Square wave represents a digital signal
- 1 or 0 translated to voltage pulses over a conductor
- Units of Bits Per Second (BPS)

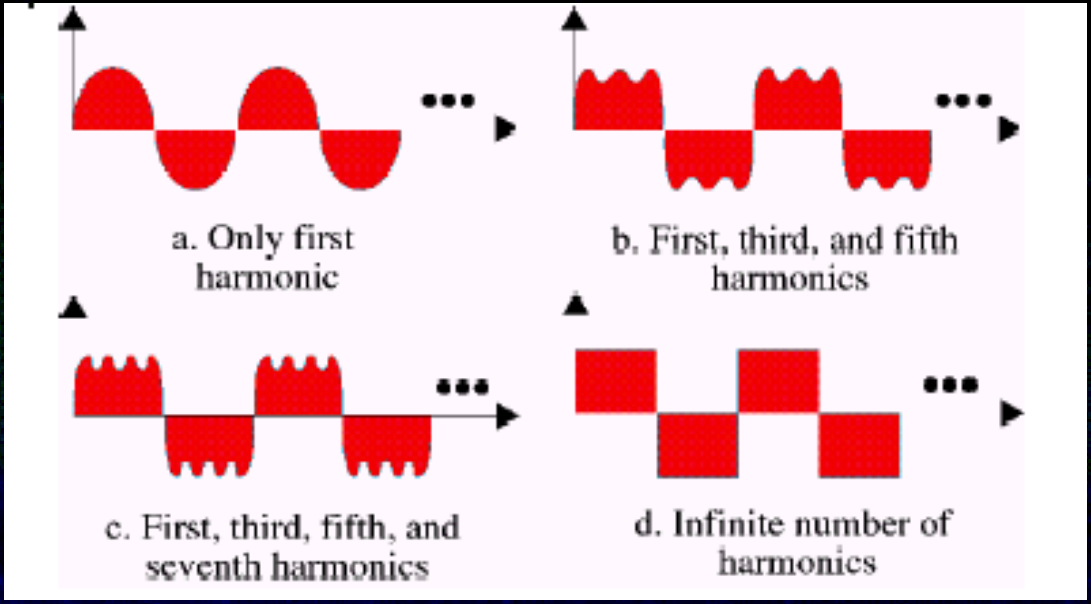


Digital signals

- A Digital signal is made up of an infinite series of of sine waveforms (analog signals)

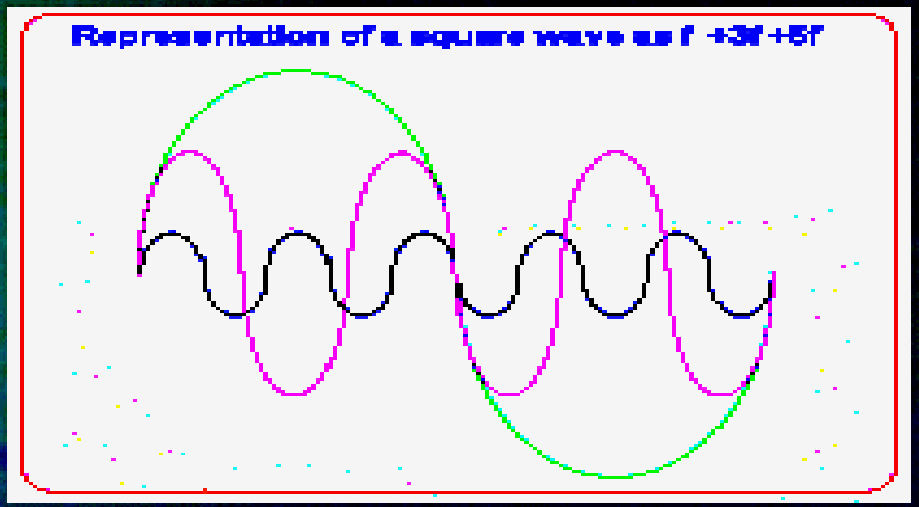
  Y=cos(wt)-cos(3wt)/3+cos(5wt)/5-cos(7wt)/7 … (etc.)

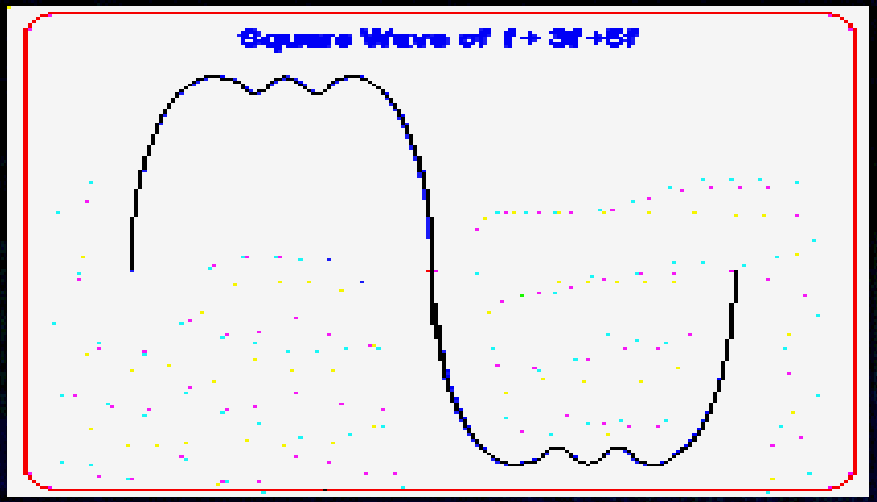
- To perfectly represent a digital signal a transmission line must pass all frequencies of sine waveforms



Digital signals

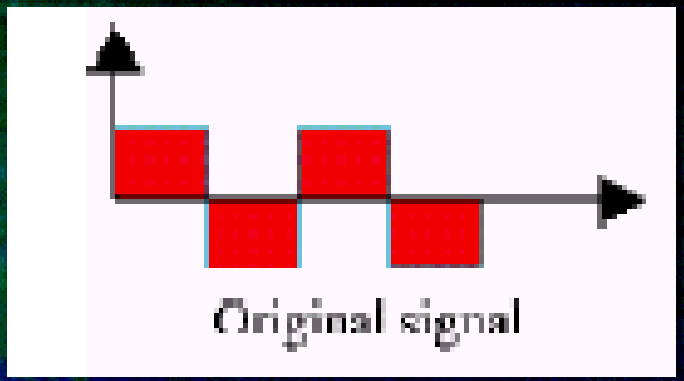
- Minimum Harmonics to represent Digital signal
  - base frequency
    - 1/2 bits per second rate
  - need fundamental plus third and fifth harmonic
    - minimum necessary to retain data when converted to digital signal

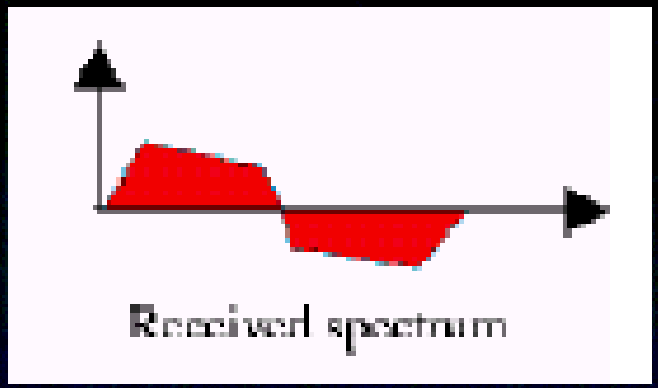




Analog and Digital Signals

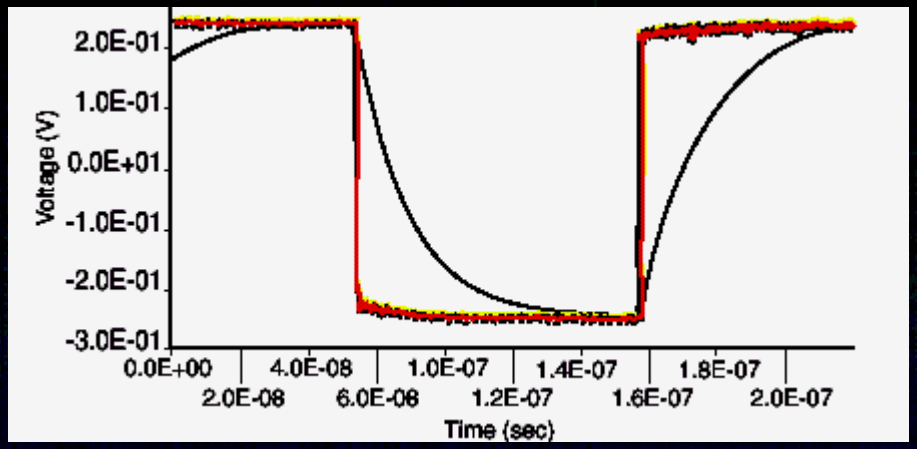
- Example
  - 1Gbps → 500MHz base frequency
  - 1.5GHz third harmonic
  - 2.5GHz fifth harmonic
  - Need at least 2.5GHz analog bandwidth to transmit 1Gbps binary digital signal





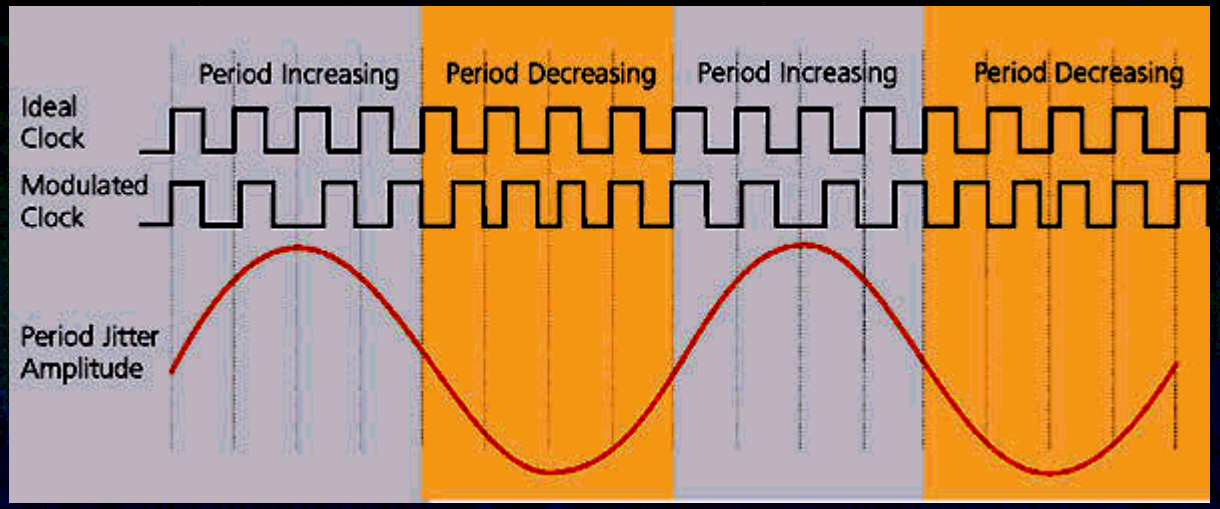
Digital signal rise time

- Relationship of Analog Bandwidth to Digital signal rise-time
  - what bandwidth is required for certain rise time
    - BW = .35/Tr
- Example
  - to pass a 100ps pulse a bandwidth of 3.5 GHz



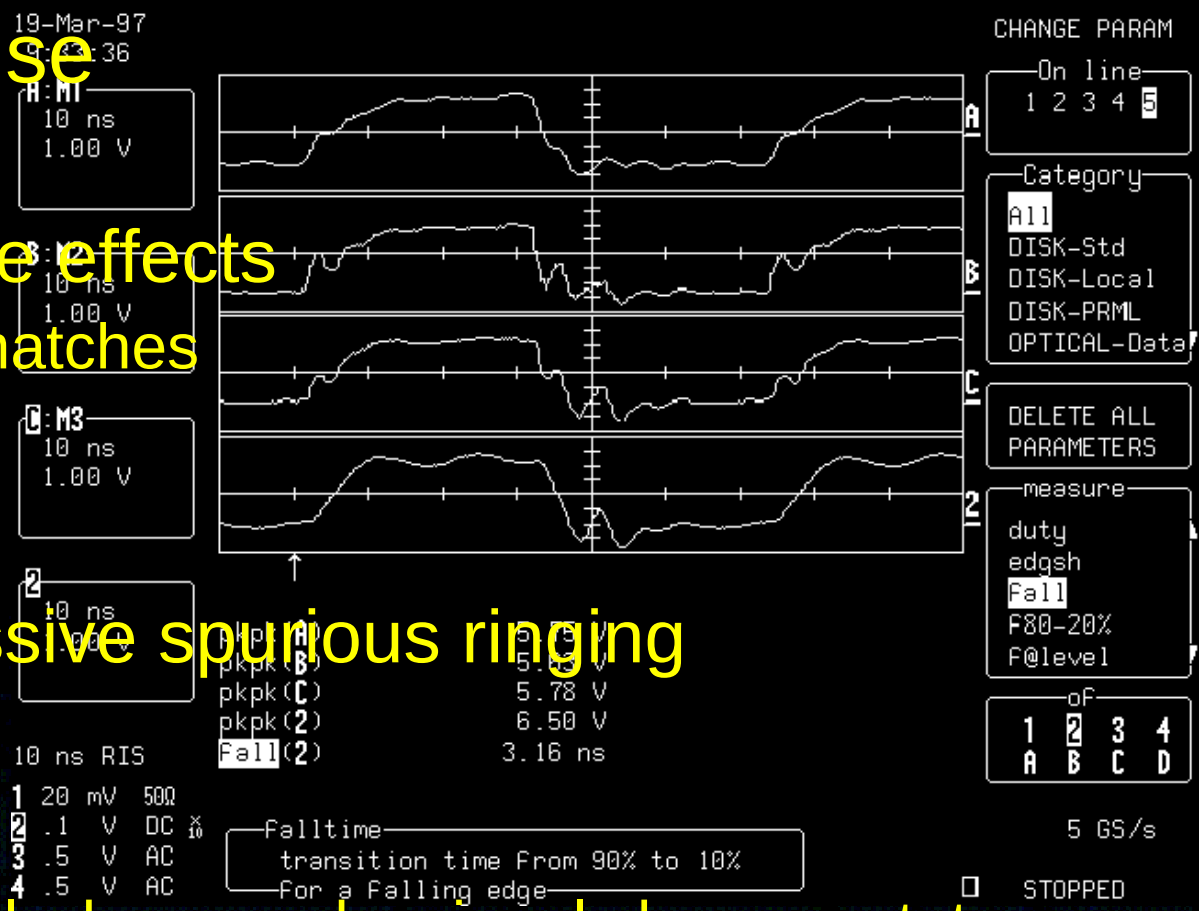
Digital signal Transmission

- What degrades digital signal transmission
  - ↗ Noise
    - – Sources of Noise
      - Connectors, PCB trace layout, IC package geometry, power and ground planes
    - – Noise Effects
      - Reflections, Crosstalk, ground shifts, inductive glitches



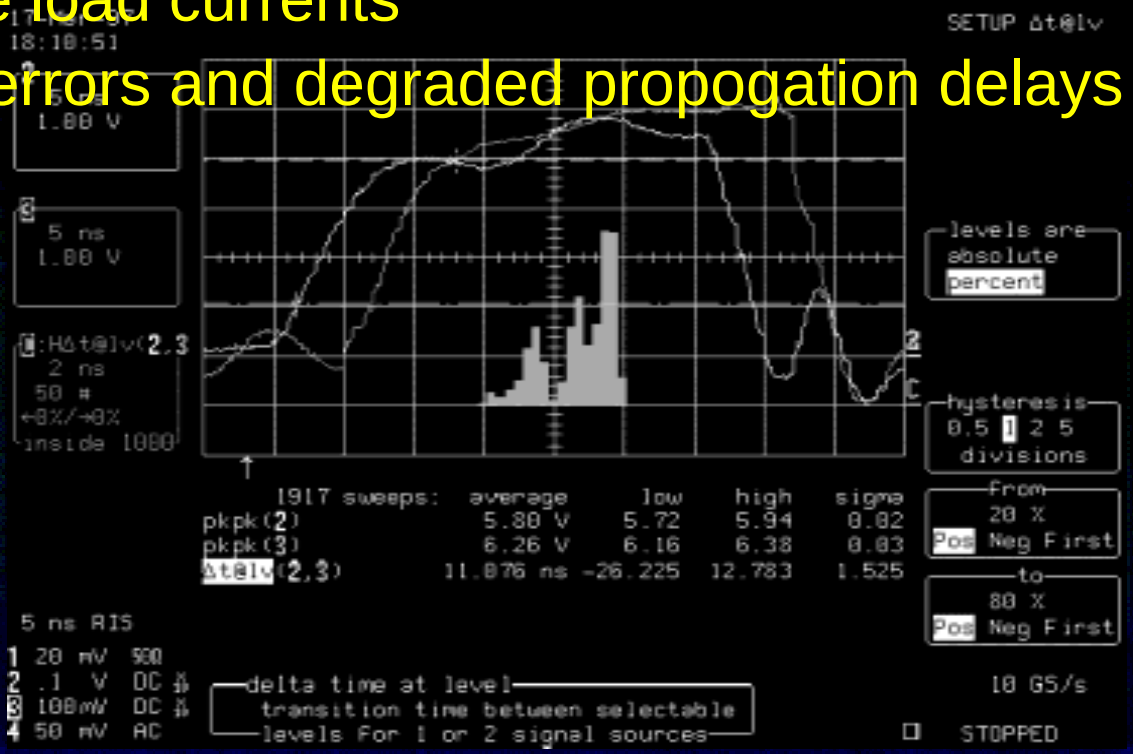
Digital signal Transmission

- Digital signal Noise
  - ↗ Transmission line effects
    - – impedance mismatches
  - ↗ Reflections
    - – leads to excessive spurious ringing
  - ↗ Crosstalk
    - – Voltage on signal when nearby signal changes state
    - – Due to capacitive and inductive coupling
    - – related to separation of line, line length, distance to ground



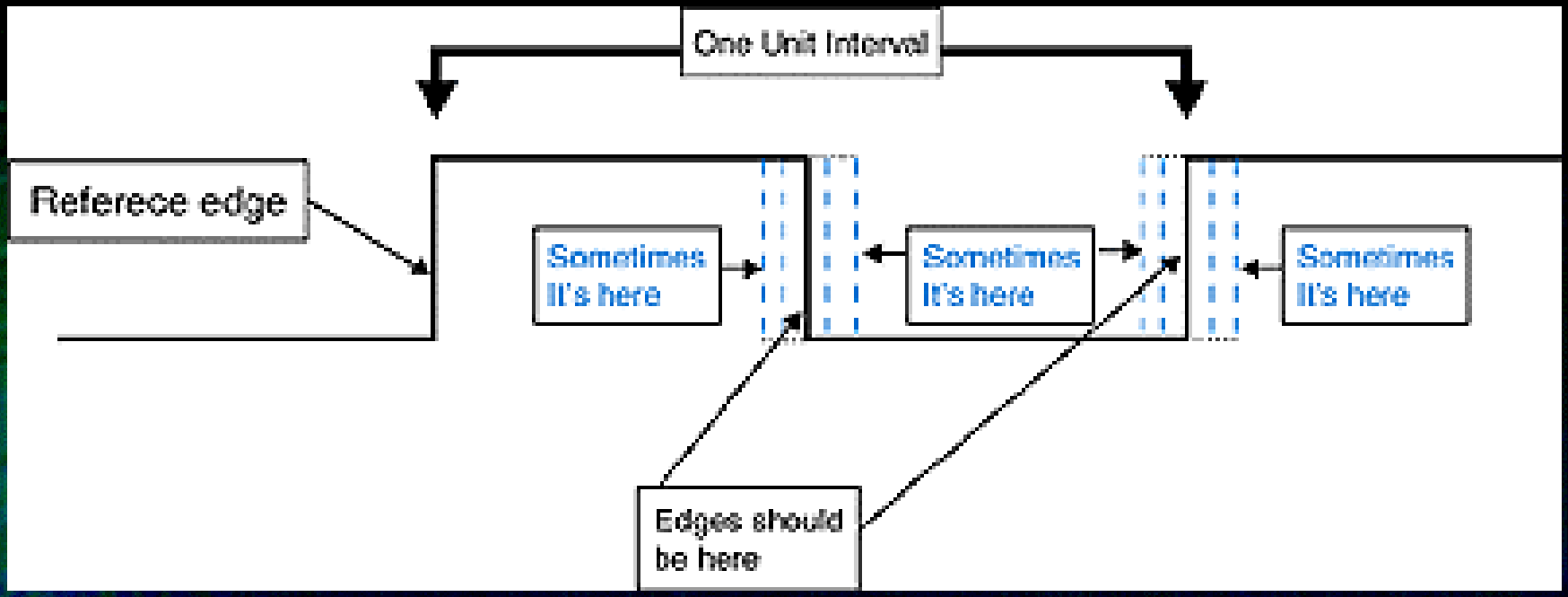
Digital signal Transmission

- Digital signal Noise cont.
  - ↗ Ground bounces
    - – shifts in reference levels due to high frequency transients
    - – caused by large load currents
    - – results in logic errors and degraded propogation delays
  - ↗ Thermal
    - – White noise

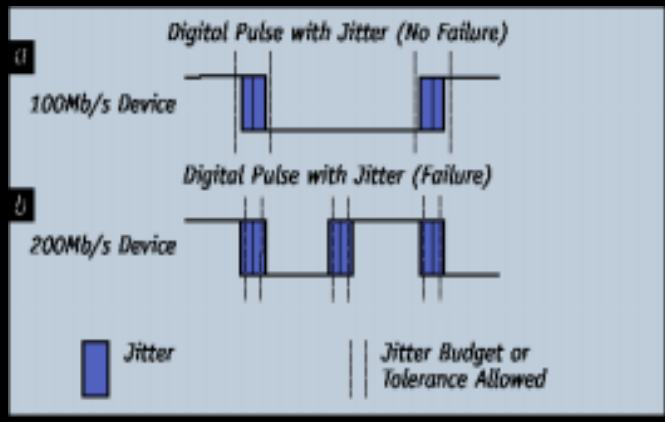


Jitter Definition

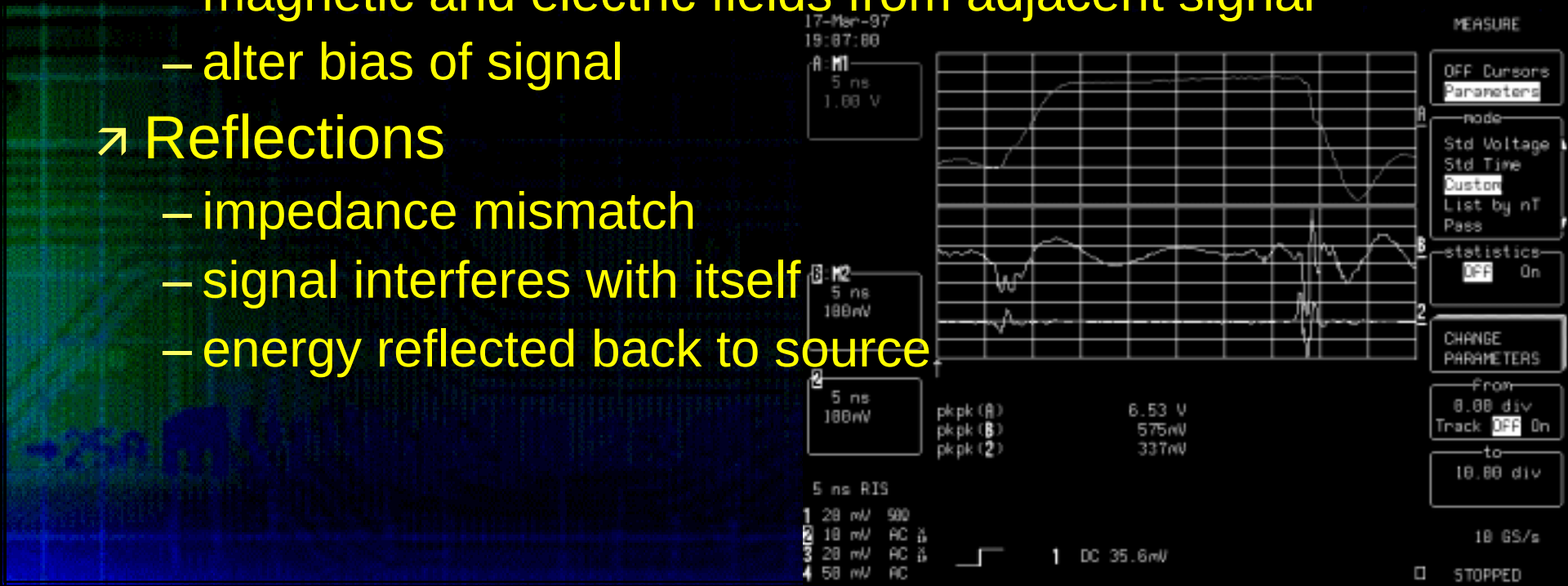
- The slight movement of a transmission signal in time or phase that can introduce errors and loss of synchronization.



Digital signal jitter

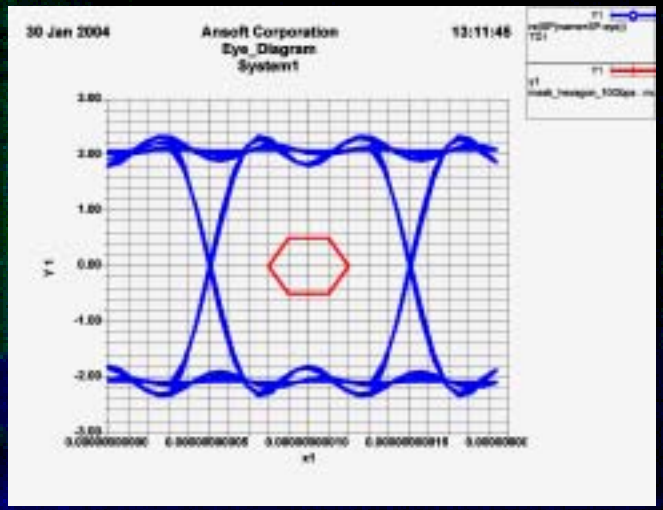


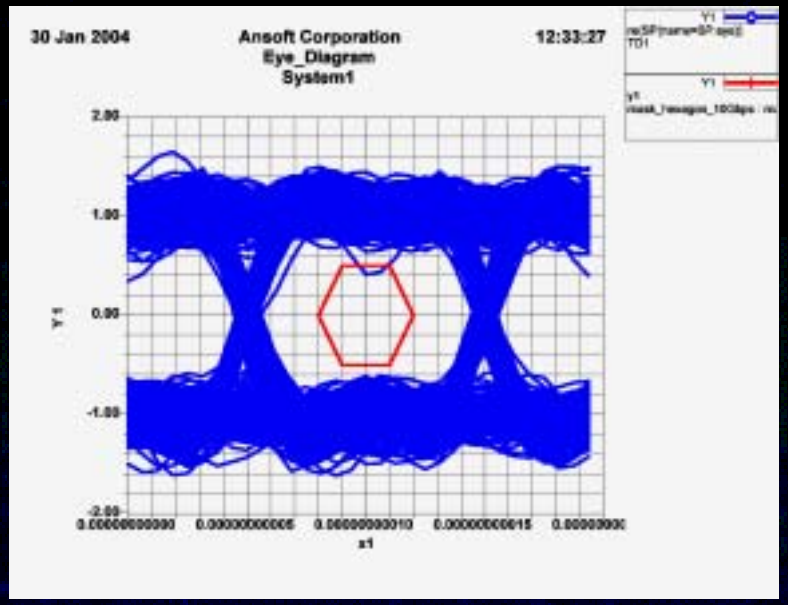
- Sources of Jitter
  - Electromagnetic interference
    - switching power supplies
    - induces noise currents into signal conductor
  - Crosstalk
    - magnetic and electric fields from adjacent signal
    - alter bias of signal
  - Reflections
    - impedance mismatch
    - signal interferes with itself
    - energy reflected back to source



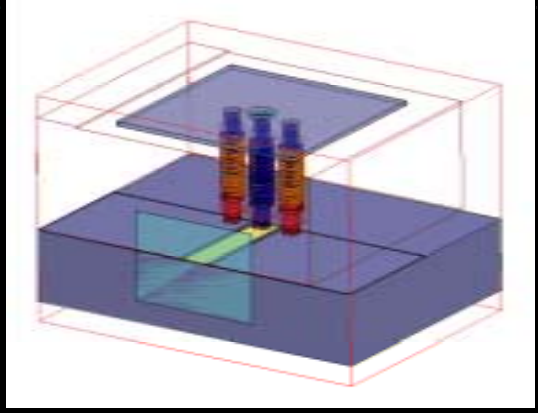
Jitter

- Conditions that improve or degrade Jitter
  - Quality of the end termination in the tester
  - Quality of the device termination
  - Physical distance between the discontinuity and terminations
  - Occurrence of other discontinuities
  - Operating data rate

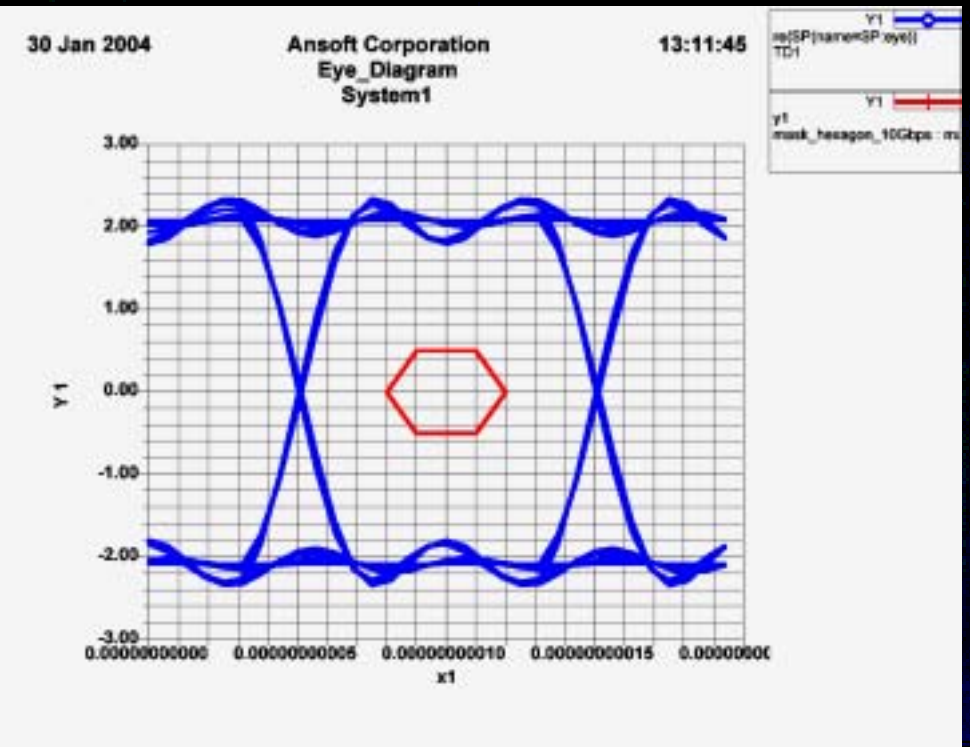




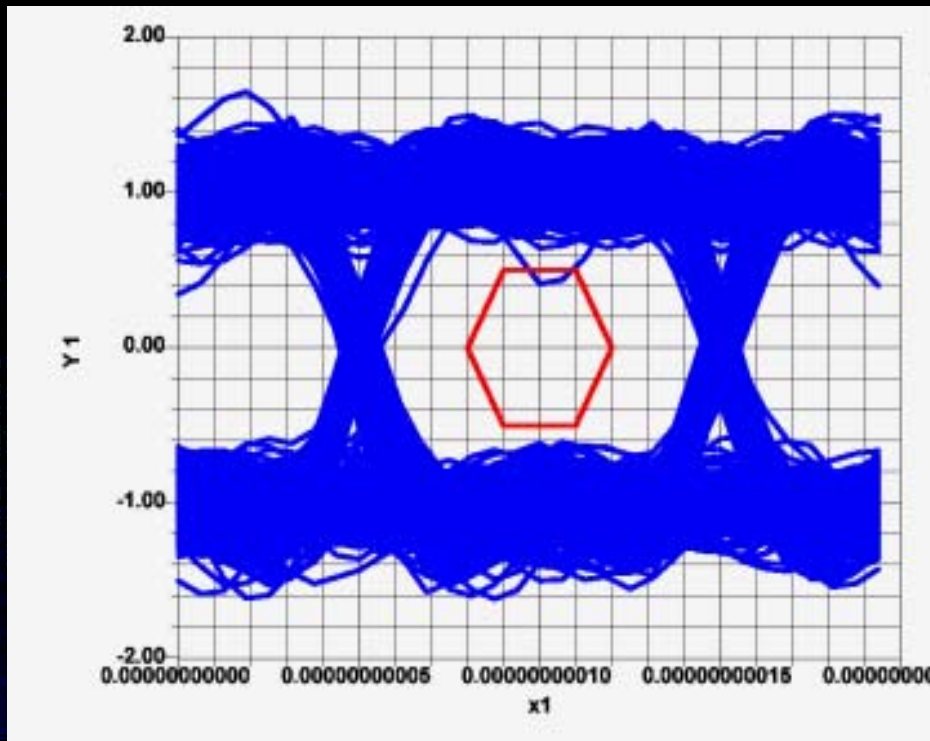
Eye Diagrams



- Ideal case
  - no noise
  - probes only

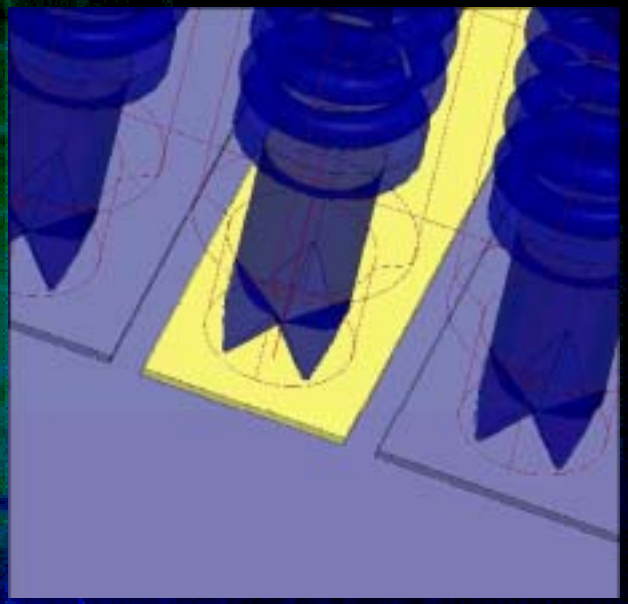


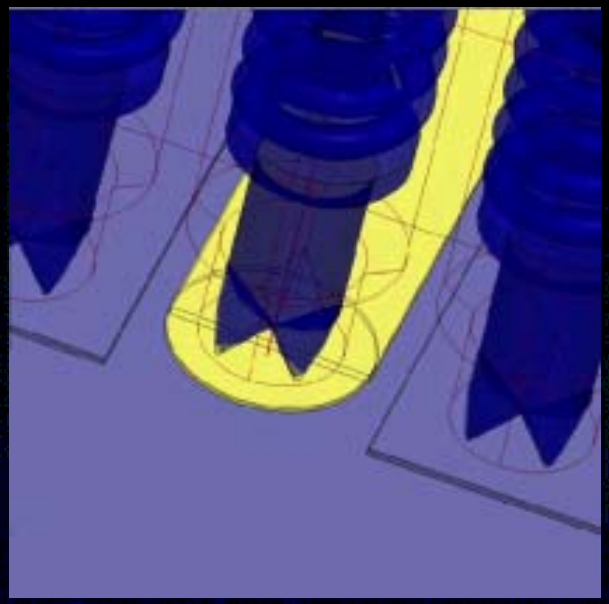
- Real case
  - added noise
  - added pcb

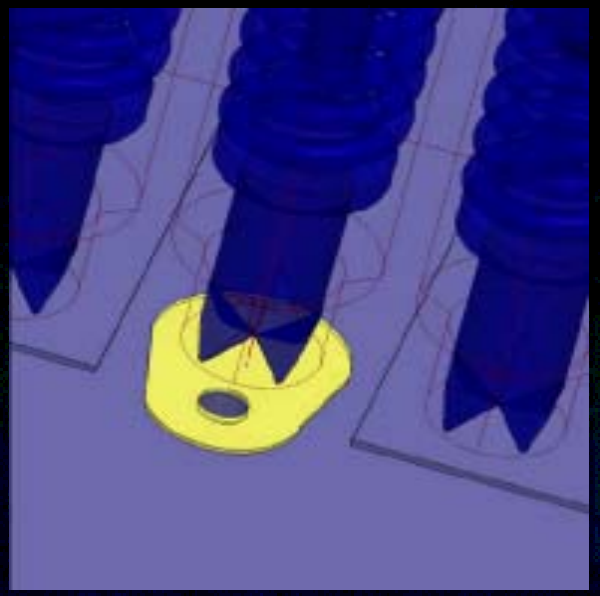


Future Design Challenge

- Optimize the interface between board and contactor
  - develop board trace characteristics that minimize the impedance mismatch
  - 90 degree transition capacitive
  - compensate with trace termination geometry







Conclusions

- Board and contactor interact and therefore must be characterized together
- For successful digital signal transmission a conductor must pass at least the 5th fundamental
- Rise time limited by bandwidth
- Noise creates jitter which leads to digital signal errors
- Optimization of board to contactor transition to increase signal integrity

References

- "Jitter effects on Analog to Digital and Digital to Analog Converters", copyright 1999, 2000, Troisi Design Limited
- **"Measurement Challenges for On-Wafer RF-SOC Test",** Wai Yuen Lau, Agilent Technologies, 1400 Fountaingrove Pkwy, Santa Rosa, CA 95403
- "DATA COMMUNICATIONS", v3.0 © Copyright Brian Brown, 1984-1997. All rights reserved.
- "Signals", Anan Phonphoem, Ph.D.anan@cpe.ku.ac.th, http://www.cpe.ku.ac.th/~anan, Computer Engineering Department, Kasetsart University, Bangkok, Thailand

A Method for Contactor Characterization to 25 GHz

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Eric Bogatin, Synergetix

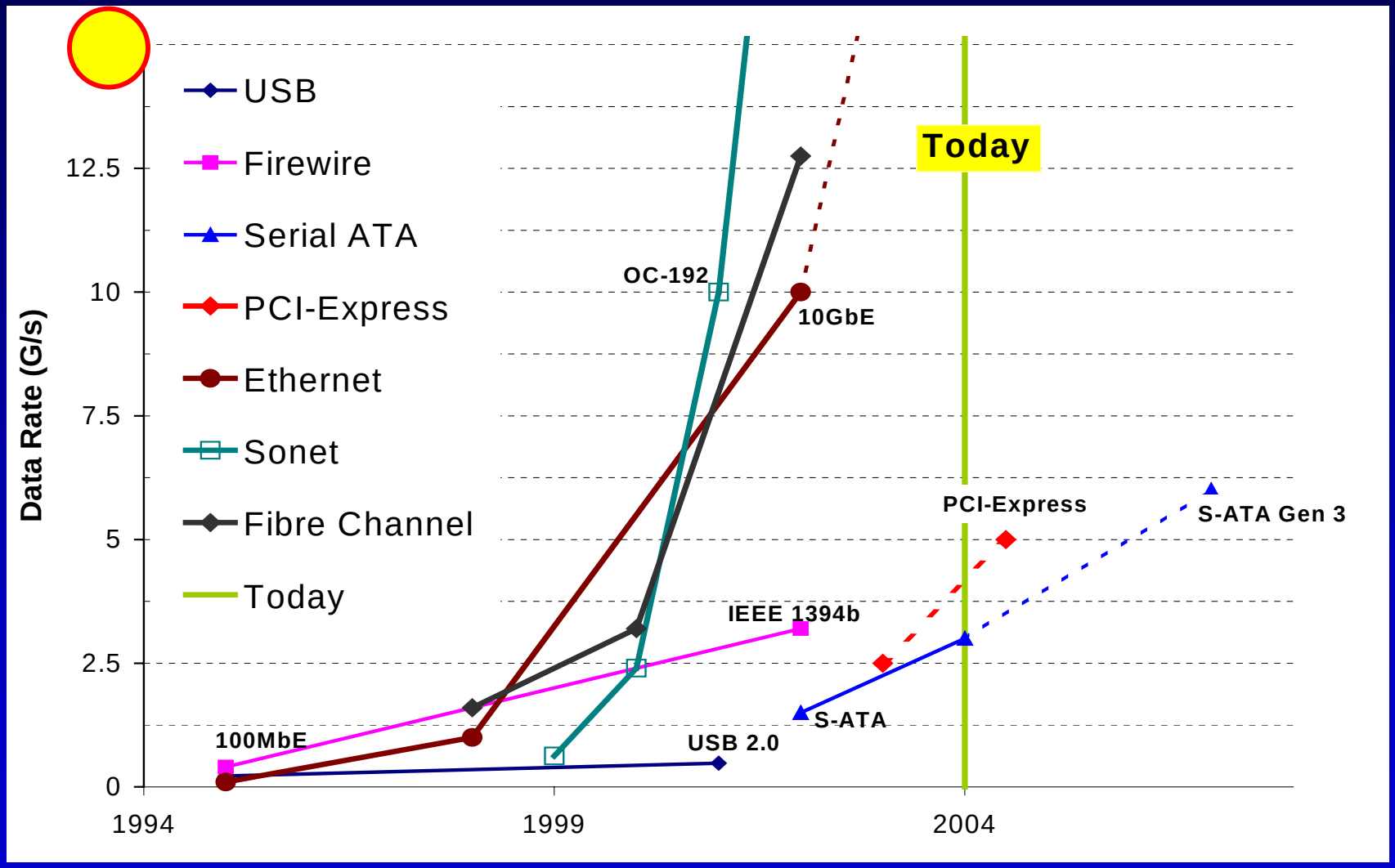
March 21, 2004

BiTS
BURN-IN & TEST SOCKET WORKSHOP

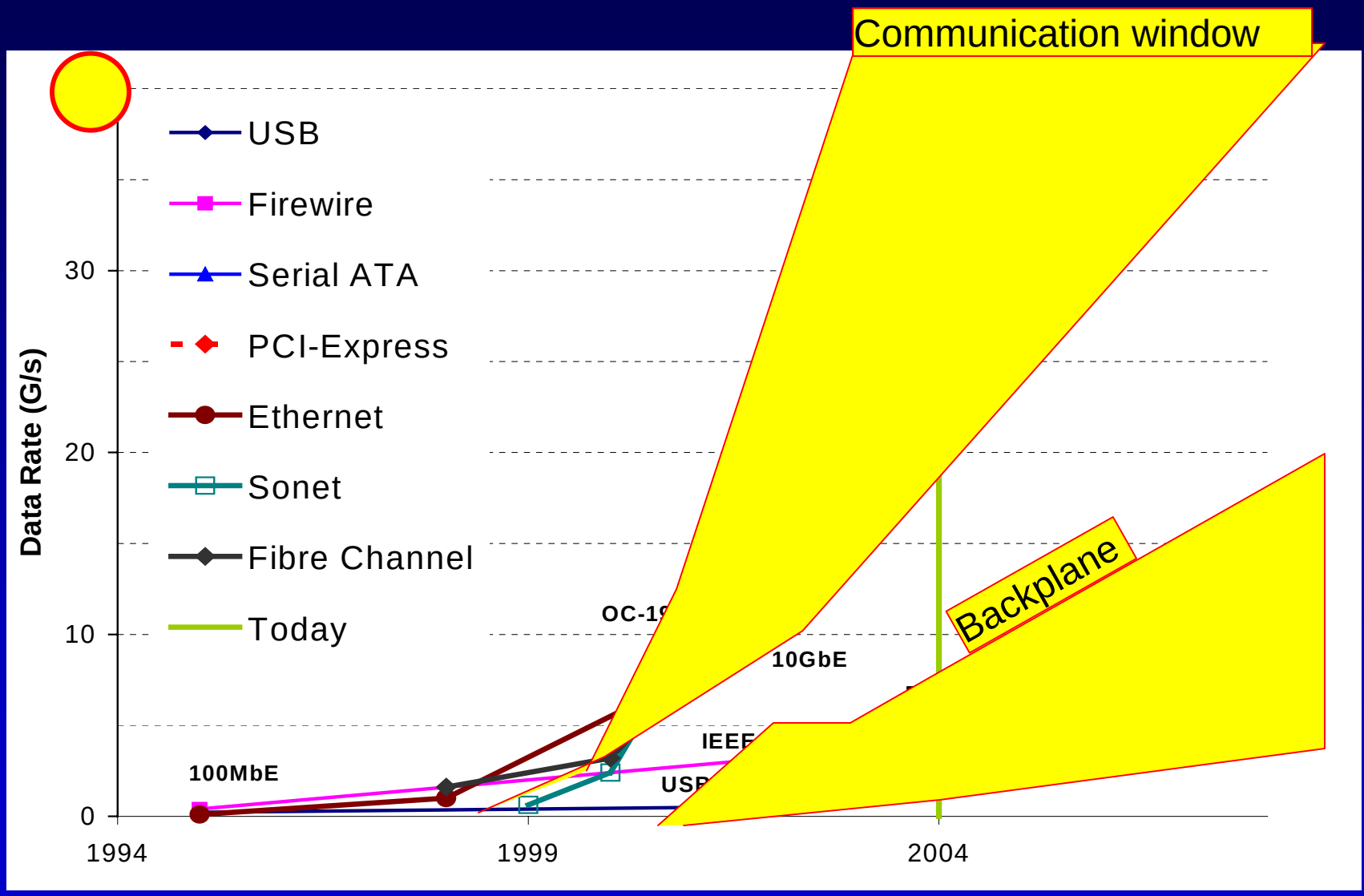
Agenda

- Driving forces on test socket requirements
- Existing Socket characterization techniques
- A higher bandwidth method
- An example
- Summary

Increasing IO data rates



IO data rates… expanded



The Challenge

- To test these devices at speed, a socket is required
  - ✓ Impact → socket must be well understood electrically
- Can have two independent requirements:
  - ✓ Power/return pins: Z(f) → 0
    - ➢ CRES stable and well below 50 mohms
    - ➢ Loop inductance less than 3.0 nH
  - ✓ Data rate pins, Z_0 → 50 Ohms
    - ➢ Insertion loss > - 1 dB over the freq range
    - ➢ Return loss < -15 dB over the freq range

      -- or --

    - ➢ Electrical lengths very short
- Data rate pins, up to <u>at least</u> the signal bandwidth

Data Rate → Signal Bandwidth

$$F_{clock} = \frac{1}{2} \times Gbps$$

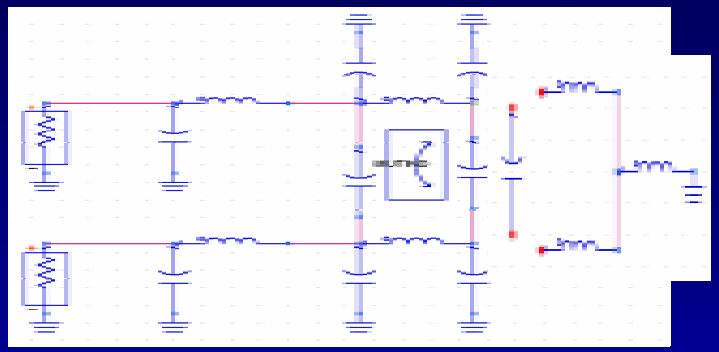
$$BW \sim (2 \rightarrow 5) \times F_{clock}$$

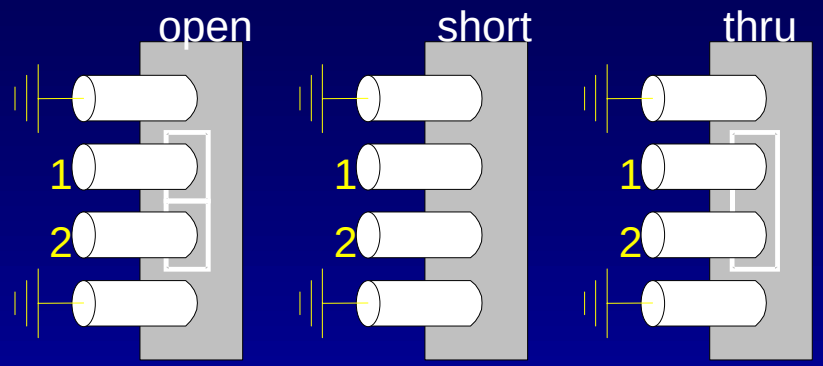
$$BW \sim (1 \rightarrow 2) \times Gbps$$

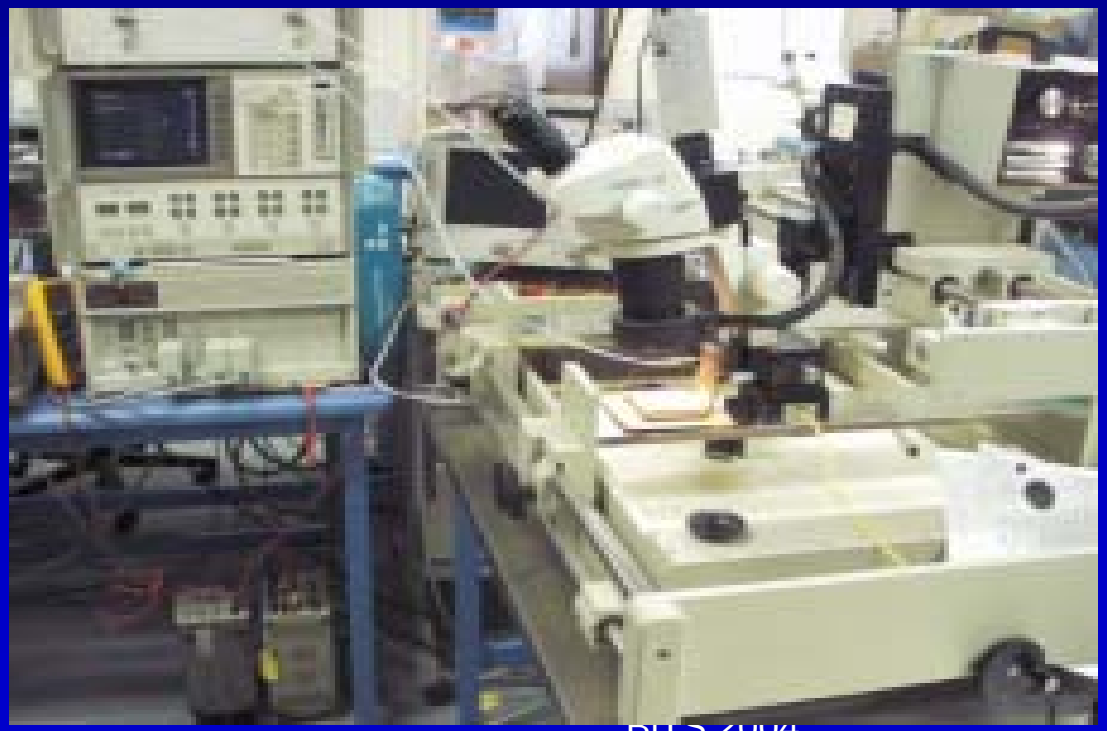
Signal bandwidths will be > 20 GHz

Traditional “High Bandwidth” Technique: open / short / loop thru

Covered in great detail in BITS 2003

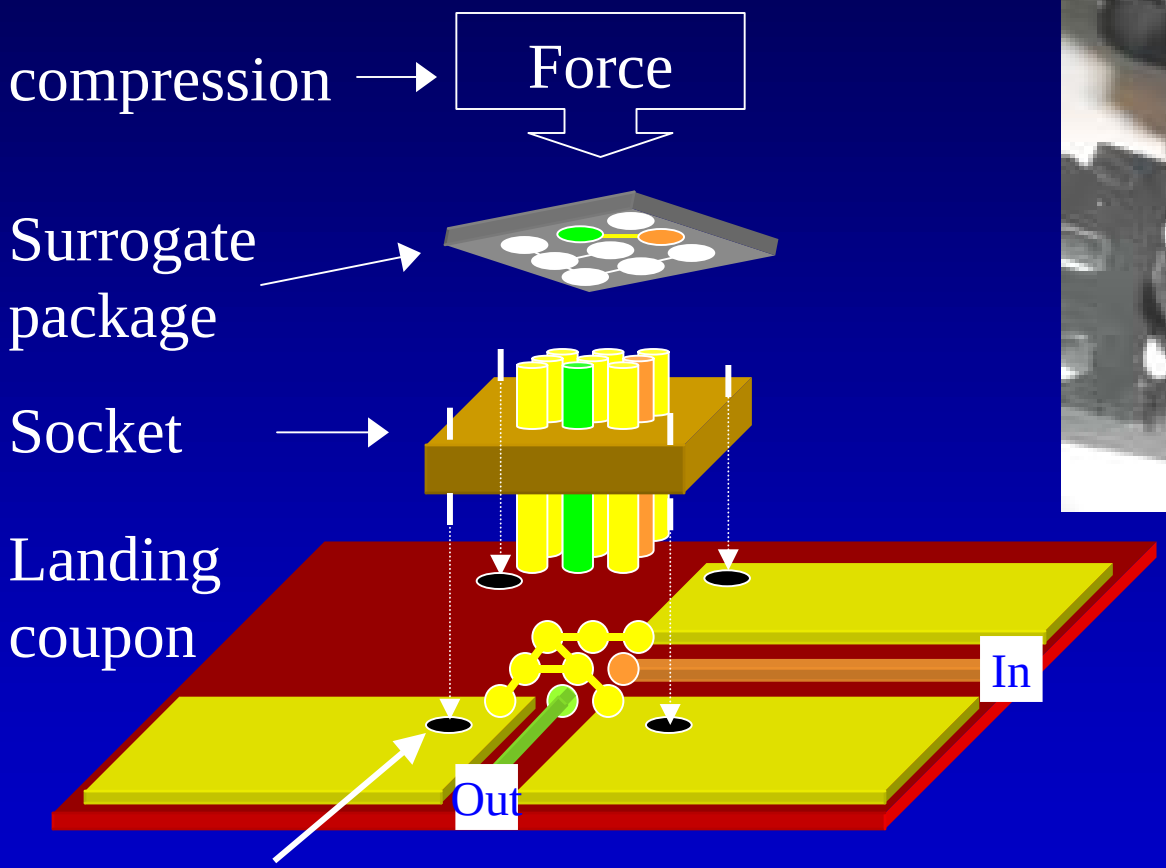


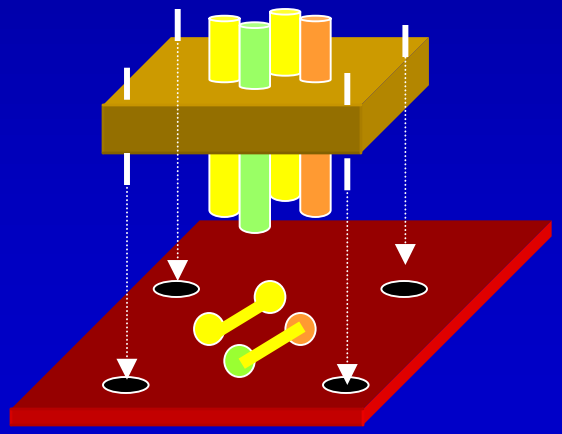




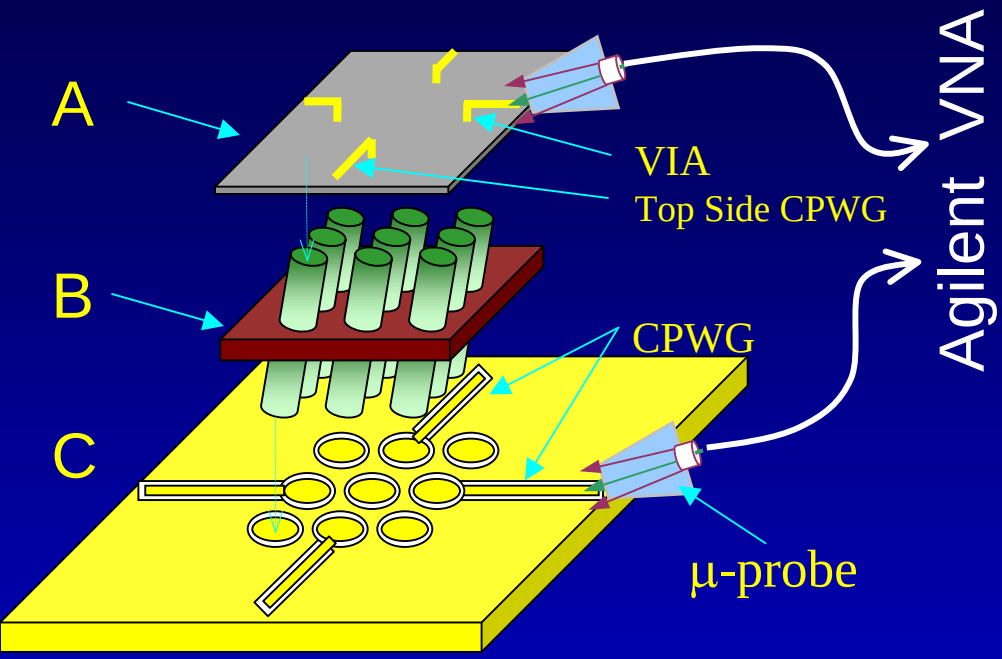
BW limitation is ability to model the surrogate chip

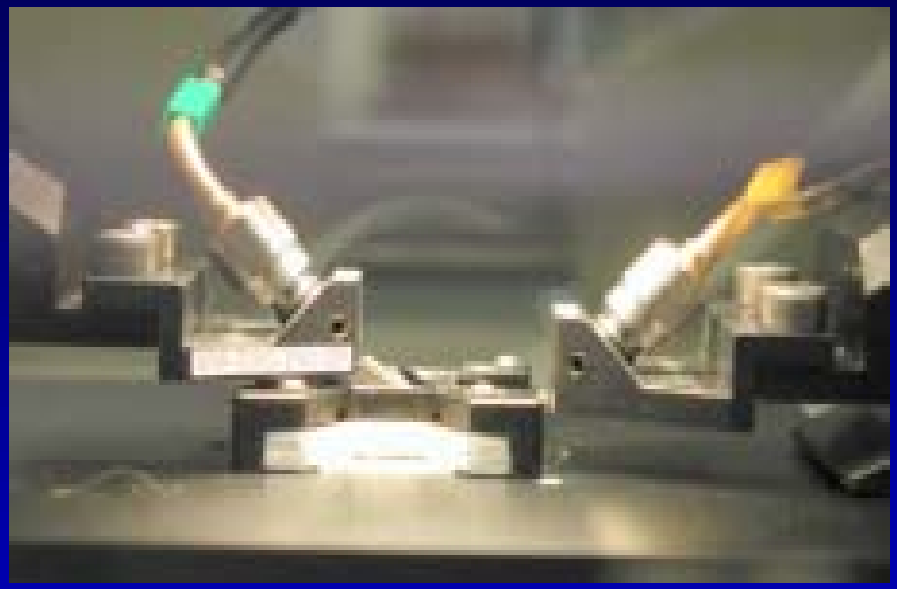
2 Traditional Loop Thru methods



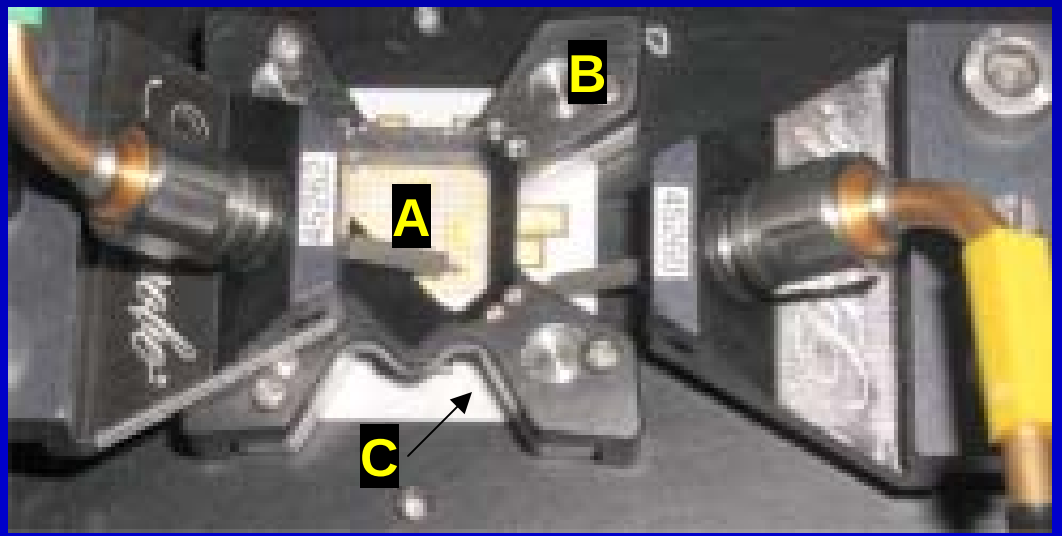


Two port through





A → Surrogate Package
B → Socket (DUT)
C → Landing coupon

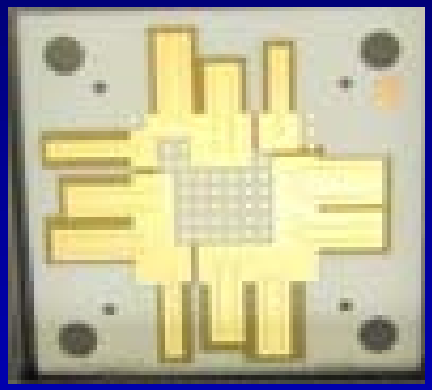


One Higher Bandwidth Technique: measure fixtures and de-embed

Measure complete system

\-

Landing coupon



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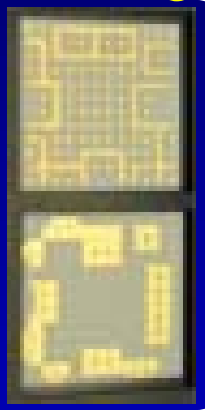
Surrogate package



Measure surrogate package and landing coupon, independently

\= Socket response

Numerically extract just the socket

Thru measurements

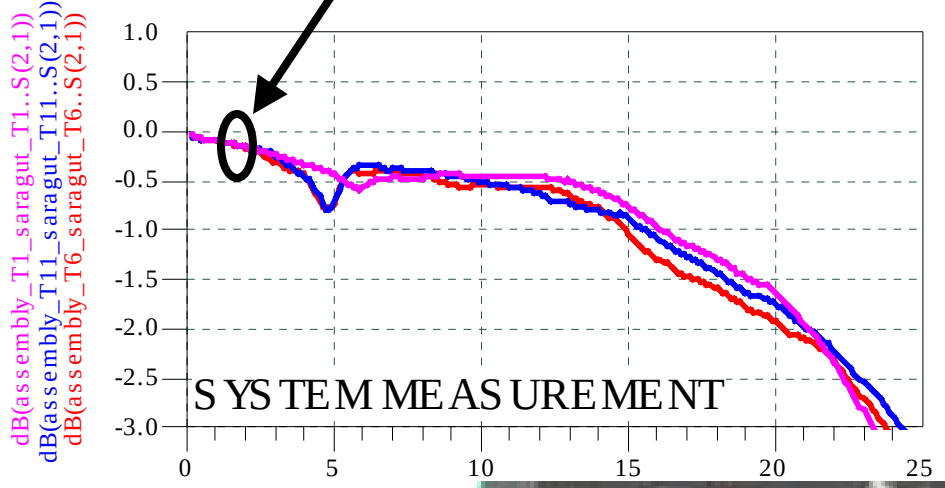
#	Description	+'s	-'s
1	**TDR and measure risetime** (socket only)	•Cheap and easy	•BW is inferred from step risetime •Pin-to-pin coupling not measured •Fixture removal more difficult
2	**Two port thru** (socket only)	•No extra hardware	•Difficult to probe 2 sides of socket simultaneously •Discontinuity at ref. plane
3	**Two port loop bandwidth** (landing coupon or shorted package)	•Relatively cheap with mostly OTS components	•Complex shorted package requires characterization and deembedding •Discontinuity at ref. plane
4	**2-port open/short/thru** (loop) (landing coupon + surrogate package)	•Measures pin-to-pin and pin-to-ground coupling	•Assumes thru = ½ loop •Open/short/thru require characterization/deembedding
5	**Two port through** (landing coupon + surrogate package)	•Most expensive •Most controlled / highest accuracy	•Coupon and surrogate only approximately emulate actual package and board

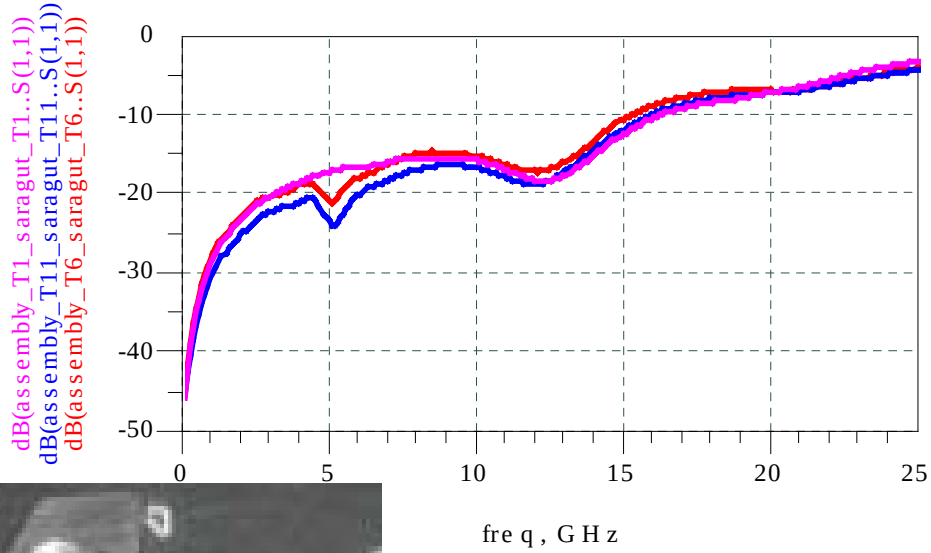
Measurement System

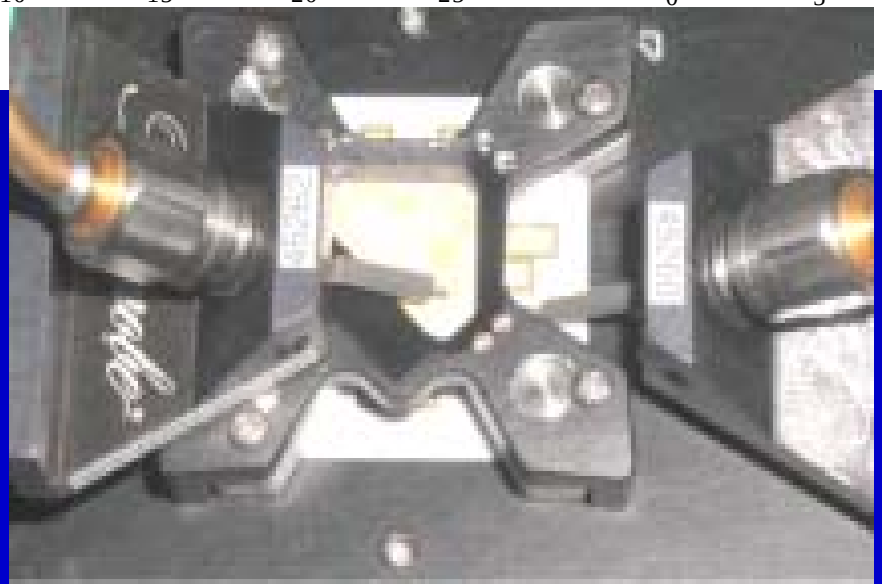
- Equipment list:
  - ✓ GigaTest Labs Probe Station
  - ✓ 35 GHz coaxial cables (3.5mm SMA connectors)
  - ✓ Agilent Technologies 8510C VNA
  - ✓ GGB probes, qty=2 (part number 40A-250-GSG-DP)
  - ✓ Cascade Microtech LRM calibration substrate
  - ✓ Cascade Microtech Wincal LRM calibration program
  - ✓ Agilent Advanced Design System software (ADS 2002C)
  - ✓ Measurements and analysis

System (Measured) Performance

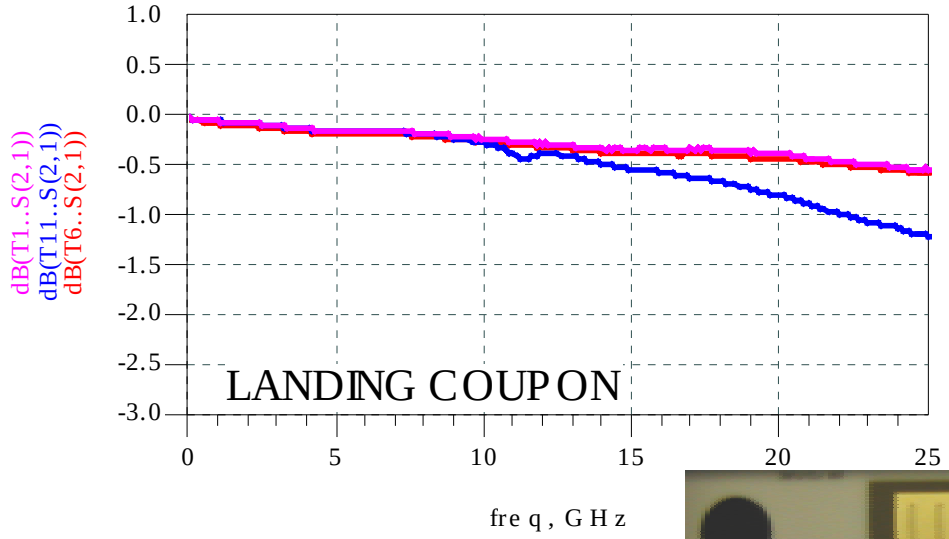
3 different single ended paths

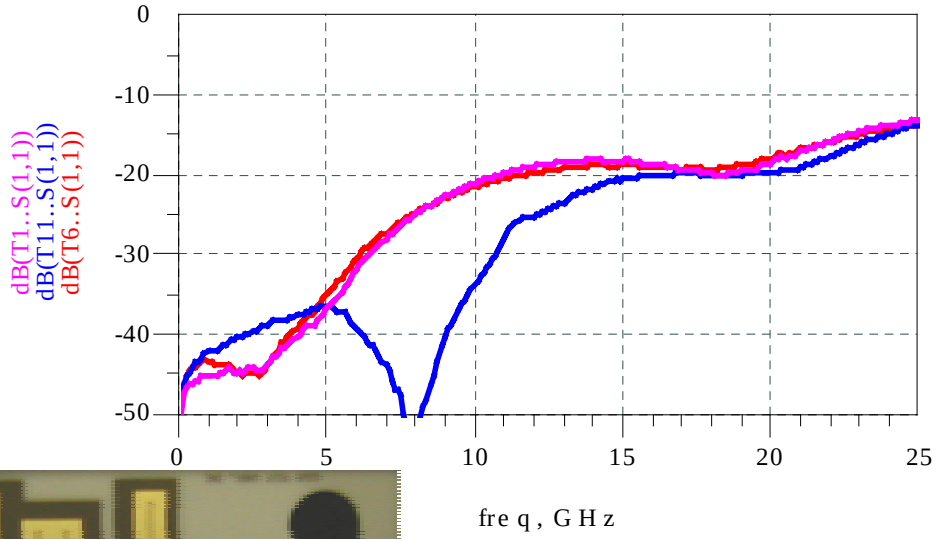


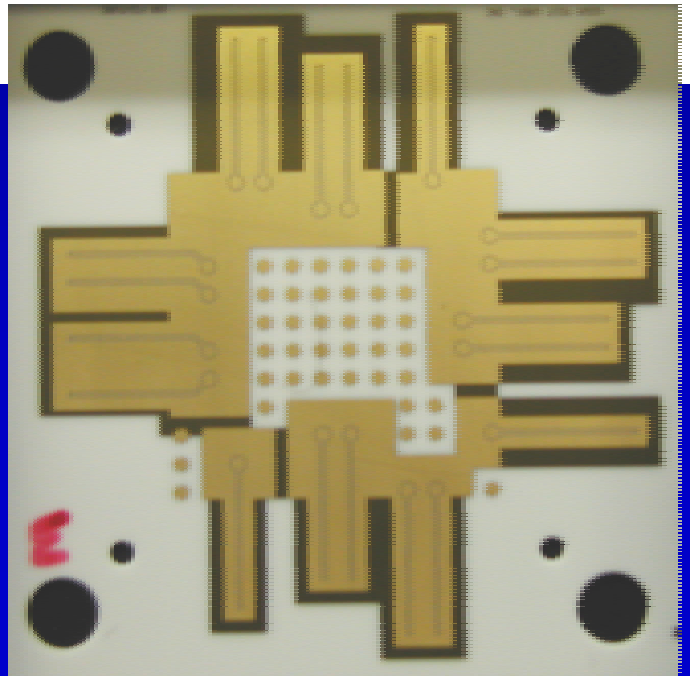




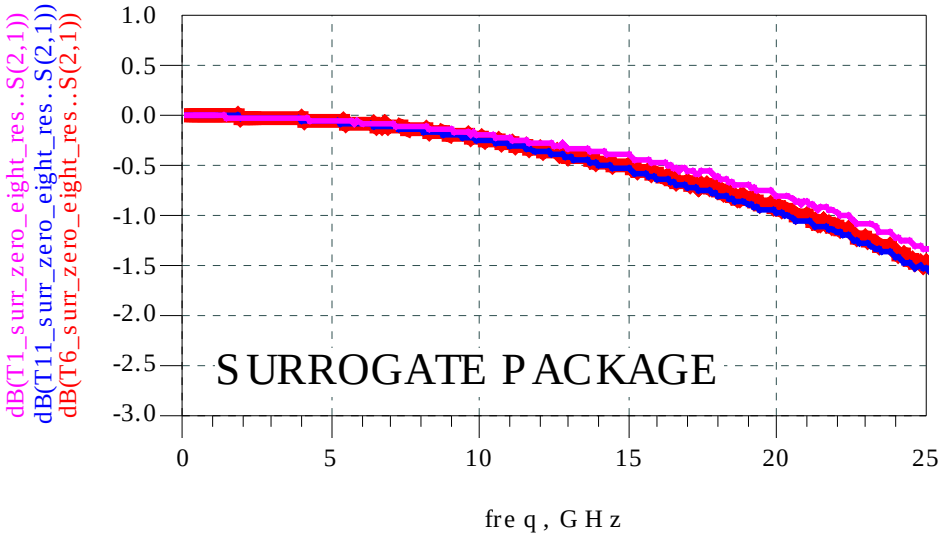
Fixture, Landing Coupon

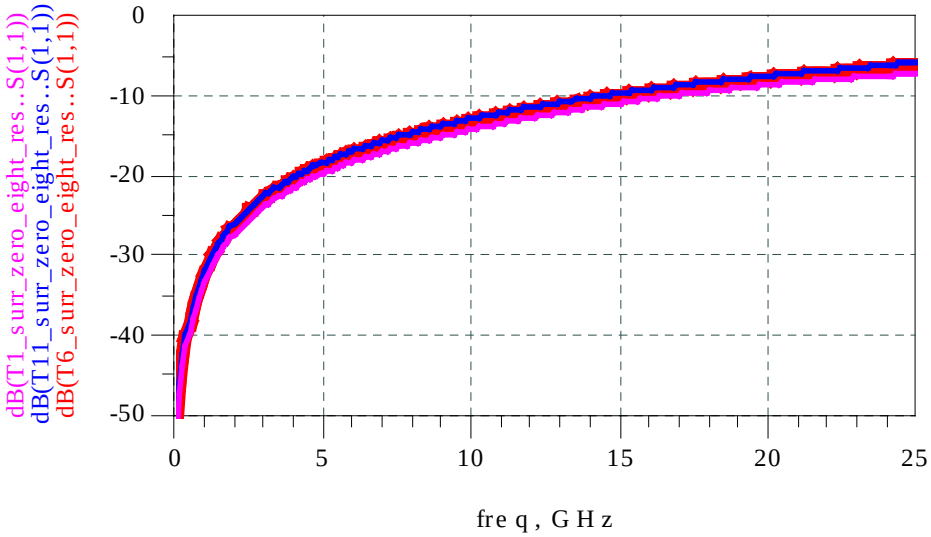






Fixture, Surrogate Chip





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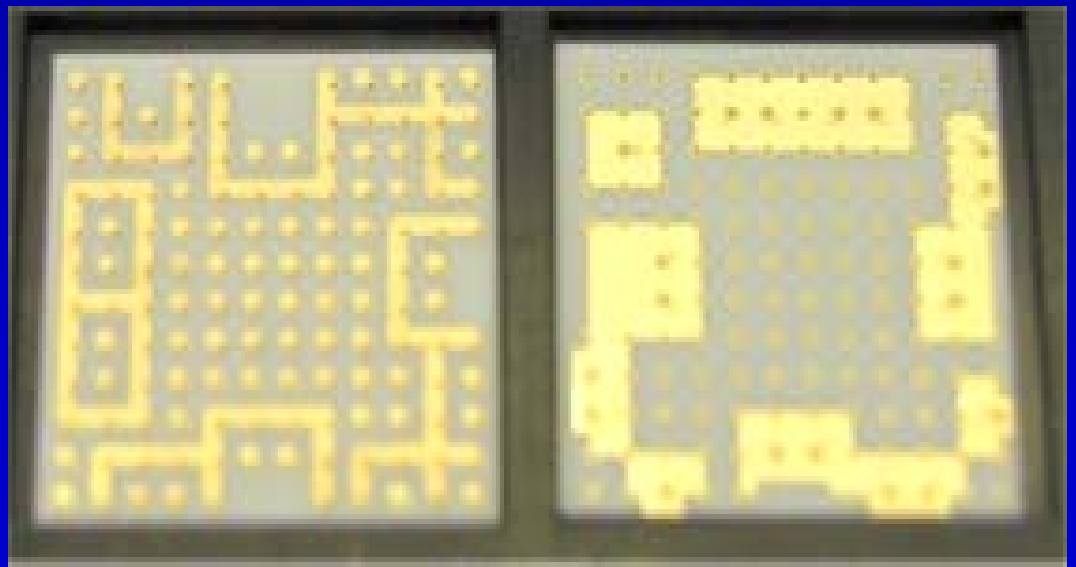
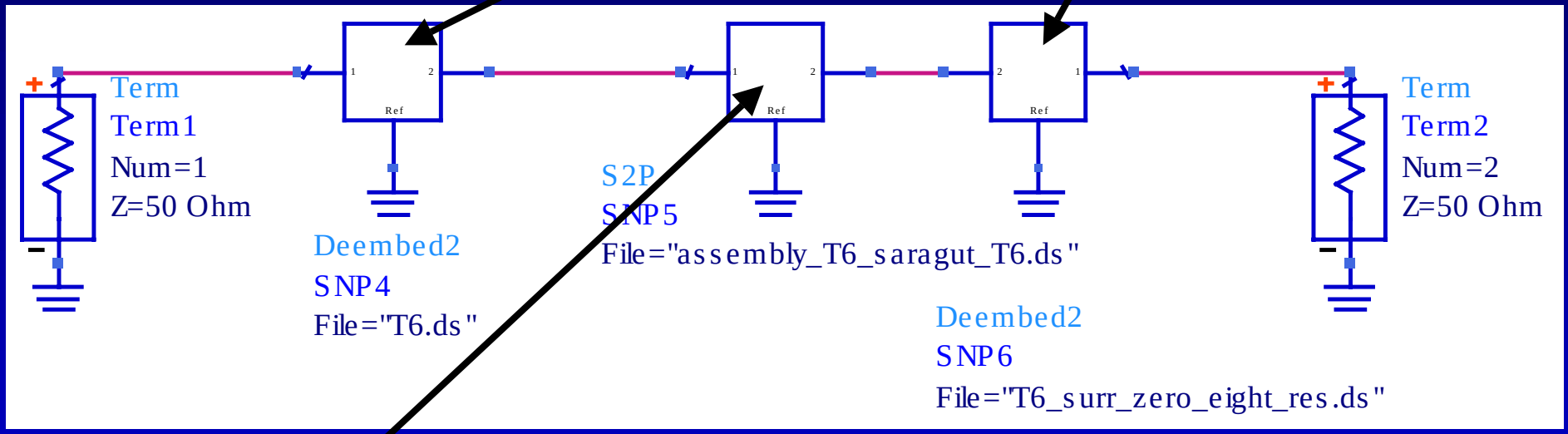


top

De-embed to Extract Just the Socket, in Agilent's ADS

Landing coupon De-embed data file (slide 14)

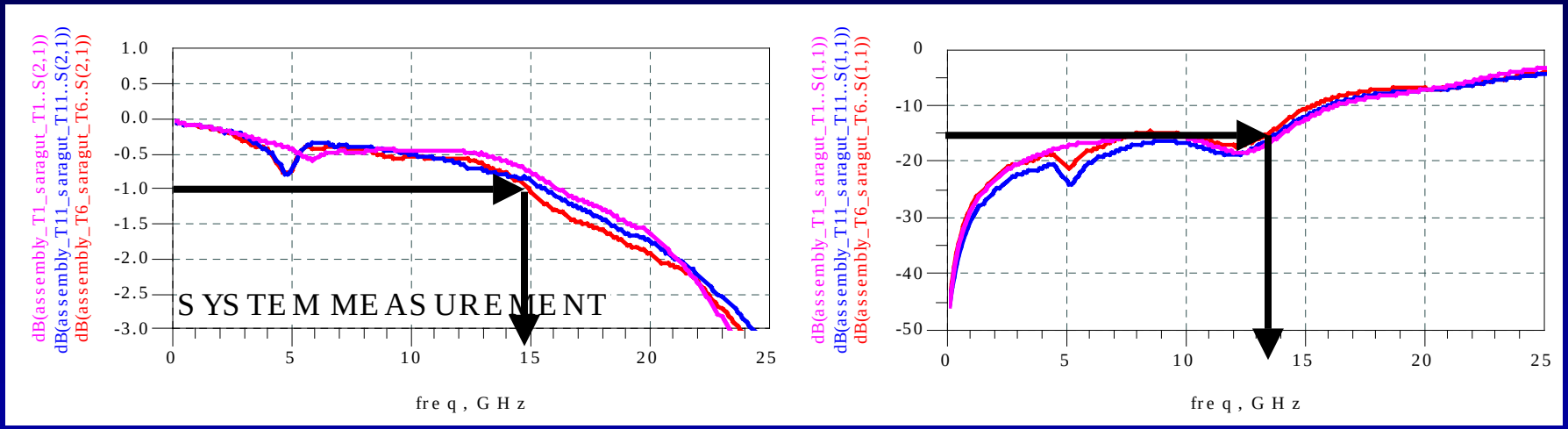
Surrogate De-embed data file (slide 15)

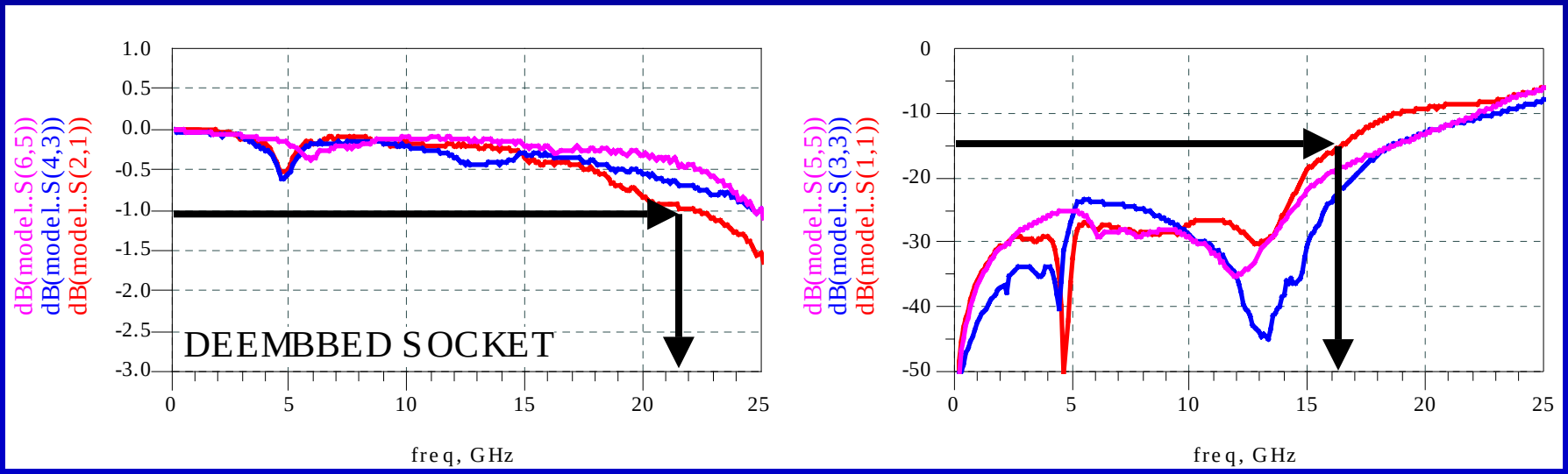


Measured Fixture/Socket/Surrogate (slide 13)

- Simulated S parameters of de-emedded socket only

Through Path, De-emedded Socket Only





Strengths

- Landing coupon and surrogate package are very clean well out to 25 GHz
- Allows for a fair “apples-to-apples” comparison of multiple sockets
  - ✓Removes any layout advantage one supplier may have over another
- Discontinuities at launch can be adjusted out if necessary
  - ✓Common for ref plane to be off from probe tip

Weaknesses

- Expensive; other options use either mechanical package samples or other ‘cheap’ fixtures
- Ceramics are not identical to final tooling environment
  - ✓ Can’t optimize the via/pad/pin as a system, only look at the pin independently.
- HTCC vias are poor. Surrogate package performance was weakest part
- More than two ports, very challenging to probe.
  - ✓ Launches too close to each other to fan out

Next steps

- Second spin on the hardware
  - ✓Increased socket size, match mechanical socket samples
  - ✓Higher number of coupled lines
  - ✓More extensive usage of LRM and TRL calibration structures
  - ✓LTCC verse HTCC tradeoffs

Conclusions

- Application bandwidths will only increase
- New characterization techniques need to evolve with new socket technologies
- The fixtures used to facilitate the measurements are as critical as the socket itself.
- Measuring each component and de-embedding techniques have a useful bandwidth above 25 GHz