BiTS™

Burn-in & Test Socket Workshop

March 7 - 10, 2004
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

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Burn-in & Test Socket Workshop

Technical Program

Session 3
Monday 3/08/04 1:00PM

MATERIALS SELECTION: PROPERTIES AND BEHAVIORS

"Polymer Material Selection For ESD Sensitive IC Processing"

Glenn Cunningham – Intel Corporation

"Dimensional Stability And High Frequency Properties Of Polymeric Materials For Machined Test Sockets"

Paul Kane P.E. – DuPont **Joy Bloom Ph.D.** – DuPont

"Visco Elastic Behavior Of Anisotropic Conductive Polymers"

Roger Weiss, Ph.D. – Paricon
Chris Cornell – Paricon **Glenn Amber** – Paricon

"Solving Cathodic (Conductive) Anodic Filament (CAF) Migration With THERMOUNT® Laminate And Prepreg"

Ceferino Gonzalez – DuPont **Subhotosh Khan** – DuPont

Polymer Material Selection for ESD Sensitive IC processing

Glenn Cunningham
Tooling Development Engineer
Intel Test Tooling Organization

BURN-IN & TEST SOCKET WORKSHOP

March 7 - 10, 2004

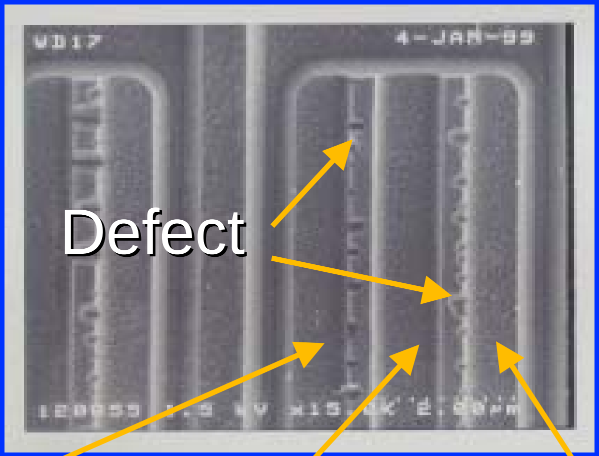
AGENDA

- ESD Problem Statement
- ESD Background
- Materials Background
- Case History
- Trends for ESD Sensitivity
- Material Challenges
- Conclusion

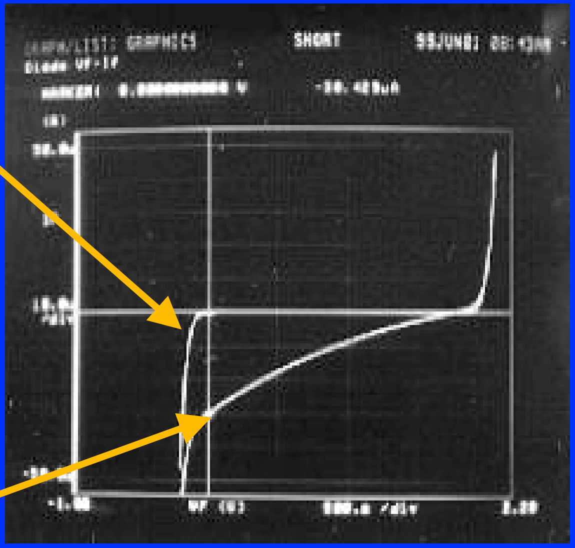
ESD Problem Statement

- **In recent years the IC industry has experienced an increase in Electrostatic Discharge (ESD) induced failures on all process platforms (microprocessor, chipsets, and flash). Contactor materials have proven to be a major contributor to the failures.**

SEM Photo of Typical ESD Failure



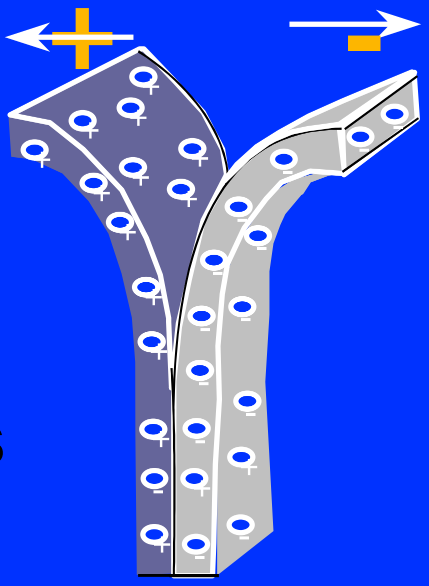
I/V Curve of ESD Failure



ESD Background (Friction Charging)

- **Triboelectric charging (AKA Friction charging) occurs when two materials come in contact and are then separated**

- **Any material may be charged, whether it stays charged depends on it being a conductor or an insulator.**

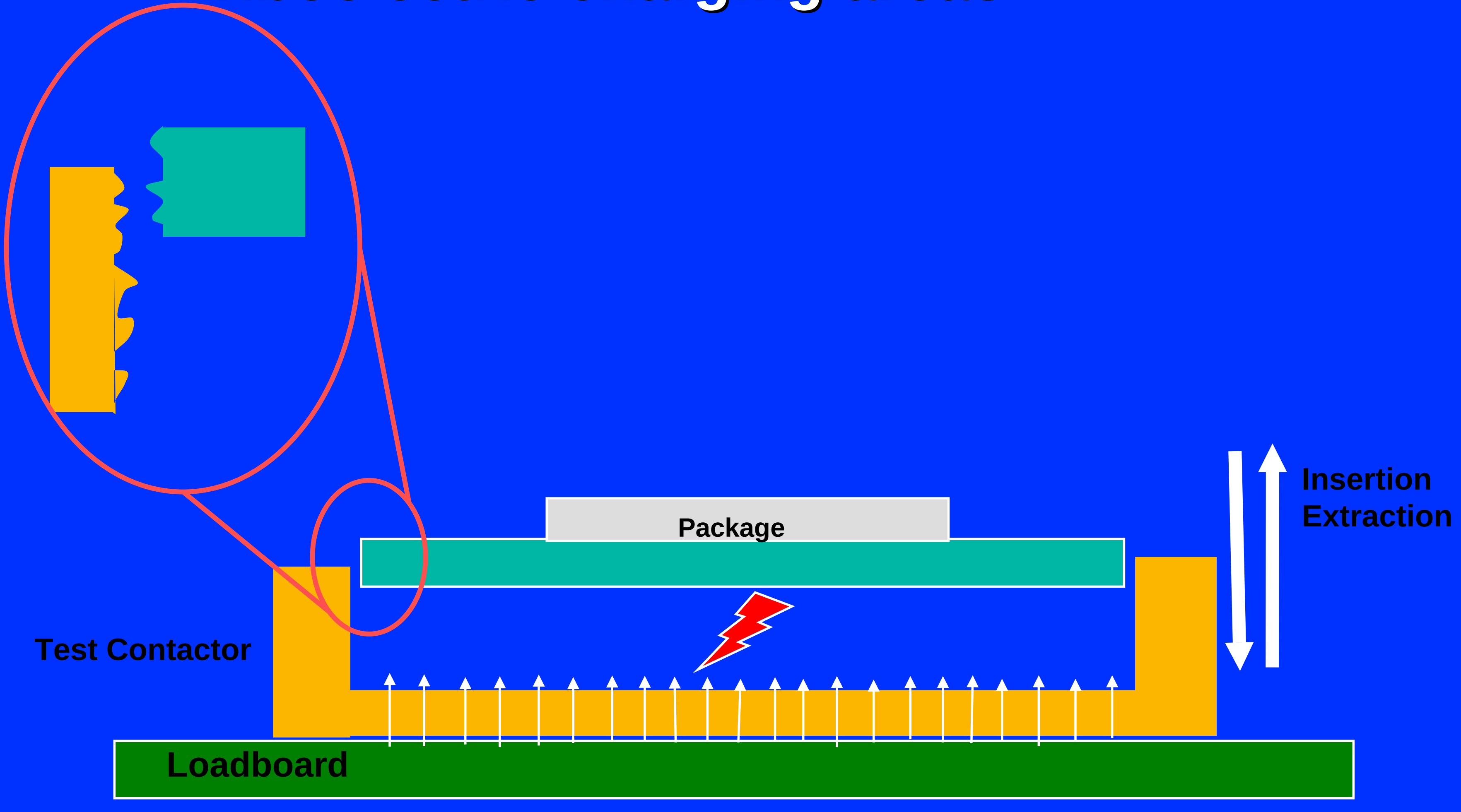


Example of Tribo Series

Positive +	P-Type Silicon
	Water
	Human Hands
	Quartz
	Nylon
	Aluminum
	Chrome
	Steel
	Polyurethane
	Polyethylene
	Polypropylene
	PVC (Vinyl)
Negative -	Silicon
	Mylar
	Teflon

ESD Background (Friction Charging)

– Triboelectric charging areas.



Materials Background

- Initially there were many polymers available for contactors, Vespel, Delrin, Ultem, and Torlon 4203 to name a few were commonly used.
- Changes in handling and packaging technologies drove the need for materials with greater mechanical attributes.
  - Glass filled polymers provided the mechanical strength but were extremely insulative.
- ESD induced device and tester failures marked the transition from insulative polymers to a highly resistive polymer with a surface resistivity range of 10^{10} – 10^{12} ohm/square.

Materials Background

- Further increase in device sensitivity initiated the move to static dissipative polymers with a surface resistivity range of 10^6 – 10^9 ohms/cm^2 were desired.
- Dimensional stability was also a concern with device pitches of 1.0mm and below.
- Currently there is a short list of materials that meet both the mechanical and electrical requirements for contactors.
  - Ultem and PEEK based ESD materials are currently available.
  - Ceramic ESD materials are being evaluated.

Case History
Tester Board Damage

- Tester Damage attributed to an ESD event.
  - Experiments concluded that socket material interaction (Tribo-charging) with the device substrate material was the main contributor to charge build up on the device that led to the ESD damage.
  - The subsequent charge generated on the device was discharged to the tester through the VSS pins of the contactor when the device was socketed.
- Issue was resolved by changing the contactor material to a highly resistive material with a surface resistivity of (10^{10} – 10^{12}). This enabled any charge buildup on the device to be slowly discharged through the material.

Case History
Processor Platform Validation

- Device failure attributed to an ESD event
  - It was concluded that charge generated by devices rubbing against test sockets made of an insulative polymer material were the cause of the charge buildup.
  - The rapid discharge of the event was the cause for the ESD failures.
- In addition to changing the contactor material to a static dissipative material air ionizers also had to be installed in the modules to reduce the charge being generated during socketing.

ITRS Trends for ESD Sensitivity

Semiconductor Device ESD Sensitivity is projected to increase as technology progresses.

Industry must prepare for this!

Static Charge Limits for Test, Assembly, and Packaging

Year Technology Node	2000 180nm	2001 130nm	2002 115nm	2003 100nm	2004 90nm	2005 80nm	2006 70nm	2007 65nm
Maximum allowable static charge on devices	2.5-10nC (250-1000V)	1-2.5nC (100-250V)	1-2.5nC (100-250V)	1-2.5nC (100-250V)	1nC (100V)	1nC (100V)	0.5nC (50V)	0.5nC (50V)

Year Technology Node	2010 45nm	2013 32nm	2016 22nm
Maximum allowable static charge on devices	0.25nC (25V)	0.25nC (25V)	0.10nC (25V)

Material Challenges

- Minimize electrical charge buildup.
  - Static dissipative (10^5 – 10^9 Ohms/cm^2)
- Be dimensionally stable for pitches below 1.0mm
  - Low Coefficient of thermal expansion (CTE)
  - Low water absorption % (<.25 24hour percentage)

Material Challenges

- Be suitable for machining and molding manufacturing processes.
  - Must maintain it's dissipative properties after manufacturing. Strive for homogeneous performance.
- Exhibit the equal or better strength and wear characteristics of current materials.

Conclusion

- **ESD is becoming a larger problem as we make our devices smaller and faster. Polymer selection will play a vital role as to whether or not we are successful in reducing ESD related device failures.**
- **Need assistance from polymer suppliers to develop and provide COST EFFECTIVE ESD friendly polymers that meet the needs of the industry.**

Dimensional Stability and High Frequency Properties of Polymeric Materials for Machined Test Sockets

Paul Kane P.E.

Joy Bloom Ph.D

DuPont Vespel® Parts and Shapes

BURN-IN & TEST SOCKET WORKSHOP

Purpose

Answer persistent questions on:

- dimensional stability with humidity of polymers used for machined test sockets
- electrical properties at high frequencies after humidity exposure
- mechanical performance under load and thermal expansion properties

This data should be useful in modeling test socket performance.

Plaque Materials Evaluated

- Torlon® 5530: 30% glass reinforced, compression molded PAI
- Torlon® 4203: extruded, unfilled PAI
- Vespel® SP-1: unfilled PI
- Vespel® TP-7950: unfilled, non-hygroscopic LCP (developmental)
- Vespel® SCP-5000 :low hygroscopic, higher modulus PI
- Vespel® CR-4638EX: electrostatic dissipative PAEK

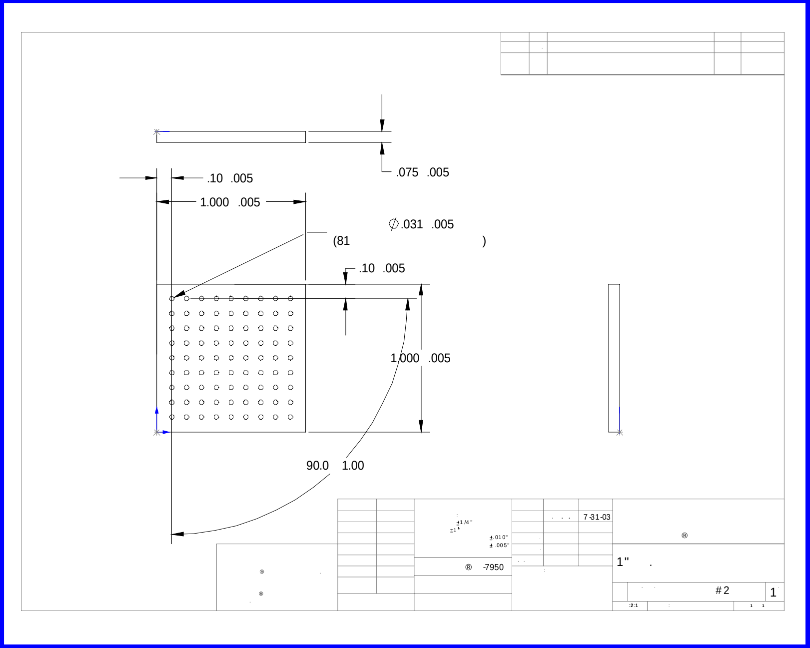
Data Generated

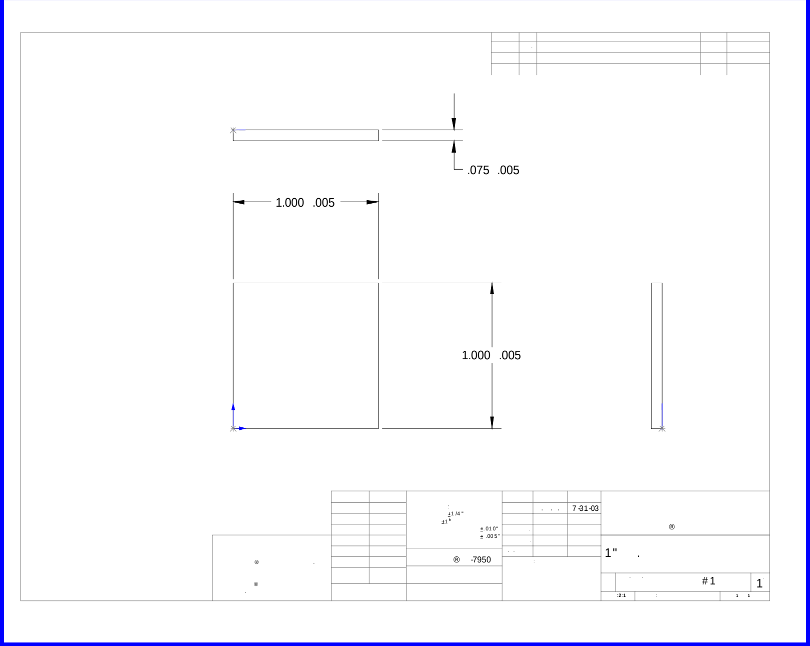
- Dimensional and weight(%) change with humidity exposure for thin samples with/without holes
- Stiffness versus temperature
- Creep
- Compressive Strength
- Dk and Df at high frequency with humidity exposure
- Thermal Expansion

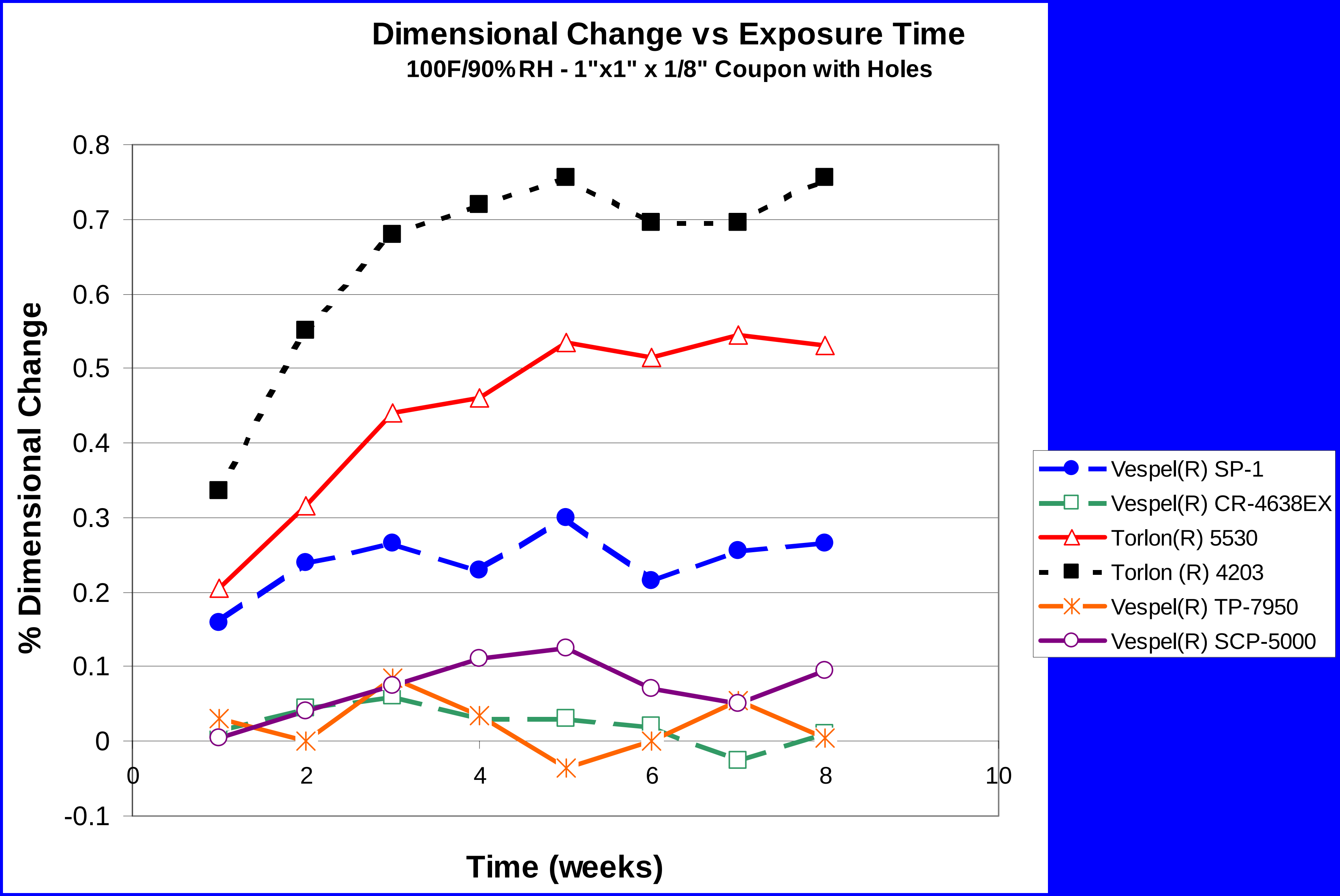
Humidity Exposure Testing

- Materials
  - machined from plaques and used “as received”
    - with “holes” size
    - no holes
    - not annealed/dried before testing
  - sample’s edge surface area:
    - .3 in^2 for “no hole”
    - .892 in^2 for “holes”
- Methodology
  - placed in constant 100F°/90% humidity chamber
  - measured weekly
  - dimension delta is “average” of length/width of 1 inch square

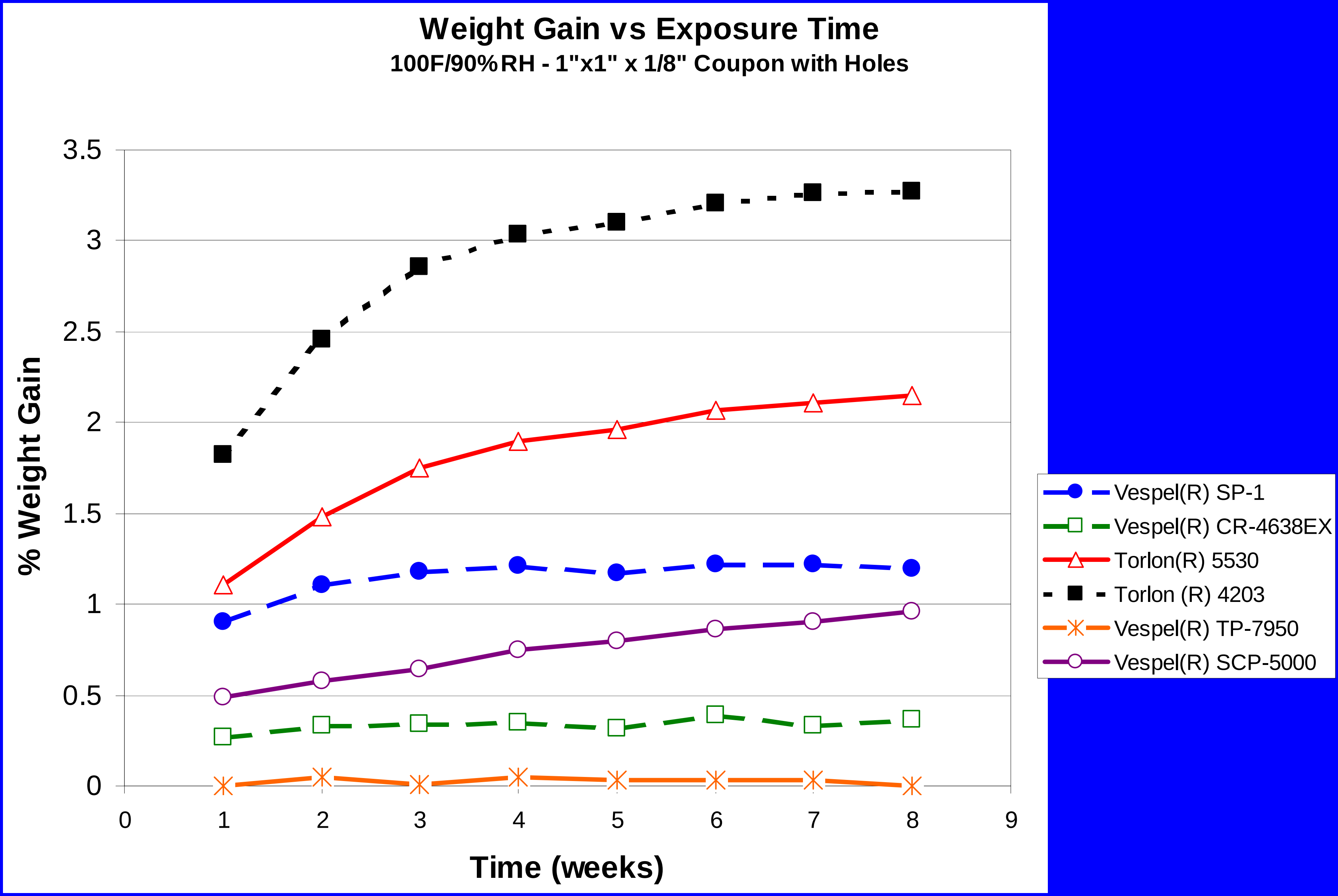
Moisture Exposure Samples
1 inch square, .075 inch thick
holes vs. no holes



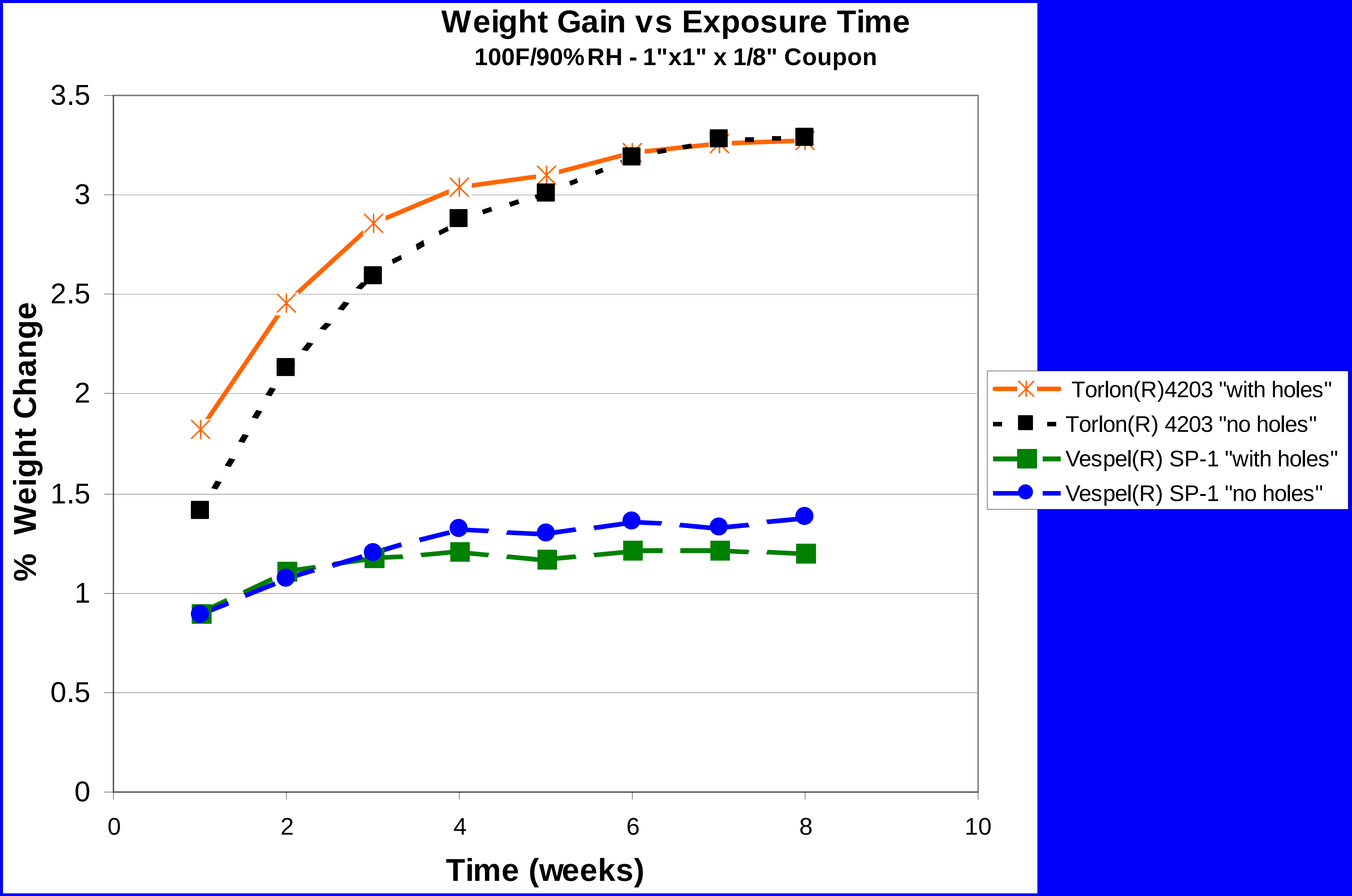




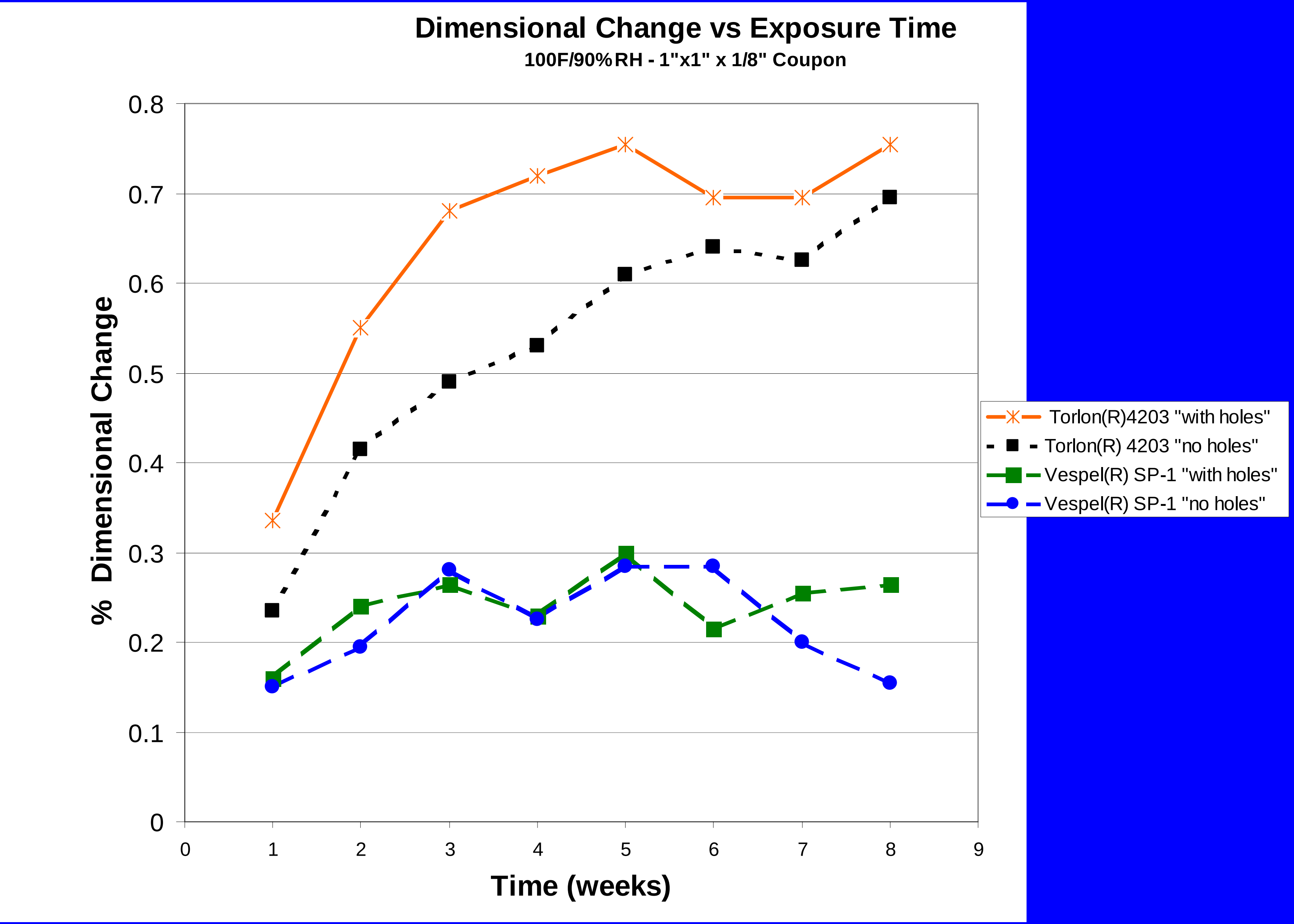
Dimensional Change vs Exposure Time
100F/90%RH - 1"x1" x 1/8" Coupon with Holes
% Dimensional Change
Time (weeks)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
0
2
4
6
8
10
Vespel(R) SP-1
Vespel(R) CR-4638EX
Torlon(R) 5530
Torlon (R) 4203
Vespel(R) TP-7950
Vespel(R) SCP-5000



Weight Gain vs Exposure Time
100F/90%RH - 1"x1" x 1/8" Coupon with Holes
% Weight Gain
3.5
3
2.5
2
1.5
1
0.5
0
0
1
2
3
4
5
6
7
8
9
Time (weeks)
Vespel(R) SP-1
Vespel(R) CR-4638EX
Torlon(R) 5530
Torlon (R) 4203
Vespel(R) TP-7950
Vespel(R) SCP-5000



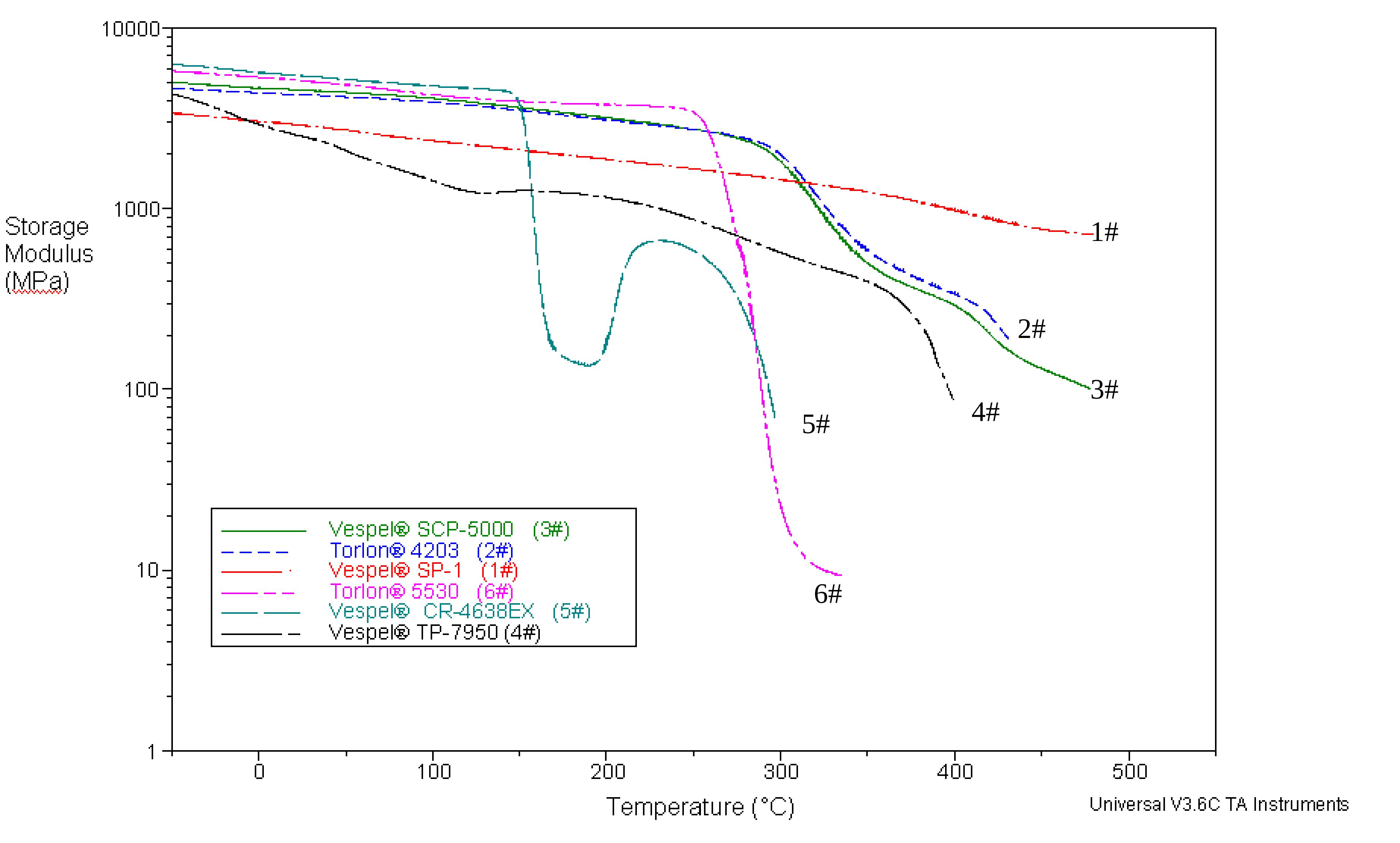
Weight Gain vs Exposure Time
100F/90%RH - 1"x1" x 1/8" Coupon
% Weight Change
3.5
3
2.5
2
1.5
1
0.5
0
0
2
4
6
8
10
Time (weeks)
Torlon(R)4203 "with holes"
Torlon(R) 4203 "no holes"
Vespel(R) SP-1 "with holes"
Vespel(R) SP-1 "no holes"


Dimensional Change vs Exposure Time
100F/90% RH - 1"x1" x 1/8" Coupon
% Dimensional Change
Time (weeks)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0
1
2
3
4
5
6
7
8
9
Torlon(R)4203 "with holes"
Torlon(R) 4203 "no holes"
Vespel(R) SP-1 "with holes"
Vespel(R) SP-1 "no holes"

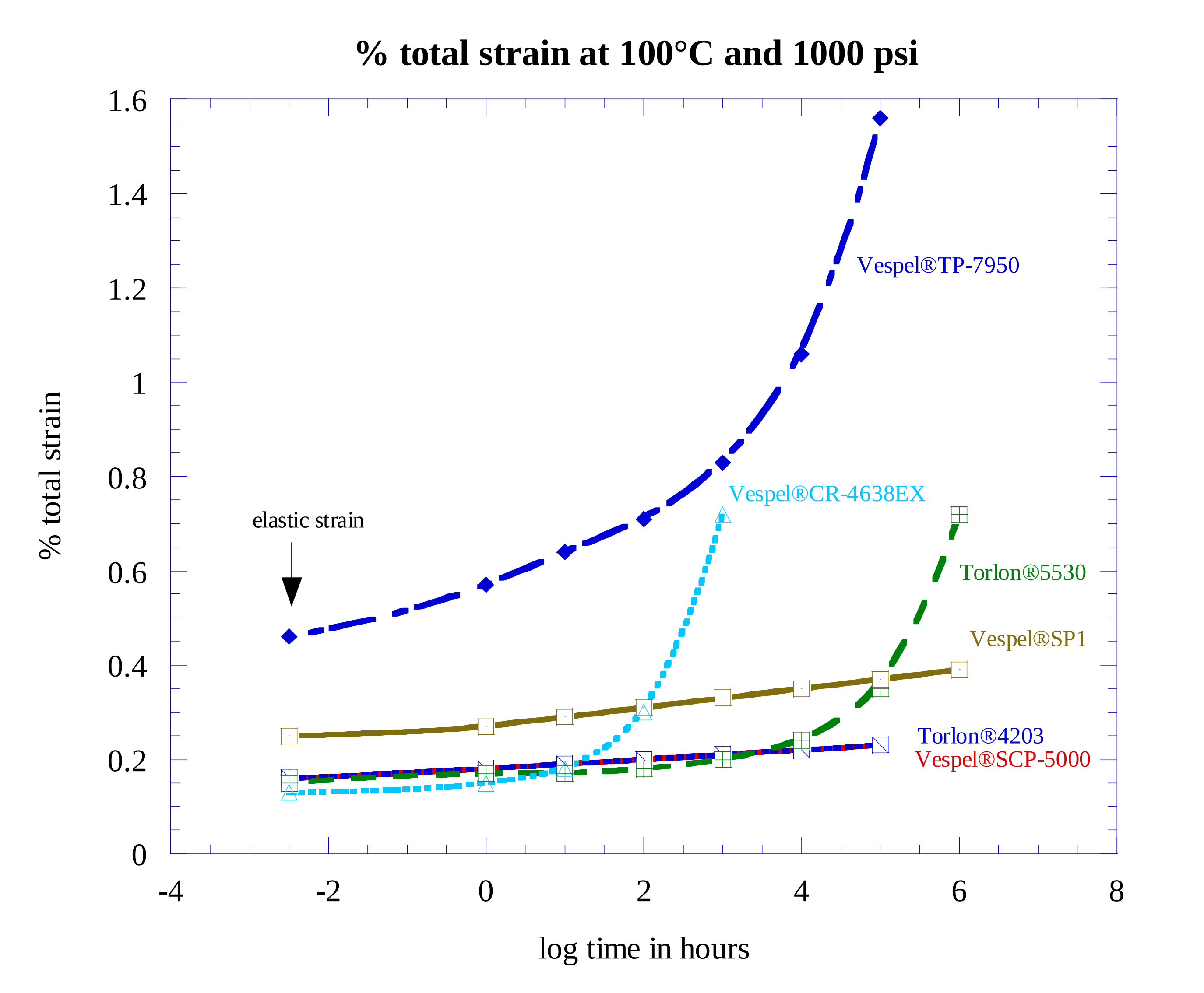
Observations

- PI lower hygroscopic growth than PAI
- Vespel® SCP-5000 sample, .001 in/in(mm/mm) growth after 8 weeks
- Rate of hygroscopic growth increases with holes
- LCP has essentially no hygroscopic growth

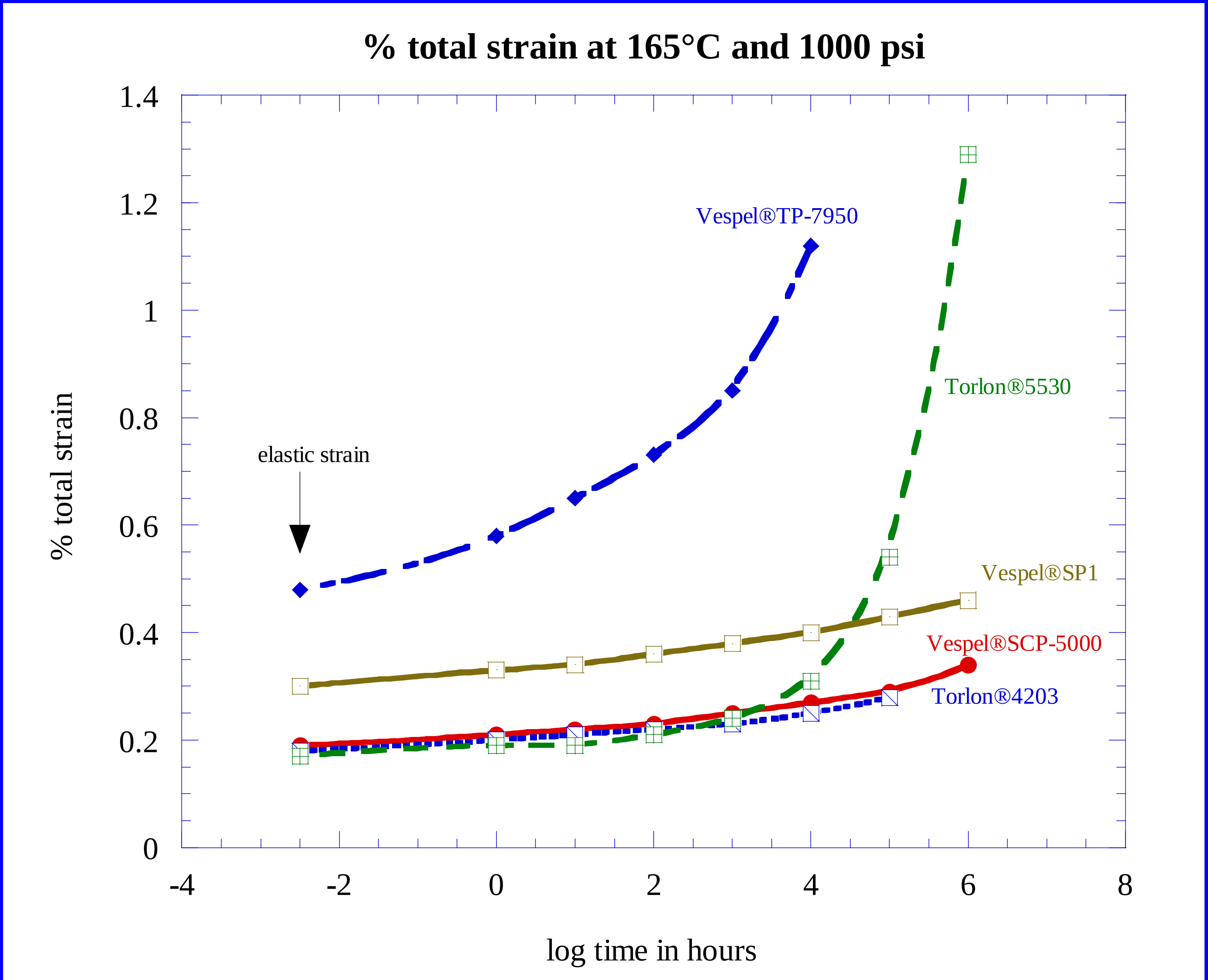
Modulus Vs. Temperature



Accelerated Creep @1000 psi/100C° Tensile Load



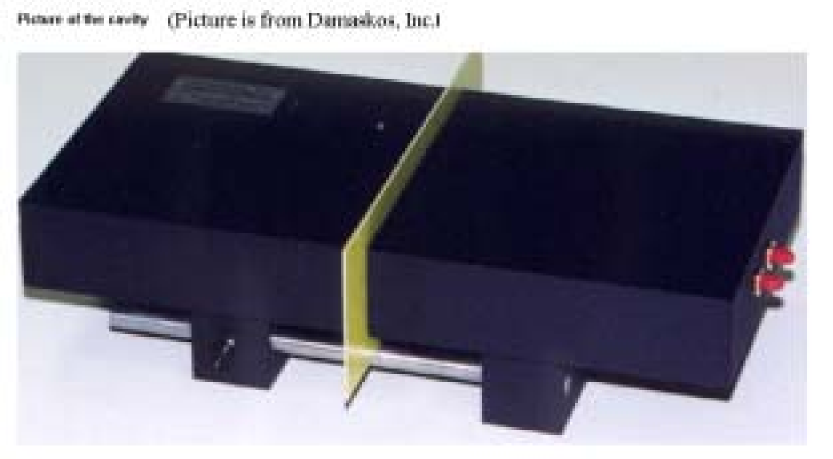
Accelerated Creep @1000 psi/165C° Tensile Load



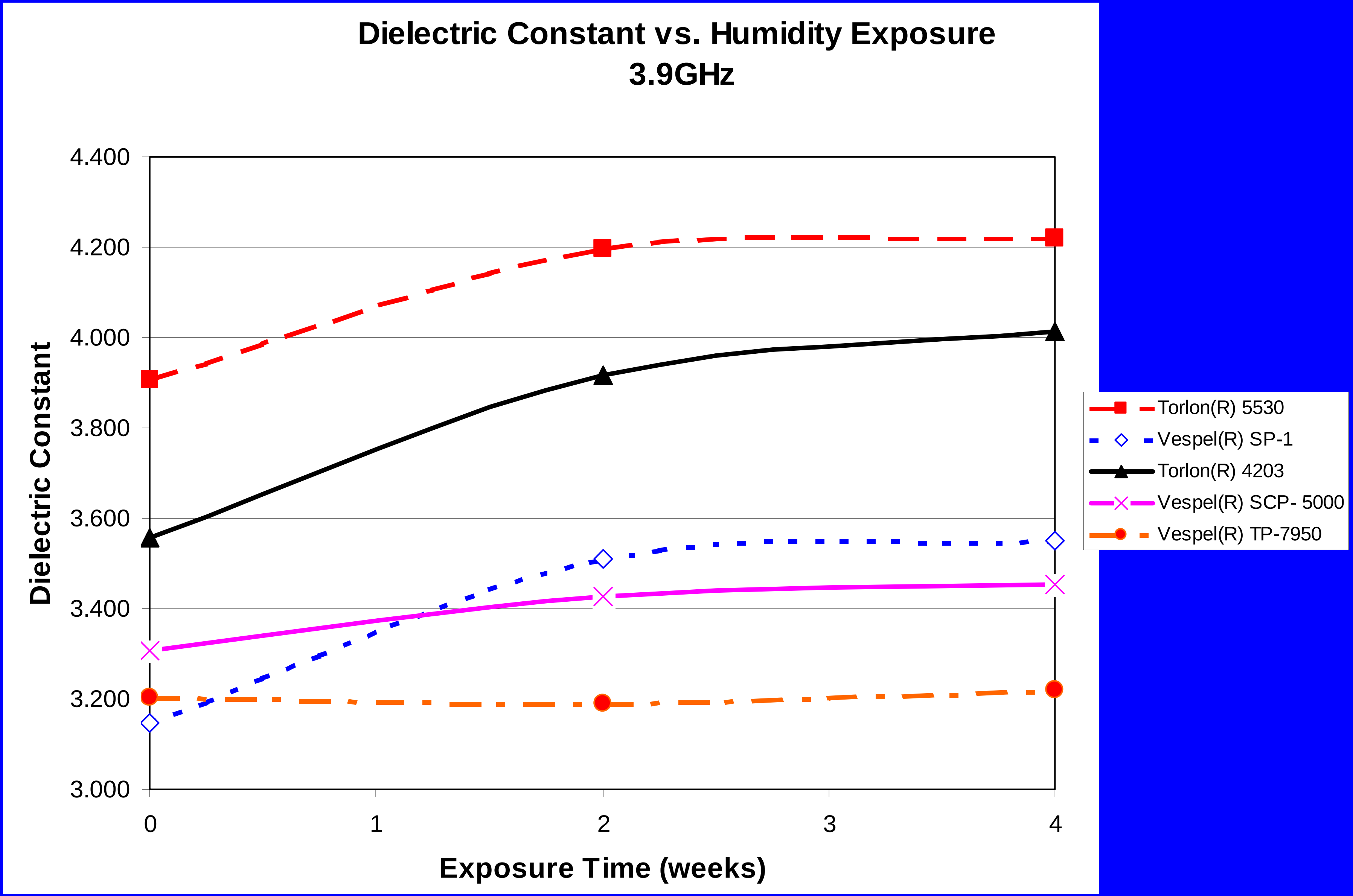
Observations

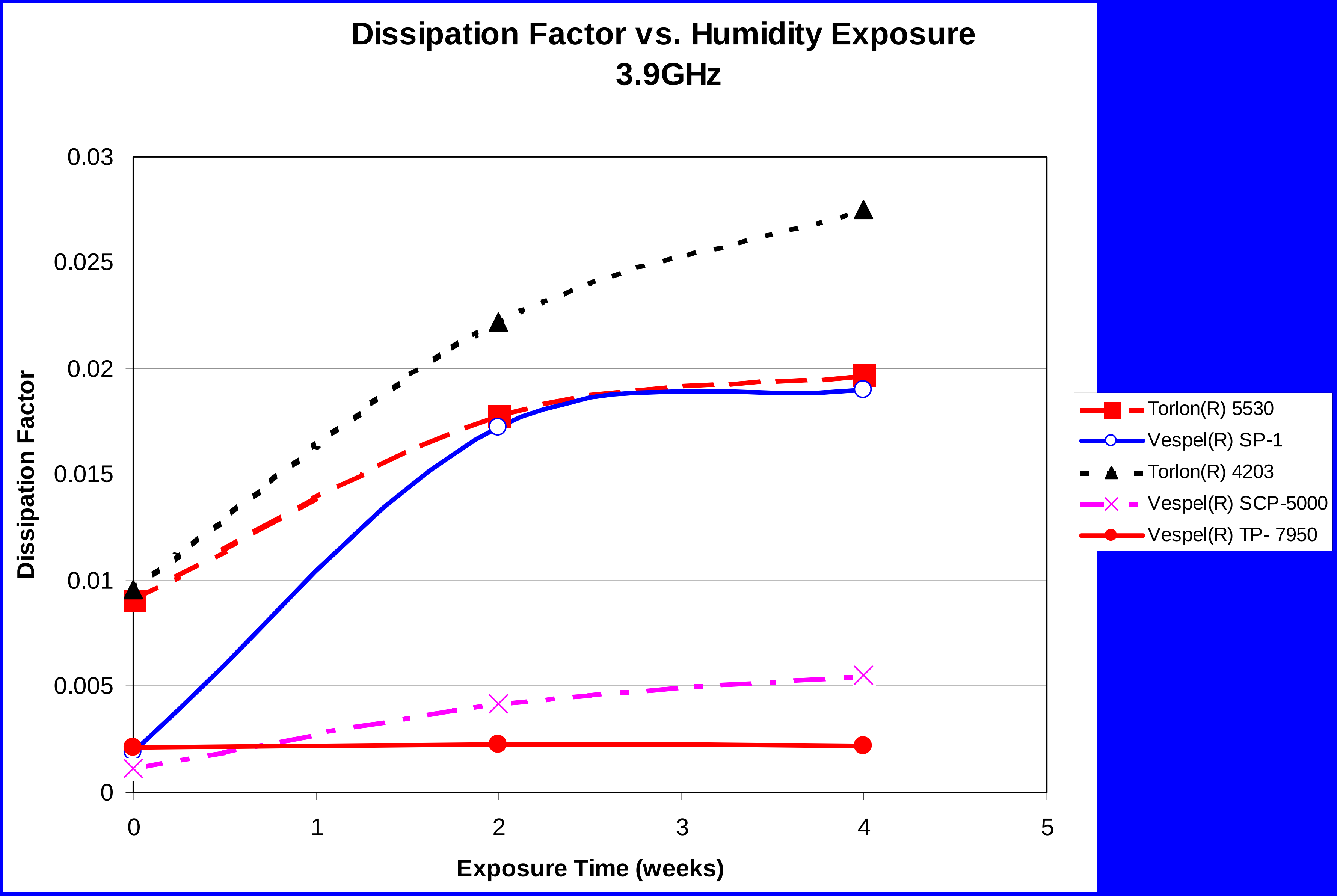
- Unfilled Vespel® SCP-5000 has equal stiffness and creep at 165C° to Torlon® 4203 and Torlon® 5530
- Vespel® CR-4638EX (ESD PAEK) limited to lower temperatures (<130C°)
- Torlon® 4203 and Torlon® 5530 have higher stiffness and lower creep at 165C° compared to Vespel® SP-1

Humidity Exposure
Test Method for Dk and Df



- test planar samples up to 4.6 GHz
- samples tested were .060 inch thick
- dried before testing
- exposed at 90°F/90% RH
- Vespel® CR-4638EX not tested


Dielectric Constant vs. Humidity Exposure
3.9GHz
Dielectric Constant
4.400
4.200
4.000
3.800
3.600
3.400
3.200
3.000
0
1
2
3
4
Exposure Time (weeks)
Torlon(R) 5530
Vespel(R) SP-1
Torlon(R) 4203
Vespel(R) SCP- 5000
Vespel(R) TP-7950


Dissipation Factor vs. Humidity Exposure
3.9GHz
Dissipation Factor
0.03
0.025
0.02
0.015
0.01
0.005
0
0
1
2
3
4
5
Exposure Time (weeks)
Torlon(R) 5530
Vespel(R) SP-1
Torlon(R) 4203
Vespel(R) SCP-5000
Vespel(R) TP- 7950

Observations

- Dielectric constant and dissipation factor increases with humidity
- Lower hygroscopic materials have smaller increase in Dk and Df with humidity exposure
- Vespel® TP-7950 has minimal/insignificant change after 4 weeks exposure

Thermal Expansion

	Z Direction CTE (ppm) 25-160C°	Z Direction CTE (ppm) 160-200C°	XY Plane CTE (ppm) 25-150C°	XY Plane CTE(ppm) 160-200C°
Vespel® SCP-5000	182	197	62	73
Torlon® 4203	37	52	39	54
Torlon® 5530	32	43	35	47
Vespel® SP-1	48	62	48	63
Vespel® CR-4638EX	40	122	8.3	17
Vespel® TP-7950	190	201	62	79

- "XY" -planar direction
- "Z"-thickness/ forming direction of sample

Summary

- Significant differences in hygroscopic absorption between PI and PAI
- Unfilled PI grade available with good creep and stiffness at high temperature
- LCP offers potential as “non-hygroscopic” test socket material

PARICON®

Paricon Technologies Corporation

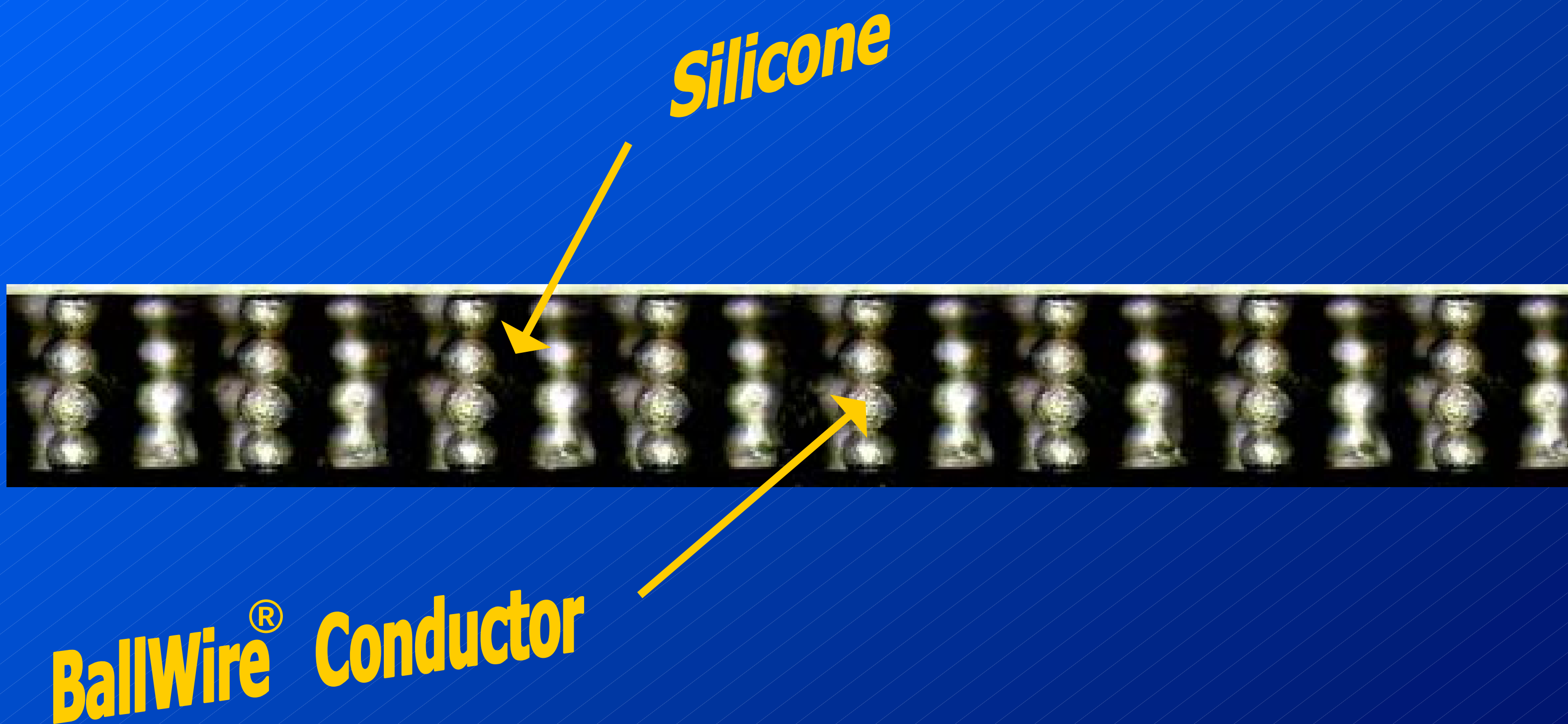
Visco Elastic Behavior of Anisotropic Conductive Polymers

Roger Weiss, PhD
Chris Cornell
Glenn Amber

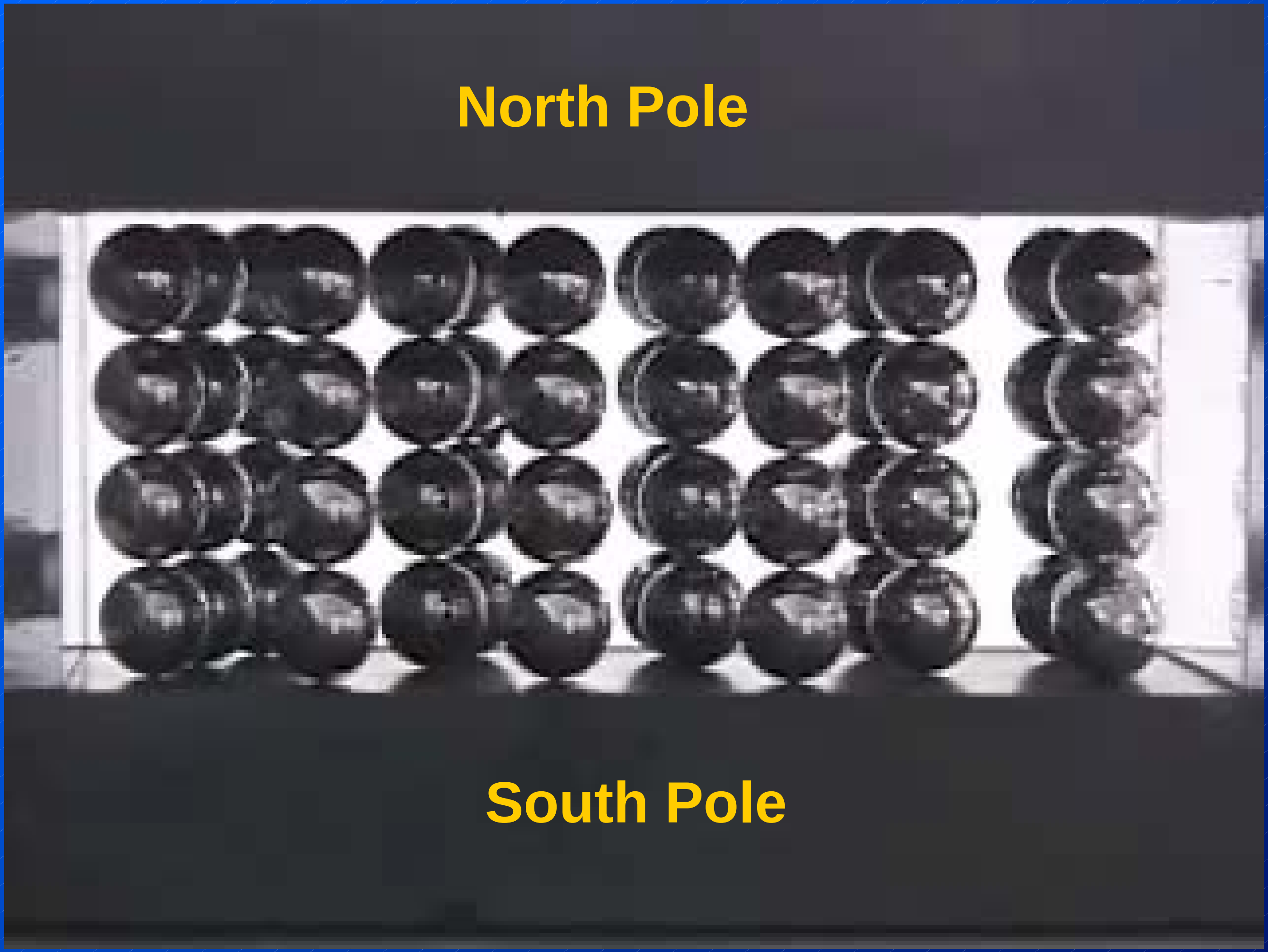
Focus

There are Many Connector Products which Utilize Elastomeric Materials in a variety of Ways. The Data Presented here is Based on the Capability of the Elastomeric Materials Produced by Paricon Technologies Corp. .

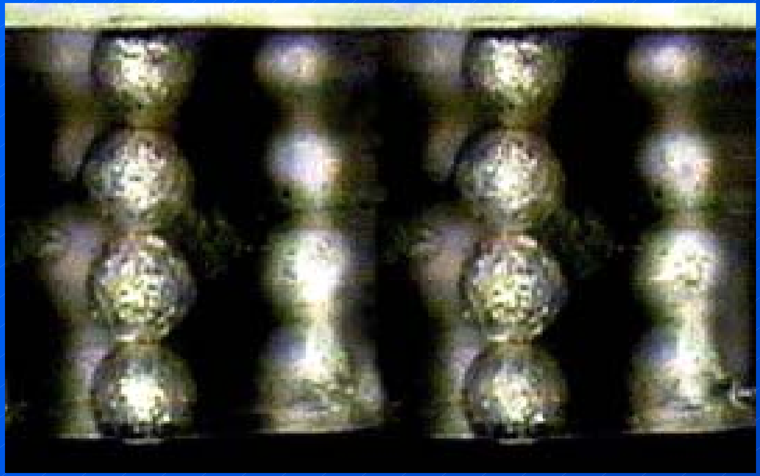
PariPoser® Interconnection Fabric

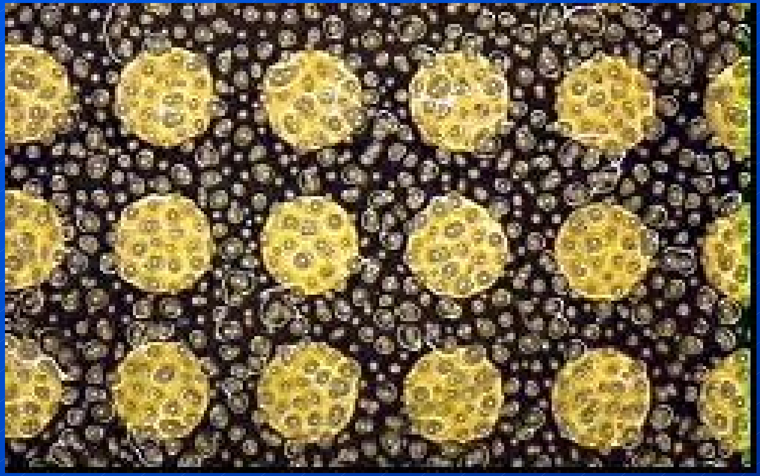


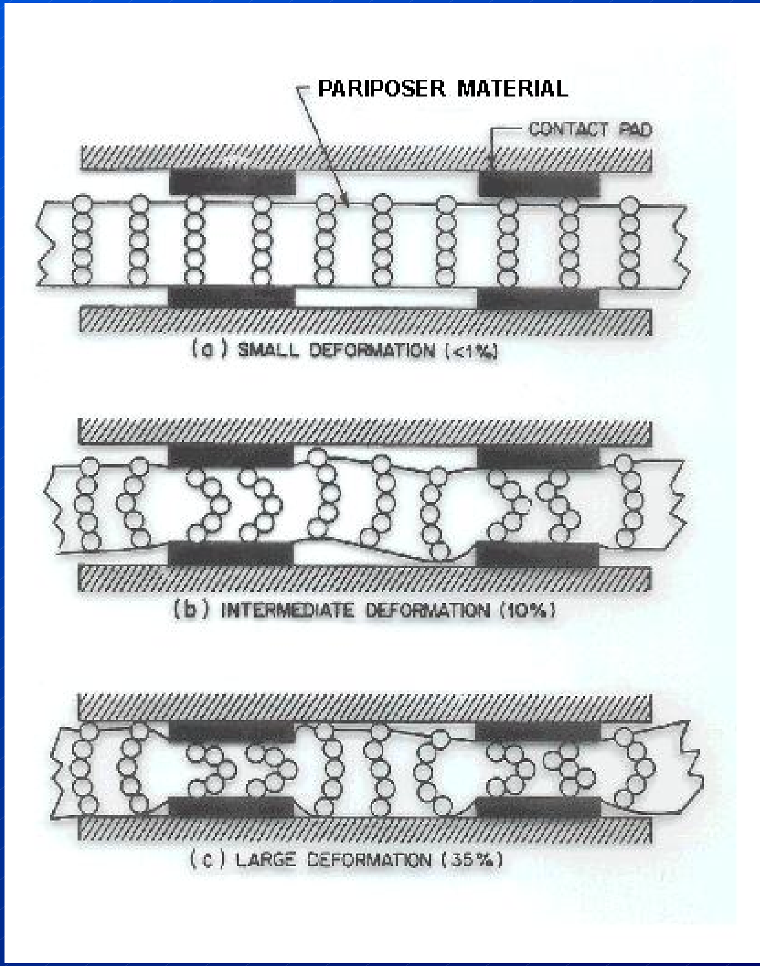
Core Technology



PariPoser® Interconnect

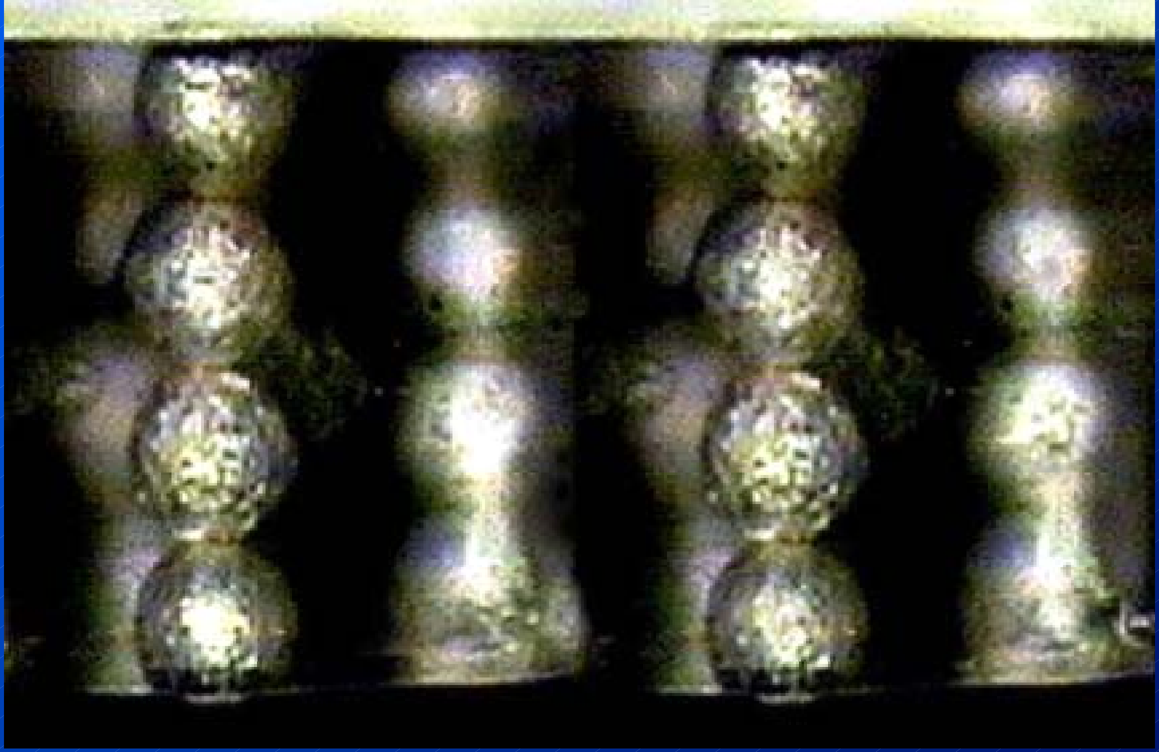






Properties of Elastomeric Conductors

Elastomer Maintains BallWire ® Column



Properties of Elastomeric Conductors

Elastomer Provides Restoring Force Against BallWire ® Column

- ***Test Probe Spring***
- ***Surface Mount Formed Contact***

Properties of Elastomeric Conductors

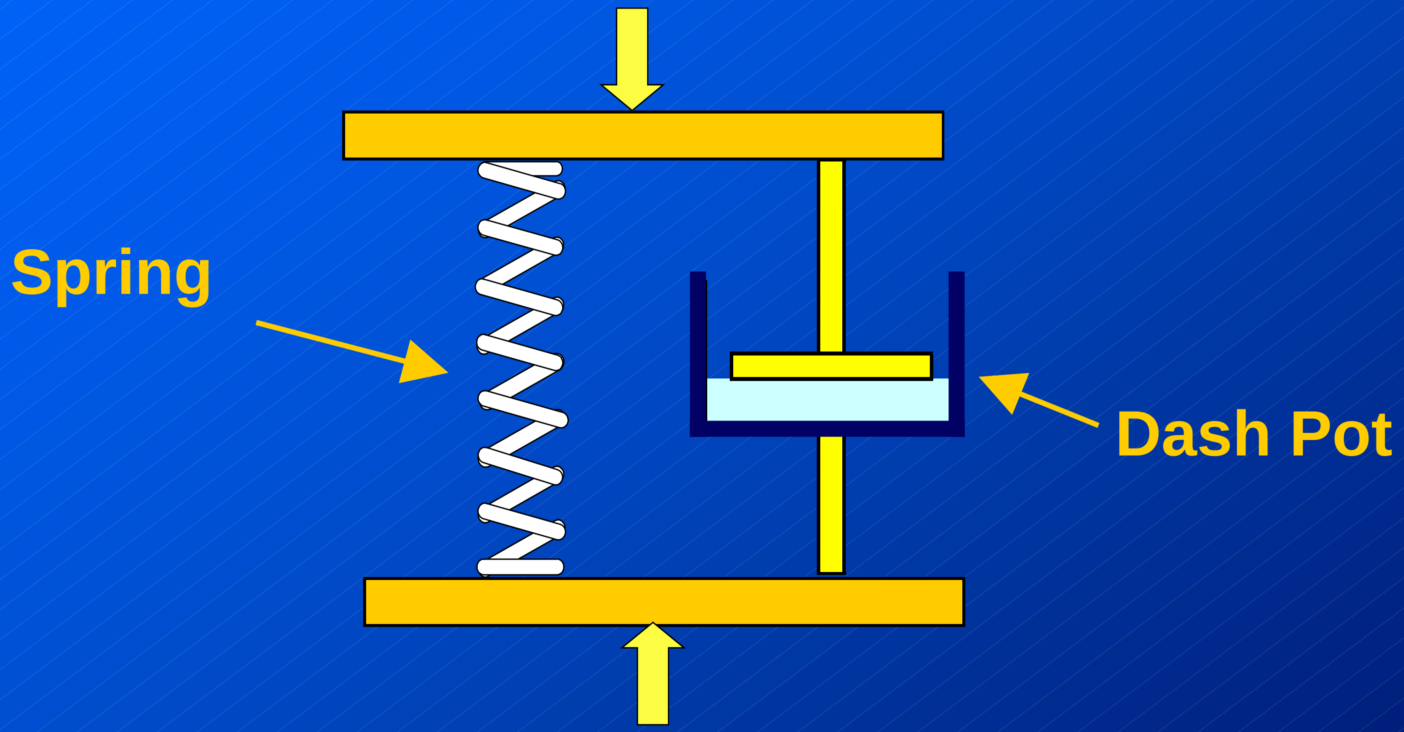
- ***Incompressible Fluid***
- ***Both Viscous and Elastic***

<u>Viscous</u> ⟷ <u>Elastic</u>

Putty ——— *Super Putty* —— *Super Ball*

Understanding of Properties Critical to Performance

Simple Visco – Elastic Model



Observations on Elastomeric Conductors

For a Given System, The Resistance Follows the Visco-Elastic Motion of the Elastomer

Rate of Resistance Decrease is Function of Pressure, Temperature and Time

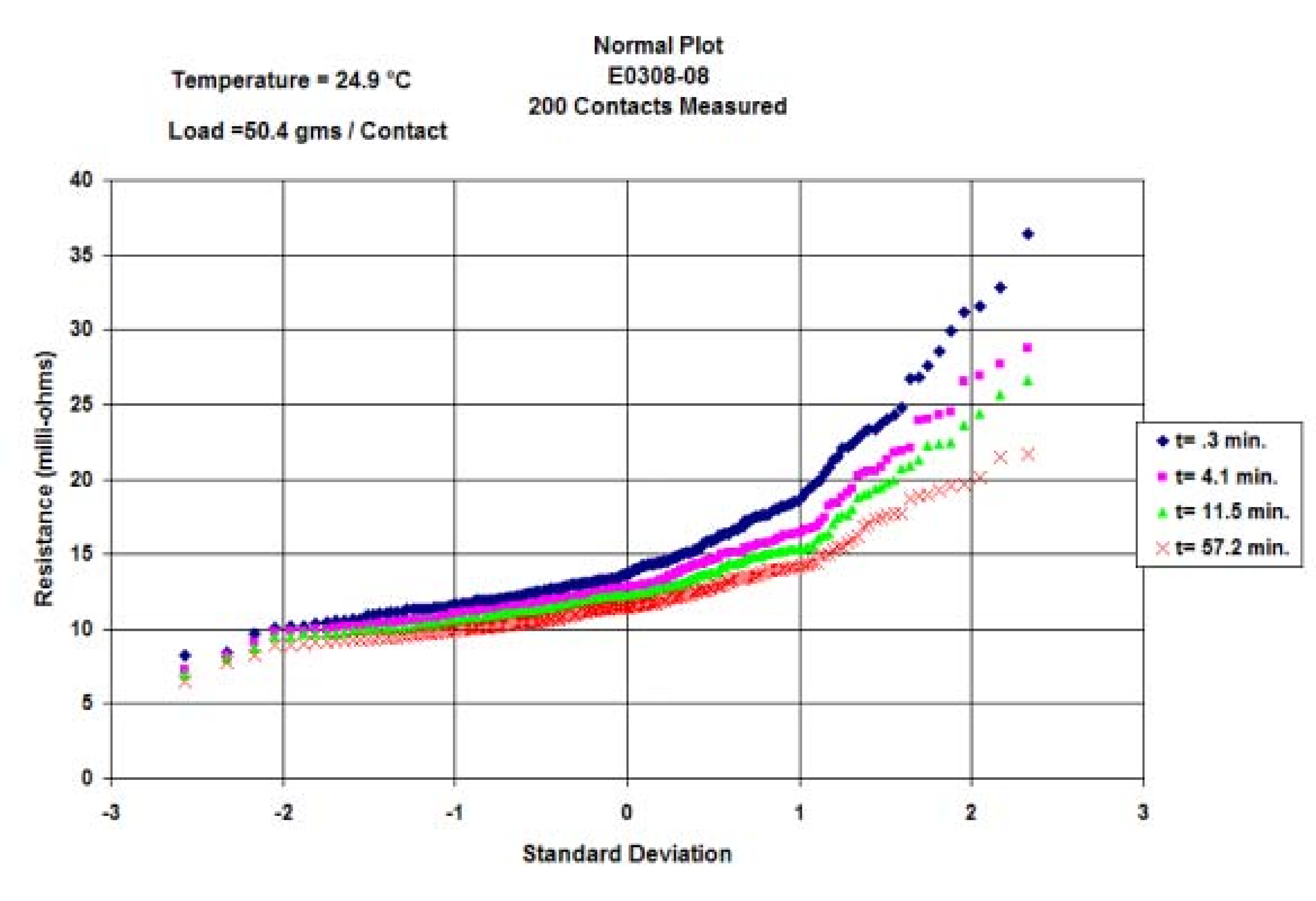
Ultimate Resistance Controlled by Other Factors

Resistance vs. Time vs. Load vs. Temperature

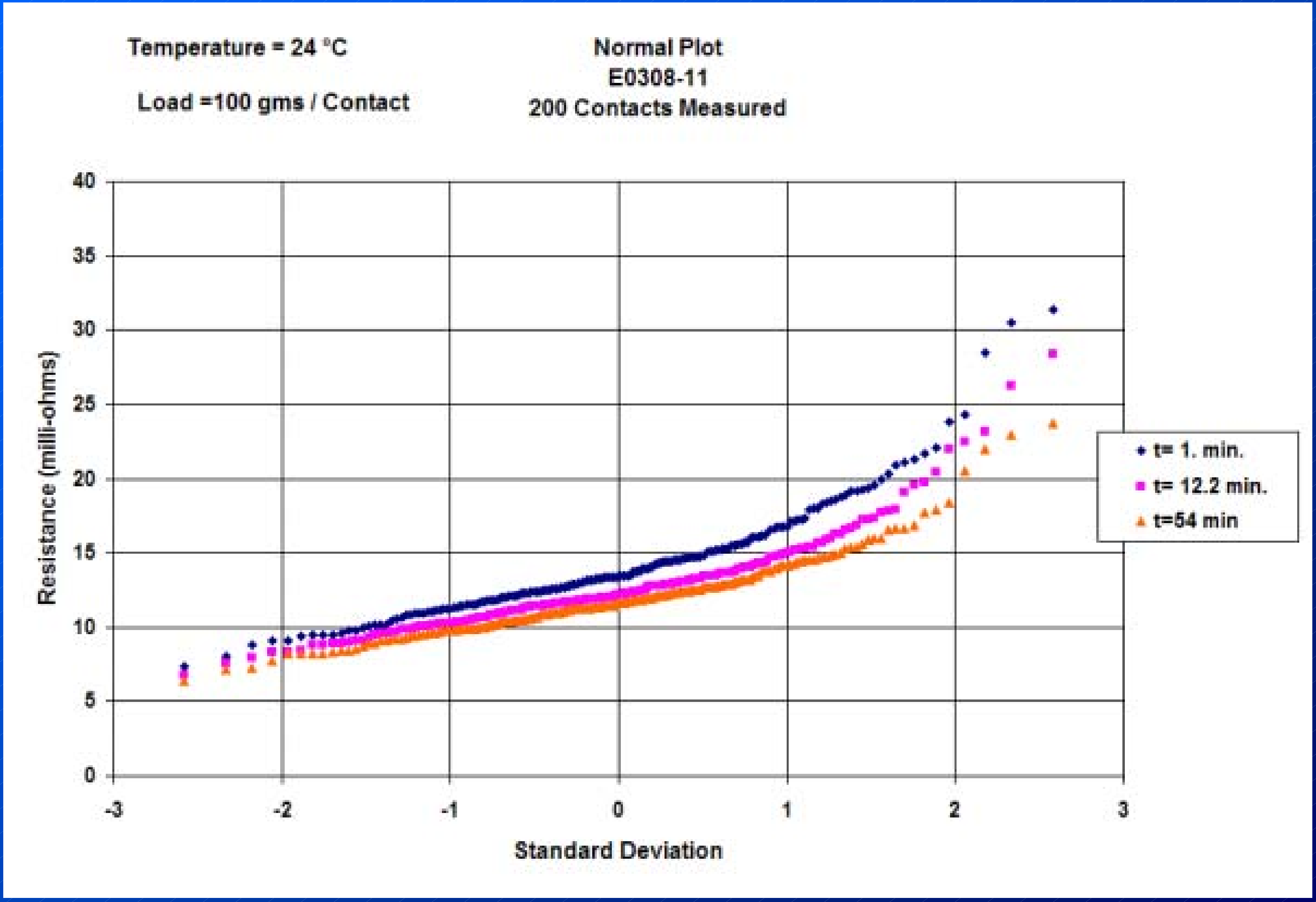
The Resistance of 200 Individual Contacts were Monitored as a Function of Time.

- ***Load: 50 and 100 Grams per Contact***
- ***Temperature: 25 and 50 °C***

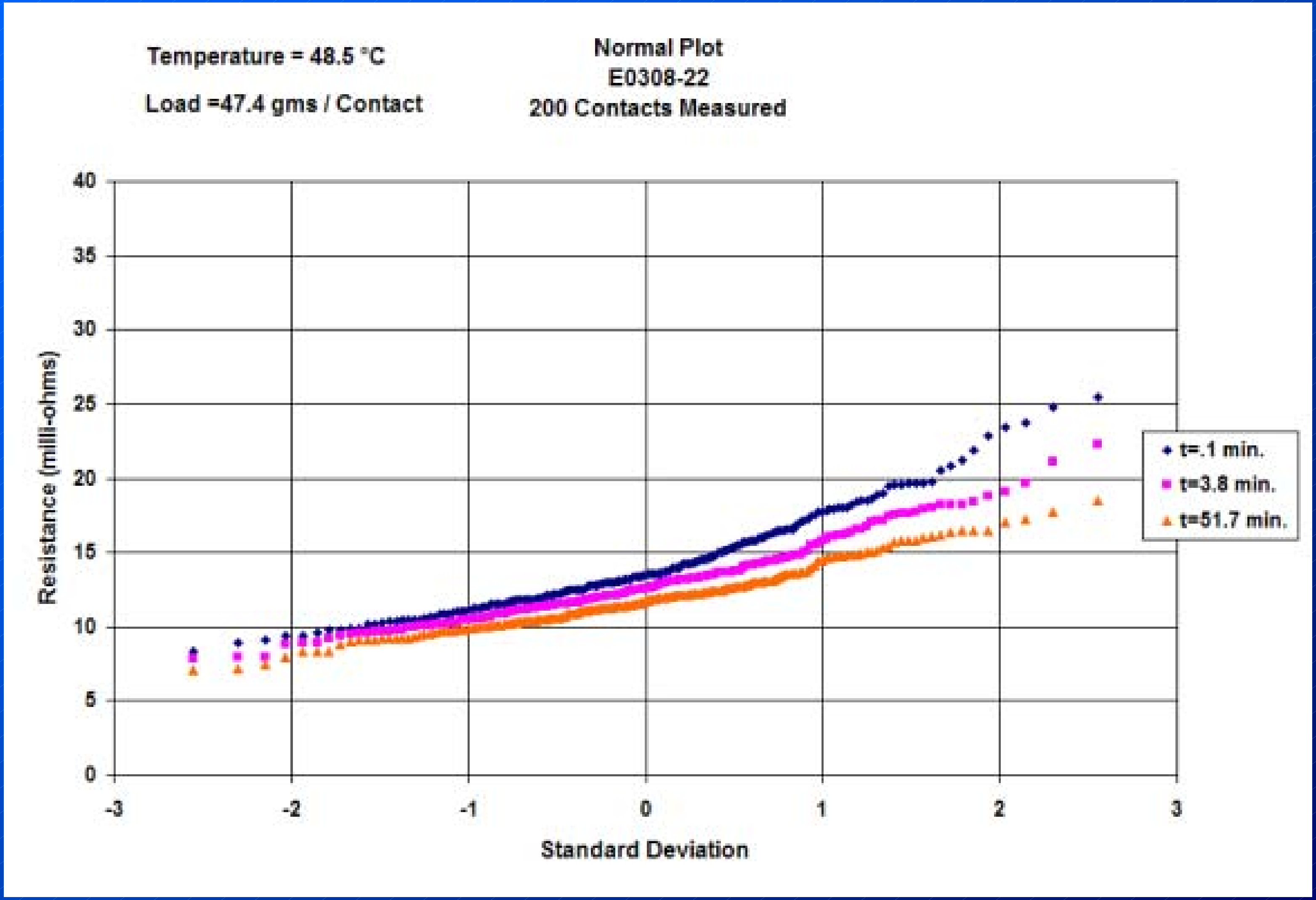
Resistance vs. Time vs. Load vs. Temperature



Resistance vs. Time vs. Load vs. Temperature



Resistance vs. Time vs. Load vs. Temperature

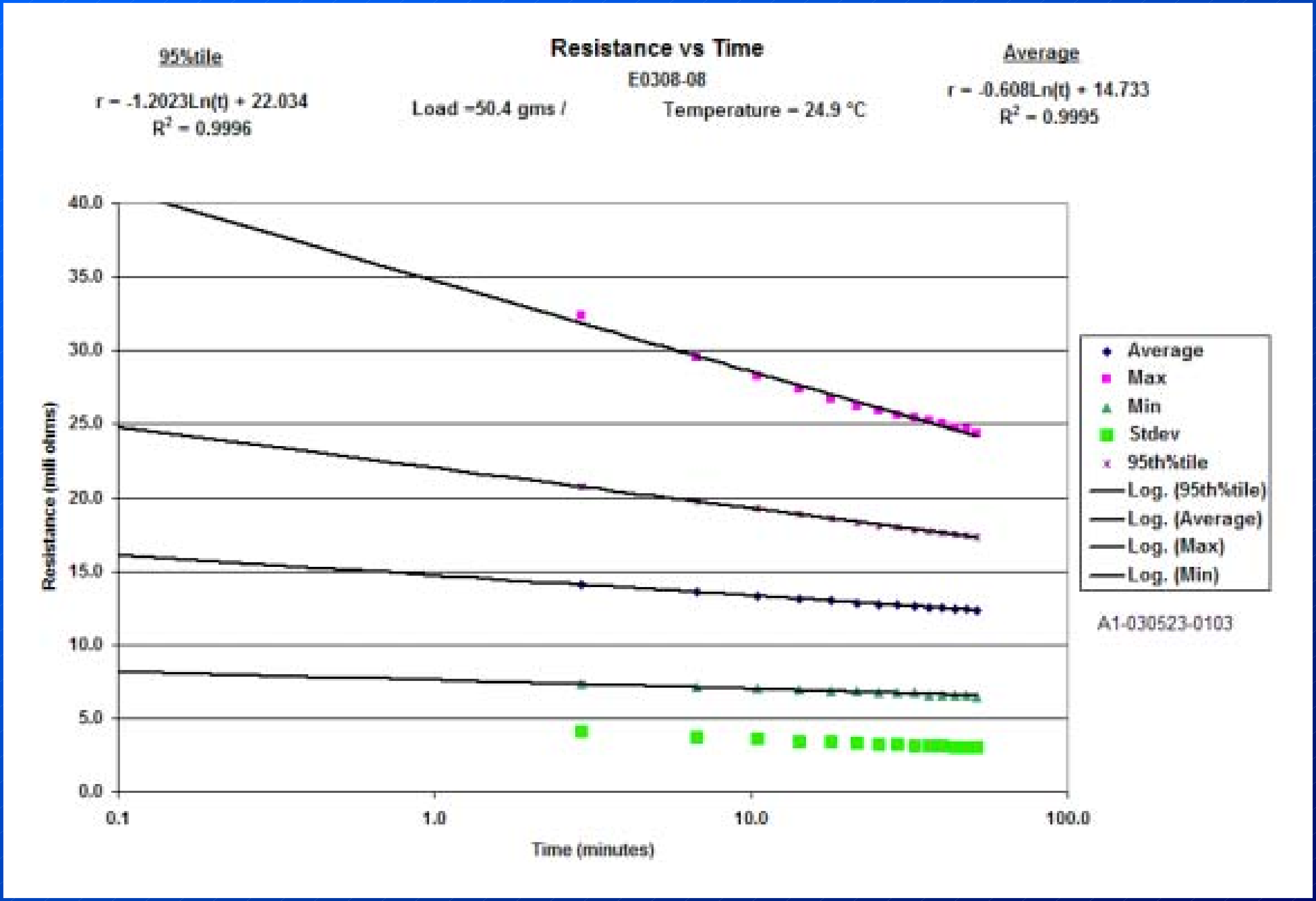


Resistance vs. Time vs. Load vs. Temperature

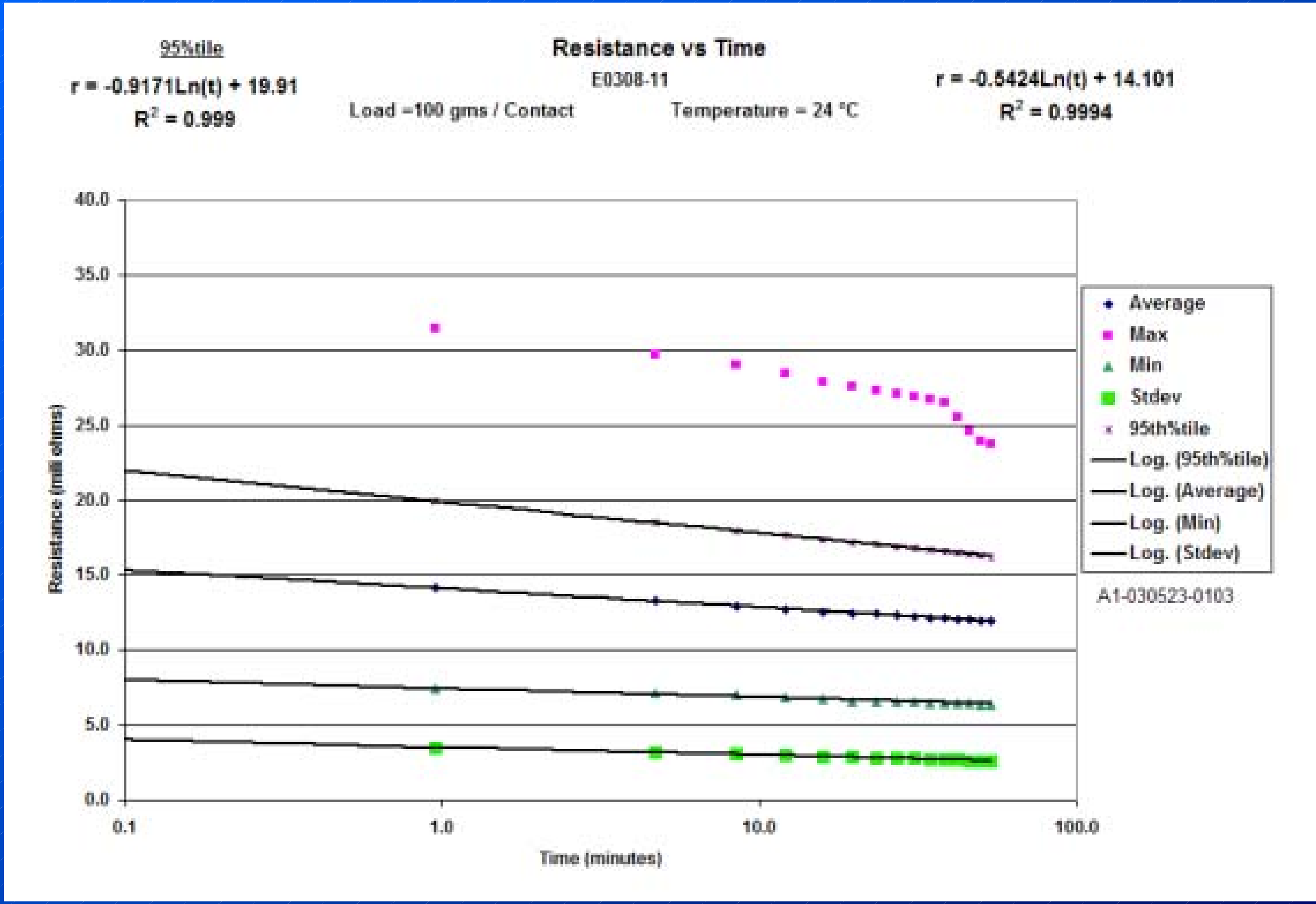
Over Time of Measurement, Data is Well Described by Resistance vs. ln(time) .

- ***Visco-Elastic Model needs to be Developed***
- ***Simple Dashpot and Spring Model Does Not Seem to Apply***

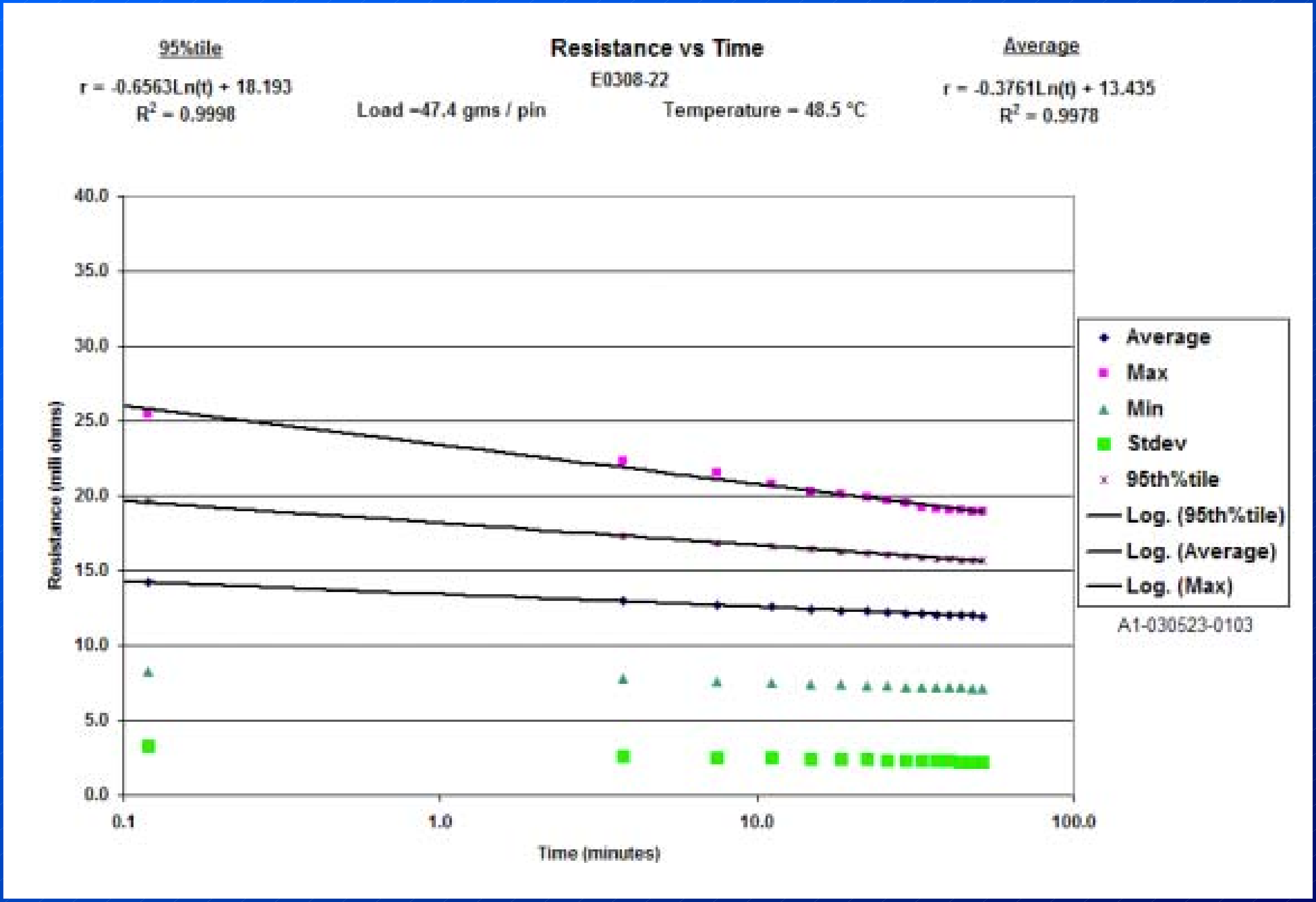
Resistance vs. Time vs. Load vs. Temperature



Resistance vs. Time vs. Load vs. Temperature



Resistance vs. Time vs. Load vs. Temperature



Resistance vs. Time vs. Load vs. Temperature

For this Behavior to Happen, Every Contact Must Have Resistance Behavior of Form: .

$$R = a(P,T)\ \ln(t) + b(P,T)$$

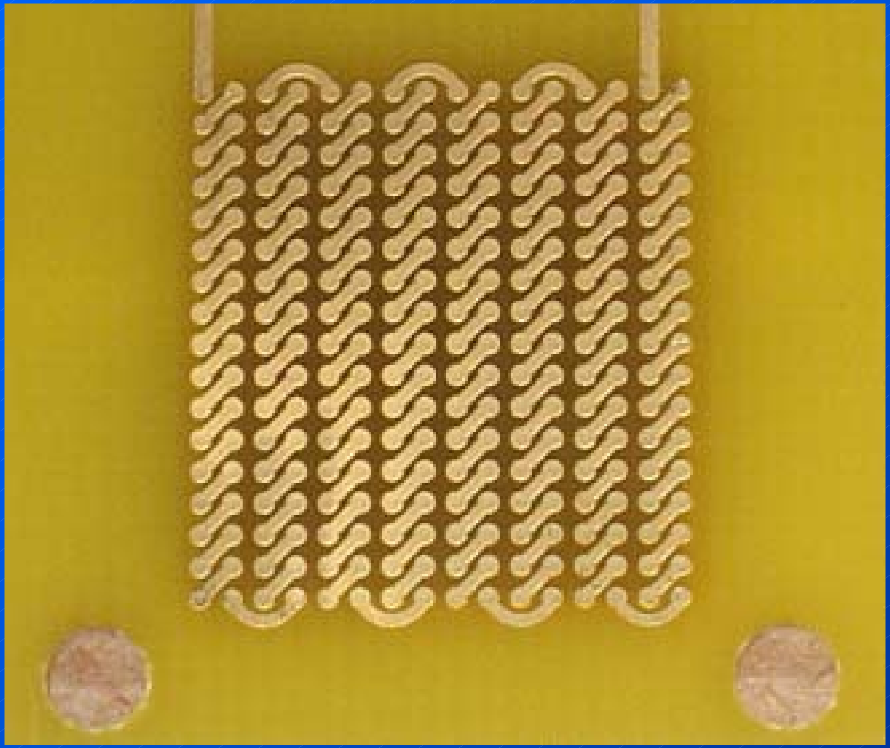
R – Resistance

t- Time

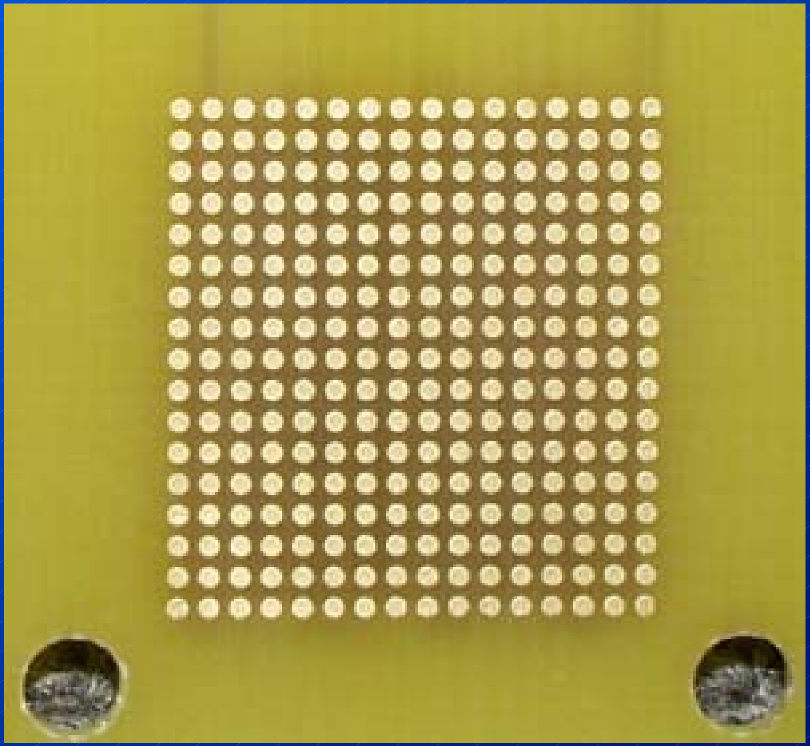
P – Pressure

T - Temperature

Response Time Test Boards

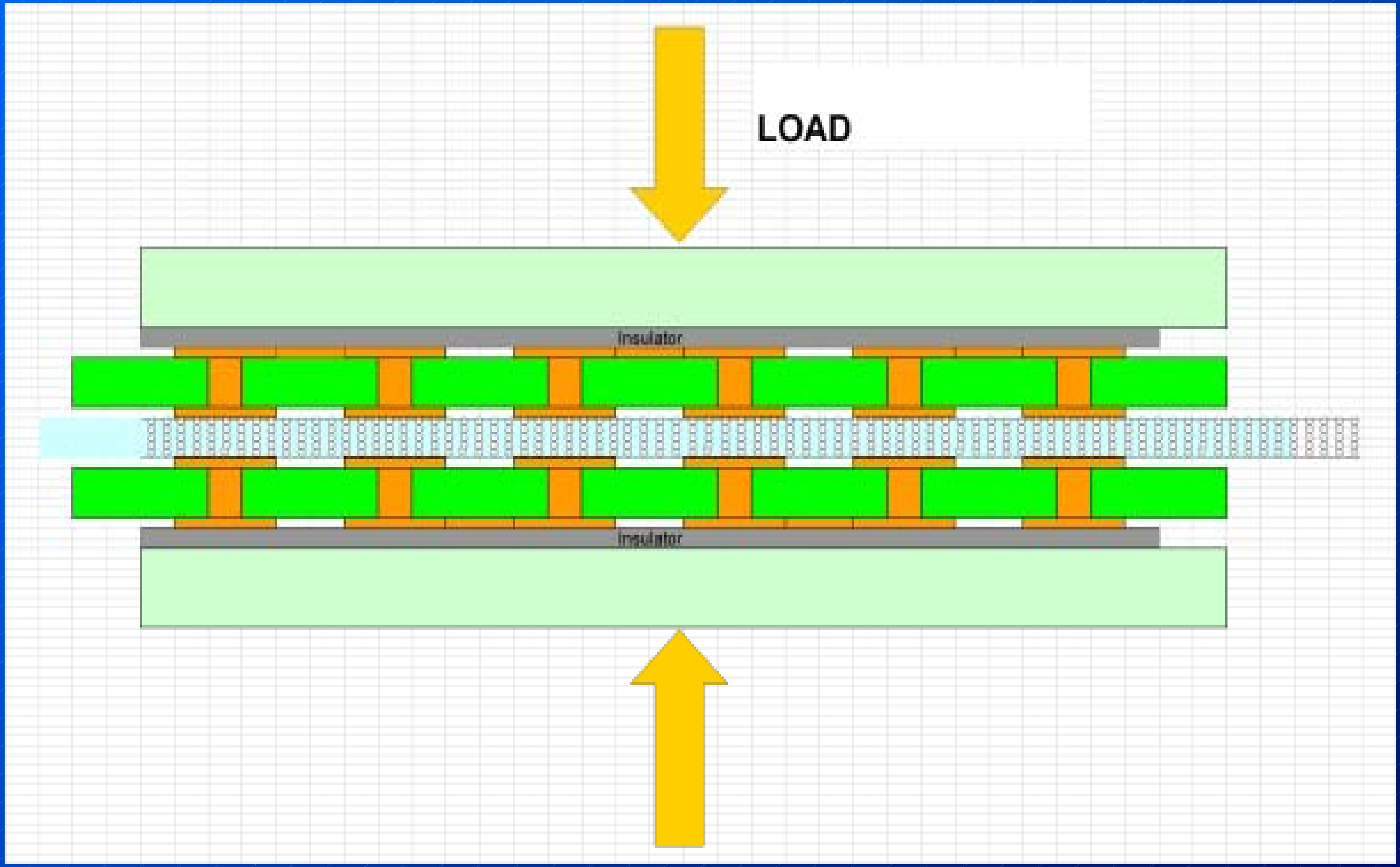


Bus Side

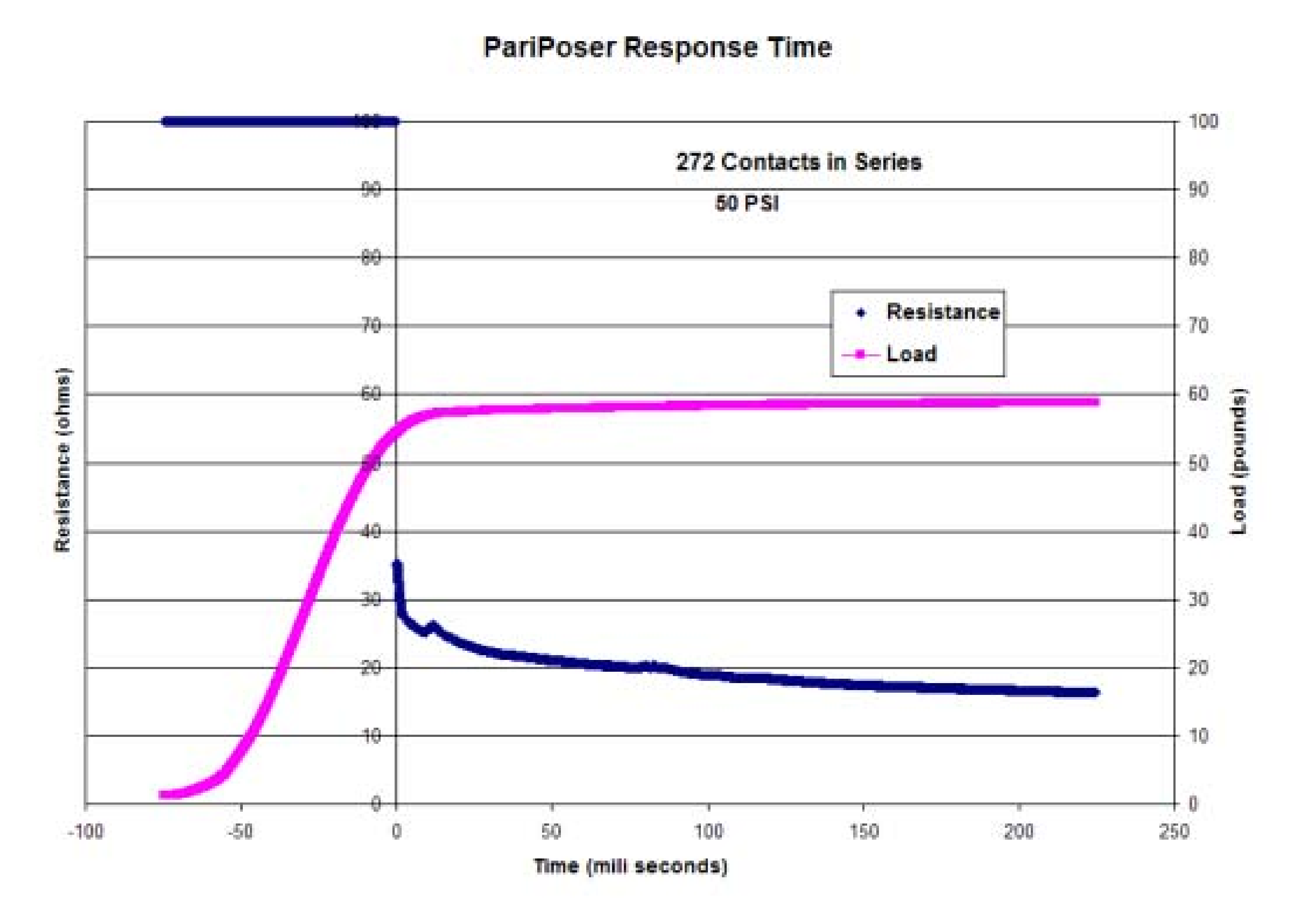


Contact Side

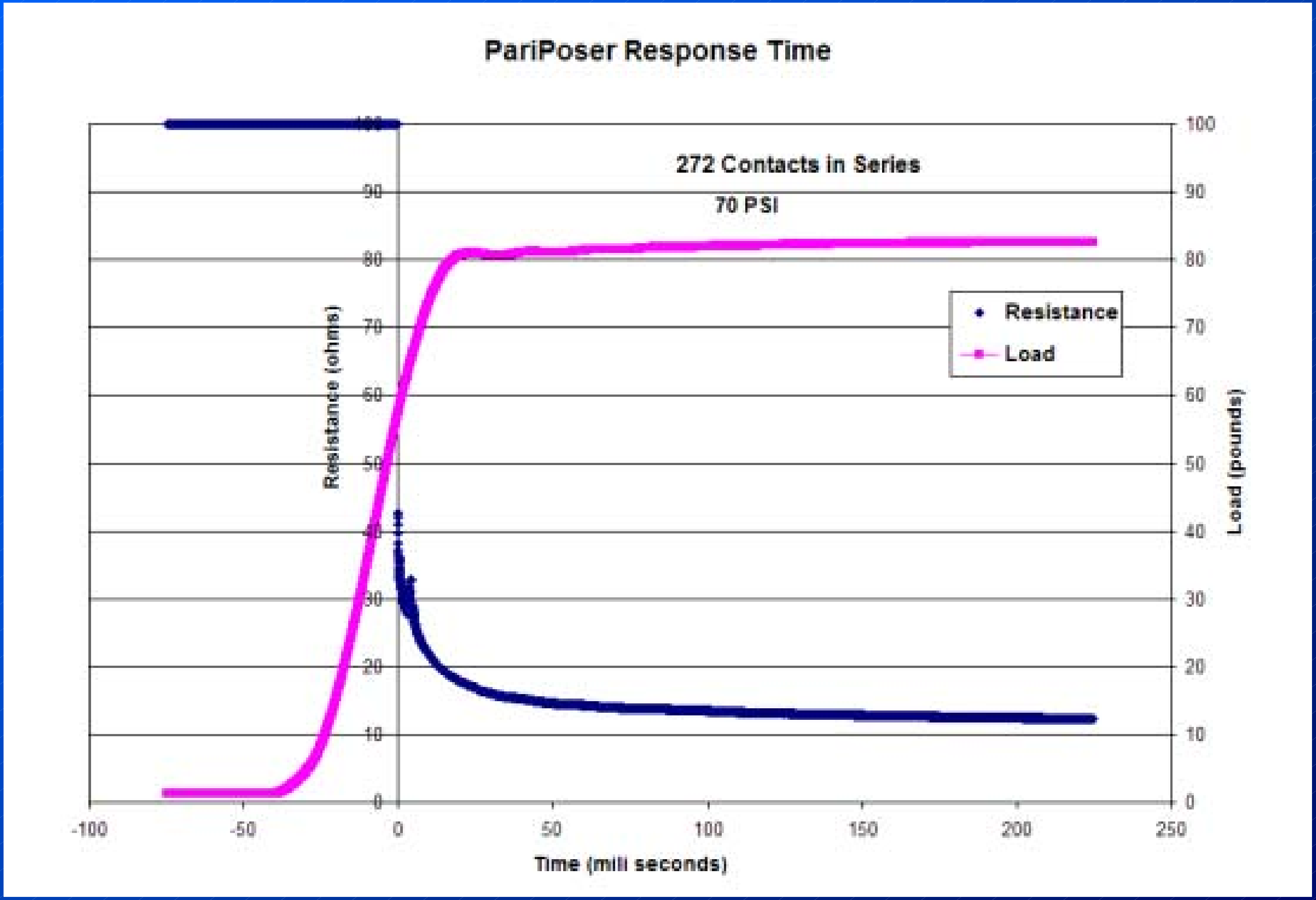
Response Time Setup



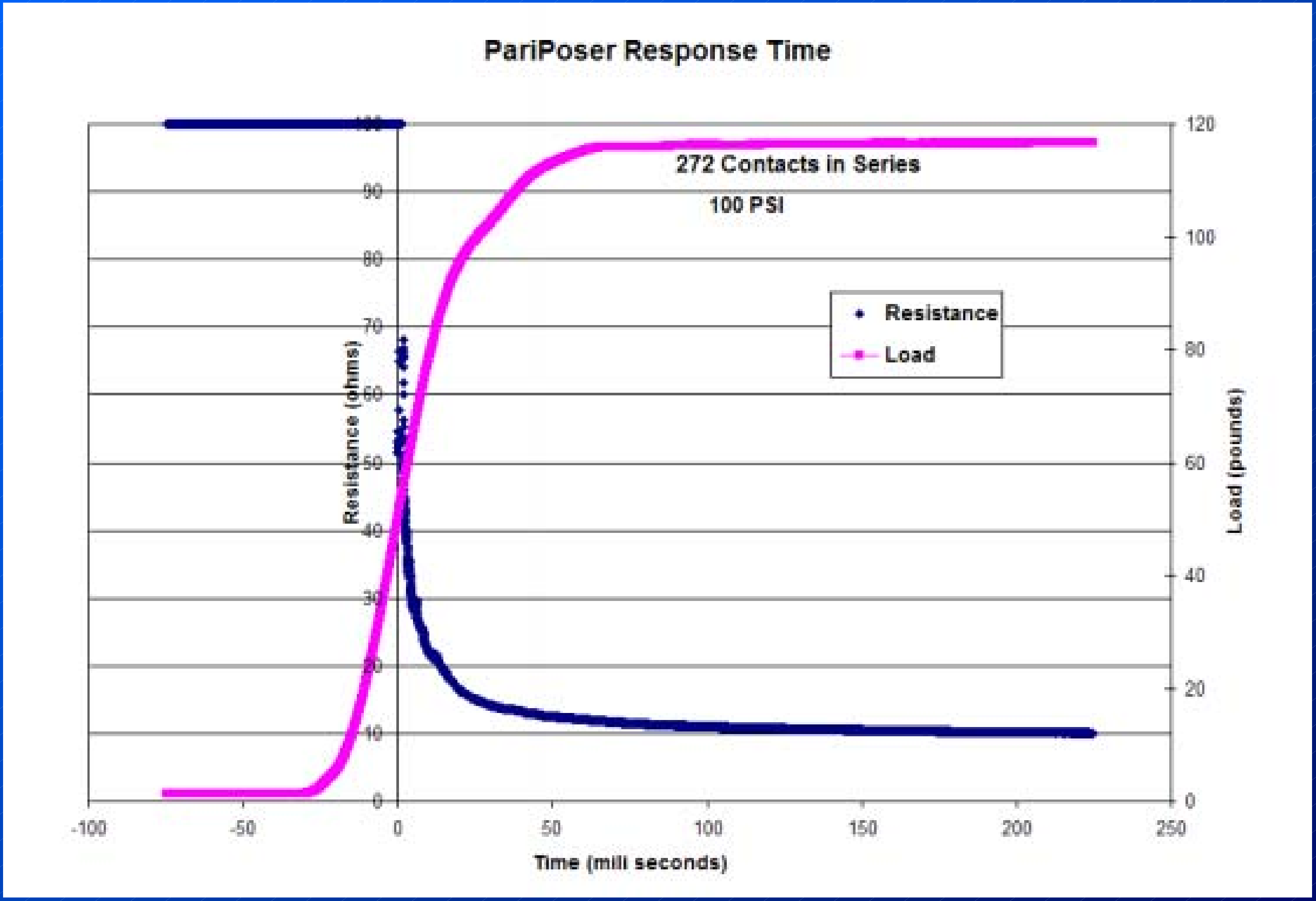
Response Time vs. Load
50 PSI 22 °C



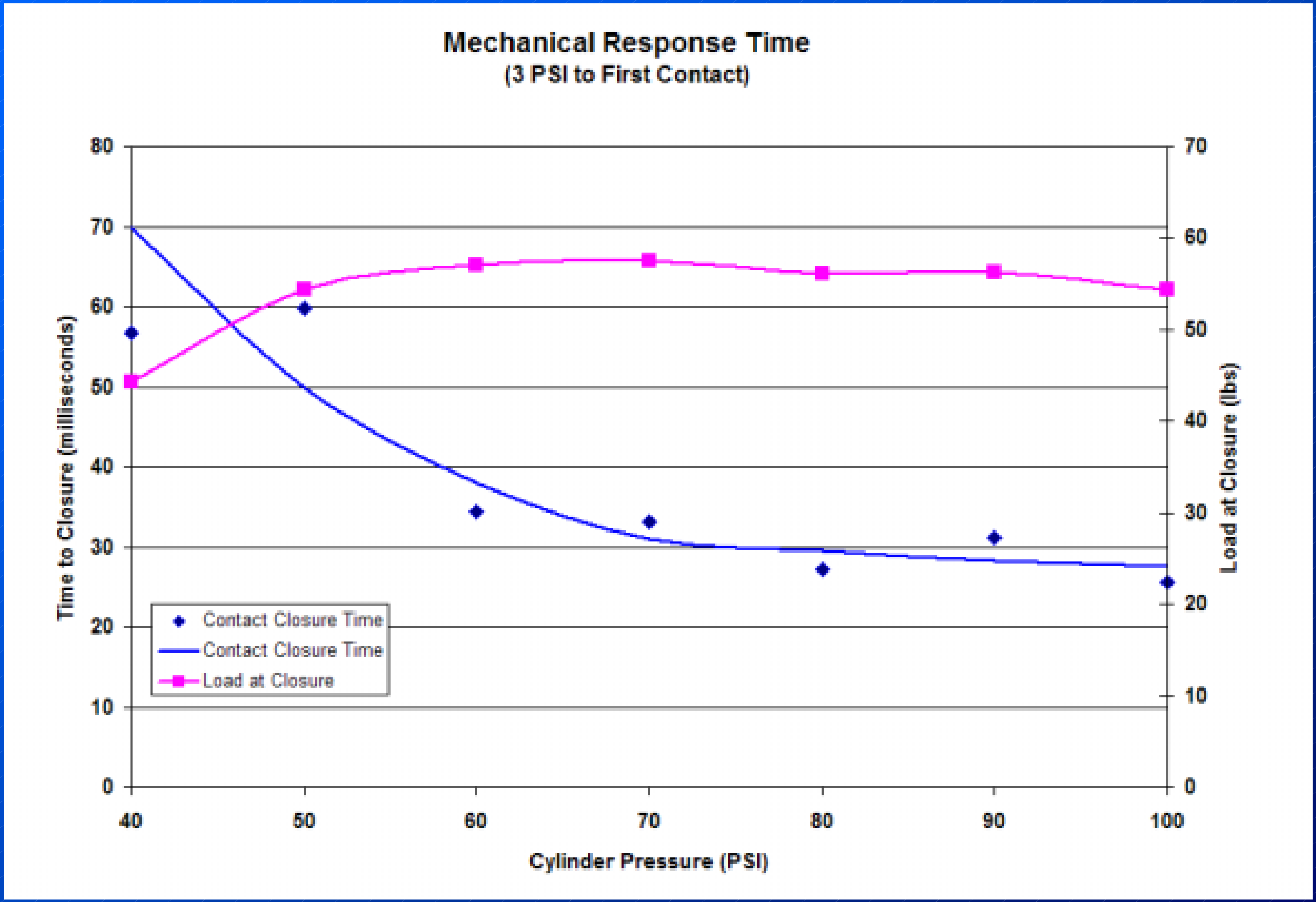
Response Time vs. Load
70 PSI 22 °C



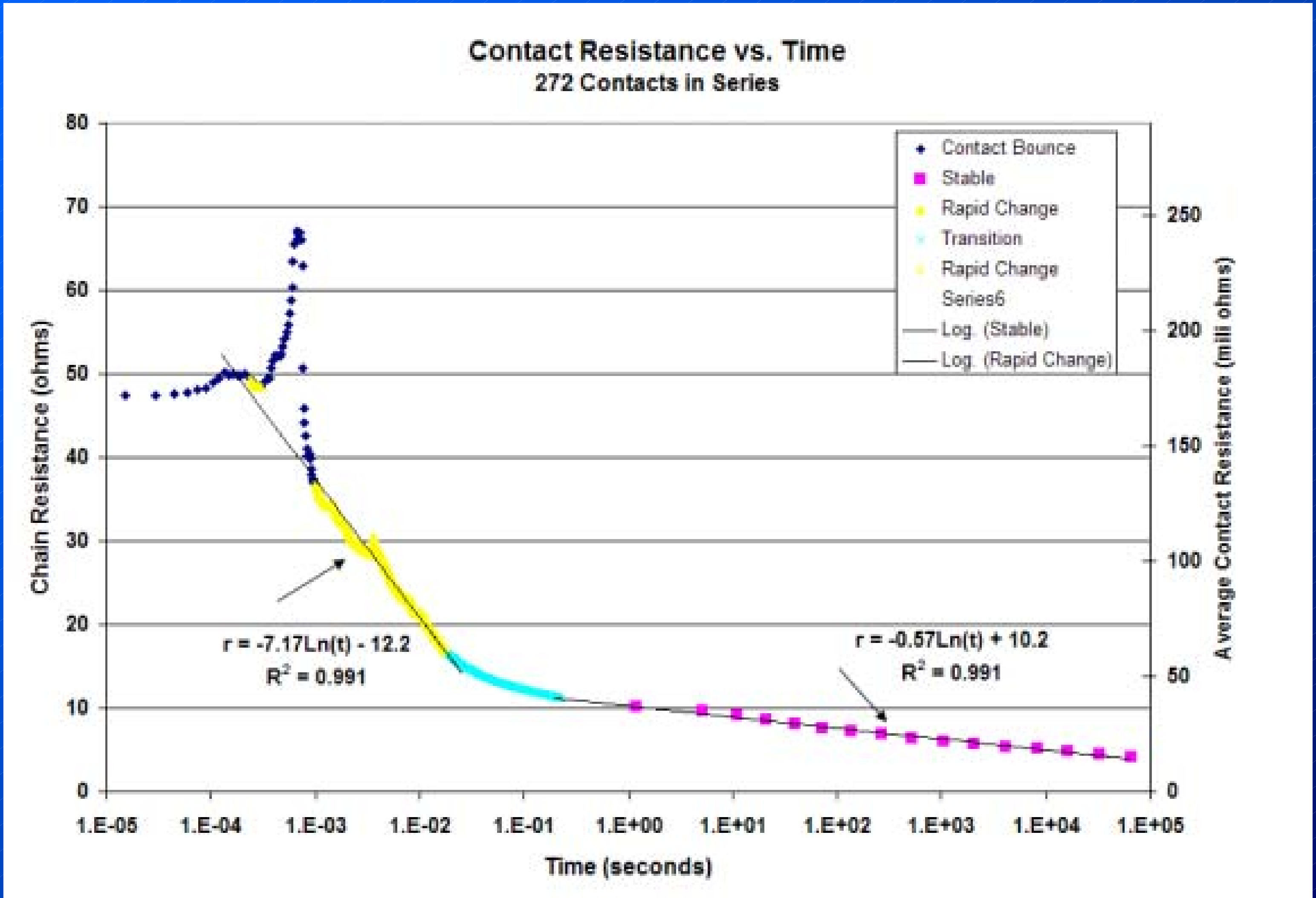
Response Time vs. Load
100 PSI 22 °C



Mechanical Response Time



Summary of Resistance vs. Time
(After Load Reaches 55 lbs)



Conclusions

Properly Designed Visco – Elastic Contacts Provide a Very Responsive and Stable Interconnection System

- ***Time to Initial Contact Dominated by Actuation System***
- ***Stable, Decreasing Resistance Seen in under 2 ms after contact made***
- ***Rate of Resistance Decrease Changes at 200 ms***
- ***Resistance Decrease Follows Ln(t) behavior for extended time***

Conclusions

- ***Resistance Decrease Follows Ln(t) behavior for extended time***
- ***Rate of Resistance Change a Function of Pressure, Temperature and Elastomer Properties***
- ***Ultimate Resistance a Function of BallWire ®***
- ***Modeling Work Needed to Better Understand Data***

Solving Cathodic (Conductive) Anodic Filament (CAF) Migration with THERMOUNT® Laminate and Prepreg

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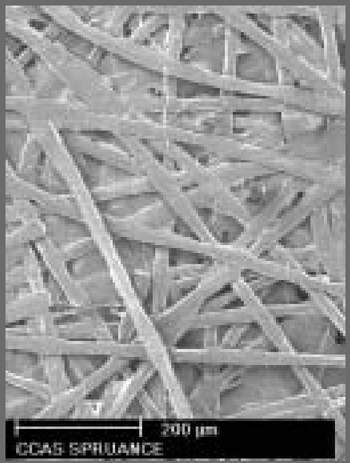
--- Special Thanks to Karl Sauter, Sun Microsystems ---

The miracles of science

What Is THERMOUNT®?

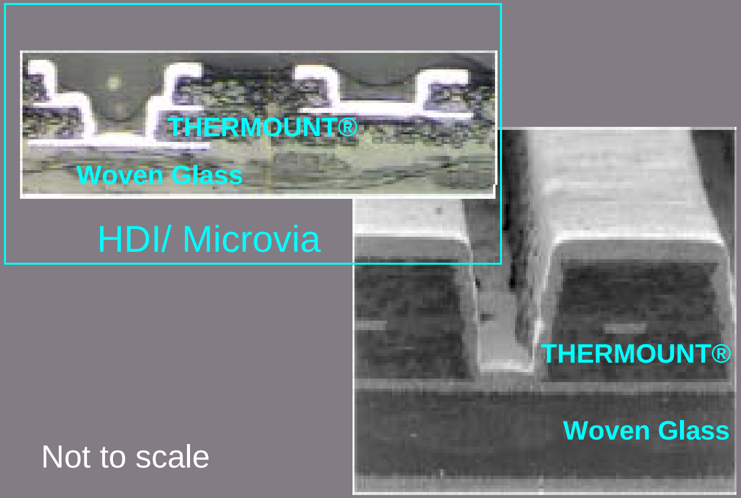
- DuPont’s trademark for laminate and prepreg containing nonwoven **100% ORGANIC aramid reinforcement** used in printed wiring boards (PWBs) and IC chip carrier (IC packages)

- Sold through licensed laminators
  - Global Licensees:
    - Arlon, Isola, Nelco
    - Nelco-Dielektra, Polyclad
  - Regional Licensees:
    - CCP for Greater China and Taiwan
    - Shin-Kobe Electric Machinery Co,. Ltd. for Japan and Asia-Pacific



THERMOUNT®)


Woven Glass



Not to scale

Source: Viasystems MicroCoax™

Outline

- *What's CAF?*
- *Why Worry?*
- *Prior Work*
- Why is THERMOUNT® CAF Resistant?
- Current Work
- Results
- Conclusion

Definitions

- *Electrochemical Migration (ECM):*

  The growth of conductive metal filaments across or through a dielectric material in the presence of moisture and under the influence of voltage bias.

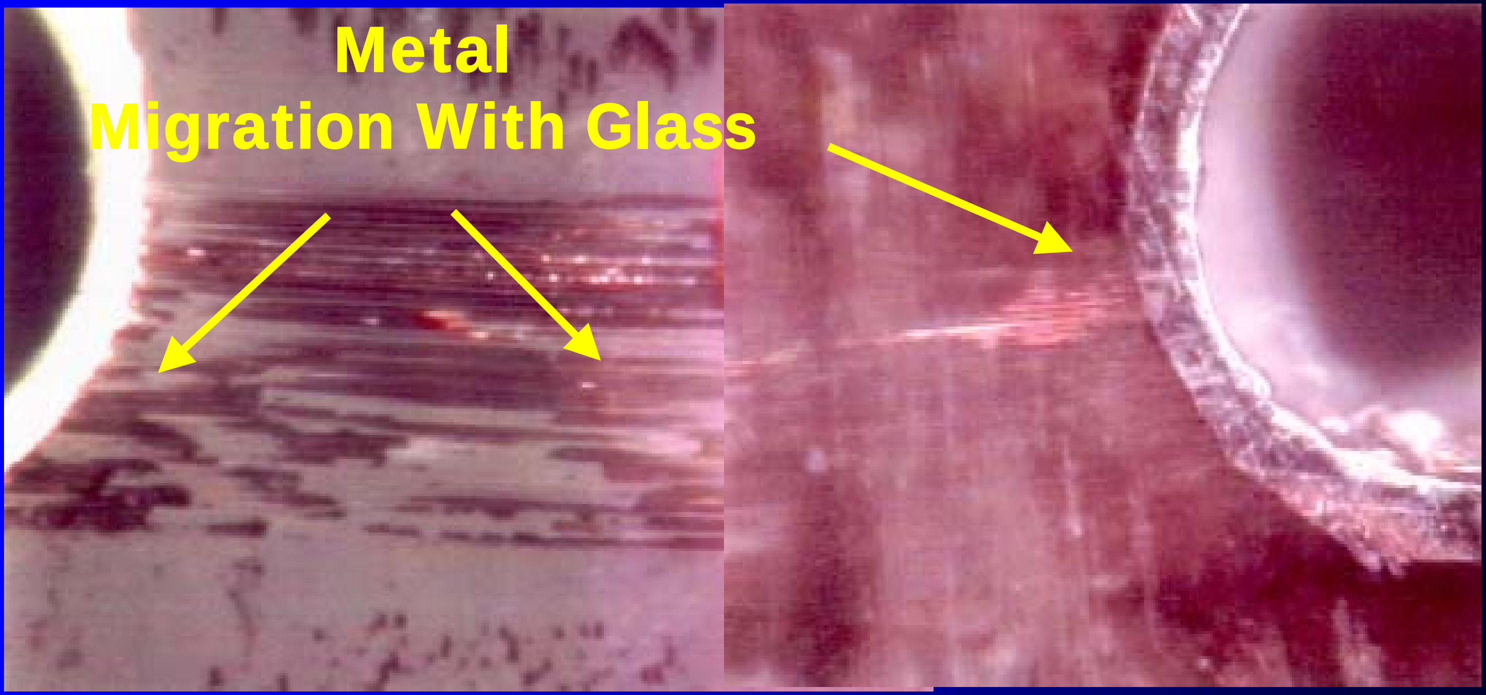
- *Cathodic or Conductive Anodic Filament (CAF) formation:*

  The growth of metallic conductive salt filaments by means of an electrochemical migration process involving the transport of conductive chemistries across a nonmetallic substrate under the influence of an applied electric field, thus producing CAF. [AT&T Labs, Lando and Mitchell, 1979]

Source: Karl Sauter, Sun Microsystems; IPC Expo 2002 paper S-08

CAF Migration In Glass

@ 50x, 28 mil Pitch, 13 mil drilled PTH



Found in 2000, @ 150°C actual operation

Prior Work

- Papers from AT&T, Sun Microsystems, etc. on CAF with glass laminates
- Data from an automotive OEM and two burn-in OEMs showing THERMOUNT® better than glass laminates for anti-CAF
- IBM Microelectronics patent citing THERMOUNT® aramid as anti-CAF substrate (see next chart)

THERMOUNT® Reduces Risk for Metal Migration IBM Patent No: US5981880

NOVELTY - Substrate (114) using epoxy glass prepreg is provided with power planes (134,152). The power planes are encapsulated within the non-conductive layers (156,158) made up of dielectric material free of continuous glass fibers.

USE - For electronic device package like BGA package, multichip module, memory chip.

ADVANTAGE - Prevents short circuit of power plane carried by migration of conductive material along continuous glass fibers. Eliminates *CAF* in PCB. Reduces cost of package by optimizing number of conductive planes. Non-woven glass-free THERMOUNT® is cited.

DESCRIPTION OF DRAWING(S) The figure shows partial cross- sectional view of PCB. PCB 133 Substrate 114 Power planes 134,152 Non-conductive layers 156,158 (Dwg.3/6)

PWB Fab Spacing Trends

Year	PTH Pitch (mils)	Package Pitch (mm)	Drilled Hole Dia (mils)	V ia Edge to Edge (mils)
1985	100.0	2.5	42.0	58.0
1990	70.7	1.8	38.0	32.7
1995	50.0	1.27	14.0	36.0
1999	39.4	1.0	12.5	26.9
2002	31.5	0.8	10.0	21.5
2004	27.8	0.7	9.0	18.8
2006	19.7	0.5	8.0	11.7

Source: Karl Sauter, Sun Microsystems; IPC Expo 2002 paper S-08

Outline

- What's CAF?
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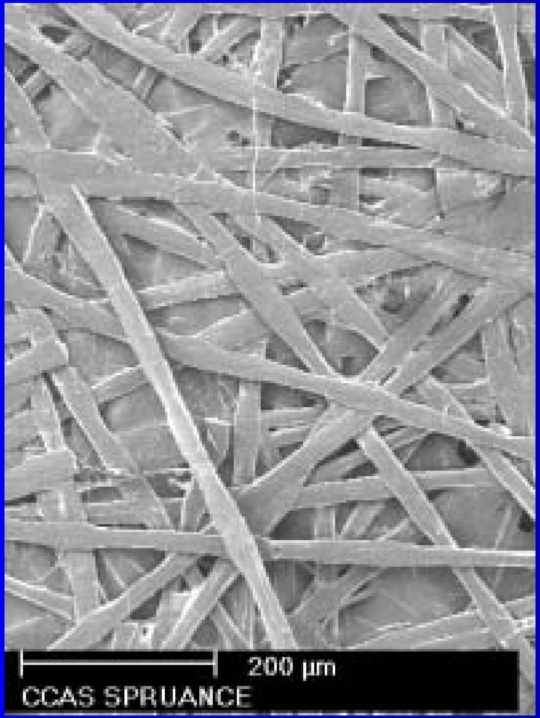
Why is THERMOUNT® Anti-CAF? V1.1

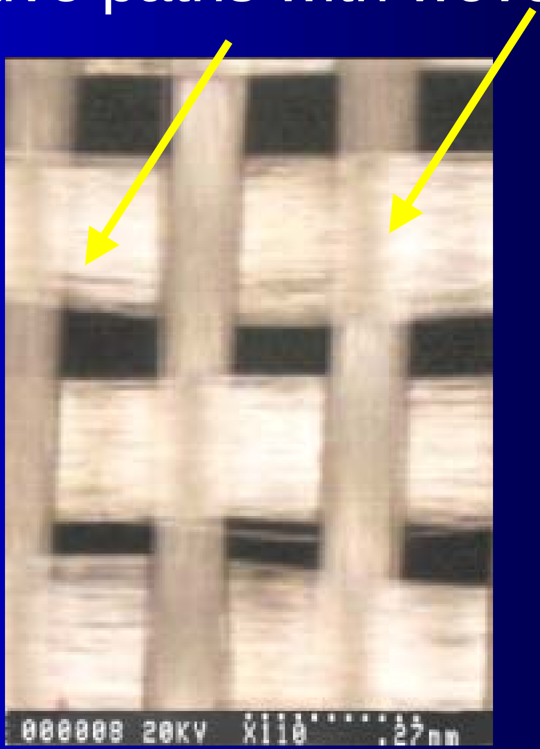
- THERMOUNT® is non-woven. There is no direct path for migration.
- During organic resin impregnation, THERMOUNT® is completely covered by resin since it's organic, too. There is no resin recession after solder shock.
- THERMOUNT® uses non-dicey, phenolic based resins that are CAF resistant
- When mechanically drilled, plated-through holes with THERMOUNT® are not smashed vs. glass, resulting in only very small wicking.

Comparing Glass and THERMOUNT®

Direct conductive paths with woven glass

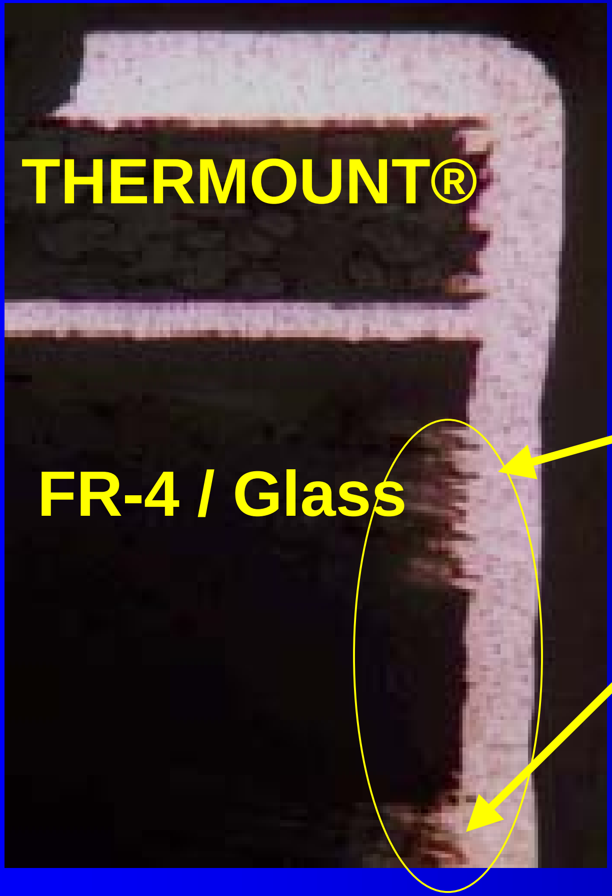


THERMOUNT®)



Woven Glass

Typical PTH Quality After Mechanical Drilling and CAF Migration

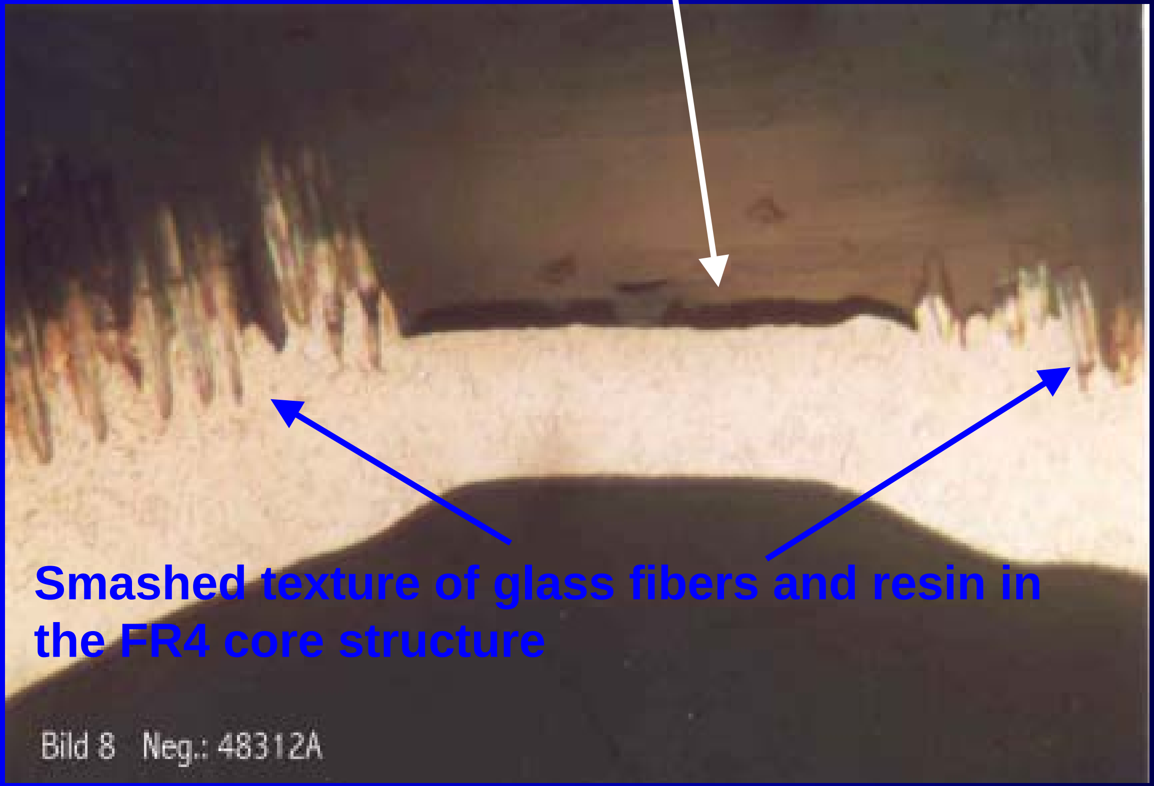


Smashed texture (wicking) of glass fibers and imperfect resin impregnation in FR4 core leads to CAF migration

FR-4/ Glass Resin Recession

(After 288 °C, 10 s Solder shock)

Delamination of the FR4-Resin Phase Void behind the plated Cu after thermal shock due to resin recession



Outline

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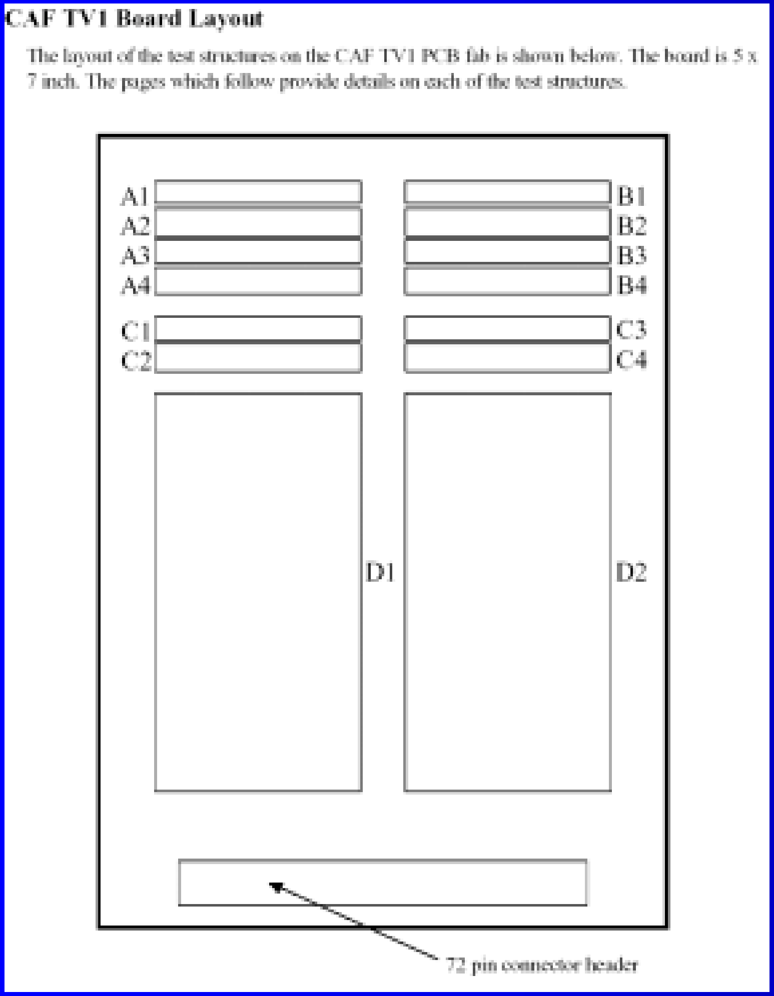
Description of CAF Test Vehicle #1

(CAF TV1) by Sun Microsystems Inc. - 1/14/00



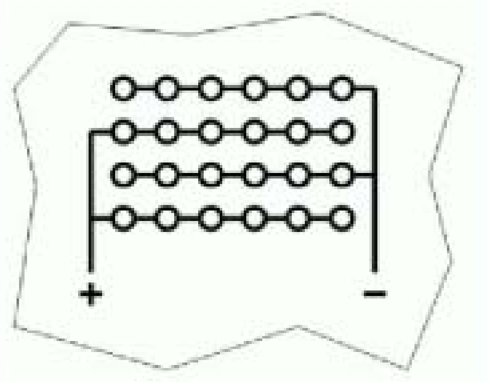
C and D slots not used per Sun's input

Courtesy: Sun Microsystems

"A" Design

Test Structures A1 through A4

The four "A" test structures have 5 alternating rows of vias. Within each structure, each row has 42 vias with alternating rows being tied to positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 40 x 40 mil via grid. The resulting via edge to via edge spacings are: 10.8, 15, 20 and 25.5 mils. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the "A" test structure are aligned with the glass fibers. Within a given test structure, the inner and outer layer pads for all ten layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change from stucture to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etchout will not effect results.



A conceptual representation of the "A" test structure is shown to the upper right. Design details on each of the four "A" test structures follows in Table 1.

Table 1 - Test Structures A1 through A4 Design Rules

	A1	*A2*	*A3*	*A4*
Outer layer pad size	34 mil	32 mil	30 mil	27 mil
Inner layer pad size	34 mil	32 mil	30 mil	27 mil
Drilled hole size	29.2 mil	25 mil	20 mil	14.5 mil
Via edge to via edge (shortest distance)	10.8 mil	15 mil	20 mil	25.5 mil
Via edge to via edge (Manhattan distance)	10.8 mil	15 mil	20 mil	25.5 mil
Bias pins	1 to 5	2 to 5	3 to 5	4 to 5

Courtesy: Sun Microsystems

"A" Design Rules

Table 1 - Test Structures A1 through A4 Design Rules

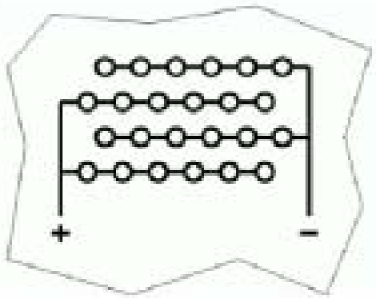
	A1	*A2*	*A3*	*A4*
Outer layer pad size	34 mil	32 mil	30 mil	27 mil
Inner layer pad size	34 mil	32 mil	30 mil	27 mil
Drilled hole size	29.2 mil	25 mil	20 mil	14.5 mil
Via edge to via edge (shortest distance)	10.8 mil	15 mil	20 mil	25.5 mil
Via edge to via edge (Manhattan distance)	10.8 mil	15 mil	20 mil	25.5 mil
Bias pins	1 to 5	2 to 5	3 to 5	4 to 5

“B” Staggered Design

(avoids direct route of CAF growth for woven structure)

Test Structures B1 through B4

The four "B" test structures have 7 alternating rows of vias. Within each structure, alternating rows have either 27 or 26 vias with the alternating rows being tied to either positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 60 x 60 mil via grid. The 60 x 60 mil grid has an interstitial via therefore, tipping at a 45° angle results in a square 42.4 x 42.4 mil grid.Note: the sketch does not look square when tipped 45° but, the CAF TV1 fabs do. The resulting via edge to via edge spacings are: 10.4, 14.4, 19.9 and 24.4 mils. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the "B" test structure are **not** aligned with the glass fibers. If the failure mode is along glass bundles it is reasonable to expect the "B" test structure to perform better than the "A" structure for equivalent via edge to via edge spacings. Within a given test structure, the inner and outer layer pads for all ten layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change from stucture to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etchout will not effect results.



A conceptual representation of the "B" test structure is shown to the upper right. Design details on each of the four "B" test structures follows in Table 2.

Courtesy: Sun Microsystems

Table 2 - Test Structures B1 through B4 Design Rules

	B1	*B2*	*B3*	*B4*
Outer layer pad size	37 mil	35 mil	33 mil	30 mil
Inner layer pad size	37 mil	35 mil	33 mil	30 mil
Drilled hole size	32 mil	28 mil	22.5 mil	18 mil
Via edge to via edge (shortest distance)	10.4 mil	14.4 mil	19.9 mil	24.4 mil
Via edge to via edge (Manhattan distance)	14.75 mil	20.4 mil	28.2 mil	34.55 mil
Bias pins	7 to 11	8 to 11	9 to 11	10 to 11

“B” Design Rules

Table 2 - Test Structures B1 through B4 Design Rules

	B1	*B2*	*B3*	*B4*
Outer layer pad size	37 mil	35 mil	33 mil	30 mil
Inner layer pad size	37 mil	35 mil	33 mil	30 mil
Drilled hole size	32 mil	28 mil	22.5 mil	18 mil
Via edge to via edge (shortest distance)	10.4 mil	14.4 mil	19.9 mil	24.4 mil
Via edge to via edge (Manhattan distance)	14.75 mil	20.4 mil	28.2 mil	34.55 mil
Bias pins	7 to 11	8 to 11	9 to 11	10 to 11

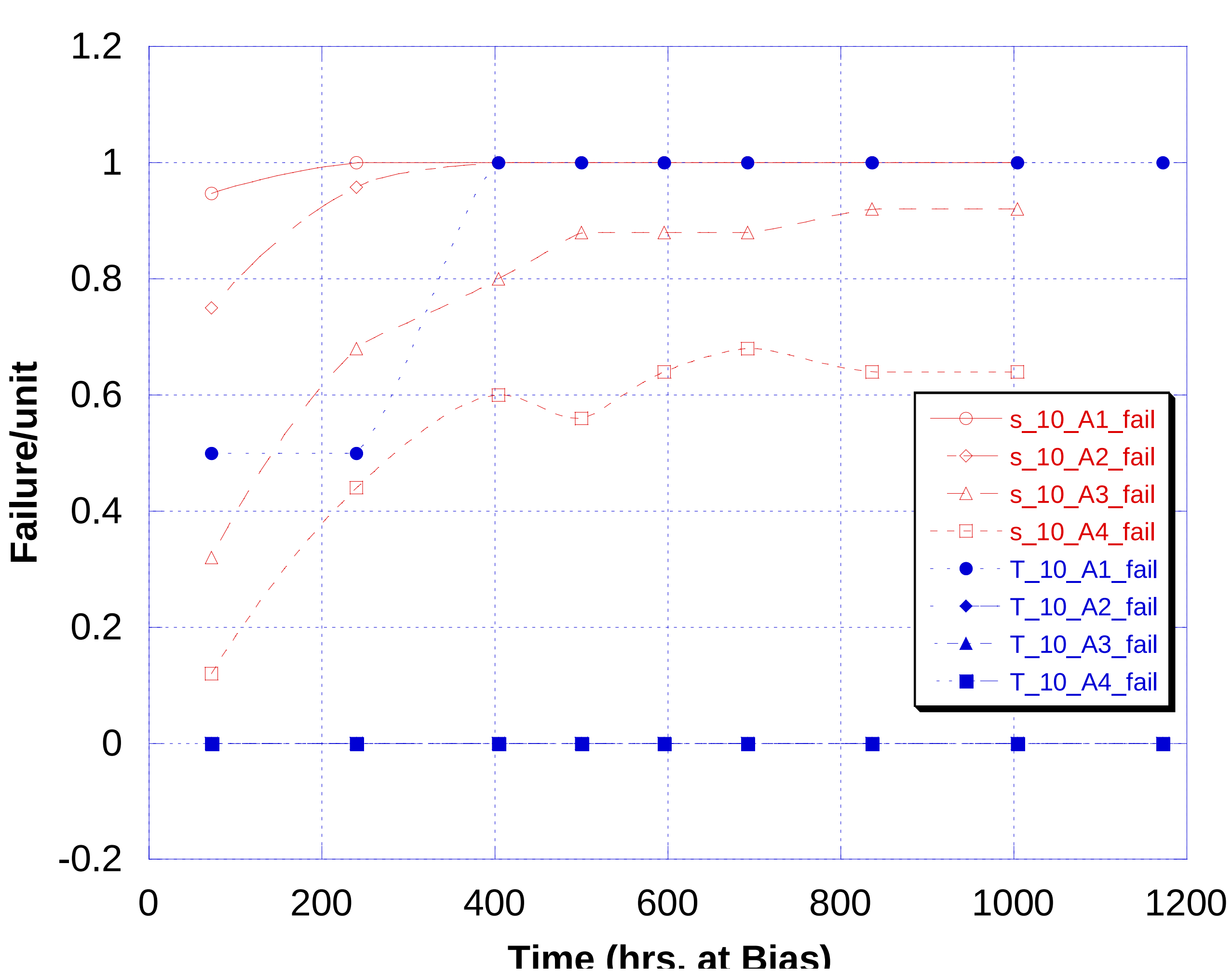
Test Details

- 10 layer PWB, 100% of each material
- “A” vs. “B” design
  - Within each design, the edge-edge distance was varied by varying drill size
- 10 vs. 100 volts and exposure to 65°C at 85%RH.
- THERMOUNT® (coded T) vs. leading CAF-resistant glass/FR-4 laminate (Coded S2)
- Time: 0, 96, 168, 336, 500, 596, 692, 788, 932, 1100, 1268 hours
  - No bias voltage up to 96 hours
  - standard CAF test must pass 500 hours only
- Output criterion: change in resistance due to CAF > 1 decade

Outline

- What's CAF?
- Why Worry?
- Prior Work
- Why is THERMOUNT® CAF Resistant?
- Current Work
- *Results*
- Conclusion

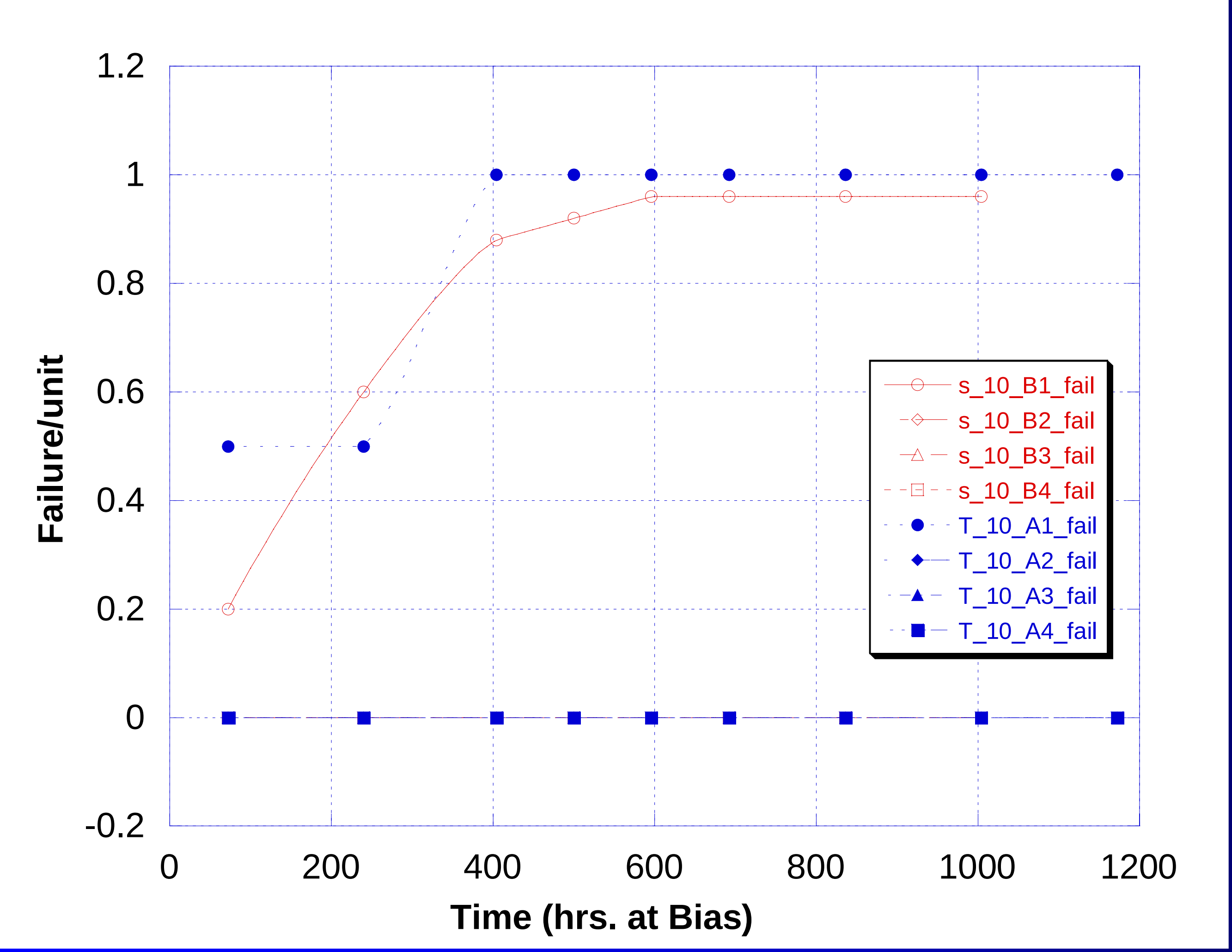
Comparative Failure Rate
for glass/epoxy and THERMOUNT®



(Bias 10 V, exposure to 65°C/85%RH - Bias applied after 96 hrs. exposure- Type A)

At **10 V** bias, THERMOUNT® has **superior** CAF resistance at every A configuration

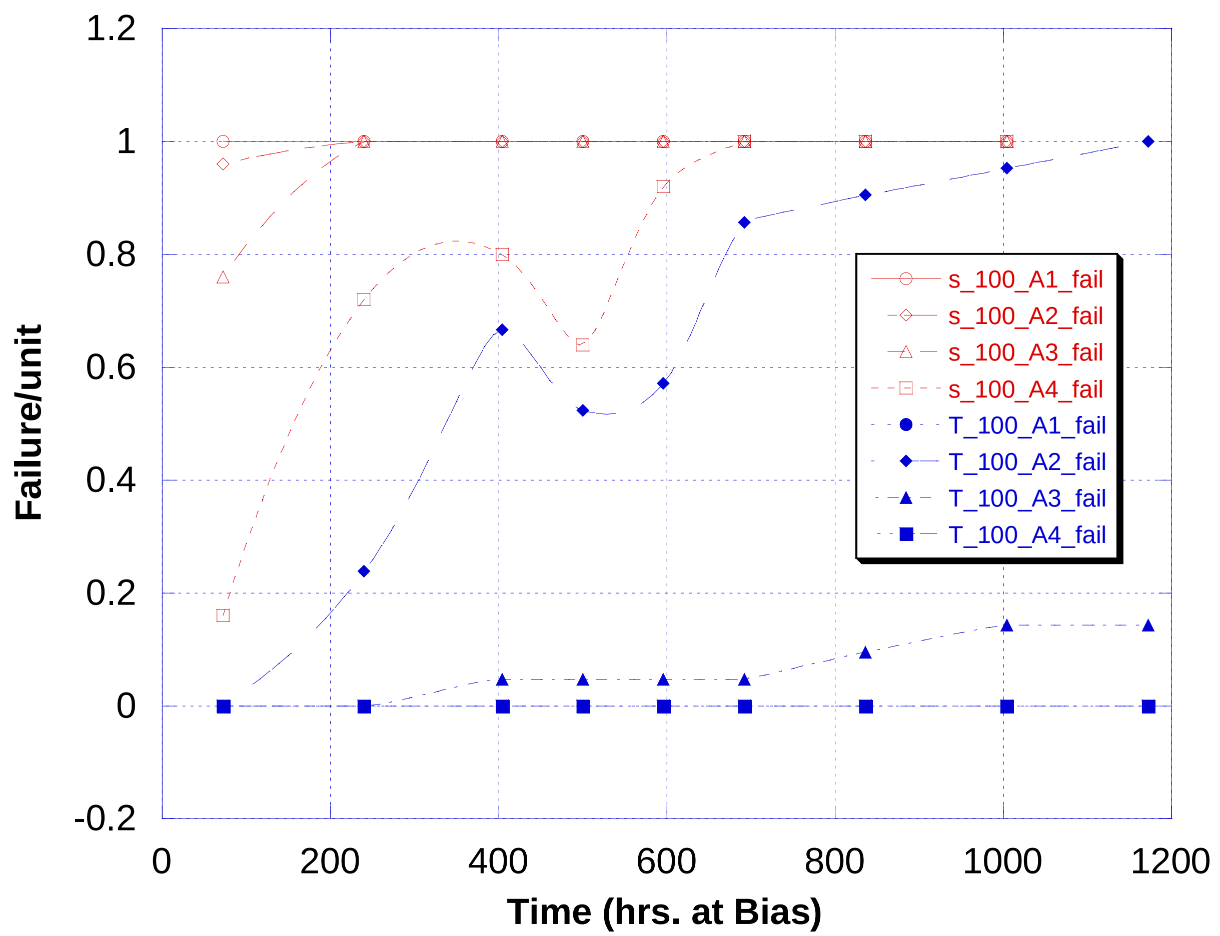
Comparative Failure Rate for glass/epoxy and THERMOUNT®



(Bias 10 V, exposure to 65°C/85%RH - Bias applied after 96 hrs. exposure- Type A)

At **10 V** bias, THERMOUNT® with A configuration has **equivalent** CAF resistance compared to FR-4 with B configuration

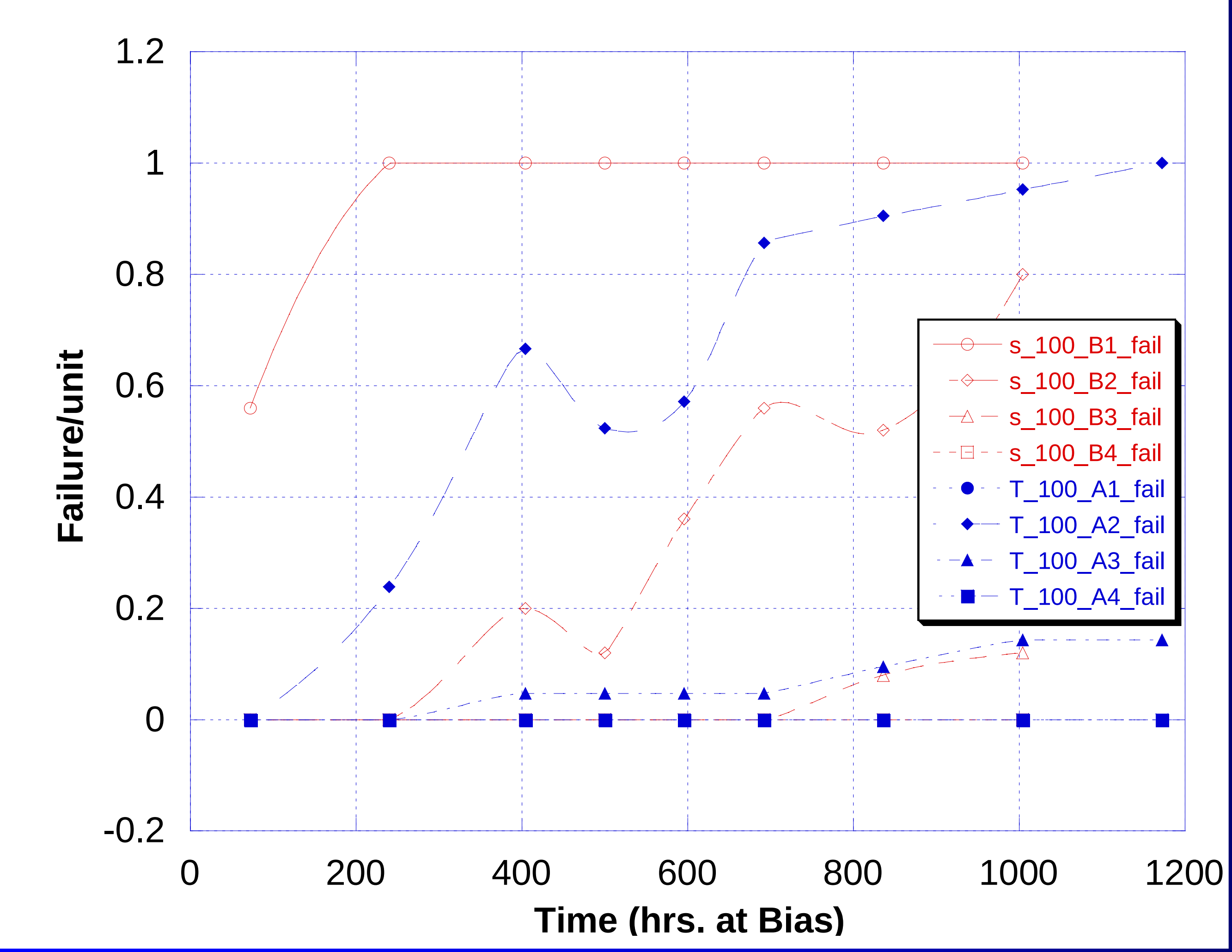
Comparative Failure Rate for glass/epoxy and THERMOUNT®



(Bias 100 V, exposure to 65°C/85%RH - Bias applied after 96 hrs. exposure- Type A)

At **100 V** bias, THERMOUNT® has **superior** CAF resistance at every A configuration

Comparative Failure Rate for glass/epoxy and THERMOUNT®



(Bias 100 V, exposure to 65°C/85%RH - Bias applied after 96 hrs. exposure- Type A)

At 100 V bias, THERMOUNT® with A configuration has equivalent CAF resistance compared to FR-4 with B configuration

Conclusions

- At **10 & 100V** bias, THERMOUNT® has **superior** CAF resistance at every A configuration
- At **10 &100 V** bias, THERMOUNT® with A configuration has **equivalent** CAF resistance compared to FR-4 with B configuration.
- B-configuration is advantageous for woven structure. No significant difference between A & B configuration for non-woven (THERMOUNT®) structure.
- In A-configuration for FR-4, at least 60% failure rate for every edge distance at 500 hours. Only B-4 configuration survived 100%.
- For THERMOUNT®, B-4 and A-4 survived 100% at 10 and 100V. At 10V, one B-2 hole failed for THERMOUNT®(<5%). Rest of 2,3,4 edge distance in both configuration survived.
- For most of the cases, failure rate remained constant after 500 hours of exposure.