Burn-in & Test Socket Workshop

March 7 - 10, 2004
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

ARCHIVE

Burn-in & Test Socket Workshop™

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BiTS Burn-in & Test Socket Workshop

Technical Program

Session 1
Monday 3/08/04 8:30AM

PUSHING THE ENVELOPE

"IC Power - The Influence And Impact Of Semiconductor Technology"

Marc Knox – IBM Microelectronics

"Reducing The Cost Of Test In Burn-in - An Integrated Approach"

Michael Noel – Motorola SPS

Don VanOverloop – Motorola SPS **Allan Dobbin** – Motorola SPS

"0.4mm Compression Mount BGA Burn-in Socket, Another Breakthrough in Socket Technology"

Helge Puhlmann – Yamaichi Electronics

Kazuhiro Matsuda – Yamaichi Electronics **Jec Sangalang** – Yamaichi Electronics

IC POWER
The INFLUENCE and IMPACT of SEMICONDUCTOR TECHNOLOGY

Marc Knox
IBM Microelectronics
Burlington VT

BiTS 2004

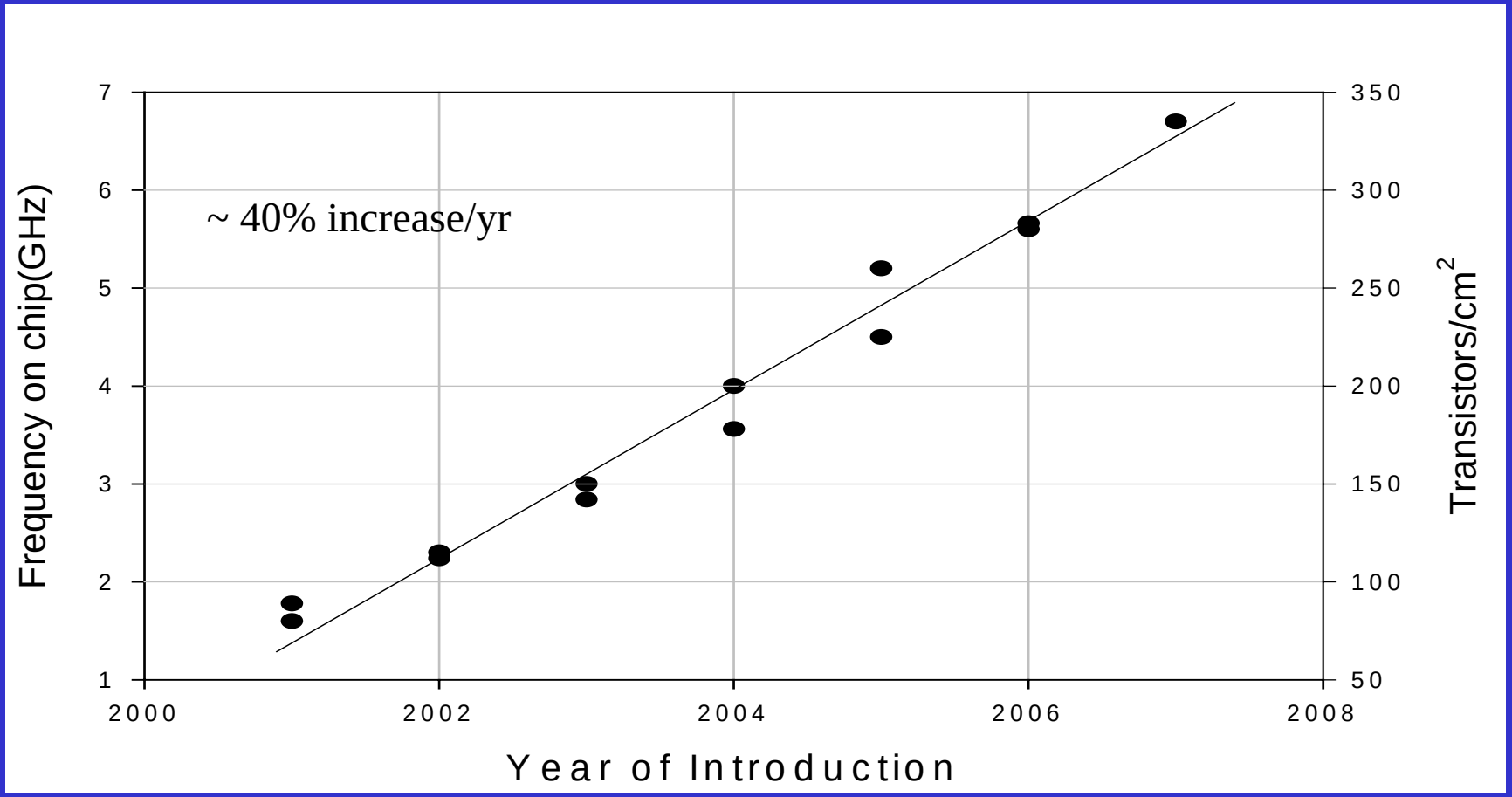
INTRODUCTION

- THE GOOD
  - The CMOS Semiconductor marketplace is demanding IC designs that are:
    - Faster, smaller, more functional and lower in cost
  - Conventional CMOS scaling has been able to maintain trends which satisfy these demands
- THE BAD AND THE UGLY
  - The technology scaling that satisfies the performance trends comes at a cost.....Increasing Power!
  - Why is this the case? Will this go on forever? Where does this leave test and burn-in?
- A base understanding of the semiconductor technology which drives our industry is an important differentiator in our business

THE GOOD PART
CMOS SCALING BENEFITS

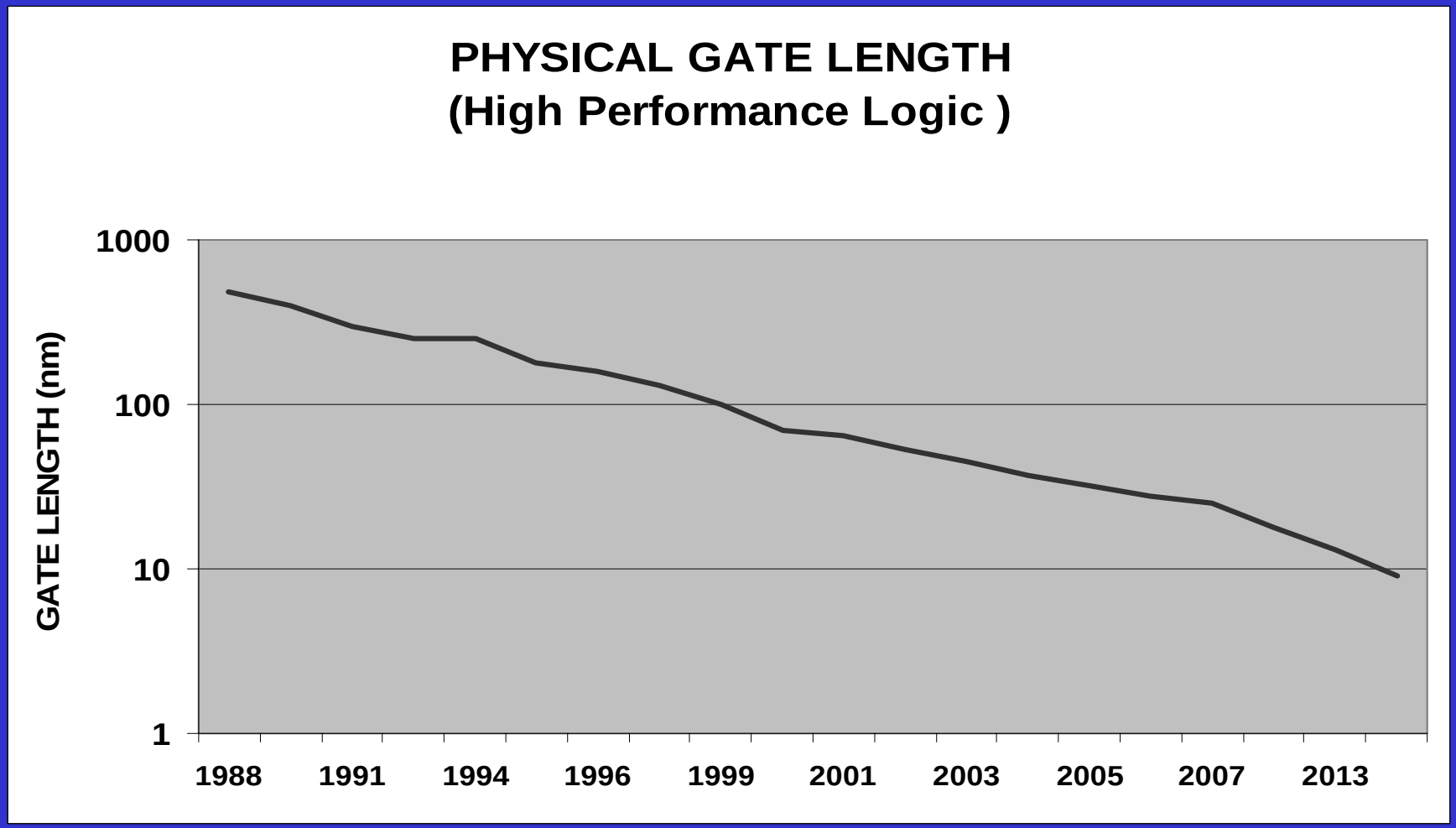
- Scaling is the primary driver in the gains made to date in CMOS performance
- The industry has stayed close to, or ahead of, the scaling predicted by Moore's Law
- Conventional scaling involves physical reduction of transistor gate length, width and oxide dimensions as well as power supply voltage
- Conventional scaling is becoming increasingly difficult to realize
- Into the future, scaling takes the form of "effective" scaling with new materials and structures

CMOS SCALING PERFORMANCE, DENSITY TREND



Adopted from [1]

CMOS SCALING
PHYSICAL Tx DIMENSION



Adopted from [1]

THE BAD AND THE UGLY PARTS CMOS POWER IS NOT SCALING

- Conventional scaling sees transistor dimensions shrinking at a high rate but supply voltage and threshold voltage are decreasing at a slower rate
- The static DC “leakage” power trend is much steeper than the AC “switching” power trend
- Leakage is on track to equal and exceed active power in the application space
- For test and burn-in, this power is a huge concern
- We will continue to see substantial power increases if performance gain trends are to continue on pace

CMOS SCALING (or lack thereof)
VOLTAGE APPLIED

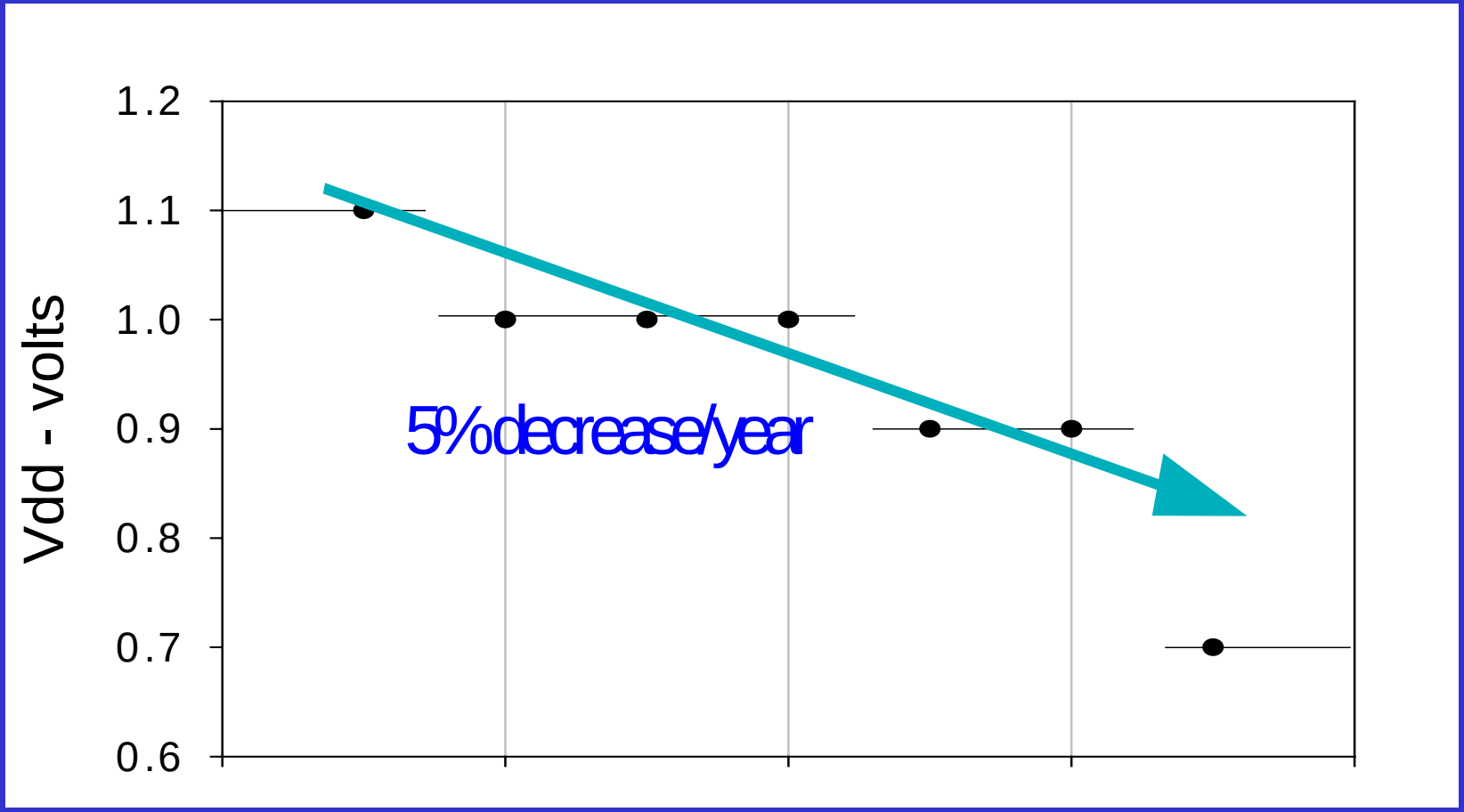


Chart courtesy of Roger Schmidt , IBM

CMOS SCALING (or lack thereof)
SYSTEM POWER

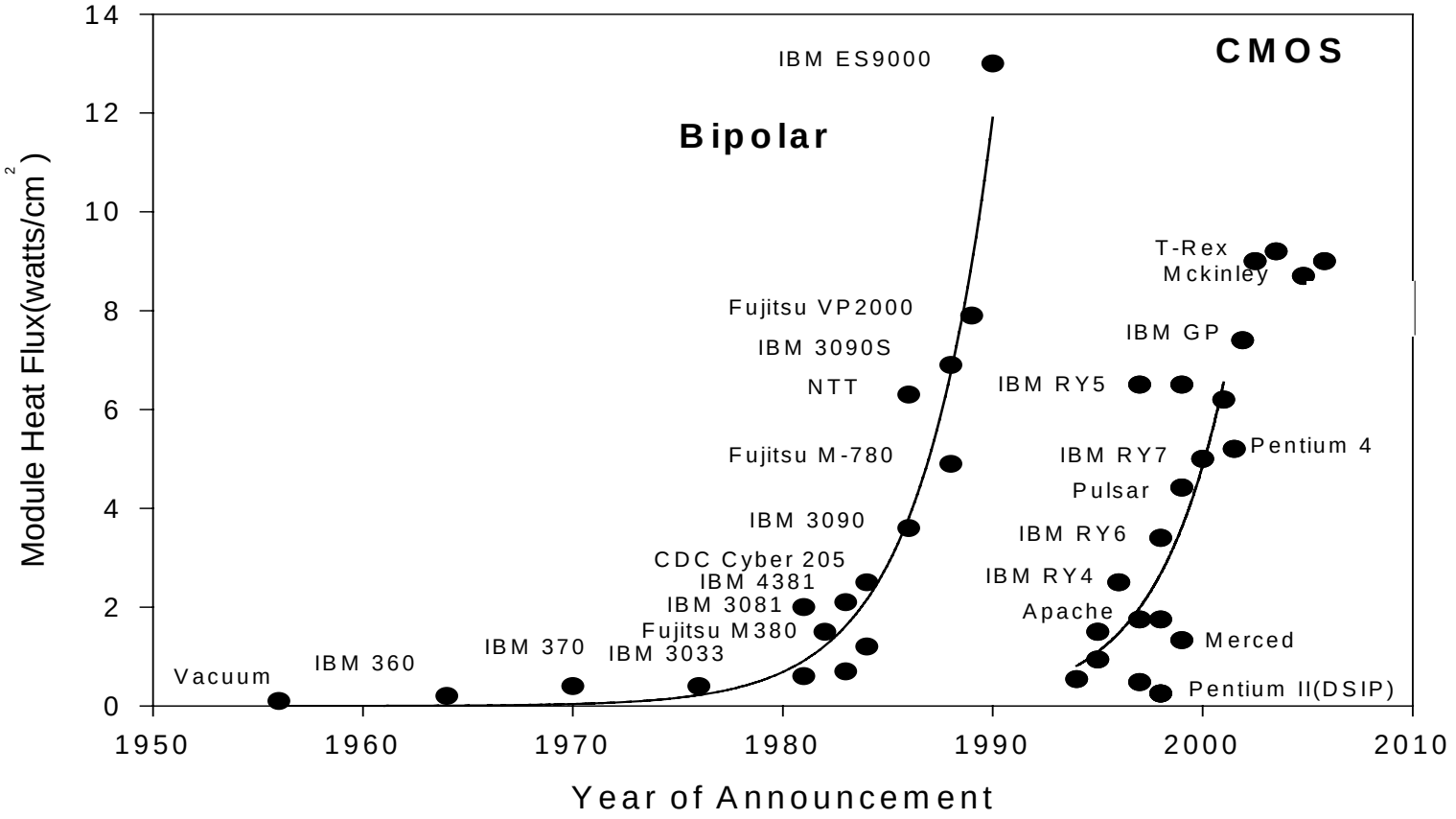
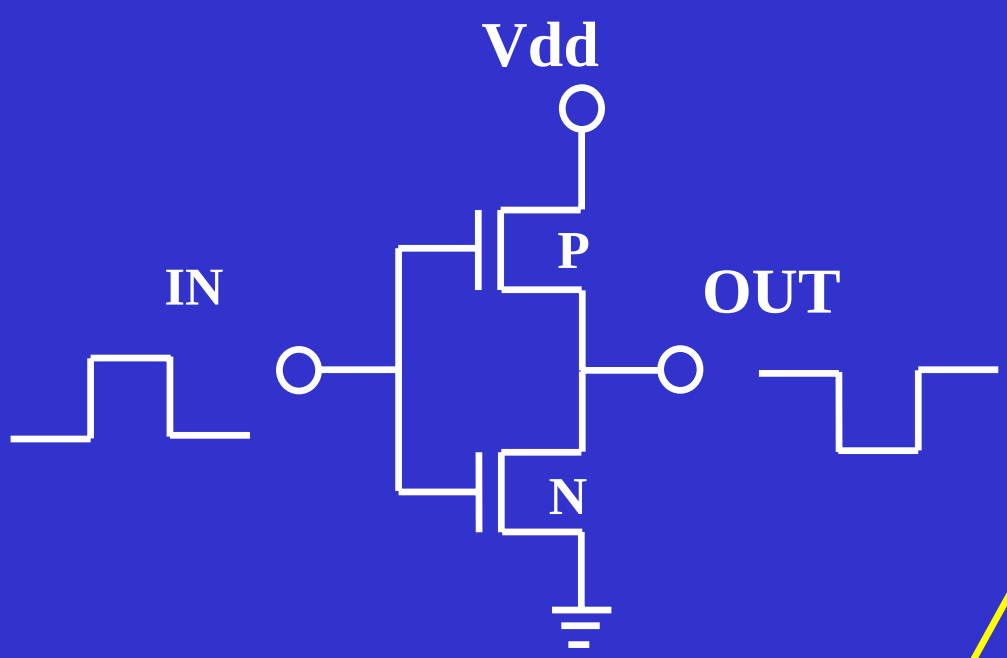
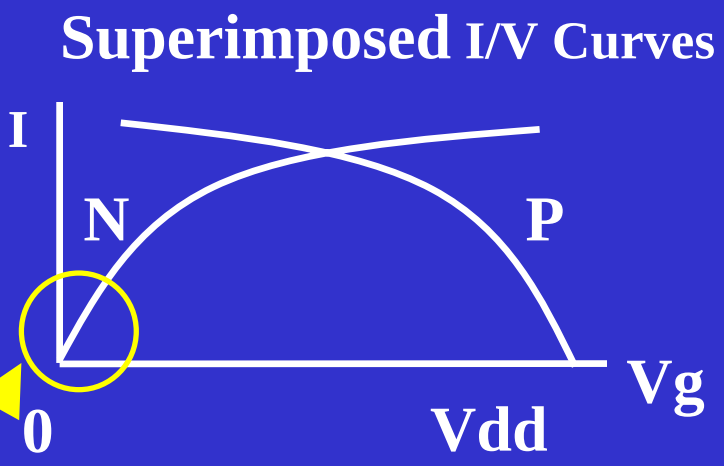


Chart courtesy of Roger Schmidt , IBM

WHY IS POWER NOT SCALING?

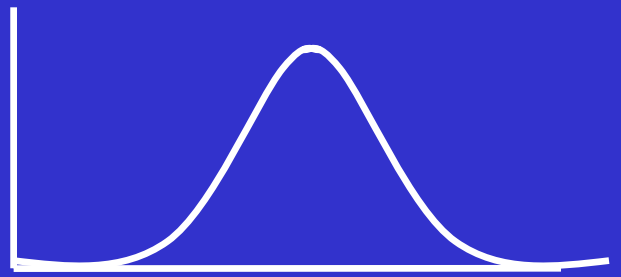
- CMOS is supposed to be low power….. right?





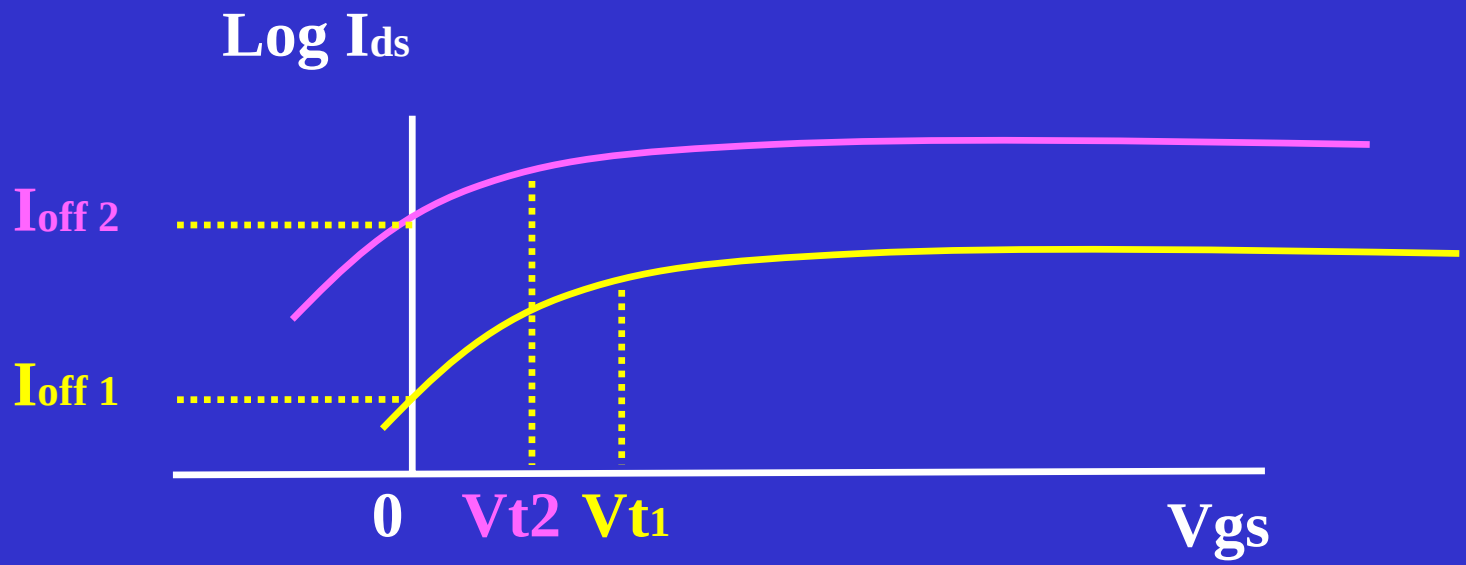
Problem Occurs Here

(subthreshold region)



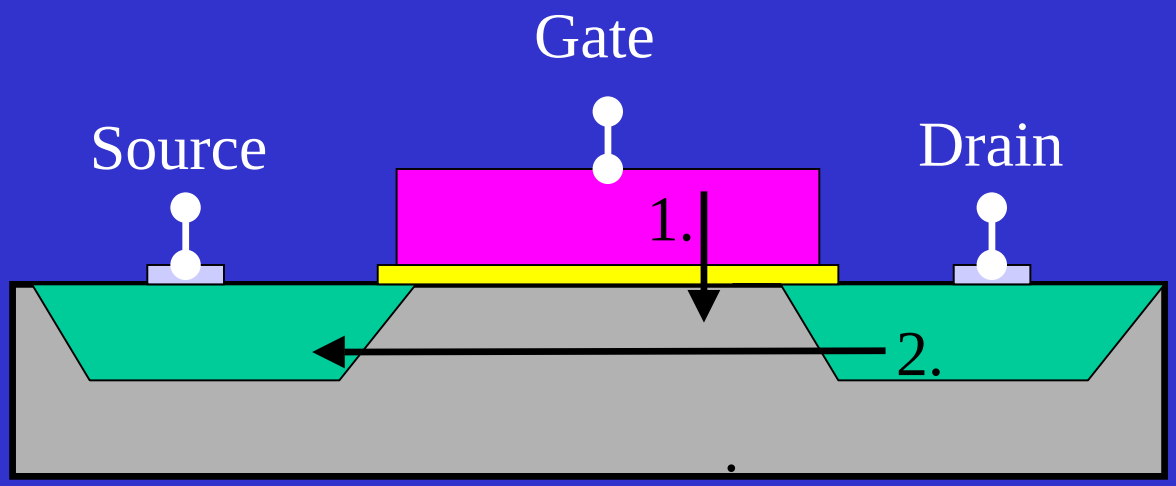
Freehand Curves for Illustration (not to scale)

WHY IS POWER NOT SCALING?
Tx Transfer Curve in the Sub Vt region



- The “off” transistor is never really “fully off”
- Vt scales along with technology supply voltage (linear)
- Ioff is exponentially related to Vt in the SubVt region
- Ioff increases exponentially with lower supply voltage!!

CMOS DC POWER ORIGINS
Main Leakage Components of Interest

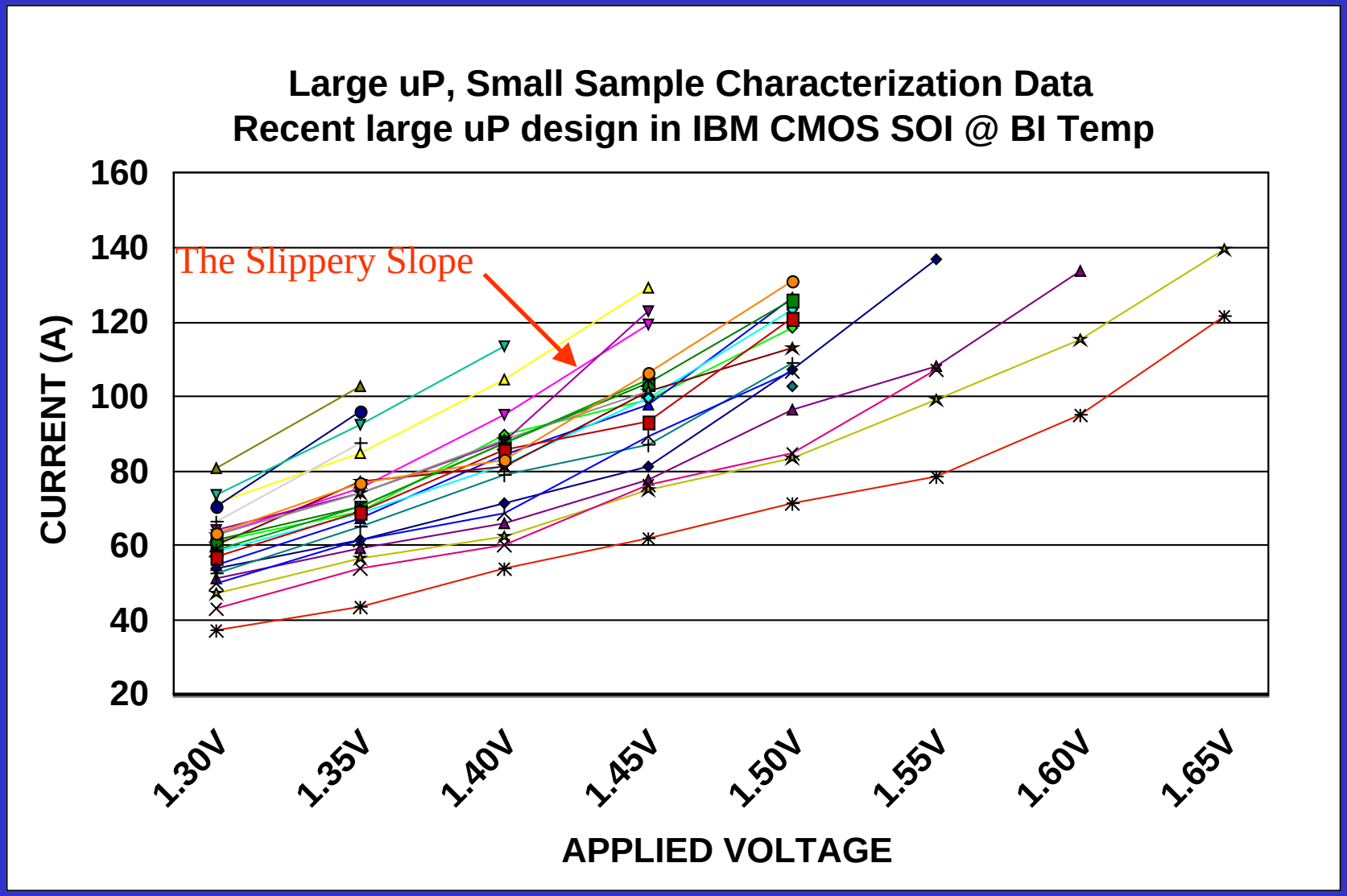


- Gate Oxide Tunneling Current
- Channel Off Current…Drain Induced Barrier Lowering, Short Channel Effect, Narrow Channel Effect, Gate Induced Drain Leakage

THE TRIPLE WHAMMY AT ELEVATED CONDITIONS

- Most test and burn-in processes require some form of elevated conditions
- These conditions produce higher currents than are typically seen in the application
- Both voltage and temperature are exponentially related to CMOS Ioff currents
- These additional currents are ON TOP OF the increasing base power/current trends
- A true triple whammy!

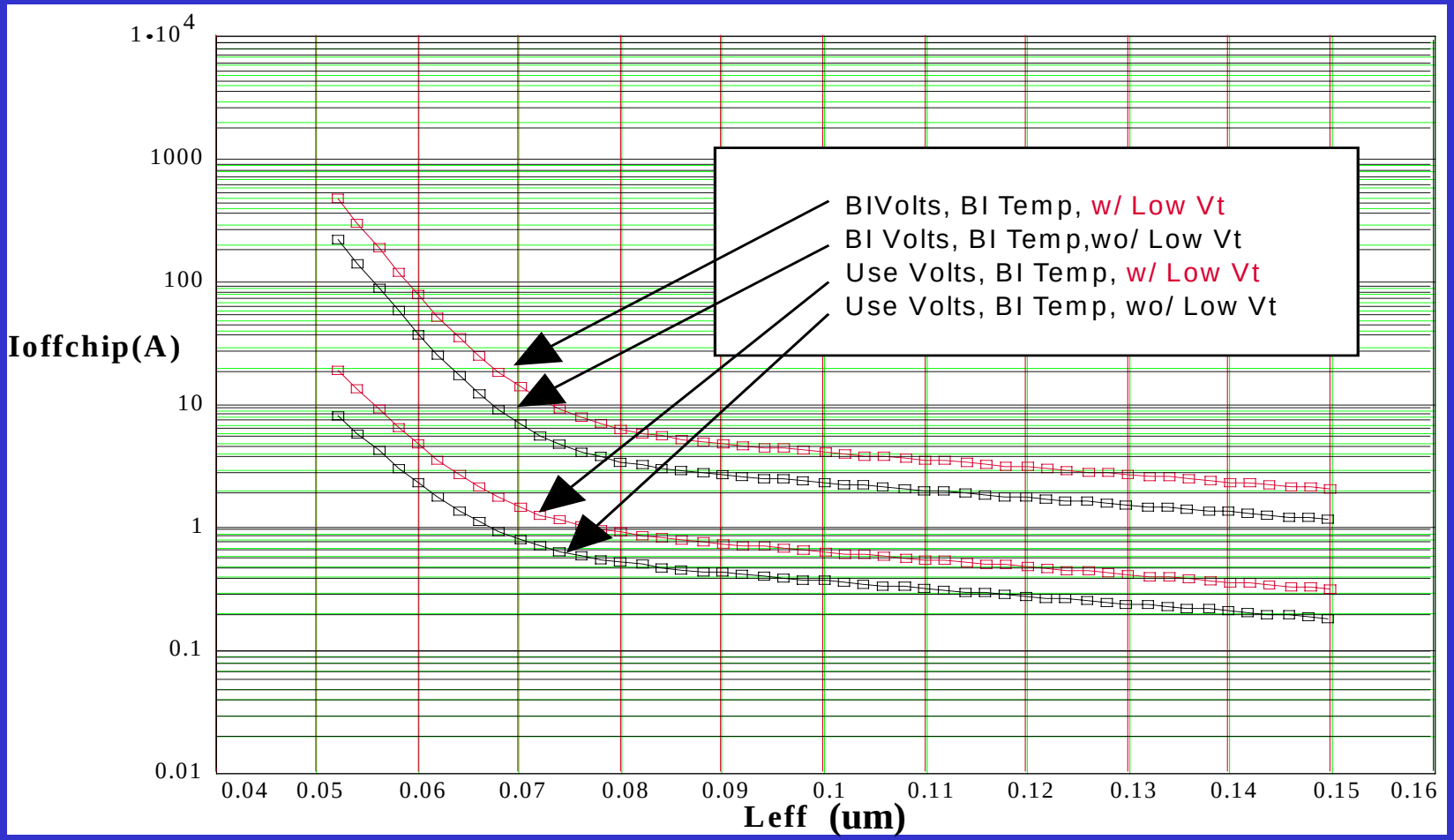
CMOS DC LEAKAGE Amps vs. Volts (multiple individual parts)



HOW DESIGN INFLUENCES POWER

- Both system and chip level design choices play a role
- Design choices are ultimately dictated by system requirements (power, reliability, speed, function)
- Historically, performance has been a key objective
- Power has become the counterpoint to performance
- Some examples of design influences/choices include:
  - Technology in use (SOI, Bulk, copper, low K, etc.)
  - Process centering (short = fast, long = slow)
  - Number of low Vt devices allowed
  - Oxide thickness
  - Power Distribution (Voltage islands)
  - System architecture (Clock throttling/gating, Pipeline depth, Compute informed power management)
  - System reliability (redundancy, ECC, FITs targets)

LOW Vt USAGE & LINE CENTER INFLUENCE ON STATIC POWER

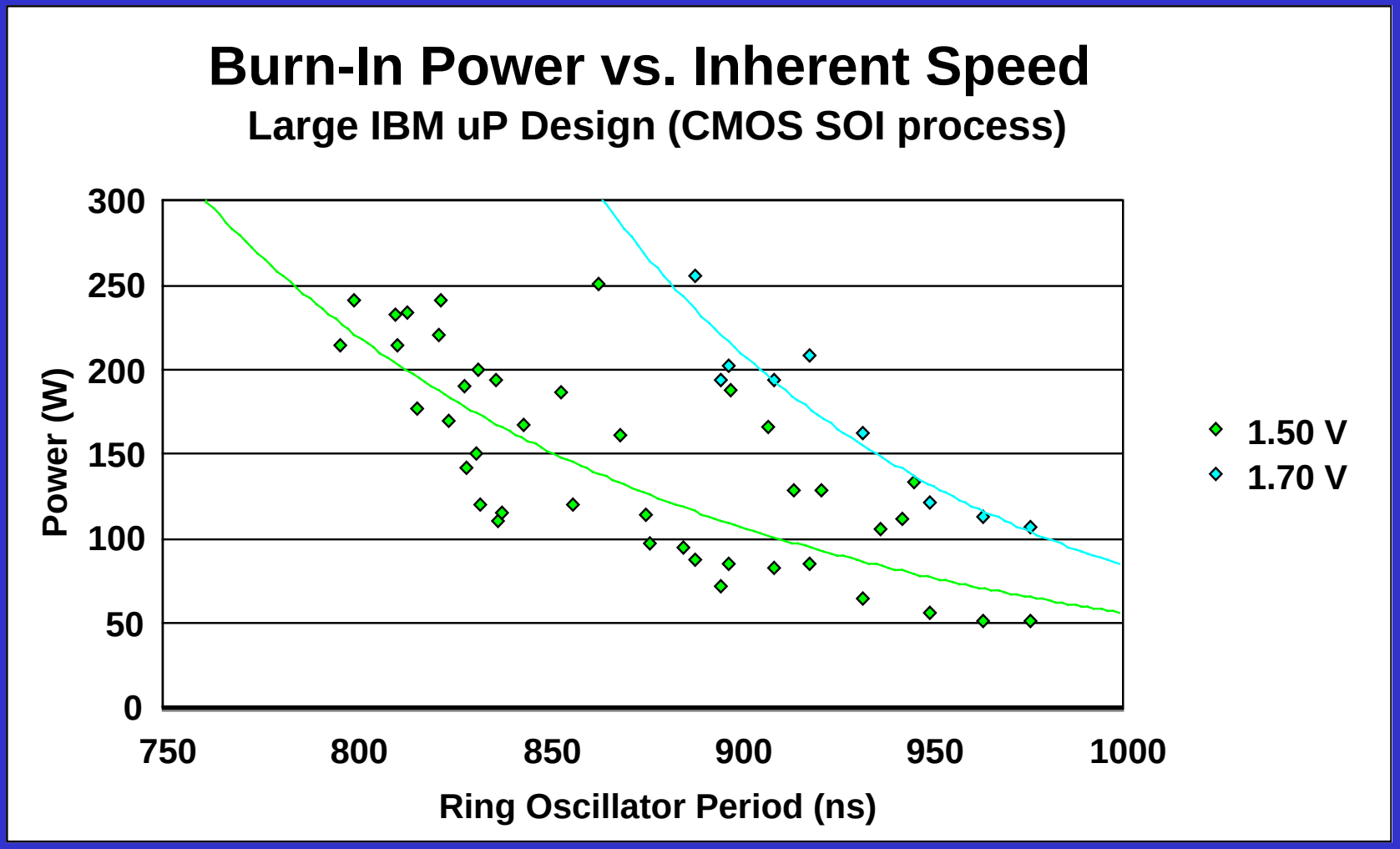


IBM 8S2 Processor model chart courtesy of Andreas Bryant, IBM

PROCESSING INFLUENCES IC POWER

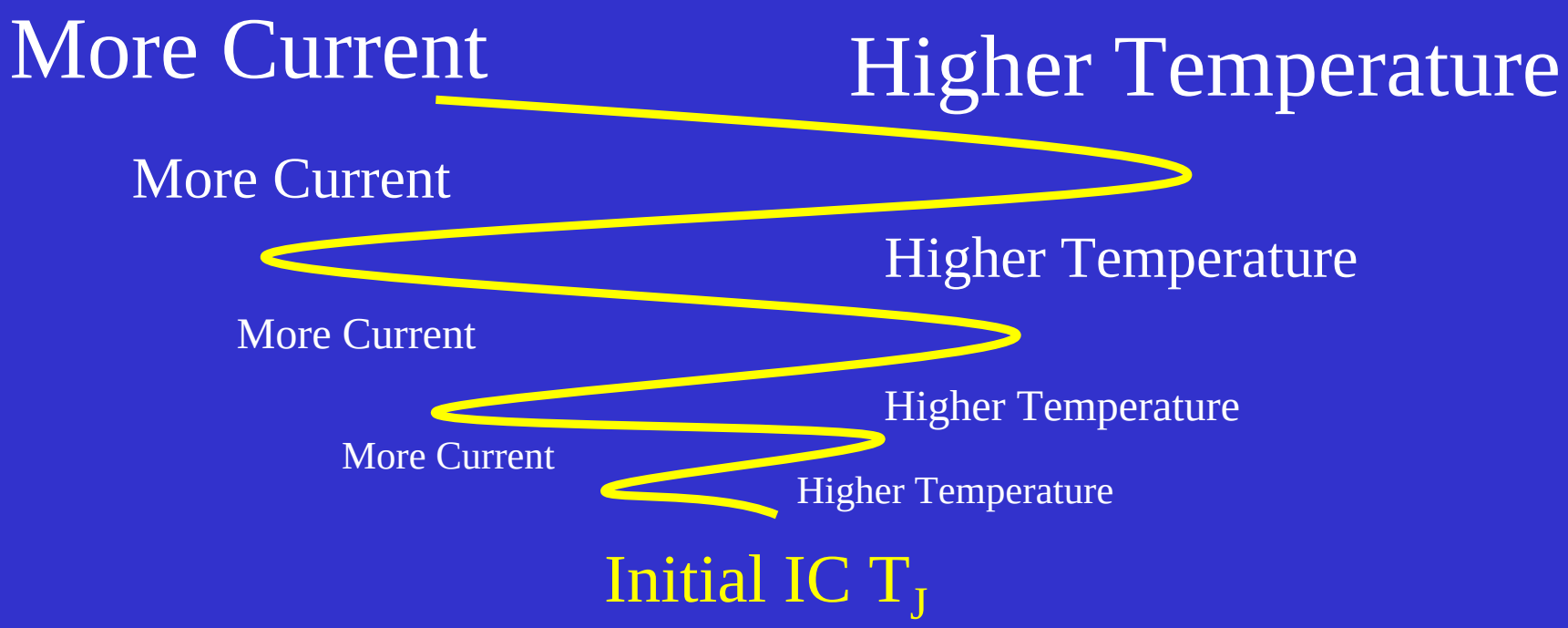
- All parts produced …….
  - in the same fabricator
  - on the same line
  - on the same tools
  - to the same process
- ……..are not exactly the same
- Deep submicron technology has large inherent processing variations
- Scaling dictates smaller dimensions and larger relative variations
- Power variation gets worse with conventional scaling
- Variations are amplified at accelerated conditions

SAME PROCESS PRODUCES WIDE RANGE OF SPEED/POWER

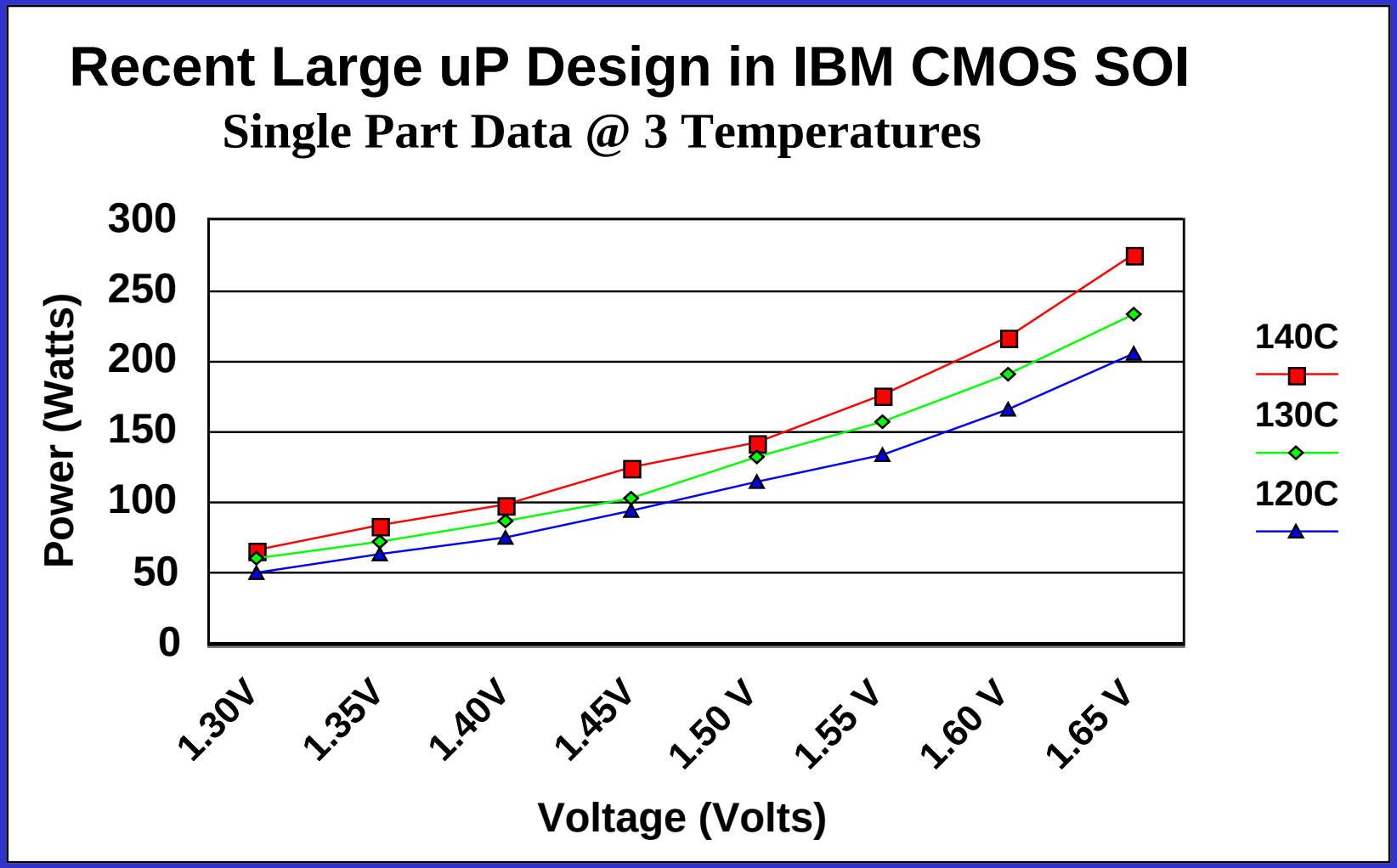


THERMAL RUNAWAY

- Thermal runaway is a positive feedback phenomena in which leakage current and temperature interact in an exponential fashion with each other



CMOS DC LEAKAGE POWER vs. TEMPERATURE



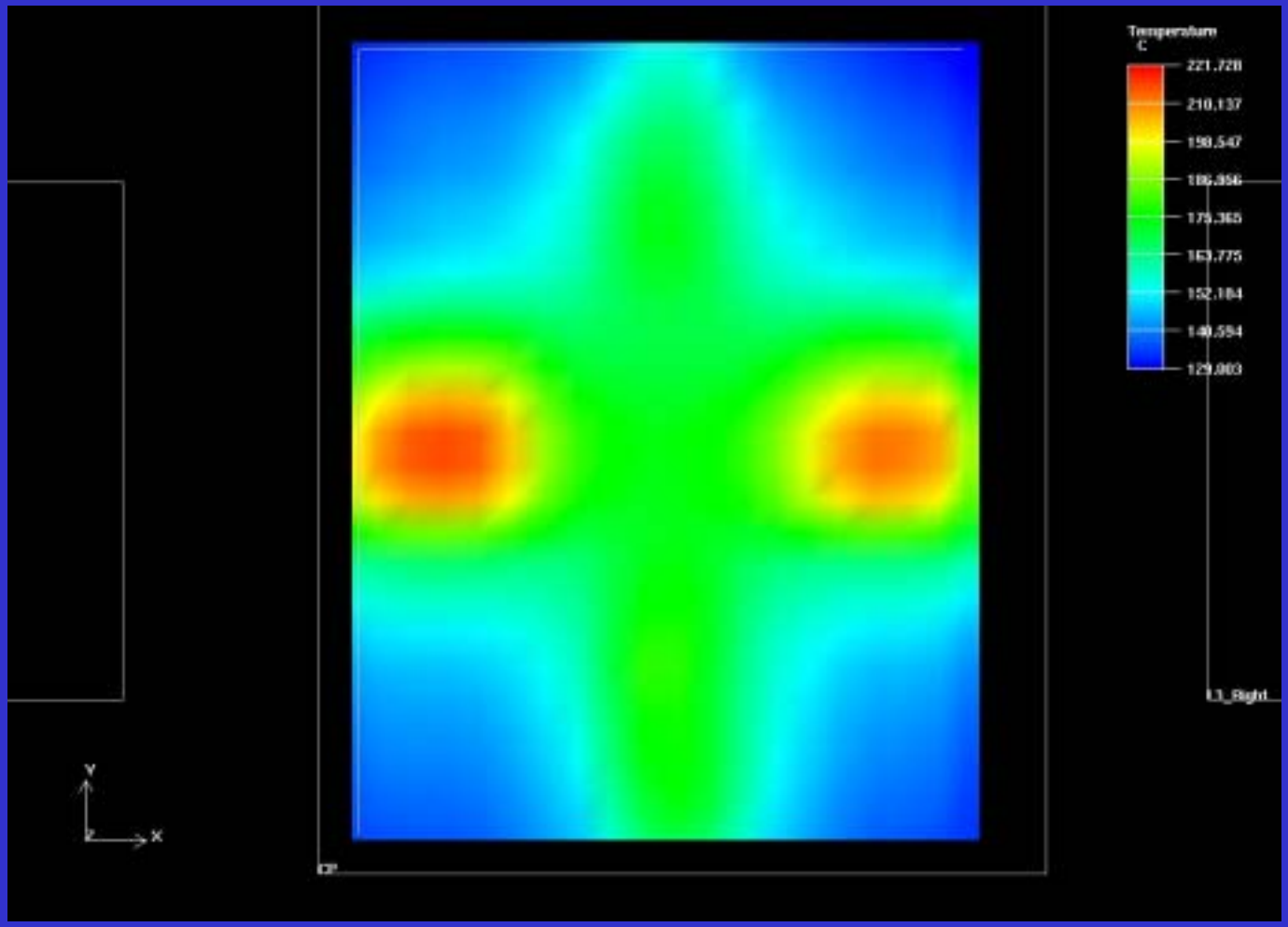
THERMAL RUNAWAY

- Thermal runaway is not necessarily attributable to a single root cause
- Thermal runaway contributors come from two interdependent categories of “influence”
  - Chip influenced
    - IC internal inherent characteristics and parameters
    - Design practices, circuit types, technology employed, line center, etc.
  - Tooling influenced
    - IC external environment and parameters
    - Thermal control, voltage control, thermal interface, etc.

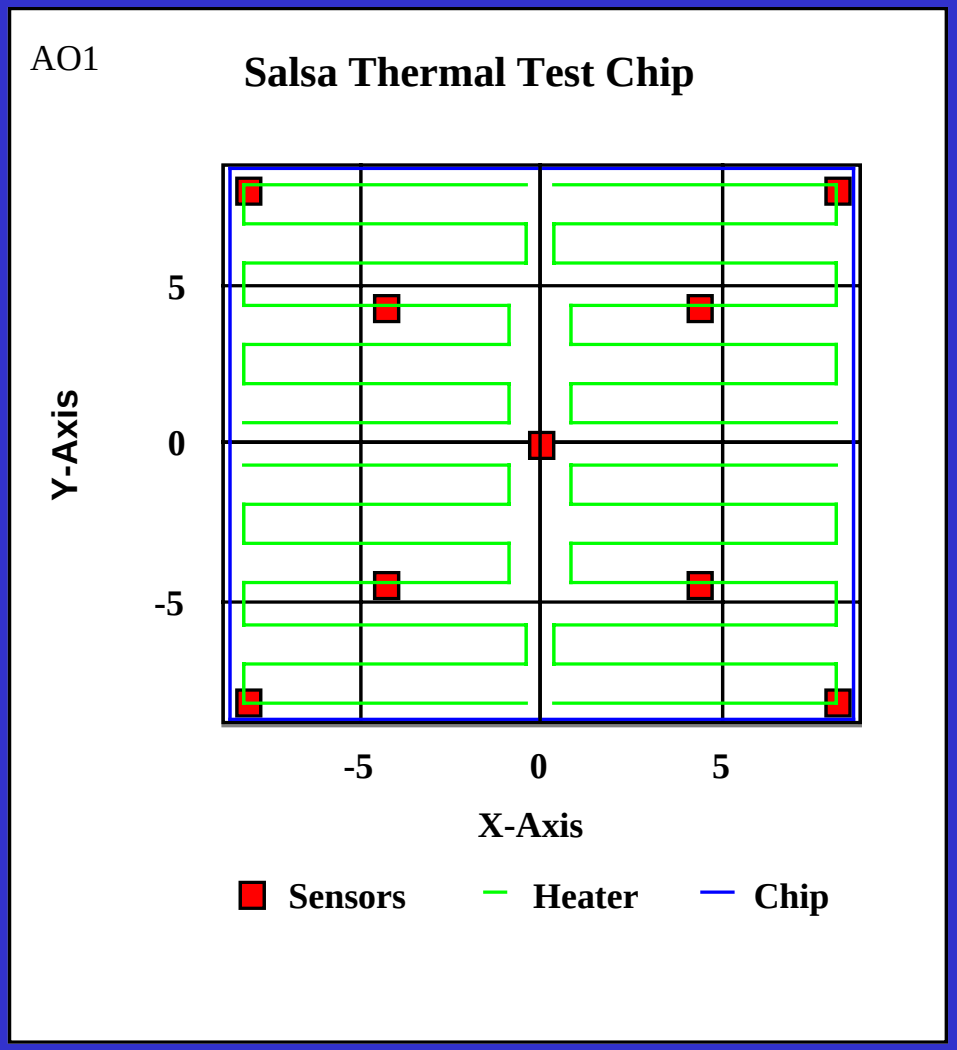
THERMAL RUNAWAY
CHIP INFLUENCES

- Chip influenced thermal runaway is more likely to occur with:
  - Short channel hardware
  - Minimum/sub-minimum ground rule design
  - SOI technology
  - Low Vt devices
  - Low K dielectric use (thermal – minor?)
  - Current dense circuit areas (hot spots)
  - Accelerated conditions

CHIP LEAKAGE HOTSPOTS
(microprocessor logic cores in this case)



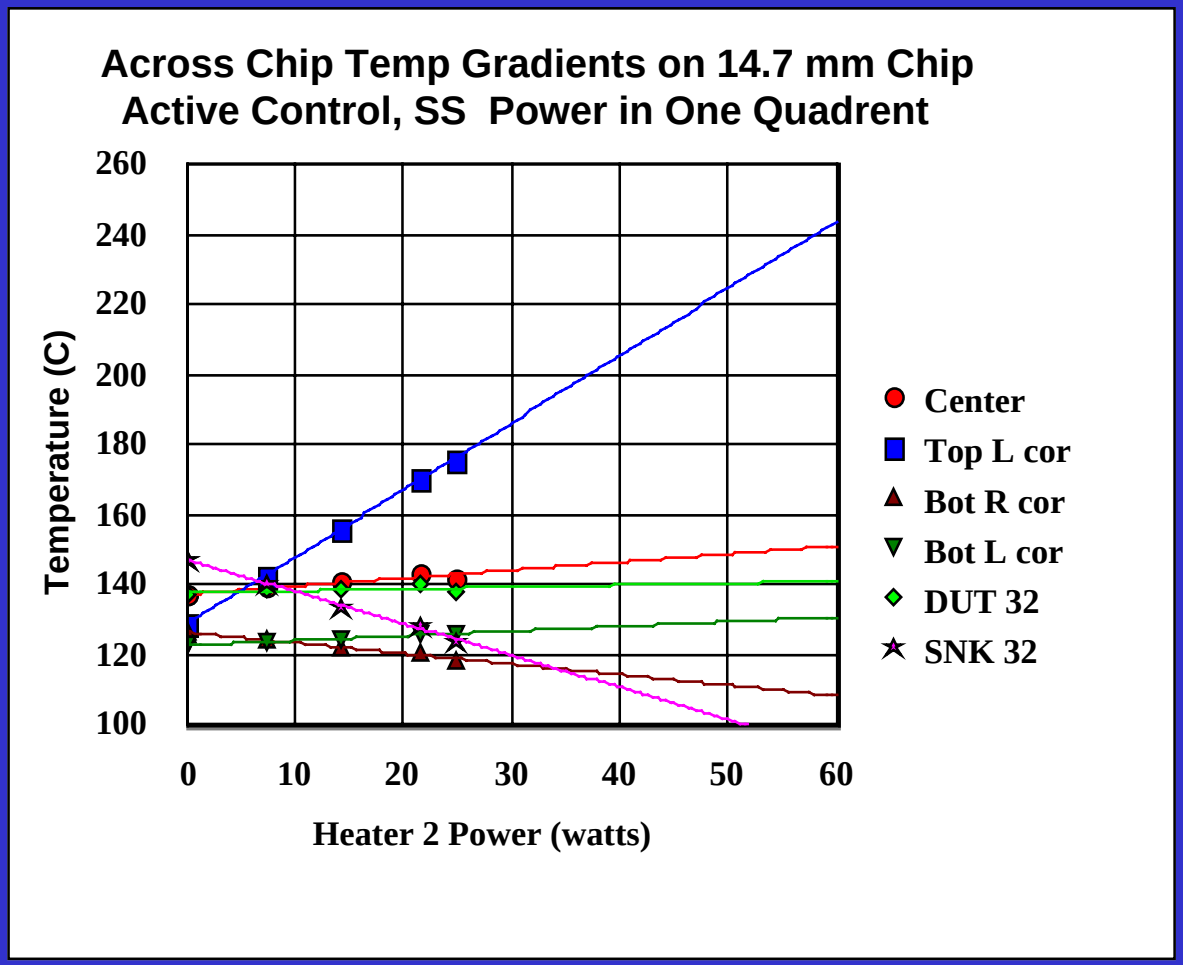
TYPICAL THERMAL TEST CHIP



- 9 temperature sensors
- Serpentine heater pattern (4 quadrants)
- Fabricated in multiple chip sizes
- Assembled in multiple packages/form factors
- Also used in wafer form
- Negligible I vs. T feedback (seen w/ICs)

Source [3]

POWER APPLIED TO ONE QUADRANT OF THERMAL TEST CHIP (Active Control Heat Sink)



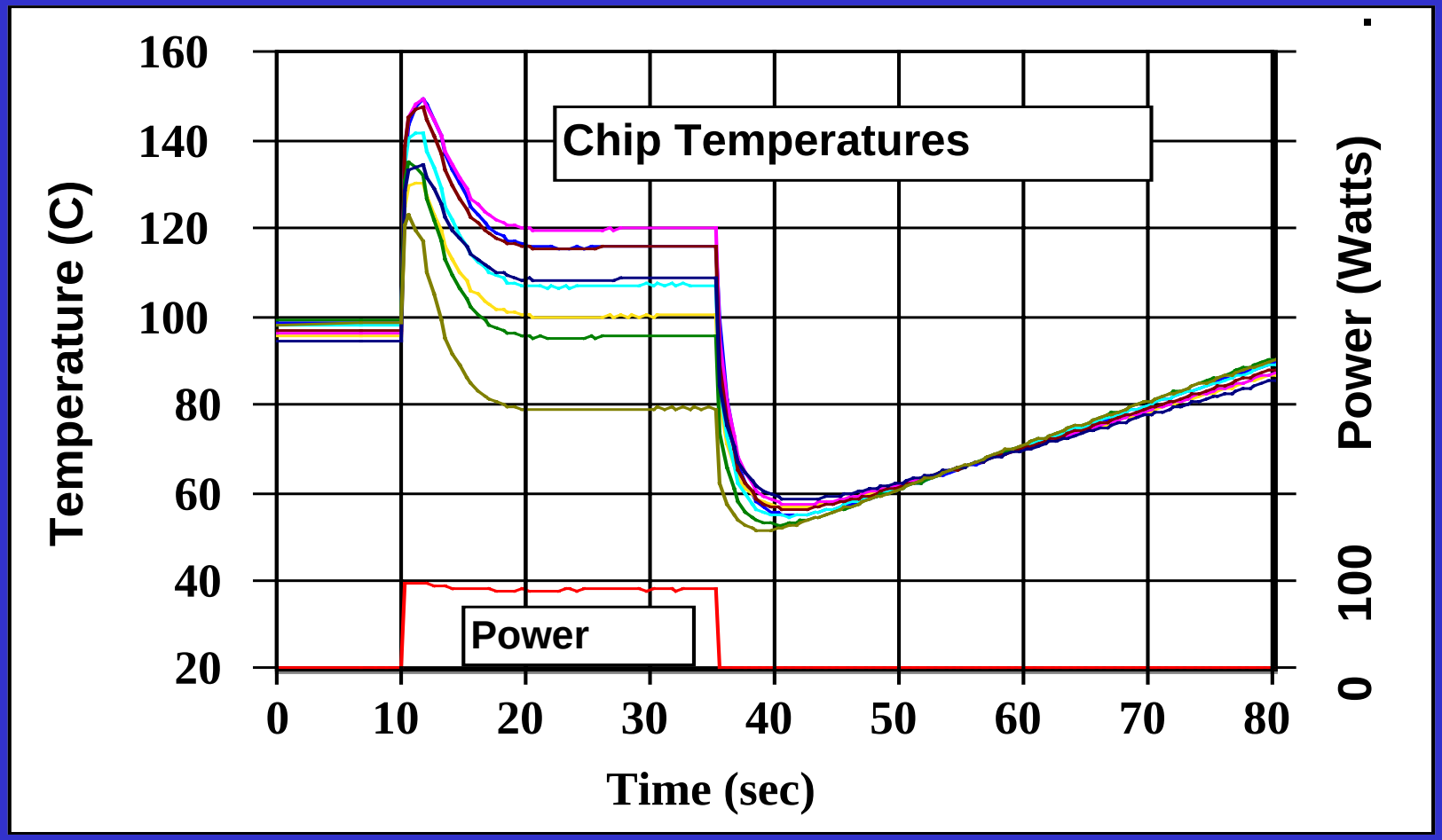
- Thermal test chip
- 4 independent quadrant heaters
- Heat sink temperature drops
- Center chip temp controlled to 140 C
- C-4's melt in corner of chip at only 50 W

Source [3]

THERMAL RUNAWAY TOOLING INFLUENCED

- Tooling influenced thermal runaway is less likely to occur with:
  - Tighter thermal control
  - Tighter voltage control (the slippery slope, p14)
  - Faster active thermal response OR slower power/thermal transitions
  - Temperature sensed at the hotspot
  - Improved thermal interface materials
    - Lower chip to heatsink thermal resistance
    - Lower thermal resistance point to point across chip

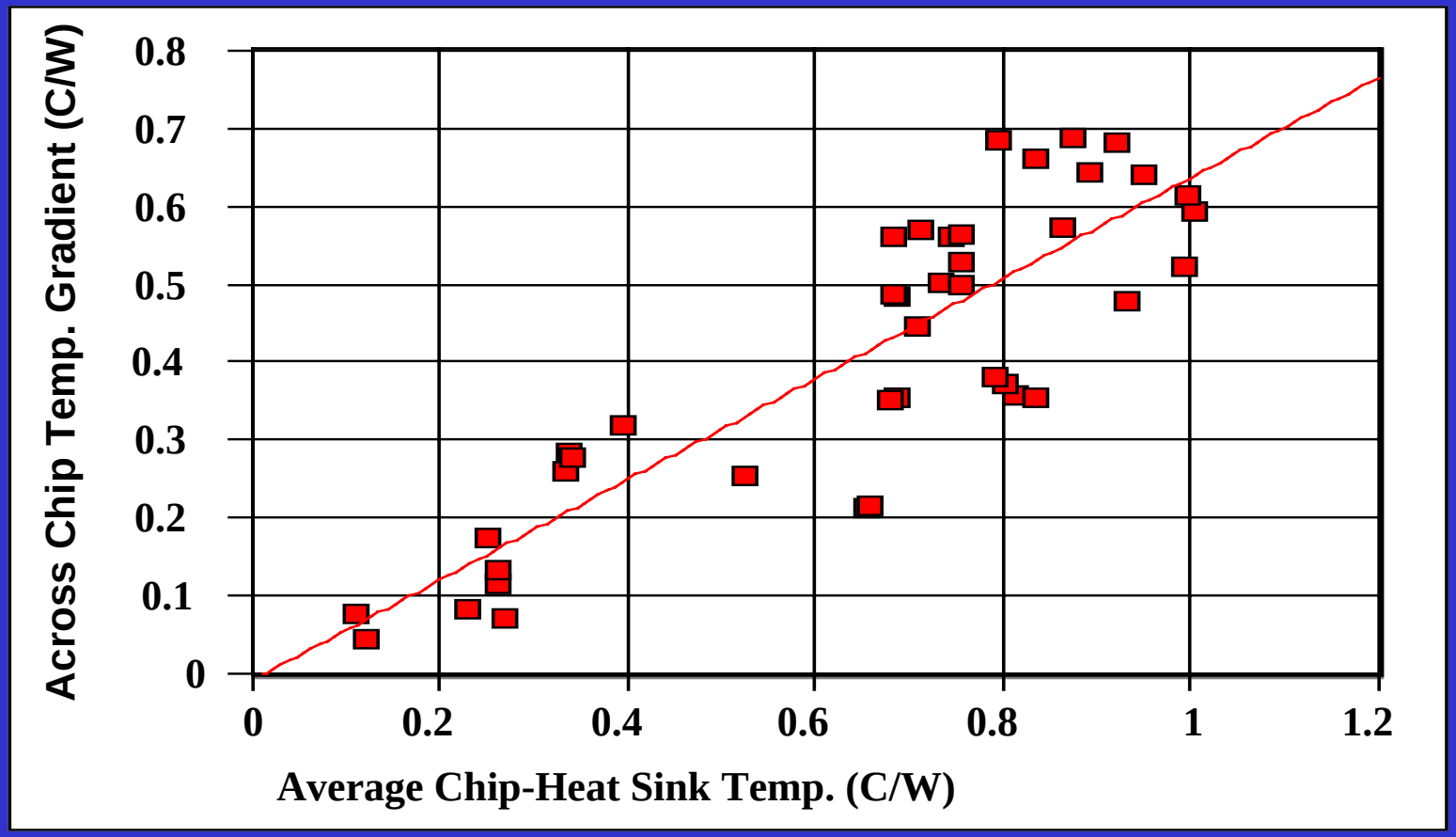
THERMAL RUNAWAY ACTIVE RESPONSE SYSTEM



Graph Shows Multiple Temperature Sensors Within the Chip with Uniform Power Applied

Source [3]

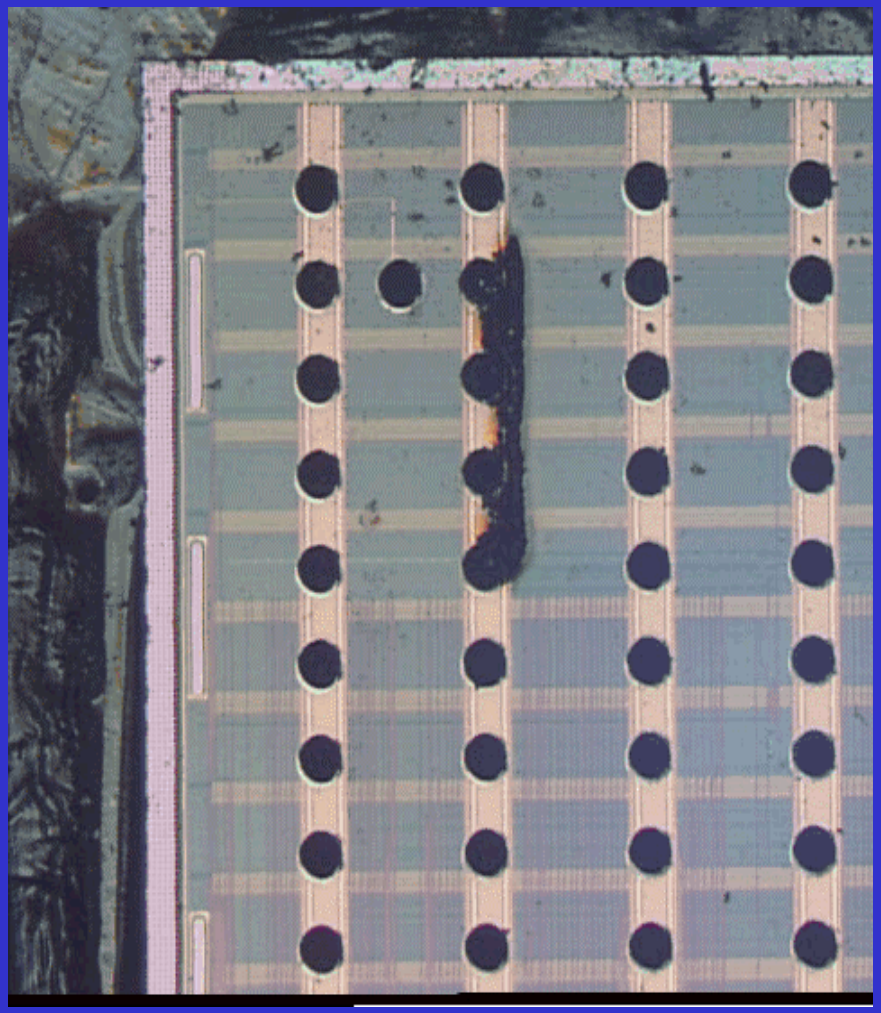
THERMAL INTERFACE INFLUENCE ON X-CHIP THERMAL



Graph Shows Multiple Thermal Interface Materials, all with Uniformly Powered Test Chip

Chart Courtesy of Dave Gardell IBM

THERMAL RUNAWAY



- View of damaged chip from C4 (solder ball) side
- Failure analysis photo
- Systematic damage on short channel parts @ BI
- Catastrophic damage above group of word line drivers (large devices)
- Solutions – lower BI conditions, power distribution changes on subsequent design pass

FUTURE TECHNOLOGIES
Will They Help?

Technology	Power Improvement Outlook	Time to Market
Low K dielectrics	Wires not scaling, attempts to keep wire delays from losing ground	1-2 yrs Hybrids in use
Strained Silicon	Improves mobility, allows performance improvement for similar leakage	1-3 yrs Low pwr apps 1st
Hybrid Crystal Silicon	Improves mobility, allows performance improvement for similar leakage	3-5 yrs
Double Gated MOSFETS	Improves Ioff characteristics, allows lower Ioff for similar performance	5+ yrs
High K Gate Materials	Improves gate leakage, allows thicker gate for same performance…less variation?	3+ yrs (Intel projection)

Author's Estimates

ACKNOWLEDGEMENTS

I would like to acknowledge the help and input received from my valued colleagues including:

Kerry Bernstein, David Gardell, Ronald Bolam, Roger Schmidt, Keith Stevens, Andreas Bryant, Brent Anderson

References:

- Semiconductor Industry Association, *International Technology Roadmap for Semiconductors*, 2002, Available Online @ http://public/itrs.net
- “Caution Flag Out, Microarchitecture’s Race for Power Performance”, Kerry Bernstein, 3 December 2003, 36th International Symposium on Microarchitecture
- “Temperature Control During Test and Burn-In, David Gardell, May 2002, Itherm Presentation

Reducing the Cost of Test in Burn-in - An Integrated Approach

Michael Noel
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Don VanOverloop

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MOTOROLA

Burn-in Limitations & Issues

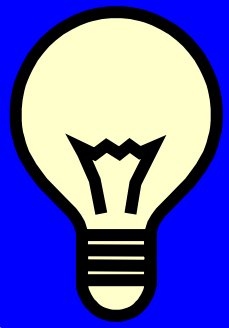
- **Traditional view**
  - **Reliability screening tool**
  - **Extra process, lots of hidden costs!**
    - Managing a variety of systems & solutions
    - Many systems are very specialized
    - Upgrades and updates are expensive, time consuming
    - “Black Hole” (product goes in, comes out later…)
    - Others….

How can we do this better?

Burn-in Limitations & Issues

- **Traditional approach**
  - **Hardware controlled drivers, possibly firmware programmed**
    - Allowed BIST, basic testing
    - Results and yields tracked manually
    - Large variety of drivers for variety of devices
    - Dedicated to specific devices and BI requirements
    - Met basic requirements
  - **Independent systems**
    - Different vendors
    - Manually operated
    - Supported Burn-in, but not much else

Burn-in Limitations & Issues



- **What if … we change our view?**
  - **Can we**
    - Simplify and standardize to reduce costs?
    - Do more types of functional testing during BI?
    - Perform value added processes during BI?
    - Upgrade equipment and technology in response to changing requirements?
    - Improve yields through better equipment tracking?
    - Track devices and processes better to reduce costs?
    - Track activities better to increase efficiencies?

Essential Elements

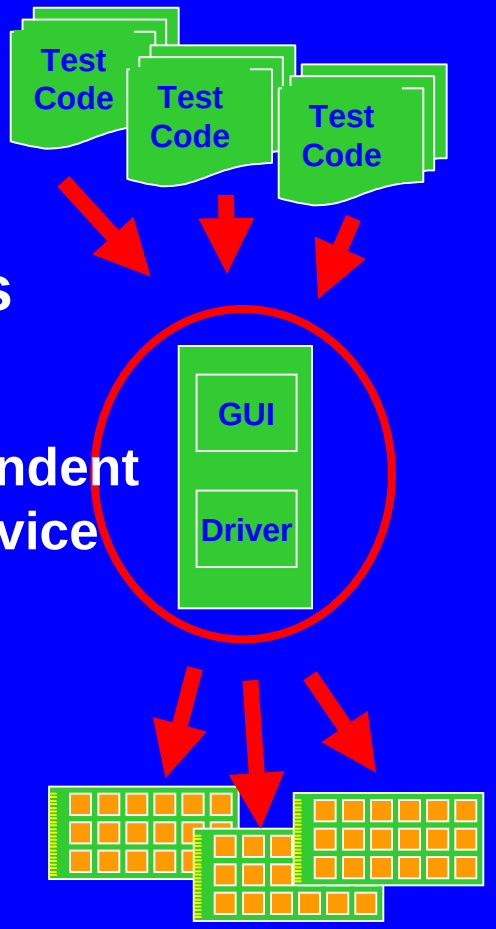
- **Computer controlled drivers**
  - **Hardware**
    - Generic
    - Skinny interface
    - Low Cost
  - **Software**
    - Real time control
    - Flexibility
- **User interface and supporting tools**
  - **Independent**
  - **Standardized**
  - **Simplified**

Essential Elements

- **Our approach - Integrated Burn-in Environment (IBE)**
  - **Computer controlled drivers**
    - CC1 – 3 pin synchronous SCI interface
    - CC2 – 2 pin asynchronous SPI interface
    - CC3 – BIST, SCI, SPI, BDM, Scan, JTAG
  - **System interface & network**
    - Graphical user interface (GUI) & driver controller (MBI)
    - Supporting tools (PM, Repair, Inventory)
    - Local networks in each site
    - Global network
    - Integrated production feedback

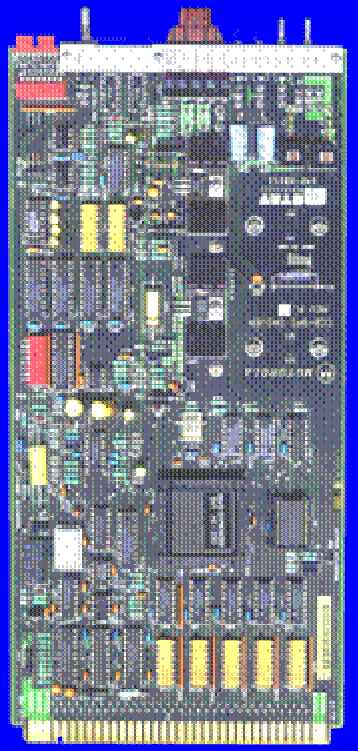
Essential Elements - Overview

- **System / driver interface**
  - Interface sends test code to driver
  - Driver sends to device
  - Device runs its own test code
  - Driver collects results/data from devices
  - Interface collects results from driver
- **This allows:**
  - Full slot independence
  - Test code is independent of interface & driver
  - Flexibility in device types supported
  - Driver hardware overhead is reduced
  - Drivers are generic



Essential Elements - Drivers

- **CC1/CC2 drivers**
  - **Pin compatible with existing (legacy) drivers**
  - **RS485 computer communications**
  - **Microcontroller and SRAM**
  - **SCI (asynchronous), SPI (synchronous) device communications**
  - **Functional tests ‘booted’ into device**
  - **Test results often stored directly into non-volatile memory for readout during final test**



Essential Elements - Drivers

- **CC1/CC2 drivers (cont.)**
  - **Interface acts as a debugger**
  - **Enables use of**
    - Device Phase Lock Loop (PLL) to multiply low frequency driver clocks
    - Device debug port for low frequency I/O interface
    - Driver CPU & computer interface with multiple downloads for minimal driver memory
    - Internal device capabilities
  - **Very low cost driver**

Essential Elements - Drivers

- **CC3 driver**
  - **Higher pin count interface with burn-in board**
  - **Synchronous, asynchronous, parallel interfaces**
  - **PPC & RAM based re-programmable logic**
    - Provides extremely flexible test capabilities
    - BIST, JTAG, SPI, DBM, CAN and SCI
  - **Programmed in C**
  - **Design of driver power supplies allows:**
    - Wide voltage range
    - High level of accuracy
    - Remote monitoring
    - Current sensing and limiting
  - **Low cost**

Essential Elements - Interface

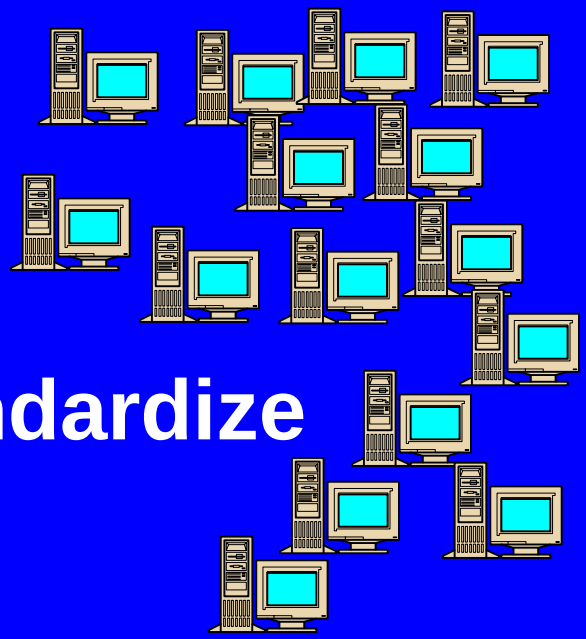
- **Driver controller (MBI)**
  - Developed in Visual Basic
  - Runs on standard Windows PC
  - Communicates to each driver independently (RS485)
  - Simple standardized interface
  - Controls oven temperature, process flow
  - Flexible data collection
  - Fully networked

Essential Elements - System

- **What does this get us?**
  - **Flexibility!**
    - Burn-in completely software controlled!
    - Drivers are device independent
    - Large testing flexibility
    - Massively parallel OTP & Flash programming
    - Reliability applications
    - Test and collect data real time
    - Change parameters quickly
    - Desktop development capability (need software and driver)

Hidden Costs - Support

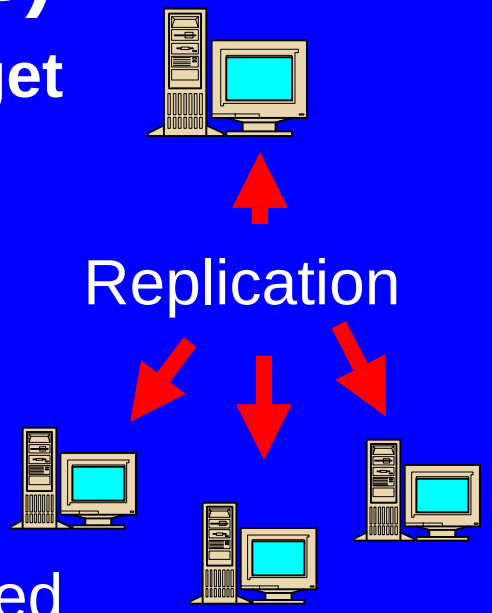
- **Problem… Support is a potential issue**
  - **Releasing program updates**
  - **Maintaining system configurations**
  - **Backups, administrative costs**
  - **Avoiding oven dedication…**



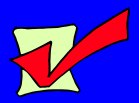
- **Solution… Network and standardize**
  - **Place all ovens on a network**
  - **Standardize configurations**
    - All controllers share “Exactly” the same software
    - All controllers have everything needed to run locally

Hidden Costs - Support

- **Workstations (oven controllers)**
  - **Replication - Ensures source and target are the same**
    - Enables automatic updates
    - Simplifies configuration
  - **Autonomy - Controllers run independent of network**
    - All software and configurations required for production are contained locally
    - Updated from server on regular basis

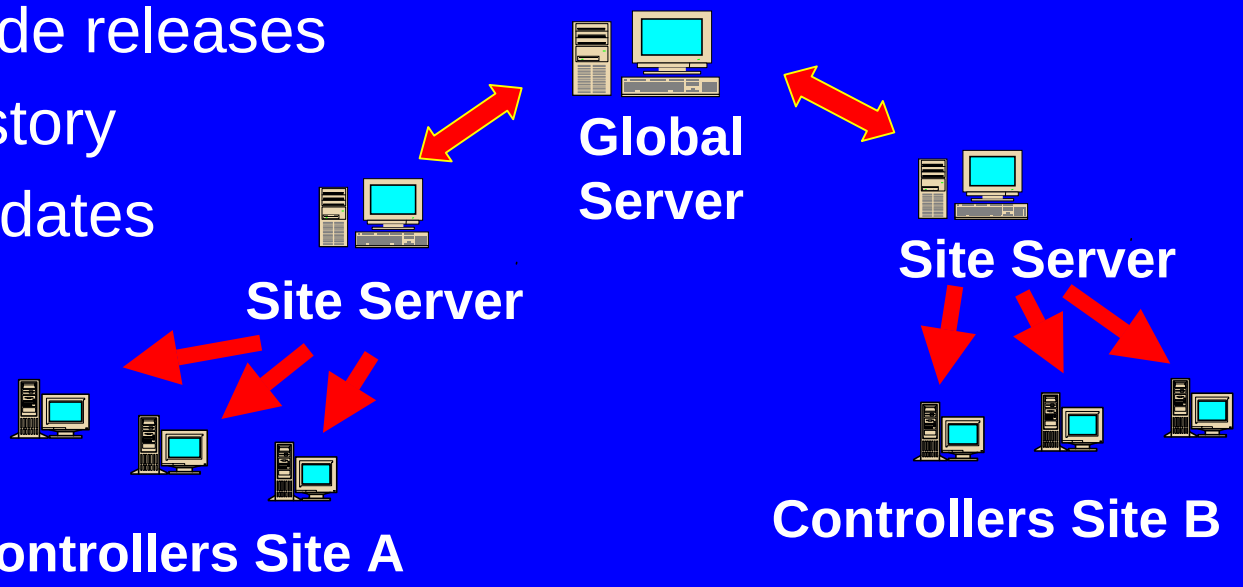


Hidden Costs - Support

- **Advantages of replication** 
  - **Lower management / administrative costs!**
    - “Swap Out” in case of failure
    - Device code updates automatically distributed
    - Full control of all systems from central location
    - Each controller always up to date
    - Full guarantee that all controllers are properly configured and have correct software
    - Ovens do not need to be dedicated to a product!
  - **Disadvantages** 
    - Updates too quick (when product running?)
    - Some changes impact all systems adversely

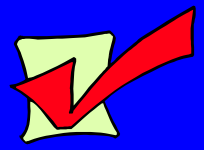
Hidden Potential - Network

- **One step further… Global network**
  - **Site data replicated to primary "World" server**
    - Global visibility – data for all sites in one location
    - Redundancy - data is always in two places!
  - **Item information replicated to all sites**
    - Global code releases
    - Global history
    - Global updates



Hidden Potential - Network

- **Advantages of a global system**



  - **Support**
    - Near-instantaneous world code release
    - Standardized capacity planning
    - Simplified product transfer
    - Global equipment tracking
  - **Visibility**
    - Monitor activity in multiple sites
    - Centralized data collection
    - Real-time access of any server / workstation

Hidden Potential - Network

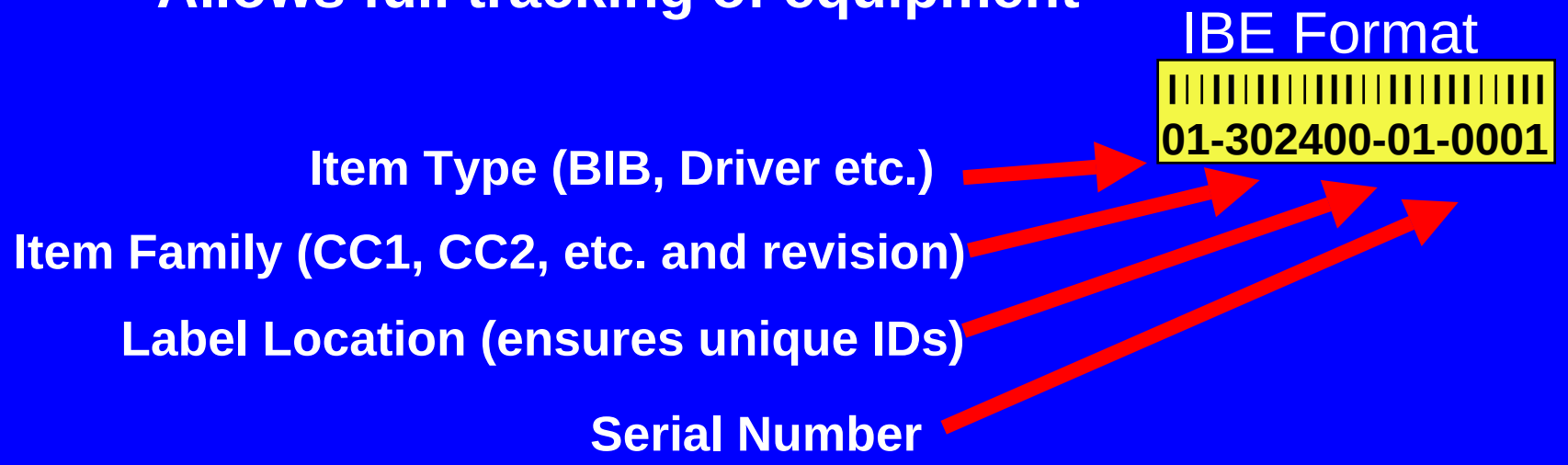
- **Not all is great…**
  - **Different sites may have different procedures**
  - **Same device may have multiple valid recipes in different sites**
  - **Code release may be too fast (other systems may need updates)**
  - **Time zones may impact some updates**

Other Opportunities

- **Additional opportunities**
  - **Build intelligence into the system!**
    - Real time process feedback
    - Equipment yield analysis
    - Equipment failure analysis
    - Integrated process results
  - **The real question**
    - How do we help the operators increase yields and quality?

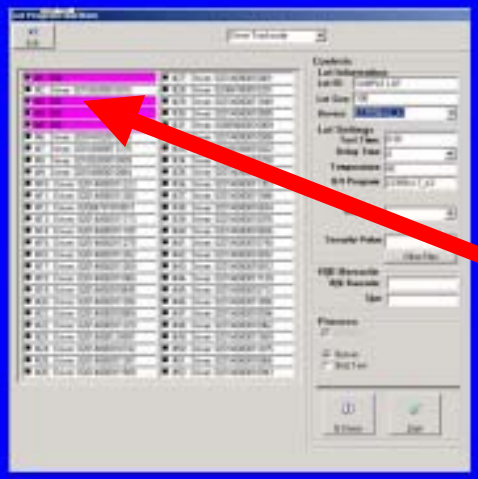
Other Opportunities

- **Barcodes**
  - **Everything gets barcodes**
  - **Data stored in database for each site and in global database (SQL)**
  - **All items globally visible**
  - **Allows full tracking of equipment**



Other Opportunities

- **Keep low overhead for system input**
  - **Operator scans lot ID & device type, assigns BIB to slots with scanner**
  - **System now knows**
    - Oven
    - Lot detail
    - Operator
    - Driver
    - Device
    - Recipe for process
    - Slot detail



Slot, Device and Burn-in Board assignments made with scanner at load time

Operator scans lot and board then slot to make assignments

All other process details collected and monitored by system!

Other Opportunities

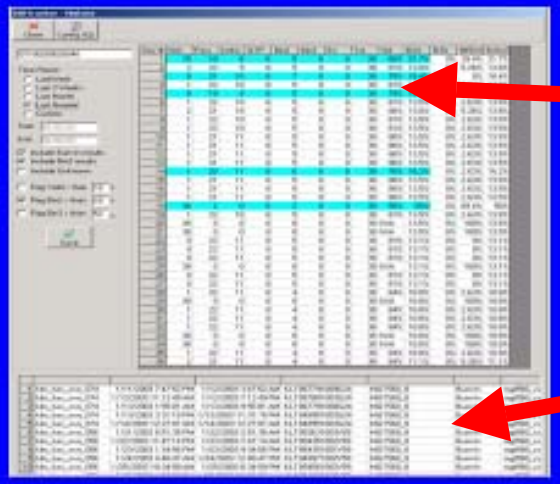
- **Site Monitor**
  - Monitors oven status within entire site
  - Lots loaded, lot status, slots used
  - Configuration, connection status
  - Remote control for support
  - Event notification (high failure rates, adverse events)

Oven has warnings (events)
Oven is running properly
Network connection has been lost

Detail – Lots currently running

Other Opportunities

- **Real-time feed back**
  - **All history available to all workstations**
    - **As burn-in boards are used, system automatically checks recent history for patterns of failures and notifies the operator so problems can be addressed**
    - **History can be checked at repair or maintenance stations**

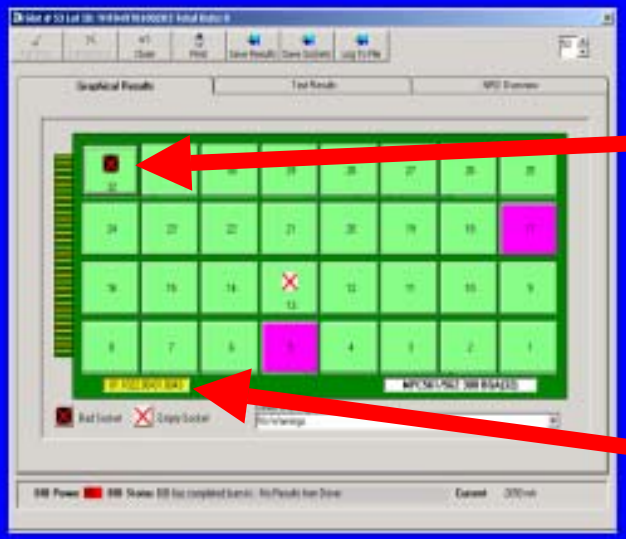


Socket positions meet flag condition, > 15% Bin2 failure in this case

Recent board history by lot

Other Opportunities

- **Track information real-time**
  - **Sockets can be “electronically” marked at repair, PM or during production**
  - **When BIB is used, socket is “flagged” to operator**



Remove part! The socket has failed in the past even though the socket check shows the part.

Barcode tells system what board layout and type are

Current Status

- **Current status…**
  - 400+ ovens in several sites
  - Majority of microcontroller burn-in at Motorola uses IBE
  - 3 drivers running several hundred different device types
  - CC4 driver being developed
  - Inventory, repair tracking, maintenance all integrated
  - Burn-in reductions based on production detail
  - Device qualification completed using the system
  - Factory OTP / flash programming with customer specific code
  - Yield trends by site, system, device, board, driver
  - Data mining (e.g. board performance by socket type)
  - One step reliability and characterization

One More Thing…

- **This entire system was developed internally**
  - **The entire team deserves thanks for their efforts in designing and implementing this system**

  - Dan Wilcox
  - Doug Grover
  - Chris Harner
  - Bill Bishop

0.4mm Compression Mount BGA Burn-in Socket, Another Breakthrough in Socket Technology

Helge Puhlmann
Kazuhiro Matsuda
Jec Sangalang
YAMAICHI ELECTRONICS GROUP

BiTS
BURN-IN & TEST SOCKET WORKSHOP

March 7 - 10

Overview

- Basic Requirements
- Burn-in Board interfaces and technology gaps
- Introduction to different methods for contacting a 0.4mm fine pitch BGA device
- Identification of current contact technology difficulties
- Discussion of potential solutions
- Conclusion

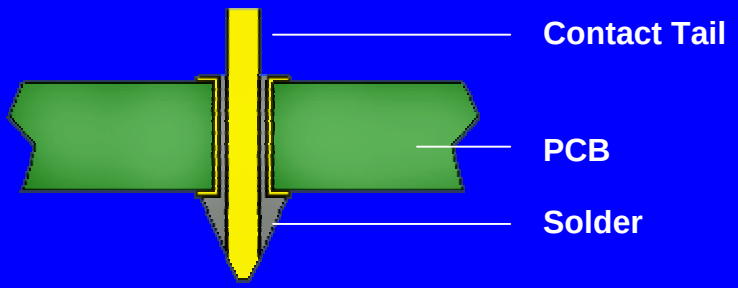
Considerations in the Development of a 0.4mm Fine Pitch BGA Socket

- Reliable alignment features
- Good contact system
  - Can deal with different ball sizes and ball composition
  - Minimized witness marks on ball
- Reliable manufacturing techniques
  - For metal contacts
  - For plastic parts
- Burn-in board manufacturability
- Cost effectiveness

Burn-in Board Interface

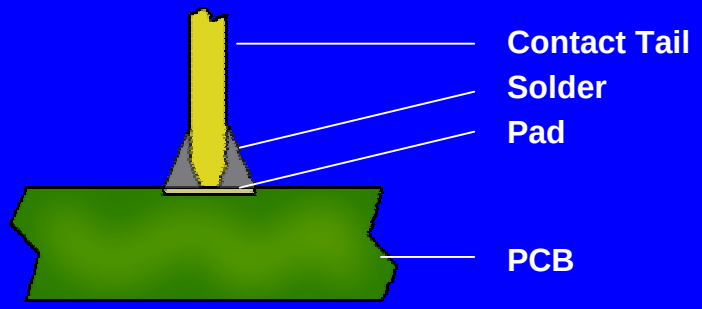
Pin Through Hole

Contact Tail is inserted in a plated through hole and soldered.



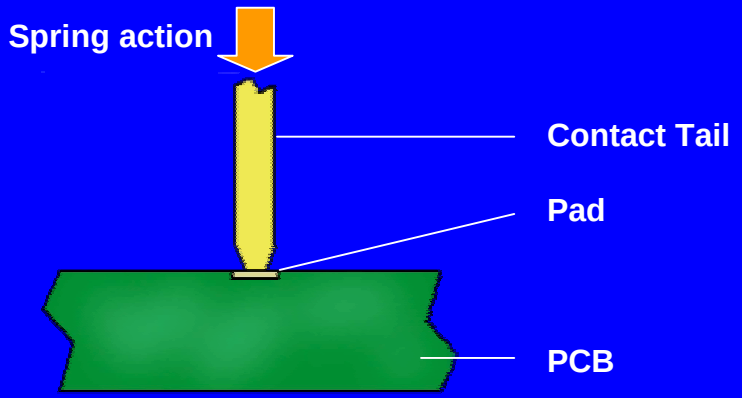
Surface Mount

Contact Tail is soldered onto a pad on the board.



Compression Mount

Contact Tail is pressed onto a pad on the board by a spring action.

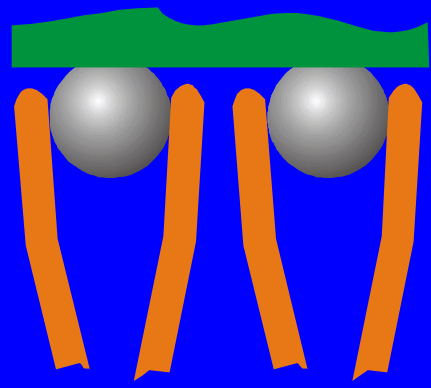


Gaps on Burn-in Board Interface

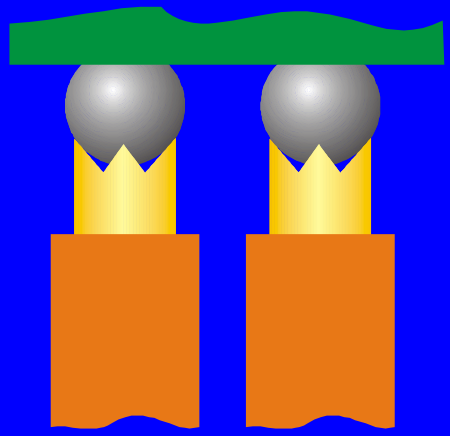
- Restriction on line and spacing for direct mounting (PTH, SMT or CMT)
  - This is a major Show Stopper for the development of a direct mount 0.4mm pitch socket
- Requires an interposer card to fan-out from a 0.4mm pitch.
  - This would incur extra cost
  - Influences the reliability

Different Methods of Contacting a 0.4mm Fine Pitch BGA Device

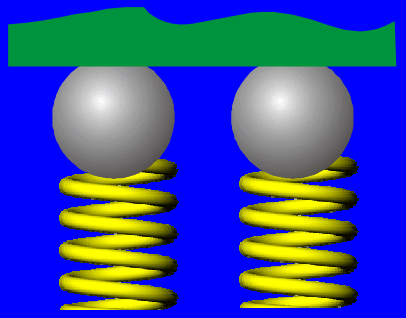
Tweezers Style Pin



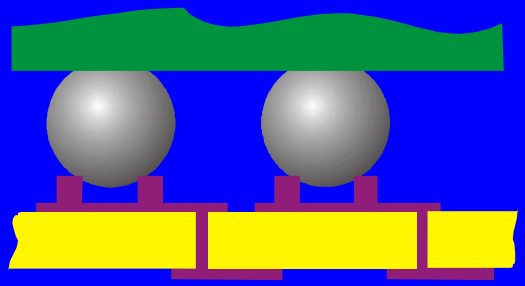
Spring Probe



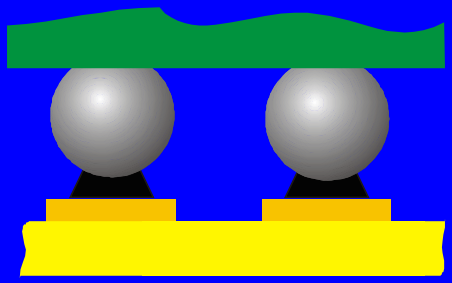
Helical Spring



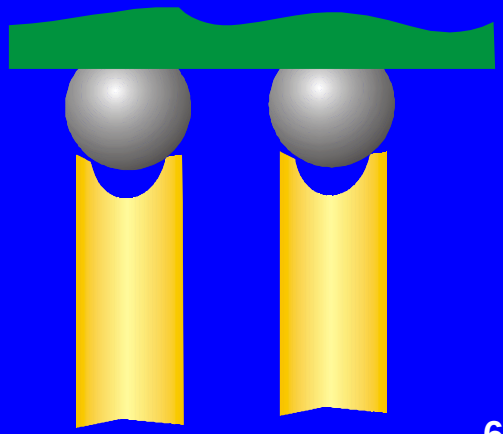
Plated Bump



Conductive Polymer

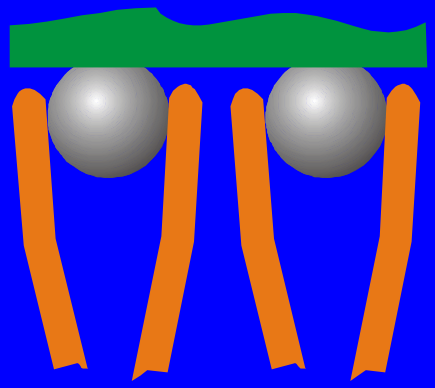


Buckling Beam



Current Contact Technology Gaps

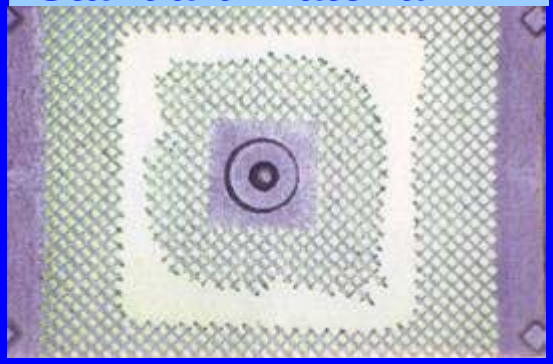
Tweezers Style Pin



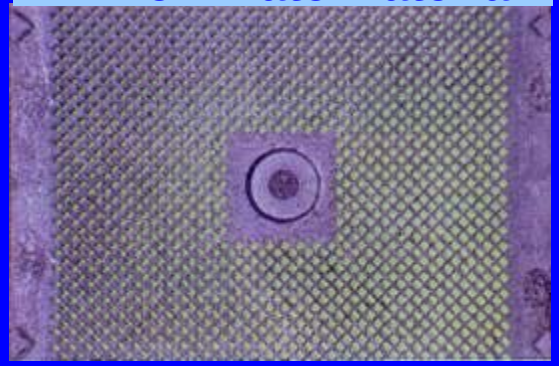
Tweezers Style

- Horizontal actuation causes limited space for contact beams
- Issue on moldability of plastic parts due to very thin wall thickness (about 5 mils)

Standard Material

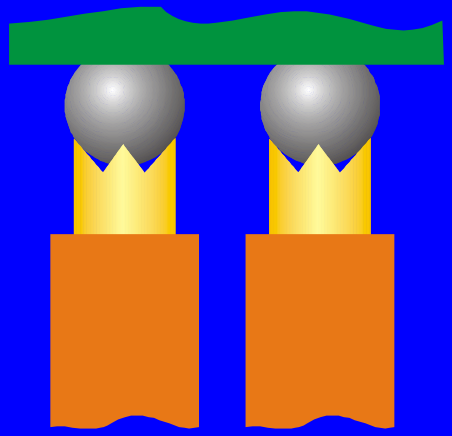


Hi Flow Rate Material



Current Contact Technology Gaps

Spring Probe



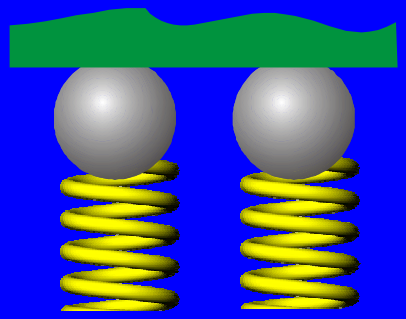
Pogo Pin

- Not cost effective for Burn-in applications

- Manual assembly constraint due to small size

Current Contact Technology Gaps

Helical Spring



Helical Spring

- Long electrical path causing a trade-off in electrical characteristics

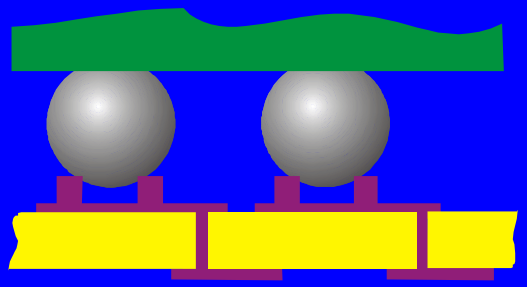
- Oxidation / contamination on PCB pad

- Damages ball geometry

- Sticking issues

Current Contact Technology Gaps

Plated Bump



Plated Bump

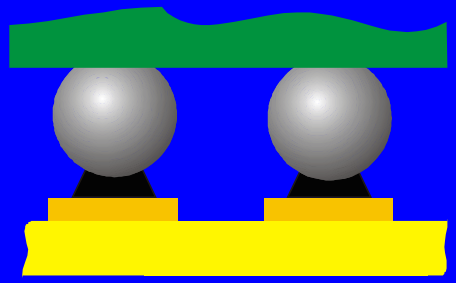
- Requires precise alignment

- Coplanarity concern

- Strong abrasion

Current Contact Technology Gaps

Conductive Polymer

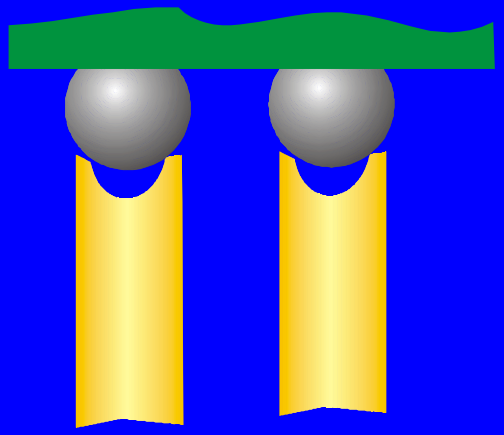


Conductive Polymer

- Requires precise alignment
- Contamination concern
- Touches the solder area
- Sticking issues

Current Contact Technology Gaps

Buckling Beam



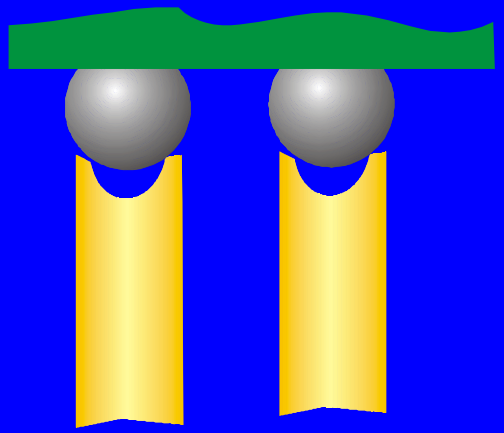
Buckling Beam

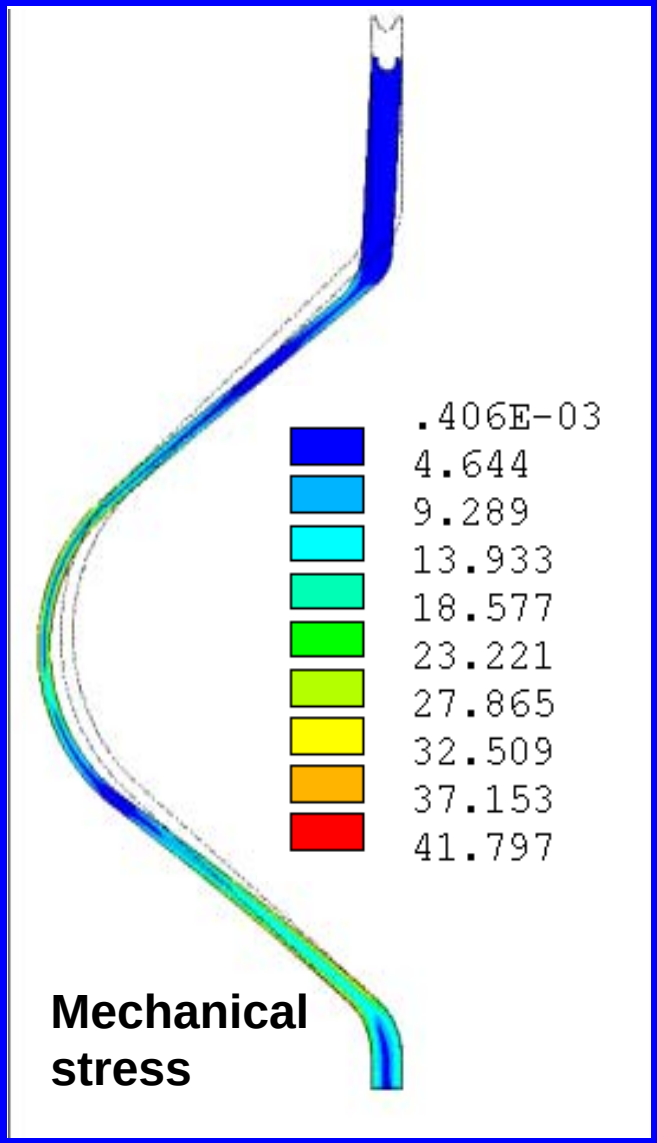
- Does not require much space because it is vertically actuated

- Less contact pin surface and longer pin length cause a slight trade-off in electrical properties
(resistance, inductance and current carrying capacity)

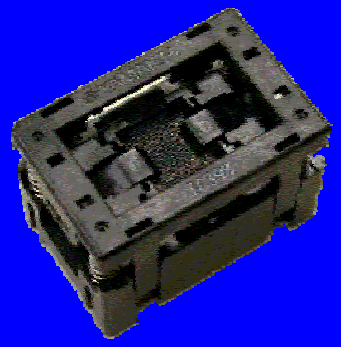
Current Contact Technology Gaps

Buckling Beam





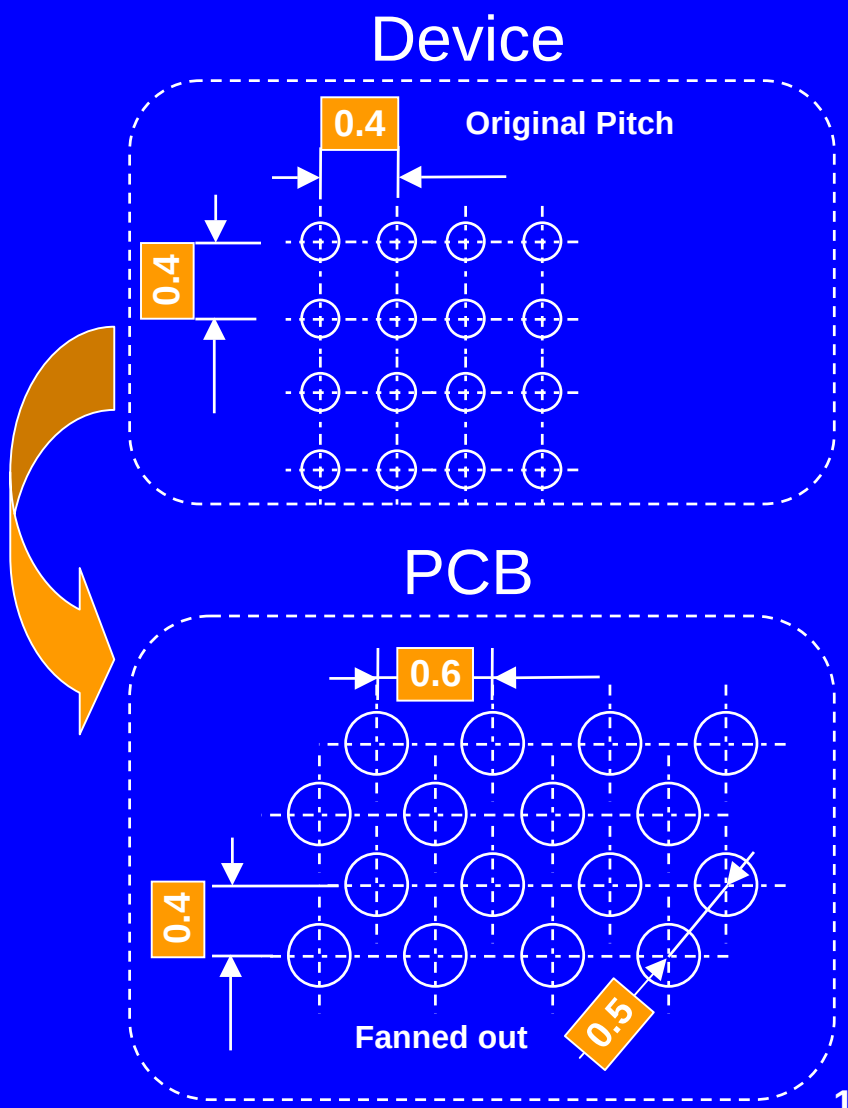
Why a Fan-out Solution for 0.4mm ?



- Enables manufacturability of boards
  - Fanned out pitch allows more space for routing traces
- Cost Effective
  - Eliminates the need for an interposer card
- Reliable
  - Allows extension of already proven socket technology

A Potential Solution

This will be achieved with a fan-out from 0.4 x 0.4mm ball-to-ball pitch to an interstitial pitch of 0.4 x 0.6mm PCB pads for a direct compression mount socket.



Conclusion

- Due to an increasing market demand for further shrinked and multifunctional applications, customers and suppliers have to stick together to develop smart and cost efficient contacting solutions.

- One of the most promising solutions is to adapt additional functionality to a socket.

That’s the way to shape **OUR** future.

Acknowledgement

My special thanks apply to

- Christian Kaemmerlen TI Europe
- Yamaichi Engineering Team Japan
- Yamaichi Engineering Team USA

and all the colleagues that participated in putting this presentation together

Any Questions?

Thank you for your attention