Burn-in & Test Socket Workshop

March 2 - 5, 2003
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

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Burn-in & Test Socket Workshop

Technical Program

Session 5

Tuesday 3/04/03 1:00PM

Thermal Management Techniques

"Thermal Interface Materials: An Implementation Process (From Cradle To Grave)"

Marc Knox - IBM Microelectronics **Qifang (Michelle) Qiao** - IBM Microelectronics

Tuknekah Noble - IBM Microelectronics **Yvan Cossette** - IBM Canada Ltd.

"Characterization Of A Thermal Control Unit Using Various Thermal Enhancers"

Jihad Y. Hammoud - Kulicke & Soffa Interconnect, Inc.

Anand V. Reddy - Intel Corporation

"Least Volume Optimization Of Finned Heat Sinks For Burn-In Air Cooling Solutions"

Patrick E. Phelan - Arizona State University **Zhaojuan (Jane) He** - Arizona State University

"Thermo Electric Coolers, Are They For Everyone?"

Giray Kaya - Reliability Incorporated

THERMAL INTERFACE MATERIALS

AN IMPLEMENTATION PROCESS

(from cradle to grave)

Yvan Cossette – Bromont, Canada

Marc Knox – Burlington, VT

Tuknekah Noble, Michelle Qiao – East Fishkill, NY

IBM Microelectronics

INTRODUCTION

- Power at burn-in and test is a first order challenge of today
- All indications are that power challenges will continue to grow
- Thermal interface materials can provide leverage against these challenges
- Finding materials ideally suited to the test and burn-in environments can be difficult
- Introducing new materials into production may not be straightforward

THERMAL INTERFACE MATERIALS

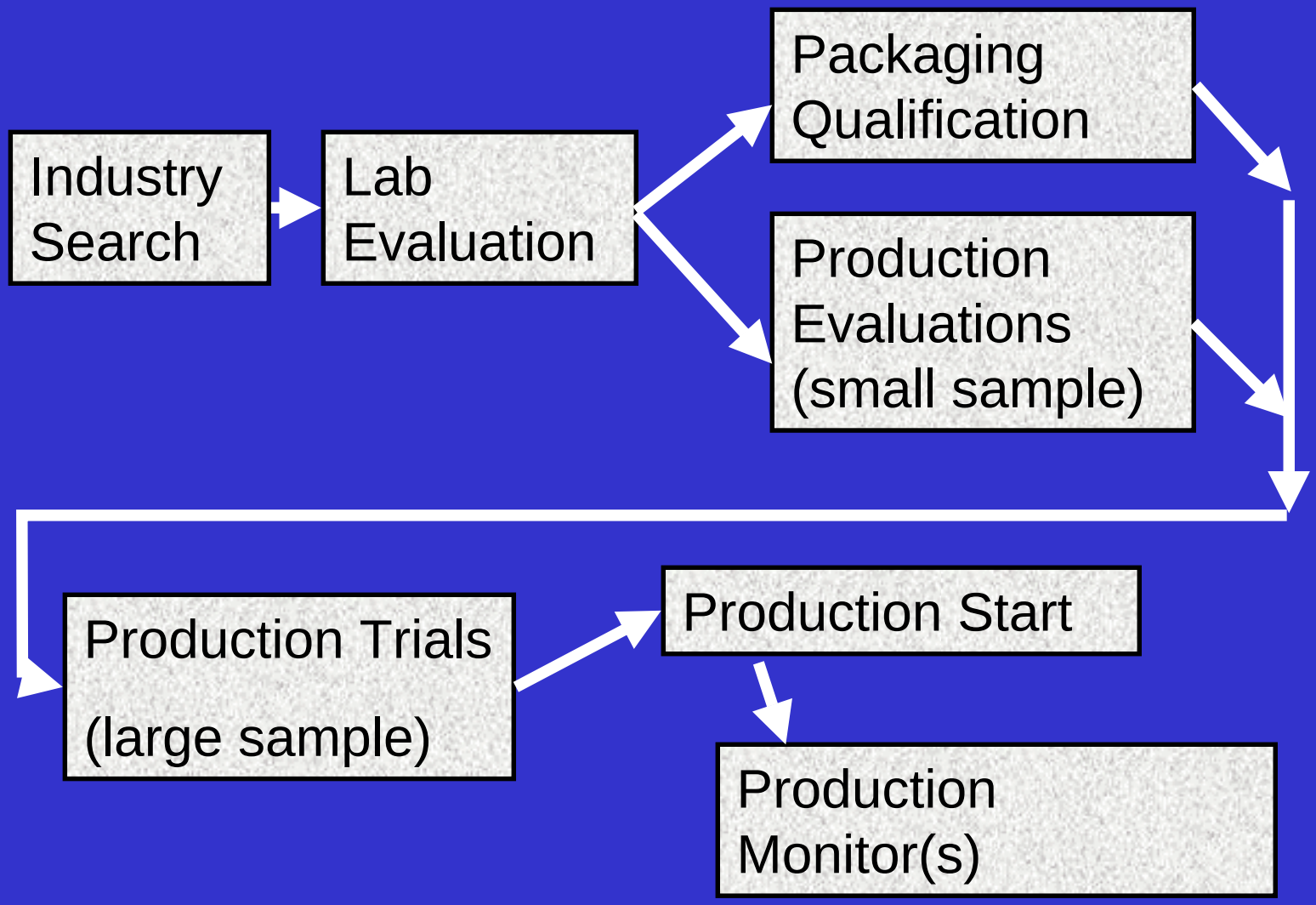
- Motivations for use may include:
  - Thermal Performance
  - Compliance (chip damage reduction)
- Various materials with a wide range of properties available
- Most materials are not suitable for temporary contact (test and burn-in)
- Material is typically applied between a heat sink and a bare die

INTERFACE PROJECT BACKGROUND AND OBJECTIVES

Interface project goals are:

- Eliminate chip size dedicated hardware
- Improve manufacturing efficiency/flexibility
- No downstream process impacts
  - clean, dry chip after processing
  - no detriment to packaging
- Thermal performance at least equivalent to plan of record

IMPLEMENTATION PROCESS



INDUSTRY SEARCH

- A consultant was used to search commercial TIM fit for application in Burn In & Test socket
- Search criteria: θ_{TIM}, cleanliness, compliance, durability, temperature uniformity across chip, residue, direct contact thermal sensor, ease of installation & replacement, contact force, cost
- 34 candidates tested & rated, 3 chosen for further evaluation

INDUSTRY SEARCH

- Thermal testing: θ_{TIM} determination
- $\theta_{j\text{-}a}$ is setup dependent (loss thru socket)

$$\theta_{j-a} = (T_{junction} - T_{ambient}) / Power \qquad 9.2^{o}C/W$$

$$P_{heatsink} = P_{total} - (T_{junction} - T_{ambient}) / \theta_{j-a}$$

$$\theta_{TIM} = (T_{junction} - T_{heatsink}) / P_{heatsink}$$

INDUSTRY SEARCH RESULTS

Vendor	Material description	Thickness (inch)	θ_{TIM} ($^oC/W$)	Clean-liness	Comp-liance	Concerns
	Bare heat sink		0.43			
A	Graphite film no PSA	0.005	0.40	2	2	Very fragile
B	Metal foil over liquid metal	N/A	0.44	4	4	Liquid metal leakage, less compliance
C	Graphite film w/ PSA	0.006	0.53	4	3	Hard to remove
D	Silicon w. fiberglass	0.010	0.63	2	2	Robust, less compliance
E	Carbon fiber composite w/silicon	0.020	0.64	4	4	Siloxane residue

LABORATORY EVALUATIONS

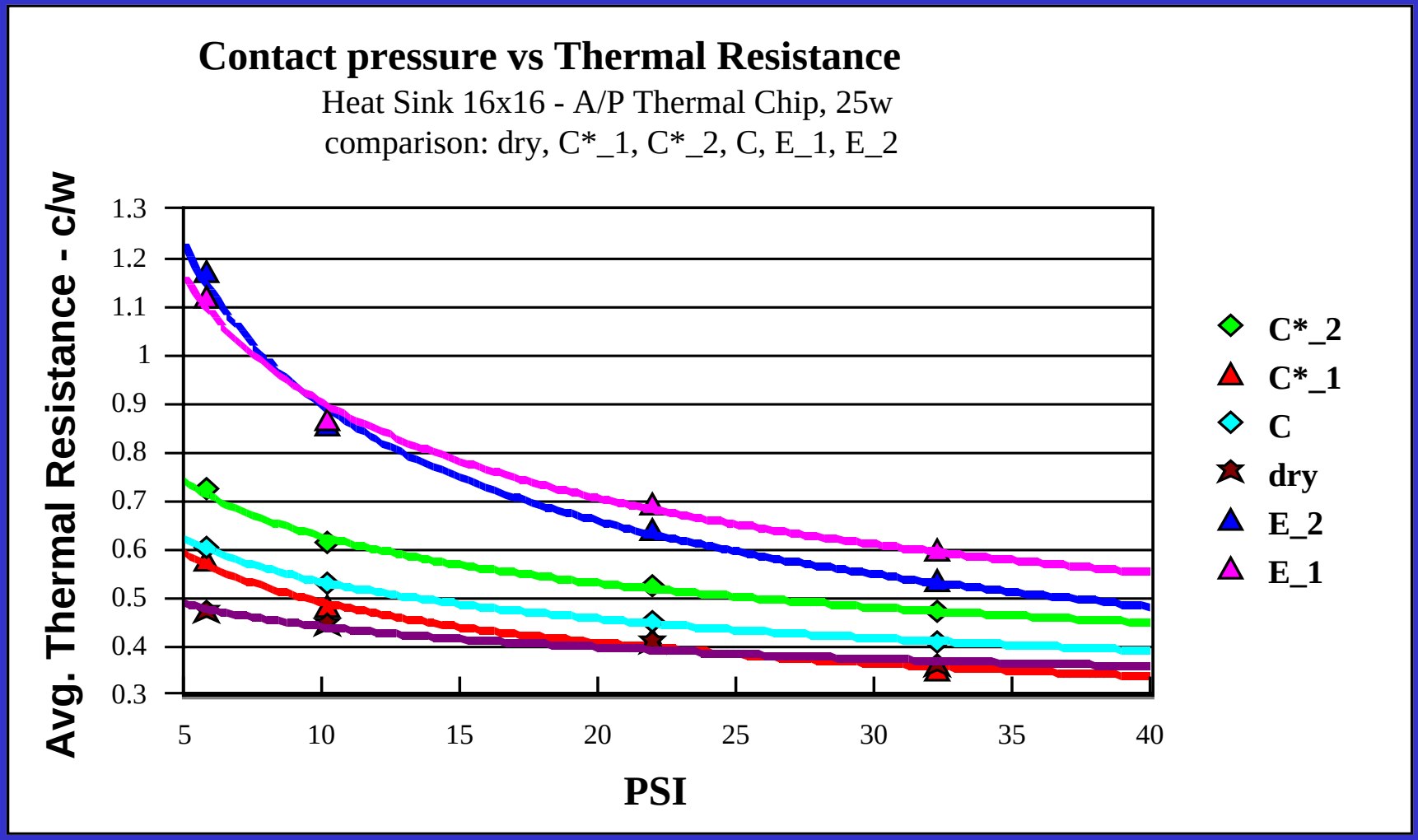
- Contact force vs. thermal performance of TIM
- Comparisons of thermal resistance
- Life-time test to simulate Burn In & test application (monitor θ_{TIM} and imprint thickness)

LABORATORY EVALUATION

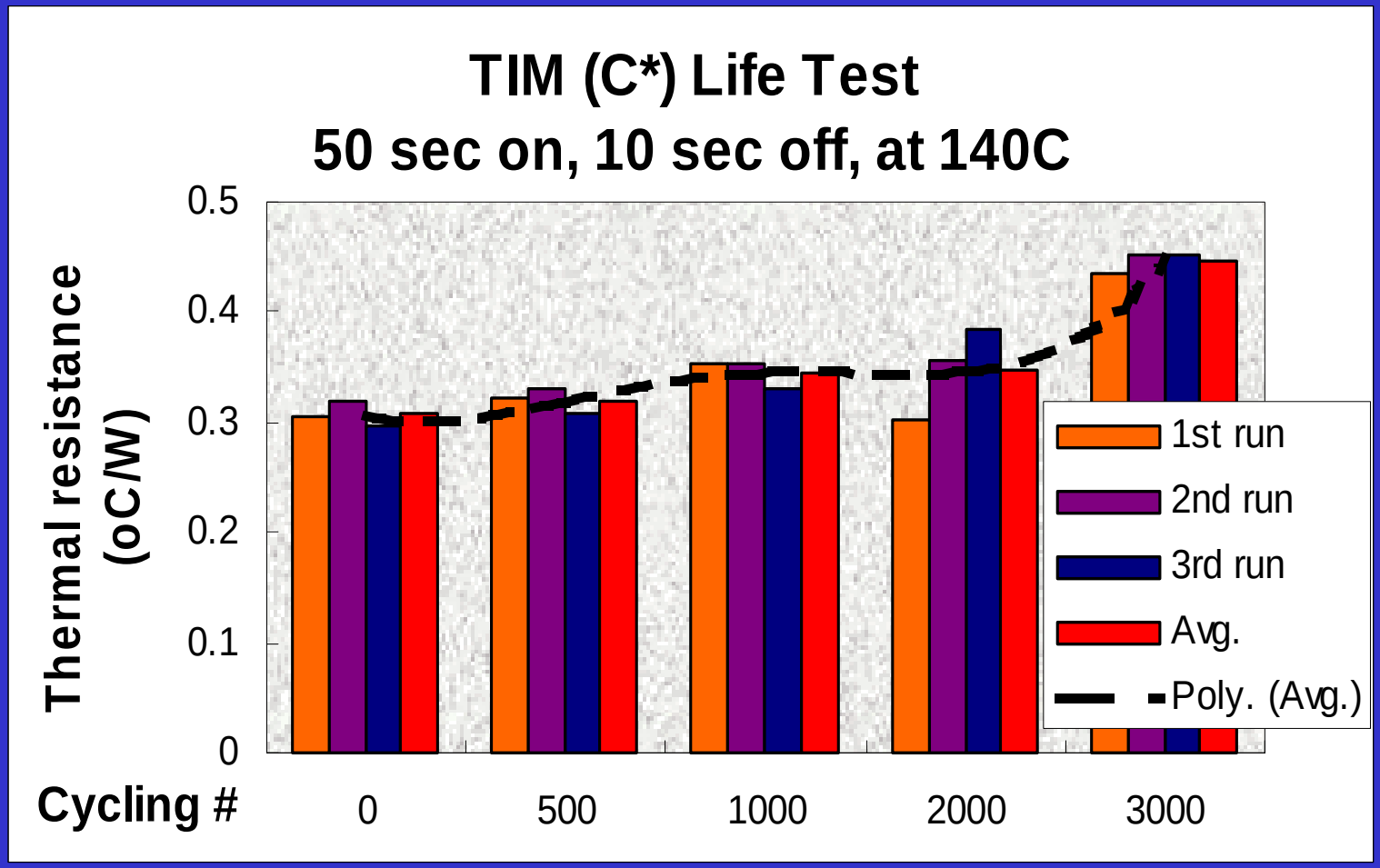
Vendor	Material Description	Thickness (in)	θ_{TIM} ($^oC/W$)
	Bare heat sink		0.47
C*	Graphite film w/o PSA	0.005	0.41
C*	Graphite film w/ PSA	0.005	0.31
C*	Graphite film w/ PSA (2nd type)	0.005	0.34
B	Metal foil over liquid metal	N/A	0.37
E	Carbon fiber composite w/silicon	0.020	0.69

LABORATORY EVALUATION

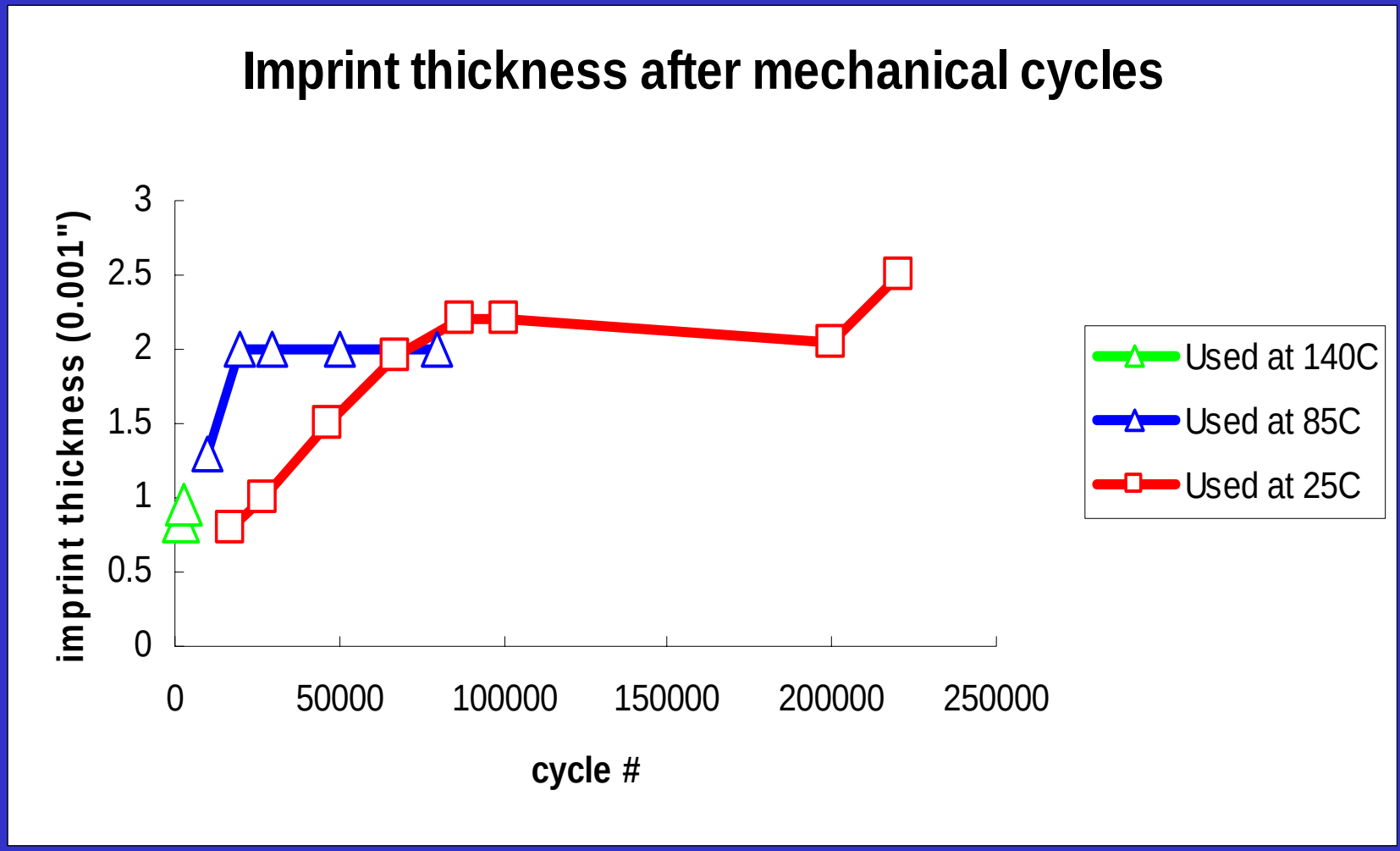
Contact Pressure vs. Thermal Performance



LABORATORY EVALUATION
Thermal Resistance (θ_{TIM}) vs. Cycles



LABORATORY EVALUATION
Imprint Thickness vs. Cycles



LABORATORY EVALUATION
RESULTS

- TIM can improve thermal performance in heat sink used in Burn in & Test socket
- Thermal performance of TIM (C*) degrades with mechanical cycles overall
- Wear-out and imprint thickness both increase with mechanical cycles and elevated temp.
- Life time of TIM must is best determined by data collected in manufacturing

PACKAGING INTERACTION
BACKGROUND

- Chip cleanliness critical for downstream packaging processes
- Many packaging operations are sensitive to presence of residue (organic or inorganic)
- Ideal interface will not leave residue
- In addition to residue, force applied at Burn-In needs to be considered as too much force may deform C4s

PACKAGING CONCERNS

- Residue may interfere with many aspects of packaging, including:
  - -Back side adhesion of thermal solution
  - -C4 re-joining
  - -Underfill adhesion
  - -2nd level attachment
  - -SMT component joining

CONSIDERATIONS

- If residue present, can it be cleaned
  - without damage, in volume production?
- Is residue made worse by
  - high temp, humidity, or electrical bias?
- Will interface absorb contamination and redeposit it on future chips?
- Does residue increase in intensity or change composition with progressive touchdowns?
- Is residue electrically conductive?
- Does it adversely impact packaging?

PACKAGING STRATEGY

- Phase 1 - Determine if materials present in incoming interface adversely effect packaging (by analytical means)
- Phase 2 – Determine if residue transfers
- Phase 3 – If residue transfers, determine if it would interfere functionally with package
- Phase 4 – Monitor pad to ensure residue does not increase or change over pad life

PACKAGING QUAL PLAN

- Pad Analysis
  - -Surface analysis of pad and backing sheet
  - -Weight loss and eluded species determination of pad and backing sheet
- Chip Backside Analysis
- Functional Tests
  - -Lid shear test
  - -Wetting angle determination
  - -Wettability
  - -Underfill adhesion

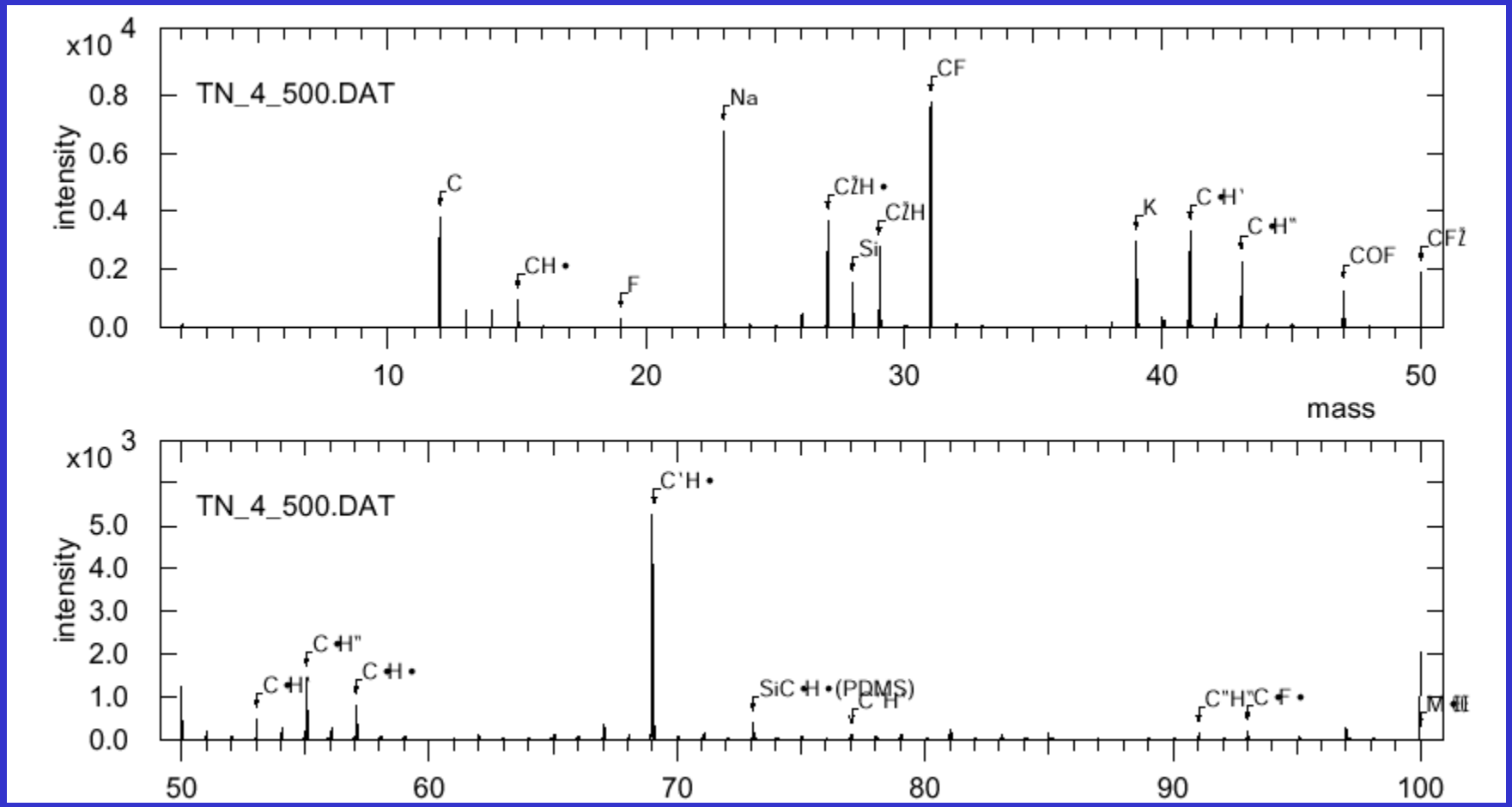
PACKAGING QUAL RESULTS

Test	Result
Functional Tests	Lid Shear - Modules showed no degrade in force req'd to shear caps
	Wetting Angle - No delta between modules exposed and controls
	Wettability - No difference between modules exposed and controls
	Underfill Adhesion - No delta between modules exposed to interface and controls

PACKAGING QUAL RESULTS

Test	Result
Pad Analysis	Analysis of new pad did not display any component detrimental to packaging (Backing sheet did but it did not transfer to pad)
Chip Backside Analysis	TOF-SIMS analysis of chip back side showed zero to negligible residue

TOF SIMS SPECTRUM OF MODULE WITH FLUORINE CONTAMINATION



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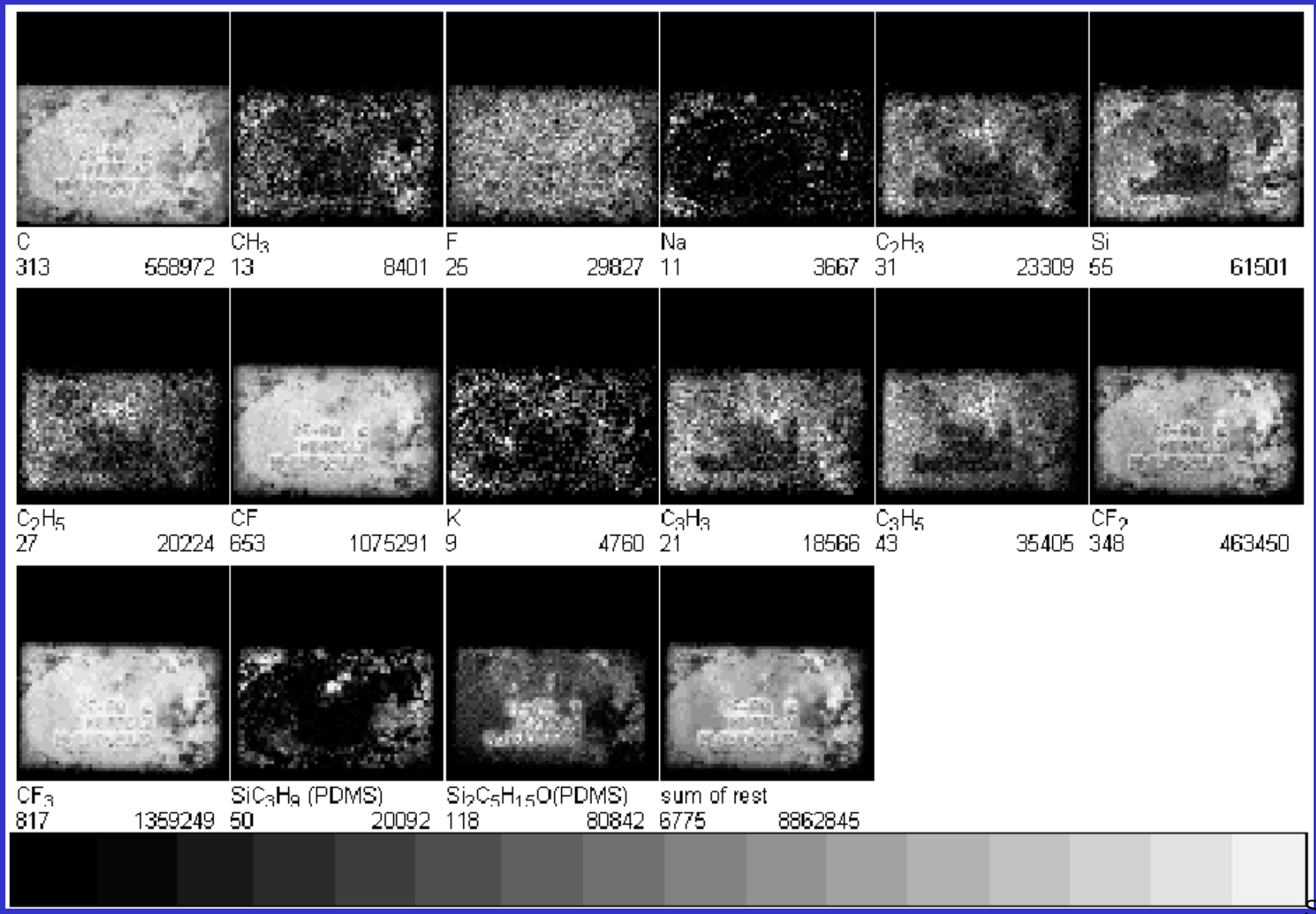
TOF-SIMS MAP OF CHIP BACKSIDE WITH FLUORINE CONTAMINATION



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PRODUCTION EVALUATIONS

- Introduction of a new material in production requires evaluations over and above lab work
- Manufacturing considerations include
  - Process development
    - installation, replacement, maintenance
- Testing in “real life” conditions
  - generally a less controlled environment
  - more handling, more exposures
  - large sample data opportunities

Production evaluations in two forms

- Production experiments, Production trials

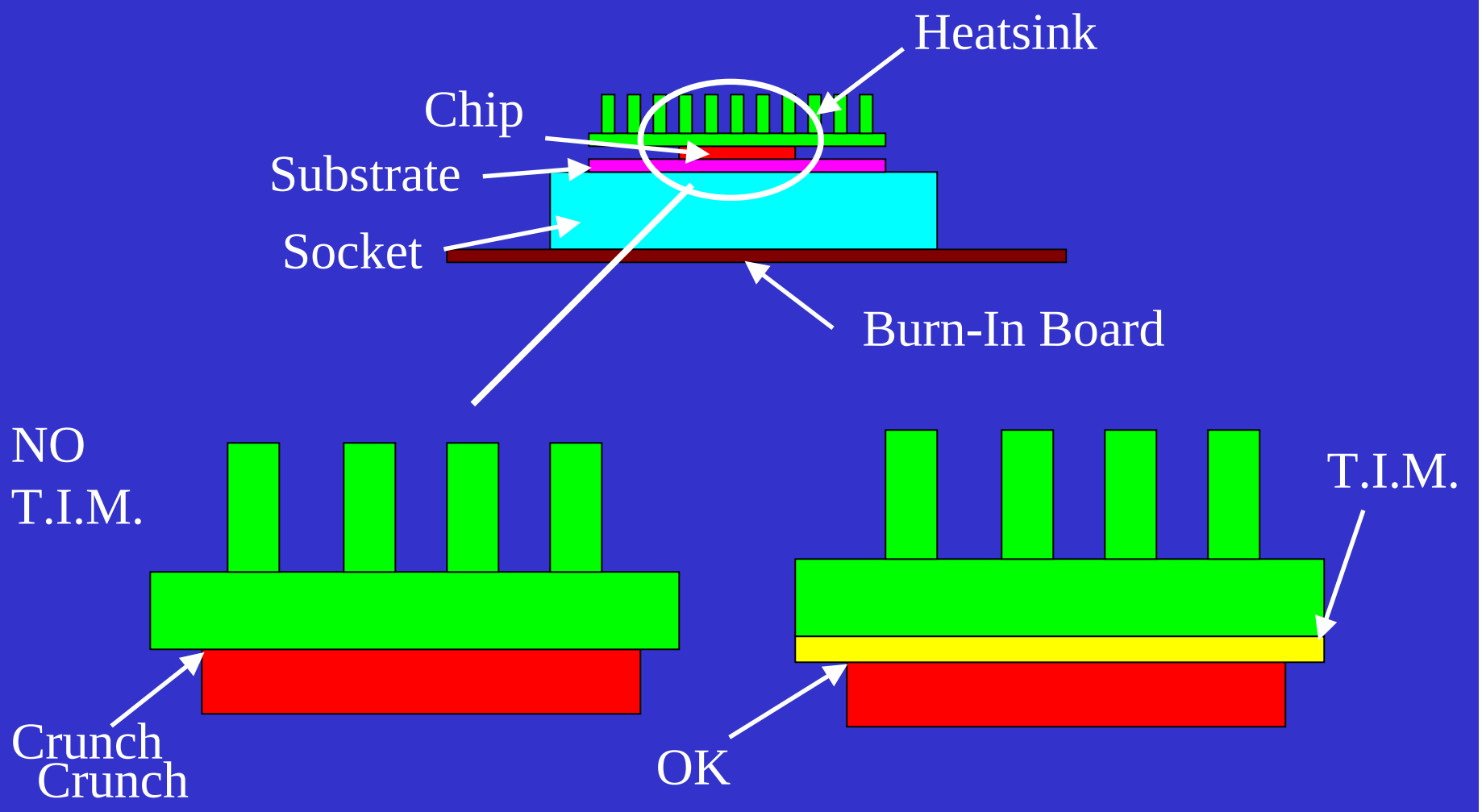
PRODUCTION TRIALS

- Pre-trial development requirements
  - Procedures defined/written
  - Operator & maintenance training
  - Implementation details (schedules, etc)
- Trials involve data from production runs
  - Inspections of interface material
  - Periodic Inspections of product
  - Laboratory analysis of product
  - Thermal performance vs. time
  - Thermal performance vs. chip size

PRODUCTION EXPERIMENT
CHIP CRACKING

- Bare die application
- Chip backside is thermal contact surface
- Historically, without socket design considerations, chip cracking fallout can reach 3%
- Cracking caused by point loading and
  - Chips not perfectly flat (convex/concave)
  - Heatsink larger than chip (overhang)
  - BIB handling induced vibration

PRODUCTION EXPERIMENT
CHIP CRACKING



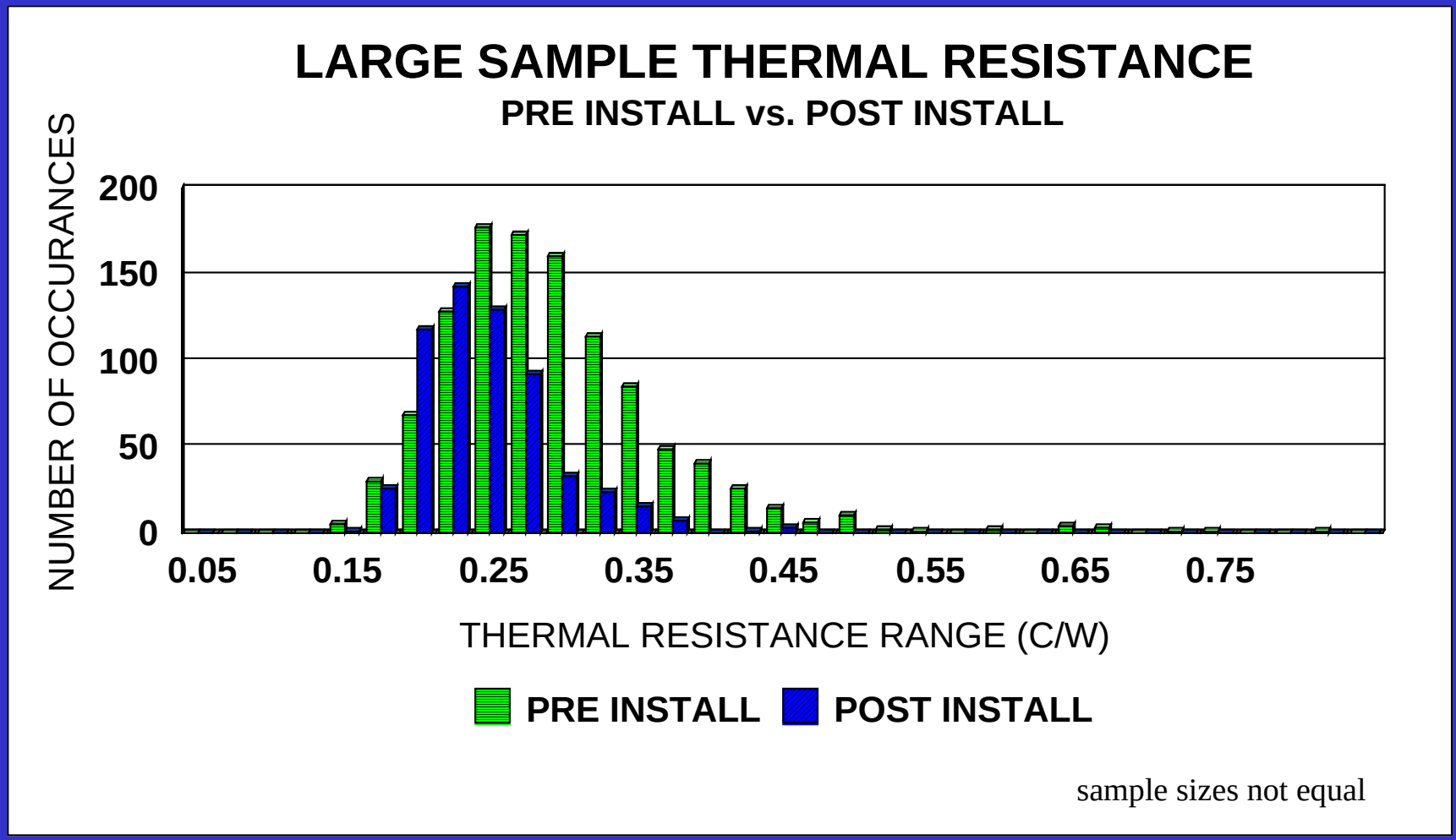
PRODUCTION EXPERIMENT
CHIP CRACKING

- Primary TIM benefit is *COMPLIANCE*
- Compliance “takes up”
  - Chip shape differences
  - Heat sink surface differences
  - Particulate contamination
- Benefits of compliant interface
  - Fills microscopic air gaps with thermally conductive material
  - Reduces overall thermal resistance variations (part to part, socket to socket)

PRODUCTION EVALUATION DATA
CHIP CRACKING

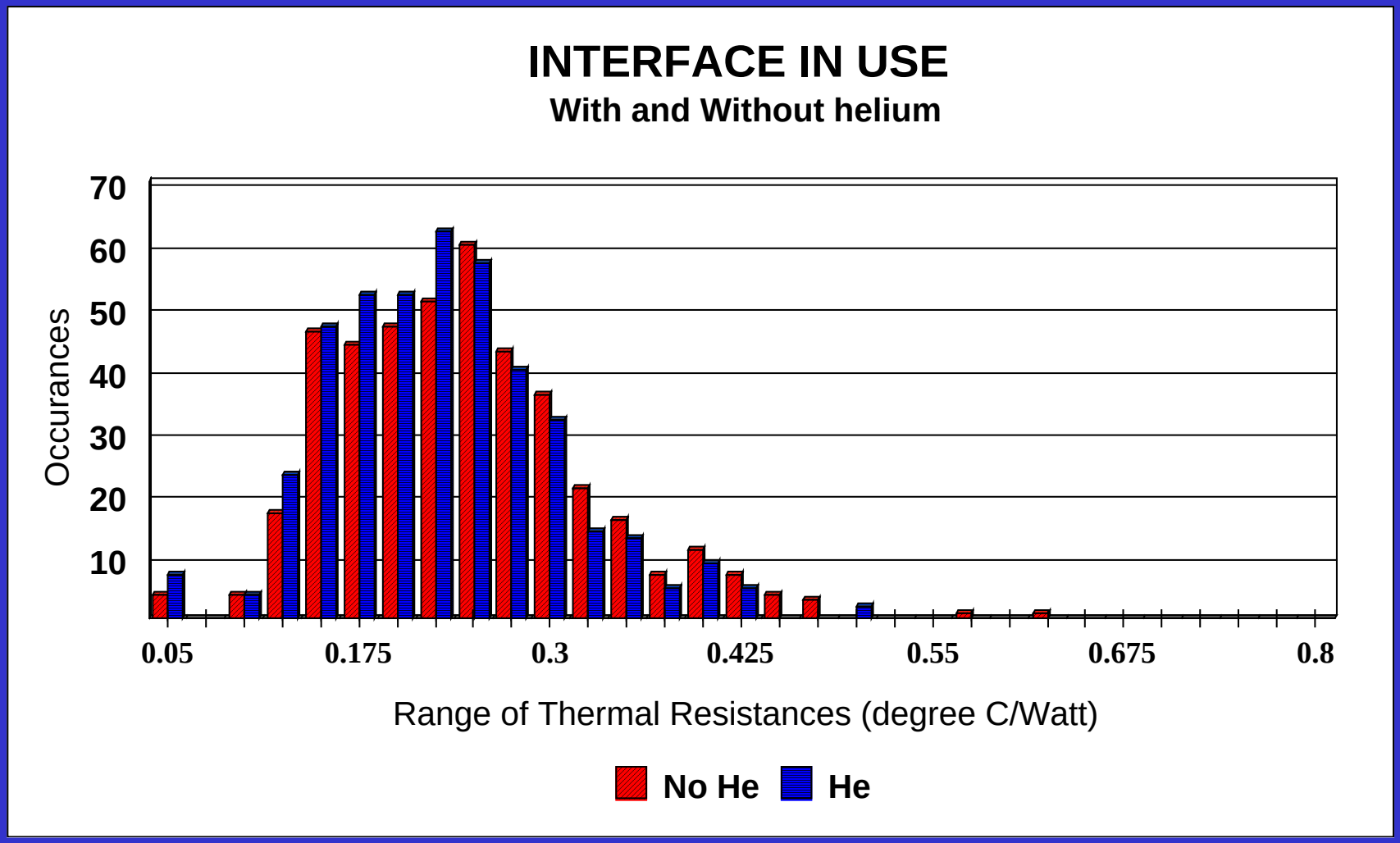
- Evaluation performed
  - Sample of product processed
  - With and without T.I.M
  - Subjected to multiple BI and load/unload cycles
  - Used same BIBs, same sockets, same tooling
- T.I.M. objectives achieved
  - Some % cracking without T.I.M
  - 0% No Cracking with T.I.M

PRODUCTION TRIALS
INTERFACE DATA SAMPLE

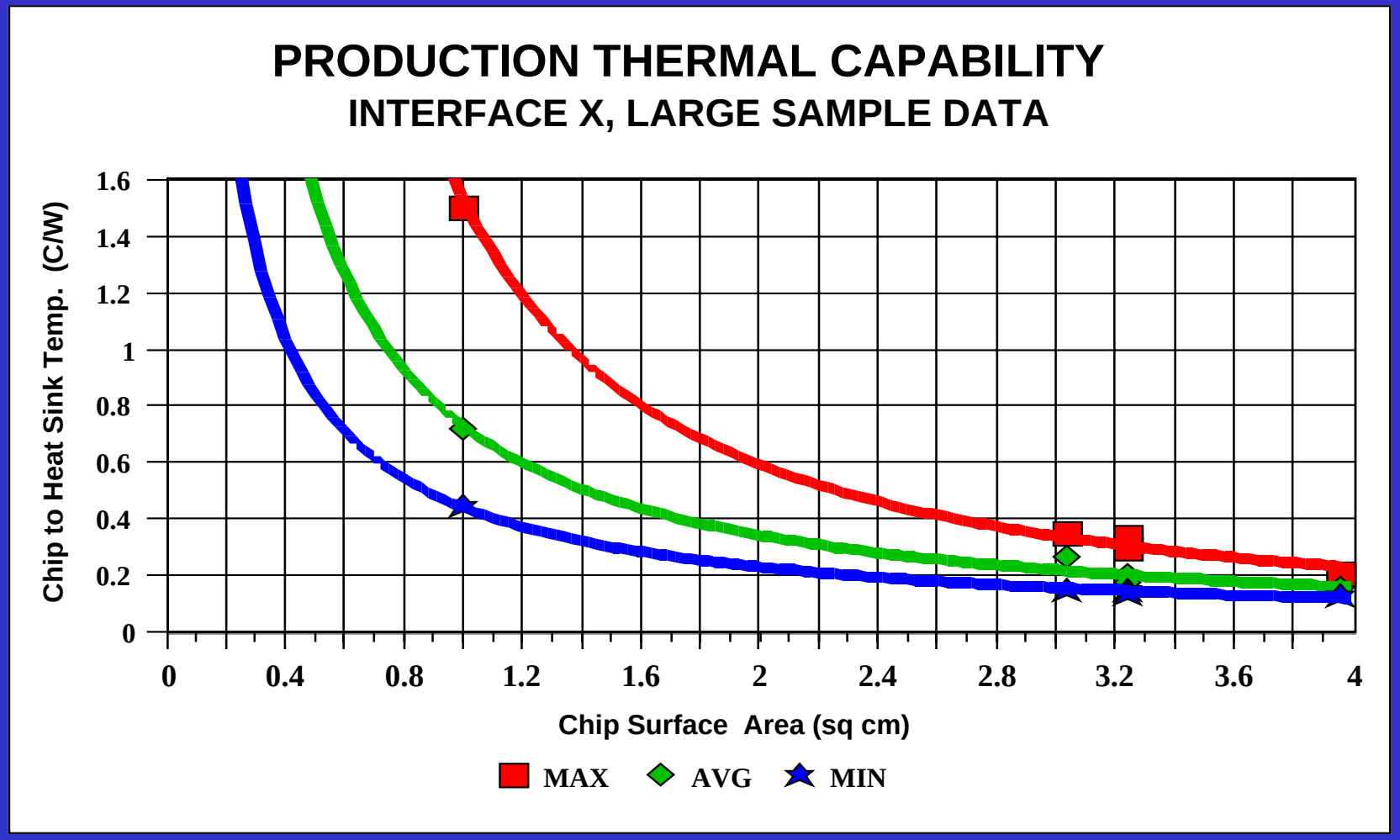


sample sizes not equal

PRODUCTION TRIALS
INTERFACE DATA SAMPLE



PRODUCTION TRIALS
INTERFACE DATA SAMPLE



PRODUCTION MONITORS

- Aimed at determining pad end of life
- Watching for indicators on a monthly basis
- Some tooling is lead tooling (out front)
- In place since first conversion to T.I.M.
- Product Samples taken from Production lots
- Sent to Reliability LAB for analysis
- Visual verification on the interface pads is performed at that time

CONCLUSIONS & LESSONS LEARNED

- Evaluate multiple interfaces for more options
- Very few interfaces are actually well suited to test and Burn-in applications
- Test applications are not necessarily equivalent to those of Burn-In (time, temp, touchdowns)
- Implementation across a widely varied product set is a significant challenge
- Cost reductions associated with the use of T.I.M.s are well worth the efforts

Thermal Solutions Division

Kulicke & Soffa Industries, Inc.

Characterization of a Thermal Control Unit Using Various Thermal Enhancers

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Introduction

- This presentation focuses on characterizing a TCU employing thermoelectricity in a liquid cooling system using selected interface materials mounted on the TEC surfaces & HE.
- Thermoelectricity is becoming very important recently especially considering its wide application and intense competition in this field.
- TEC-HE contact resistance is least investigated and hardly defined.
- Interface materials enhance heat transfer by reducing thermal resistance across contact surfaces. This improves surface contact by forming a continuous path of heat across an interface.
- Thermal interface materials becomes critical to the overall performance of the active device and the design/selection of the thermal management system.

The Role of Interface Materials

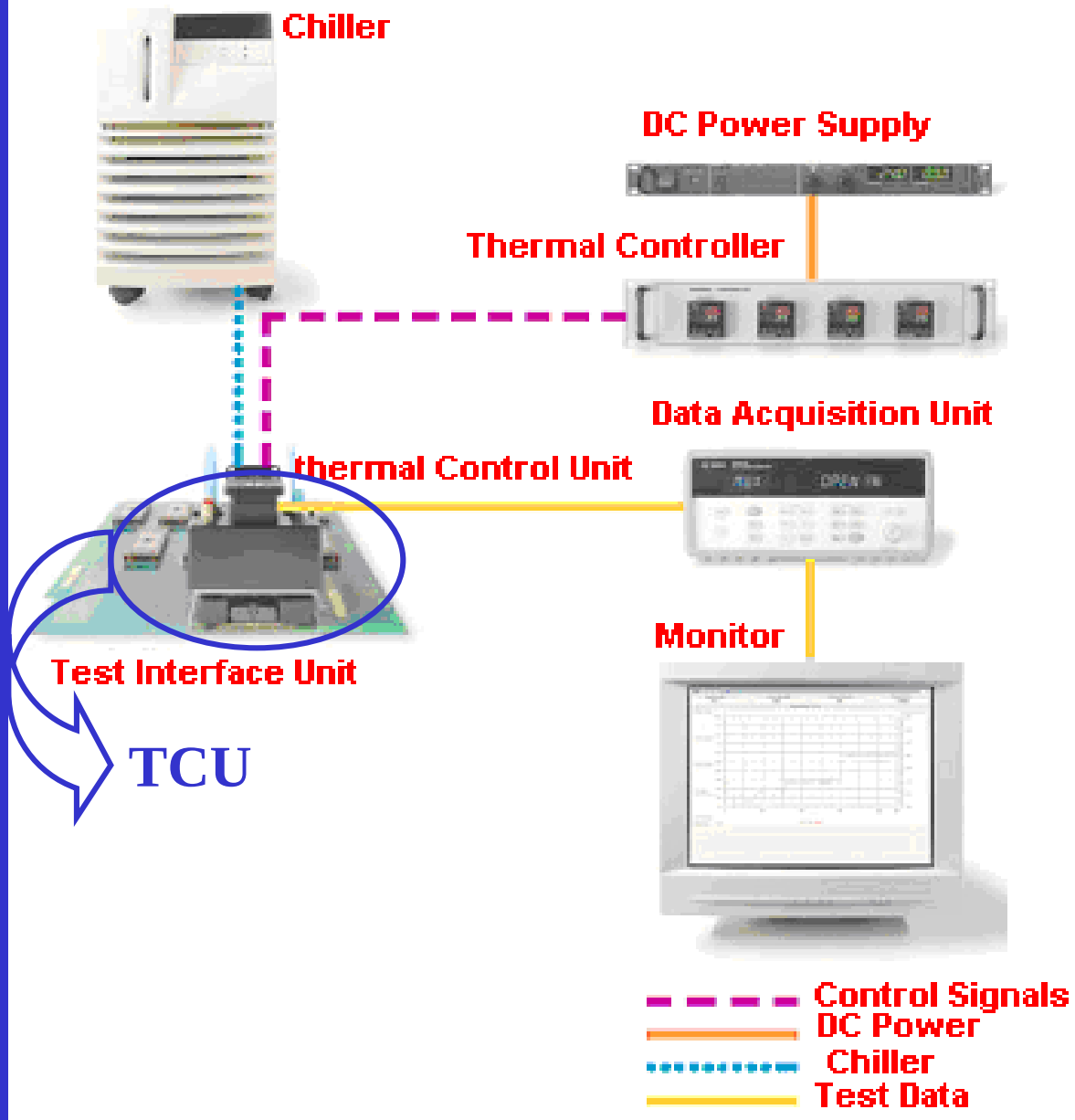
- All surfaces have a microscopic roughness and microscopic non-planarity.
- Solid surfaces are never completely smooth to create a perfect thermal contact. In most cases, as two surfaces are brought together, less than 1% of surfaces make physical contact while as many as 99% of the surfaces are separated by a very thin layer of interstitial air. Therefore, most of the heat is handled by the thin air film.
- With air thermal resistivity of 0.027W/m°C, air film must be eliminated by using a more conductive material.
- A typical interface material will minimize the amount of air between contact surfaces by forcing out air and forming a continuous path for the conducted heat to flow across the interface.

- Although interface materials introduce an interlayer of finite thickness, they enhanced heat transfer by filling the air voids created by an imperfect surface finish. Such heat transfer is essential in thermal management.
- Thermal resistance of contact surfaces is a function of the interface materials, surface properties and contact pressure.
- Thermal resistance is directly proportional to the interface thickness. It is inversely proportional to the thermal conductivity of the interface material, and to the area of the heat transfer {$R = t/(k\,A)$ }
- Thermal resistance can be minimized by making the interface as thin as possible, increasing thermal conductivity by eliminating interstitial air voids and providing intimate contact pressure.

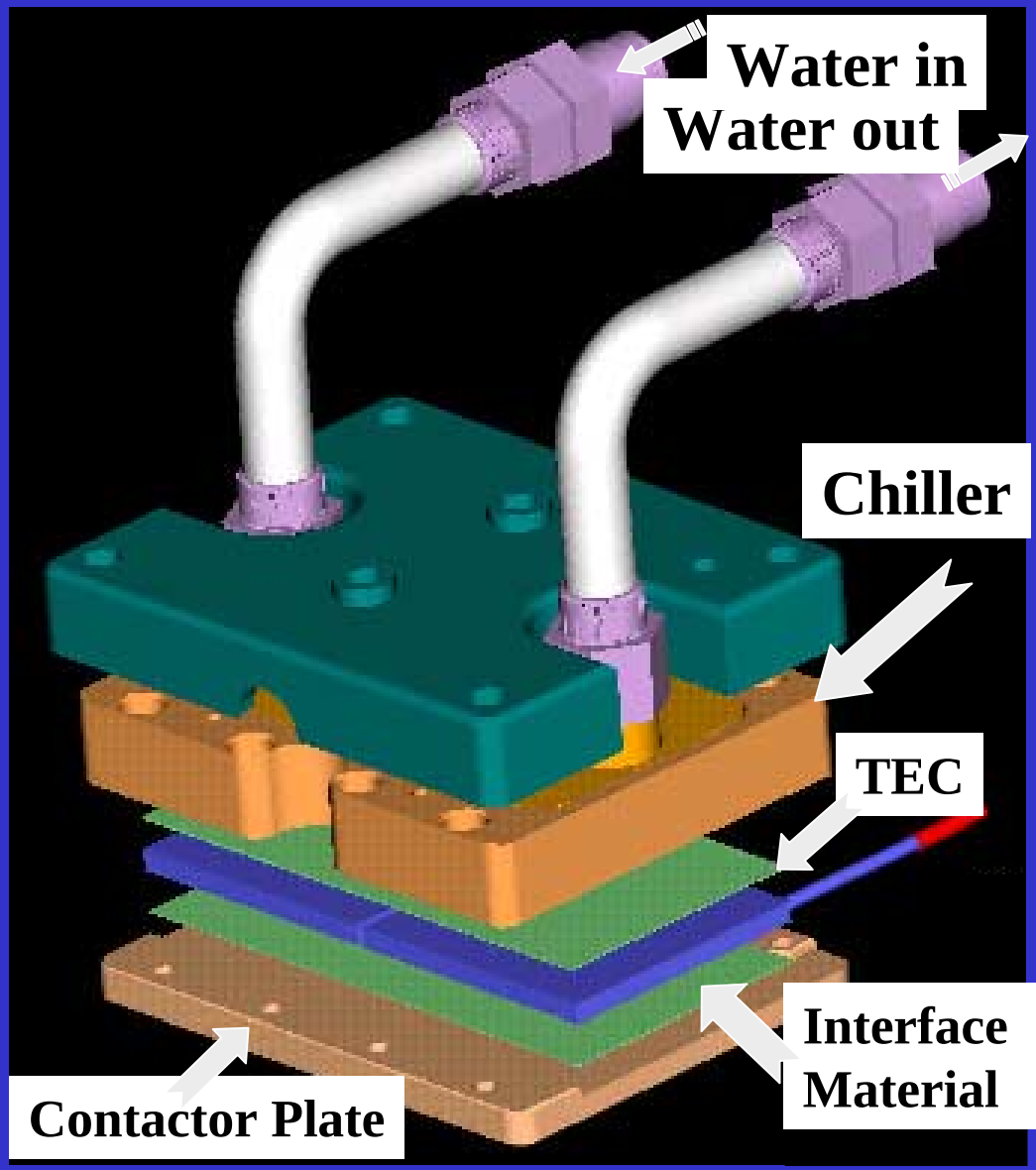
Goal of this Study

- Merit of TEC-HE contact resistance and it's significant influence on final TCU thermal performance will be investigated.
- Results of this study will assist in the optimum selection of interface materials to improve TCU thermal performance and to improve TEC design.

Test Set-up


Chiller
DC Power Supply
Thermal Controller
Data Acquisition Unit
thermal Control Unit
Test Interface Unit
TCU
Monitor
Control Signals
DC Power
Chiller
Test Data

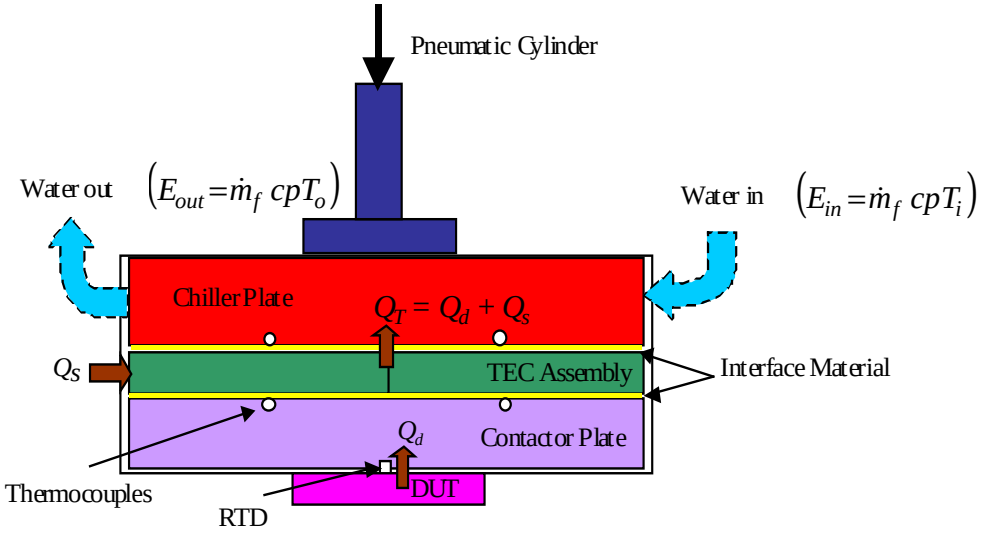
Thermal Control Unit
Active Liquid-Thermoelectric Cooling Technology

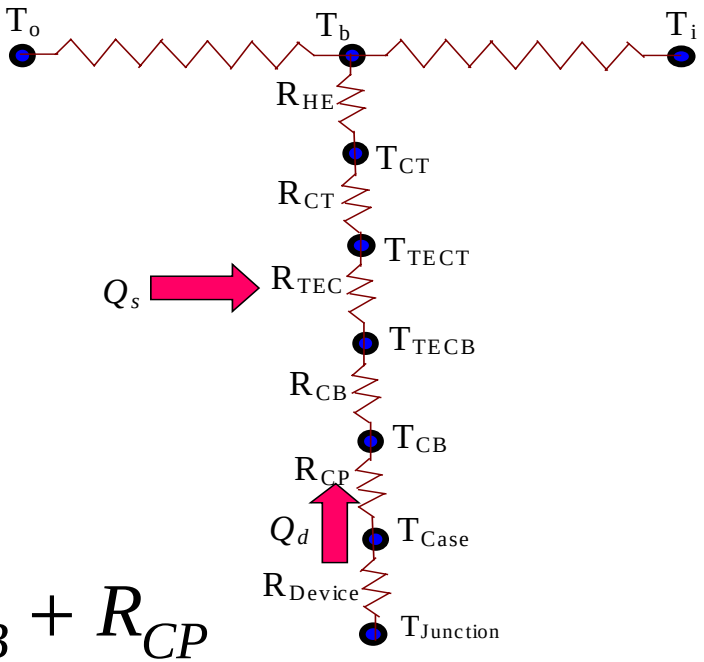


Why Liquid-TEC Technology

THERMAL MANAGEMENT METHOD	ACCURACY & STABILITY	TEMP RANGE	THERMAL EFFICIENCY	DYNAMIC RESPONSE	COST	ENVIRONMENTAL & ERGONOMIC ISSUES
Refrigeration	Very High	Wide (Cool)	Very High	Very Fast	Very High	Yes
TEC w/Liquid	High	Wide (Cool & Heat)	Moderate-High	Fast	Moderate	Condensation (can be insulated)
Liquid	Low	Narrow (Cool)	High	Slow	Low	Condensation (can be insulated)
Active Heat Sink	Low	Narrow (Cool)	Moderate	Slow	Very Low	Noise & Vibration
Passive Heat Sink	Low	Narrow (Cool)	Low	Slow	Very Low	No

TCU 1-D Thermal Resistive Network





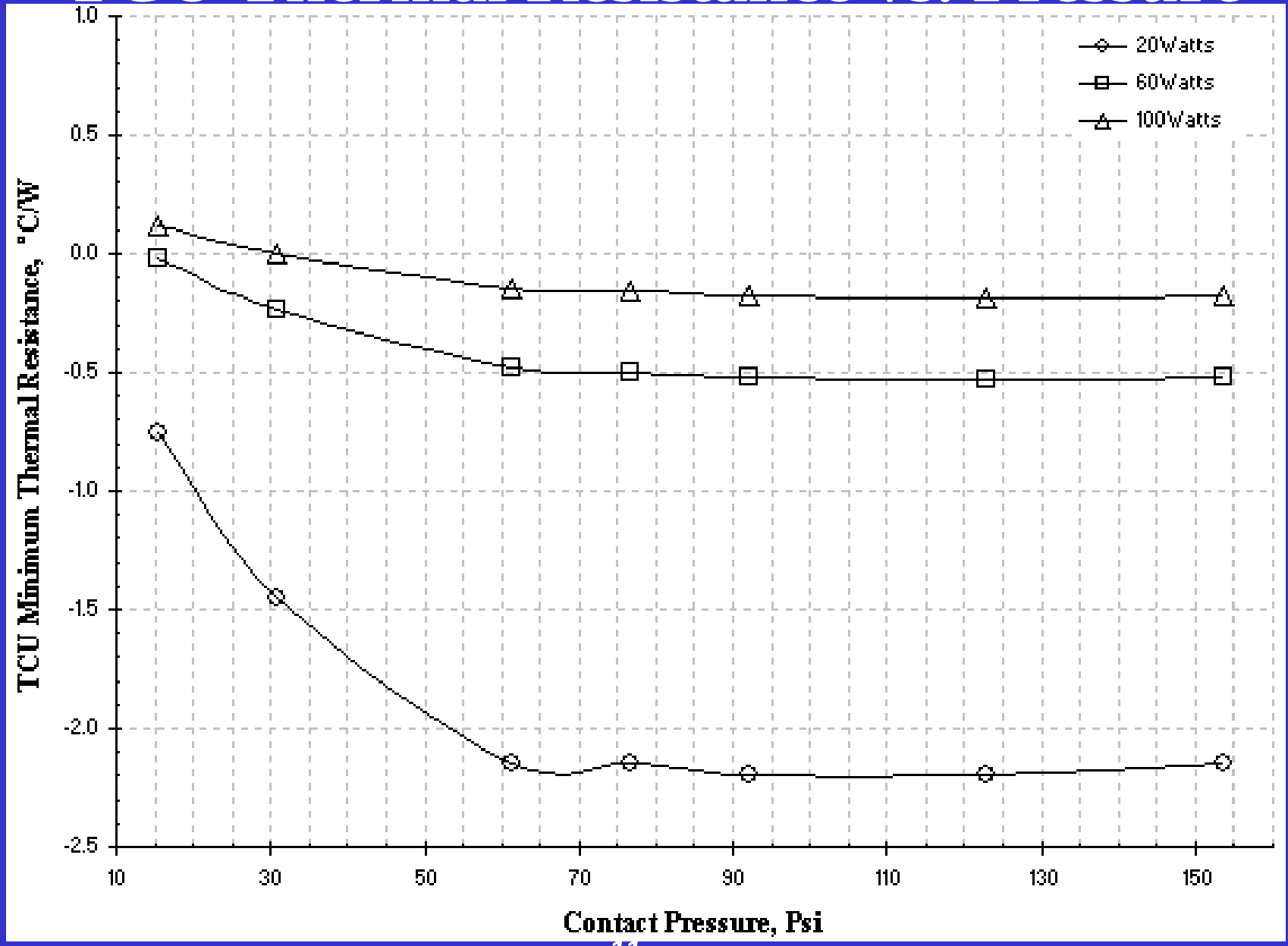
$$R_{System} = R_{HE} + R_{CT} + R_{TEC} + R_{CB} + R_{CP}$$

$$R_{TEC} = \frac{Z\,\Delta T^2}{Q_s}\left(\left(\frac{1}{a-1}\right)^2 + \frac{1}{a-1}\right) \qquad a = \frac{U}{I\,R} > 1$$

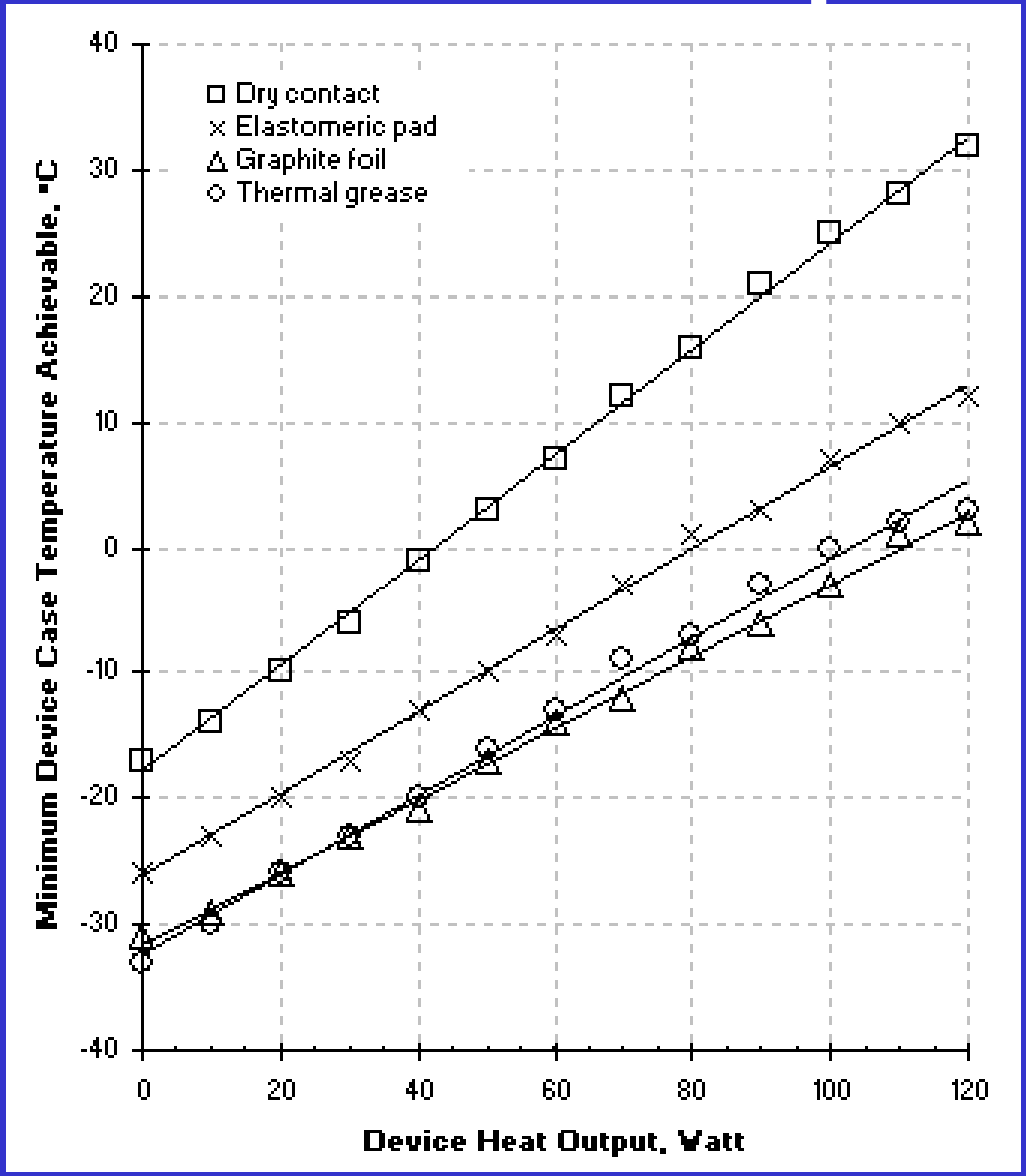
Interface Materials Tested

Type	Description	Thermal Resistance	Thickness
Dry contact		N/A	N/A
Graphite base		0.03 (°C-in^2/W)	0.01(in)
Thermal compound	Synthetic thermal grease	0.06 (°C/W)	N/A
Elastomeric pad	Conductive filler	0.05 (°C-in^2/W)	0.01 (in)

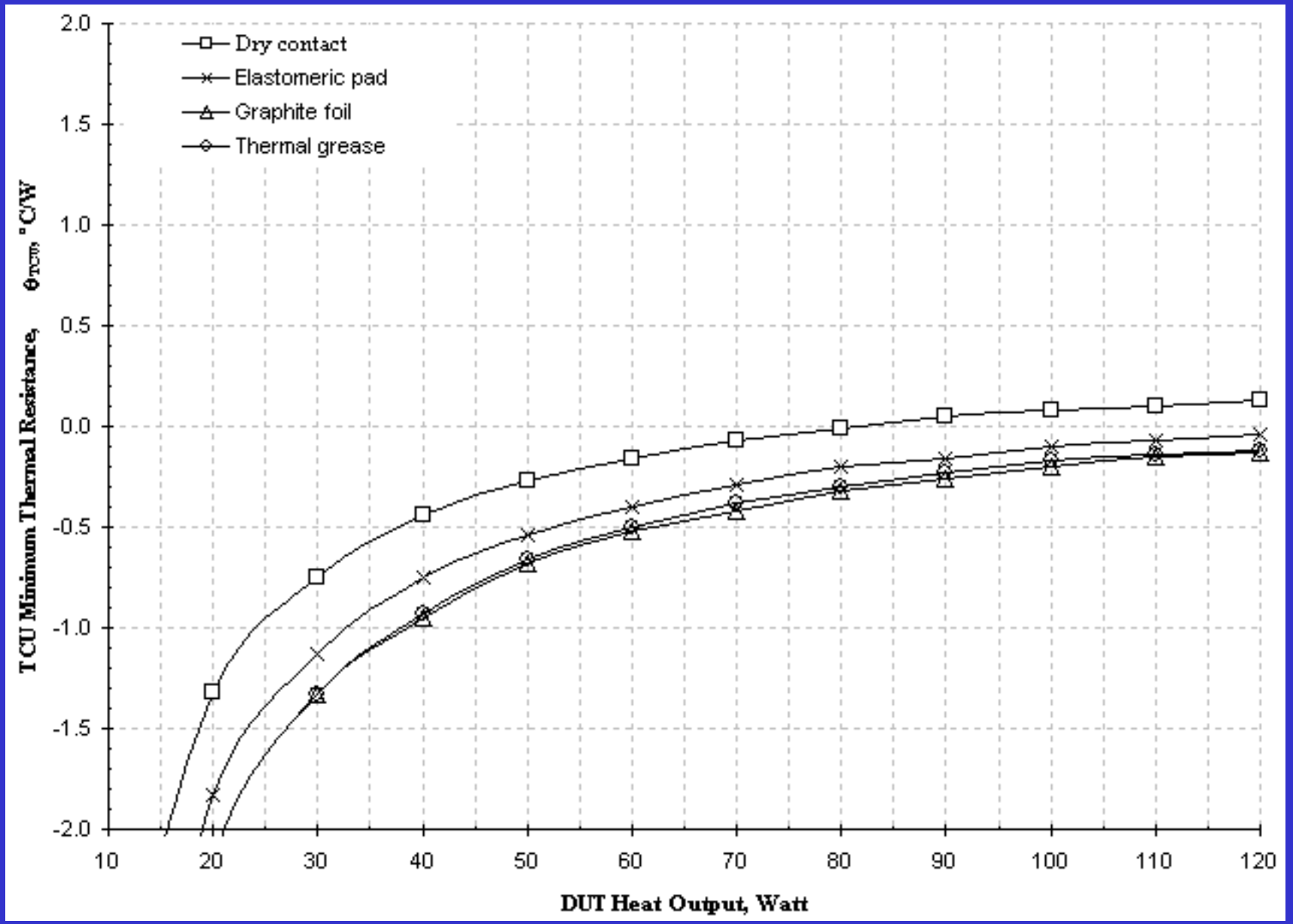
TCU Thermal Resistance vs. Pressure



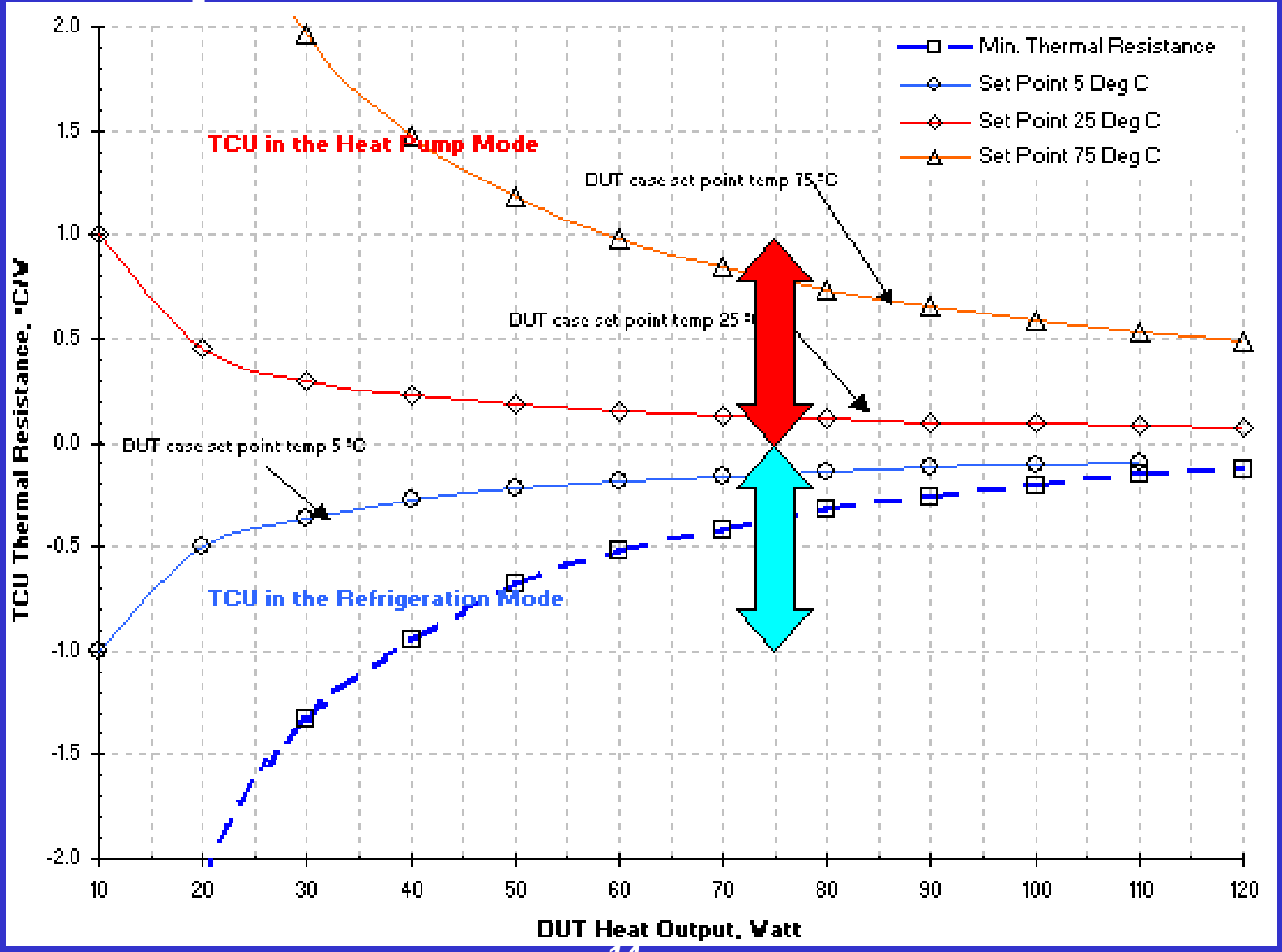
Min. Device Case Temperature vs. DUT Heat Output.



TCU min. Thermal Resistance



TCU Thermal Resistance Using Graphite Base Interface Material



Conclusions

- TCU performance is optimized when using selected interfacial materials.
- Dry surface contact produced the highest TCU thermal resistance.
- Interfacial materials improved heat transfer and reduced the TCU thermal resistance.
- With a rise in the thermal load (TCU cooling capacity), the TCU thermal resistance increases respectively.

- Graphite base interface material proved the best choice among interface materials.
- Graphite base interface materials significantly reduced thermal resistance.
- These materials also conform to mounting surfaces under low contact pressure.
- It also can be easily replaced without any surface cleaning, as in the case of thermal grease.

LEAST-VOLUME OPTIMIZATION OF FINNED HEAT SINKS FOR BURN-IN AIR COOLING SOLUTIONS

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Patrick E. Phelan

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Department of Mechanical & Aerospace Engineering

BiTS
BURN-IN & TEST SOCKET WORKSHOP

ASU ARIZONA STATE UNIVERSITY

Overview

- Introduction
- Heat sink review
- Thermal performance comparison of finned heat sinks
- Least-volume optimization for burn-in air solutions
- Conclusions

Introduction

Thermal Challenges of the BI Process

- Control of the Junction Temperature (T_j)
- Maximizing heat dissipation per Device Under Test (Q/DUT)
- Minimizing the BI oven volume (DUT/V)

Heat Sink Review

- BI Heat Sink Requirements
- Previous Research

BI Heat Sink Requirements

Requirements	Packaging	BI
Minimizing heat sink weight	✓	--
Minimizing manufacturing costs	✓	--
Maximizing heat dissipation	✓	✓
Minimizing heat sink volume	✓	✓
Minimizing and maintaining a stable, reliable junction-to-air thermal resistance (θ_{ja})	✓	✓

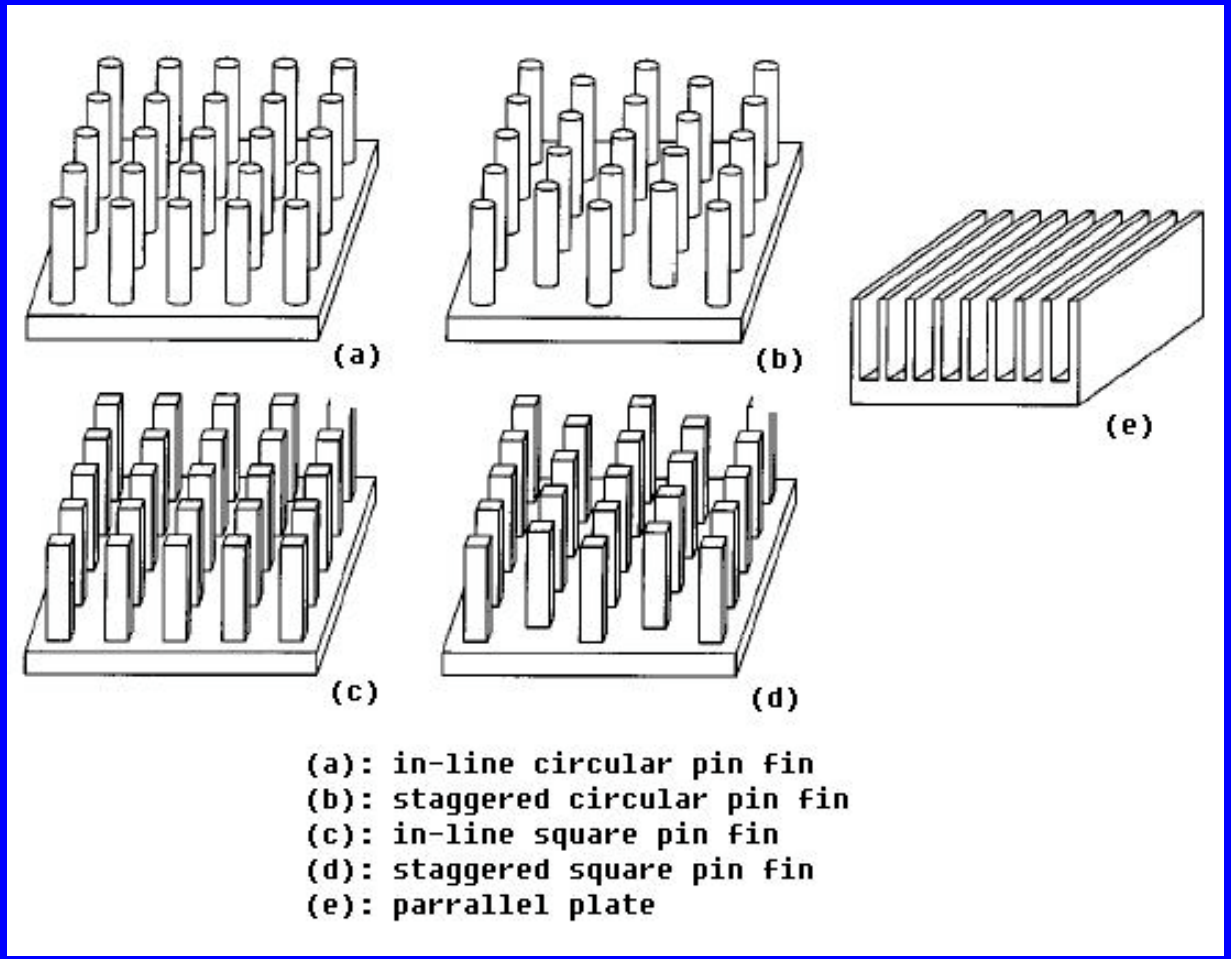
Previous Research on Air-Cooled Heat Sinks

- Heat sink parametric optimization
- Least-material optimization of finned heat sinks in natural convection heat transfer (Iyengar & Bar-Cohen, 1998)
  - ☞ Minimize manufacturing costs
- Least-energy optimization of forced convection plate-fin heat sinks (Iyengar & Bar-Cohen, 2002)
  - ☞ Minimize manufacturing & operating costs

Thermal Performance Comparison of Finned Heat Sinks for BI

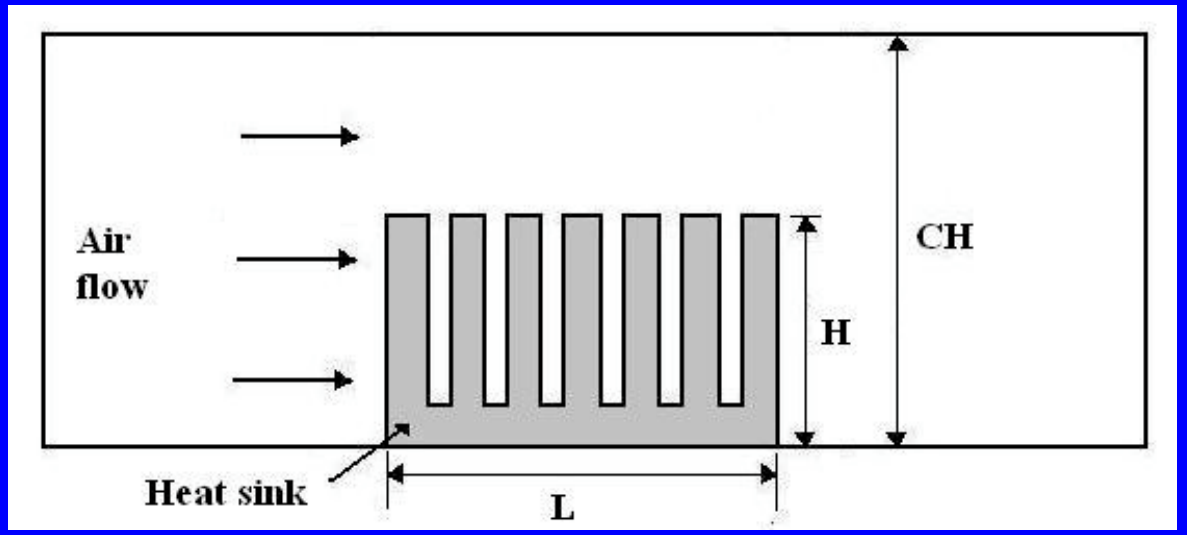
Heat sink geometries

Jonsson & Moshfegh (2001)

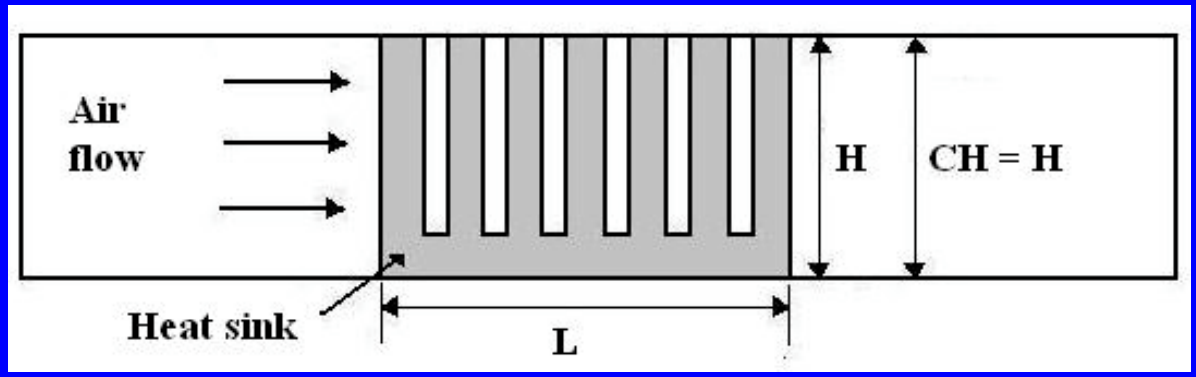


Heat Sink Side Views

With air bypass
(CH/H>1)

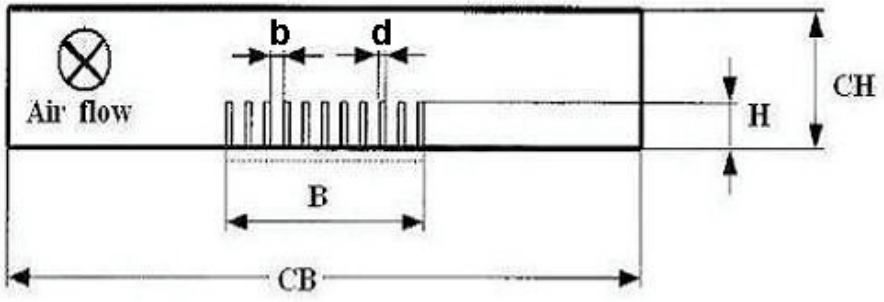


No air bypass
(CH/H=1)



The Nusselt Number Correlation
(Plate fin, strip fin, and pin fin heat sinks)

Jonsson & Moshfegh (2001)



$$Nu_L = C_1 \cdot \left(\frac{\mathrm{Re}_{dh}}{1000}\right)^{m1} \cdot \left(\frac{CB}{B}\right)^{m2} \cdot \left(\frac{CH}{H}\right)^{m3} \cdot \left(\frac{b}{H}\right)^{m4} \cdot \left(\frac{d}{H}\right)^{m5}$$

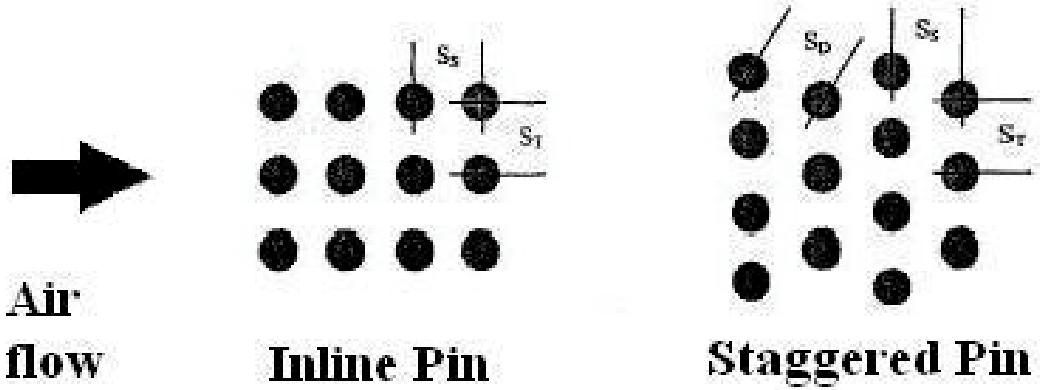
$$\frac{CB}{B} = 1.2,\quad 2,\quad 3$$

$$1.5 \le \frac{CH}{H} \le 3$$

$$2{,}000 \le \mathrm{Re}_{dh} \le 16{,}500$$

Existing Nusselt Number Correlation
(In-line and staggered pin fin heat sinks)

Zapach et al. (2000)

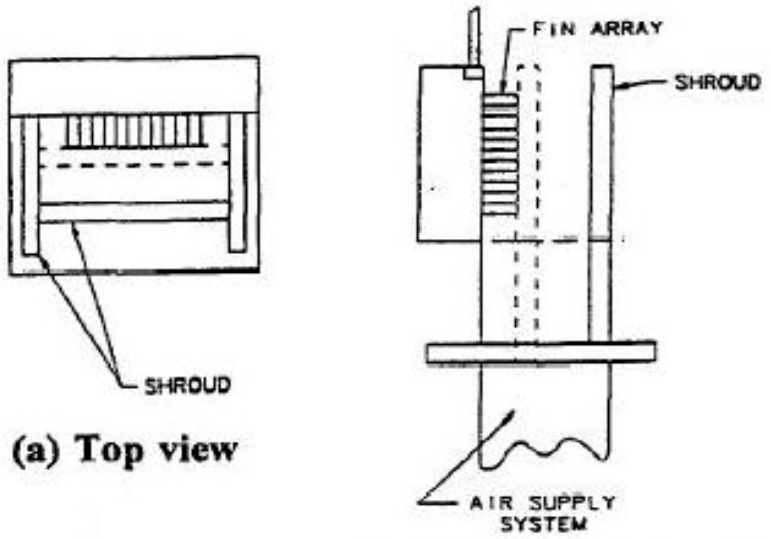


$$Nu_D = C_1 \cdot C_2 \cdot \mathrm{Re}_{D,\max}^{m} \cdot \mathrm{Pr}^{0.36}$$

$$C_H = 1 \quad (\text{no air bypass})$$

Existing Nusselt Number Correlation
(Vertical in-line pin fin heat sinks)

Maudgal et al. (1997)



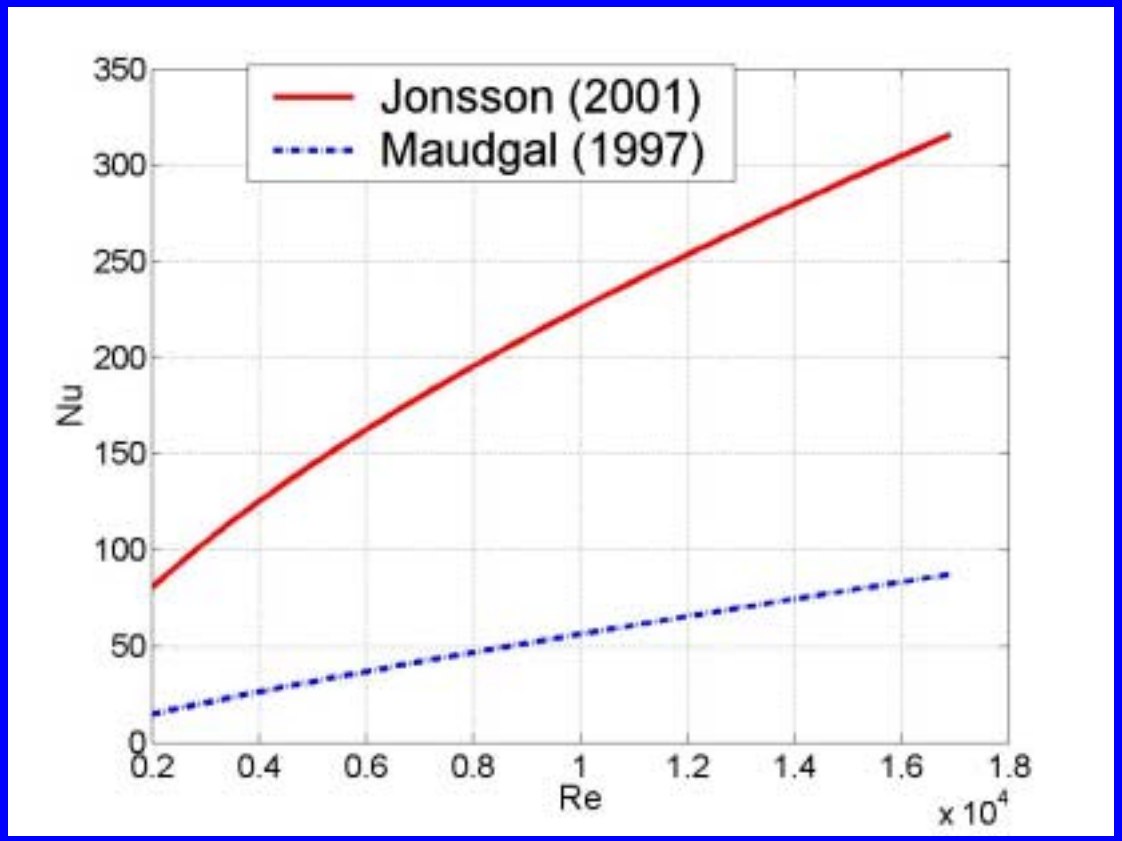
(a) Top view

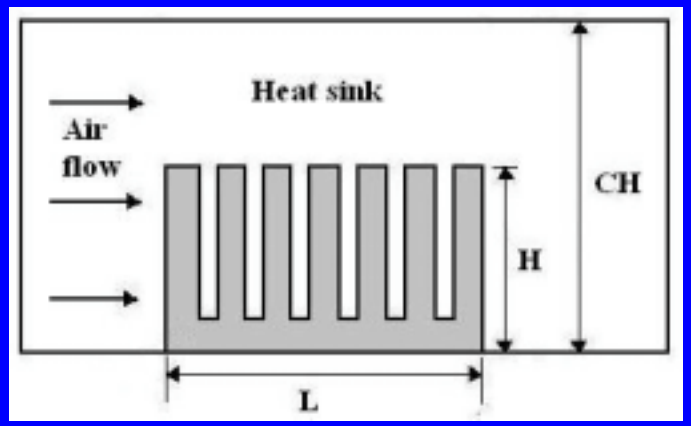
(b) side view of shrouds

$$Nu = C_1 \cdot (\mathrm{Re})^n$$

$$CH/H = 1 \sim 1.66$$

Comparison of In-Line Pin Fin Heat Sinks with Air Bypass (CH/H=1.66)





$Re_{dh} = V \cdot d_h/\nu$

Where,

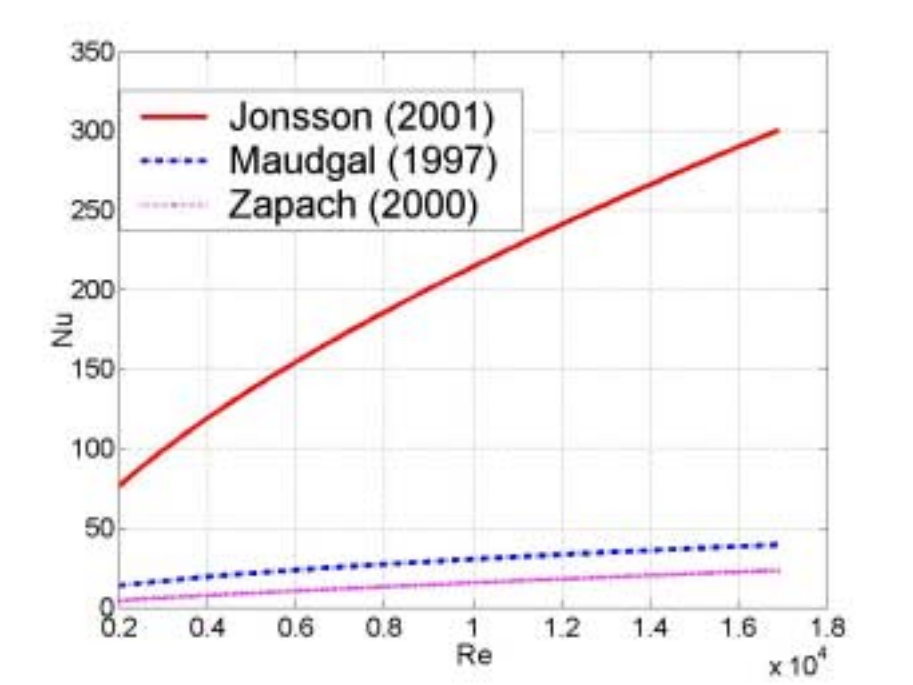
V = average air velocity [m/s]

$d_h = 2\ CH \cdot CB/(CH+CB)$ [m]

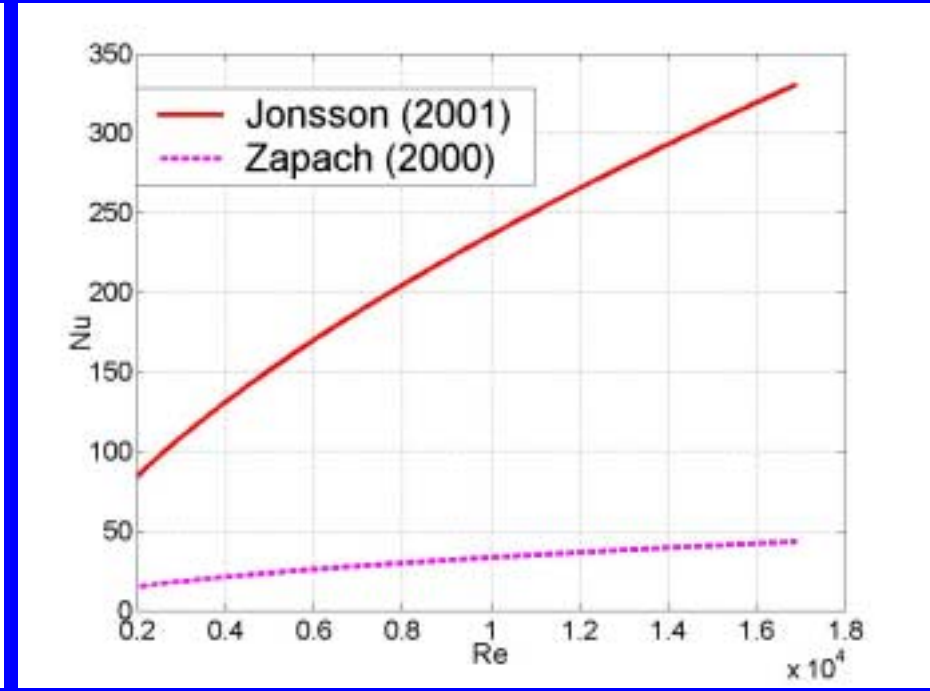
ν = kinematic viscosity of air [m^2/s]

Comparison of In-Line and Staggered Pin Fin Heat Sinks without Air Bypass (CH/H=1)

In-line pin fin



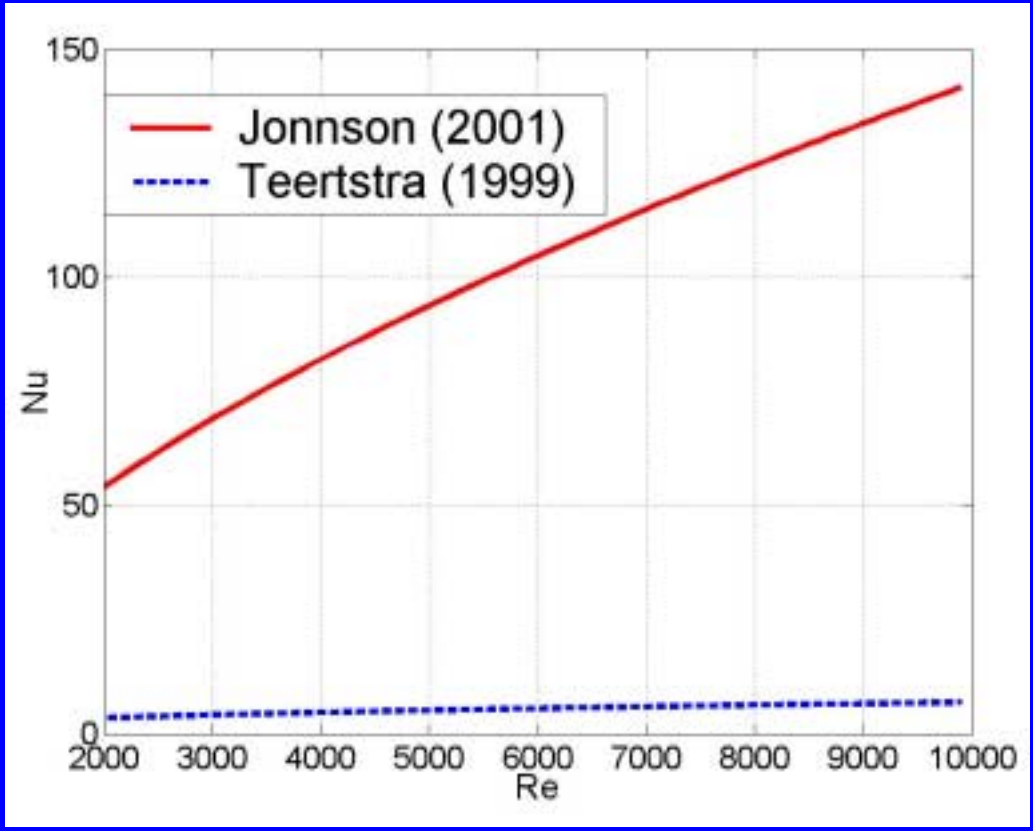
Staggered pin fin

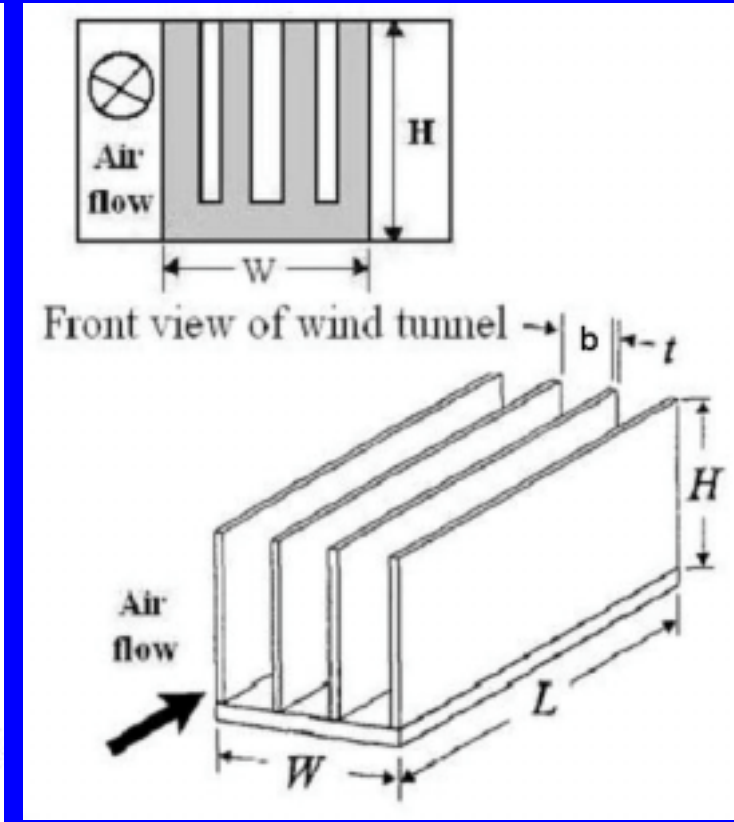


Existing Nusselt Number Correlations of Parallel Plate Heat Sinks

Jonsson et al. (2001) **Plate fin, strip fin, pin fin heat sinks**	$$Nu_L = C_1 \cdot \left(\frac{\mathrm{Re}_{dh}}{1000}\right)^{m1} \cdot \left(\frac{CB}{B}\right)^{m2} \cdot \left(\frac{CH}{H}\right)^{m3} \cdot \left(\frac{b}{H}\right)^{m4} \cdot \left(\frac{d}{H}\right)^{m5}$$
Teertstra et al. (1999) **Plate fin heat sinks**	$$Nu = \left[\frac{1}{\left(\frac{\mathrm{Re}_\delta^* \cdot \mathrm{Pr}}{2}\right)^n} + \frac{1}{\left(0.664\sqrt{\mathrm{Re}_\delta^*} \cdot \mathrm{Pr}^{1/3} \cdot \sqrt{1+\frac{3.65}{\sqrt{\mathrm{Re}_\delta^*}}}\right)^n}\right]^{-1/n}$$

Comparison of Parallel Plate Heat Sinks (CH/H=1)



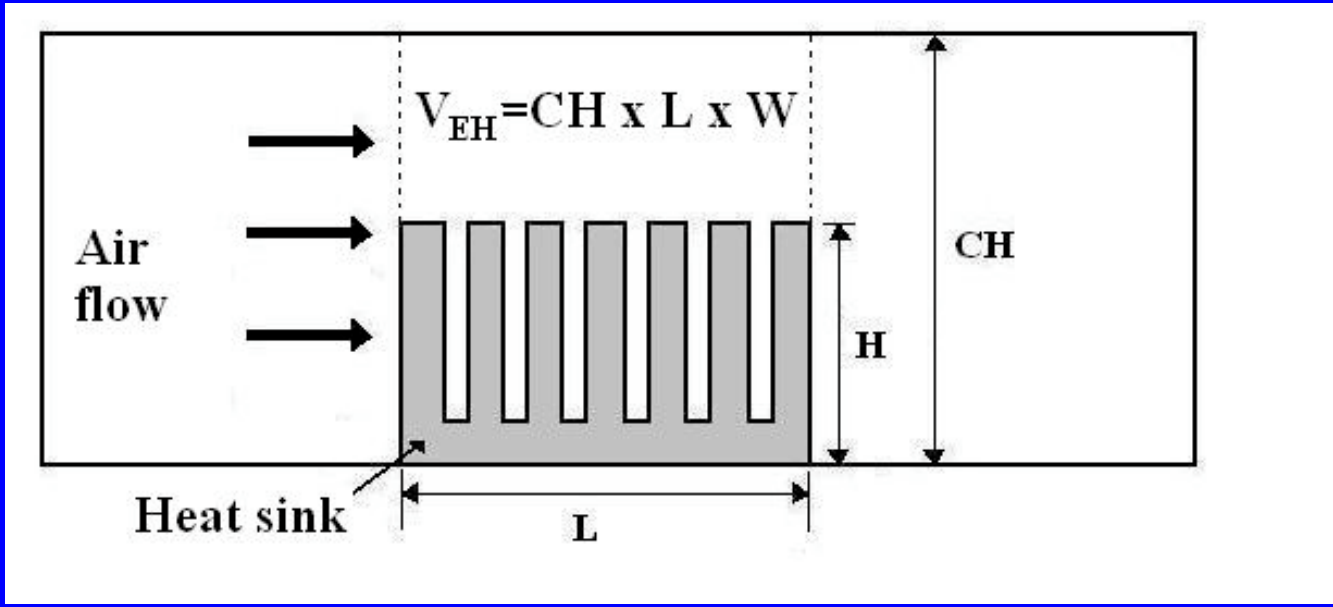


Summary of Comparison

- Nusselt number increases as Re increases for all the correlations
- Considerable disagreement among existing experimental results for both cases: with and without air bypass
- What happens as the bypass height is decreased in order to minimize the total volume?

Least-Volume Optimization for BI Solutions

- Heat Sink Extended Volume, V_{EH}
- Extended volumetric heat dissipation, Q/V_{EH}



Least-Volume Optimization for BI Solutions

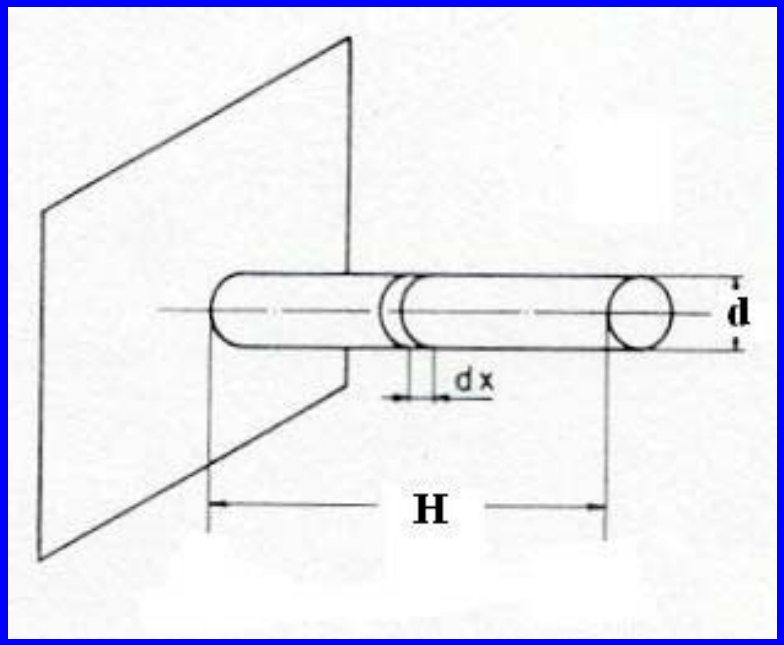
The optimal fin geometry

Heat transfer from the single fin

Extended volumetric heat transfer comparison

Optimal Pin Fin Geometry

(Sonn & Bar-Cohen, 1981)



$$d = 4.73 \cdot h_{fin} \cdot H^2 / k$$

Where,

d: diameter of pin fin [m]

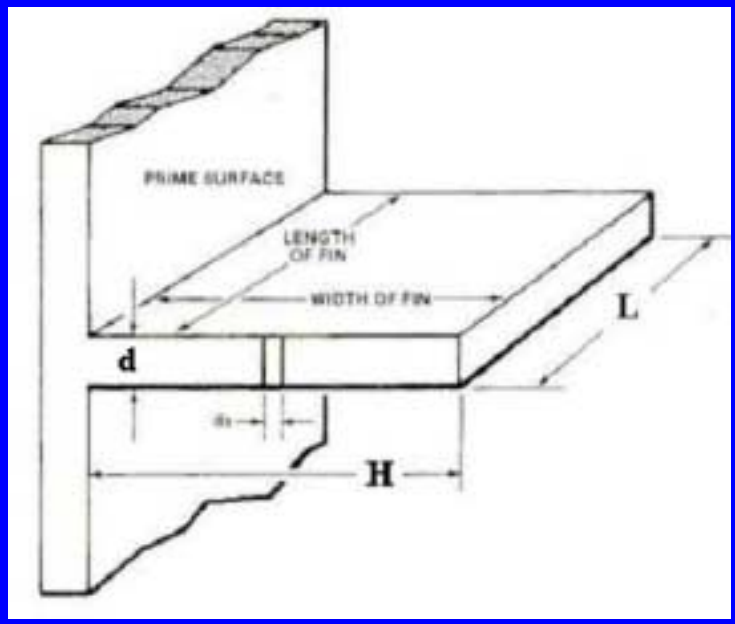
h_{fin}: average fin heat transfer coefficient [W/m^2-K]

H: fin height [m]

k: thermal conductivity of heat sink material [W/m-K]

Optimal Parallel Plate Geometry

(Bar-Cohen & Jelinek, 1986)



$$d = 0.993 \cdot h_{fin} \cdot H^2 / k$$

Where,

d: thickness of fin for plate arrays [m]

h_{fin}: average fin heat transfer coefficient [W/m^2-K]

H: fin height [m]

k: thermal conductivity of heat sink material [W/m-K]

Heat Transfer from the Optimal Fin Heat Sinks

Heat transfer from a single pin fin:

$$q_{pin\ fin} = 11.736 \cdot \mathbf{?}\ \mathbf{T} \cdot\ \mathbf{h_{fin}^{2} \cdot H^{3} / k}$$

Heat transfer from a single parallel plate:

$$q_{plate} = 1.25 \cdot L \cdot \mathbf{?}\ \mathbf{T} \cdot\ \mathbf{(h_{fin}^{2} \cdot d \cdot H \cdot k)^{1/3}}$$

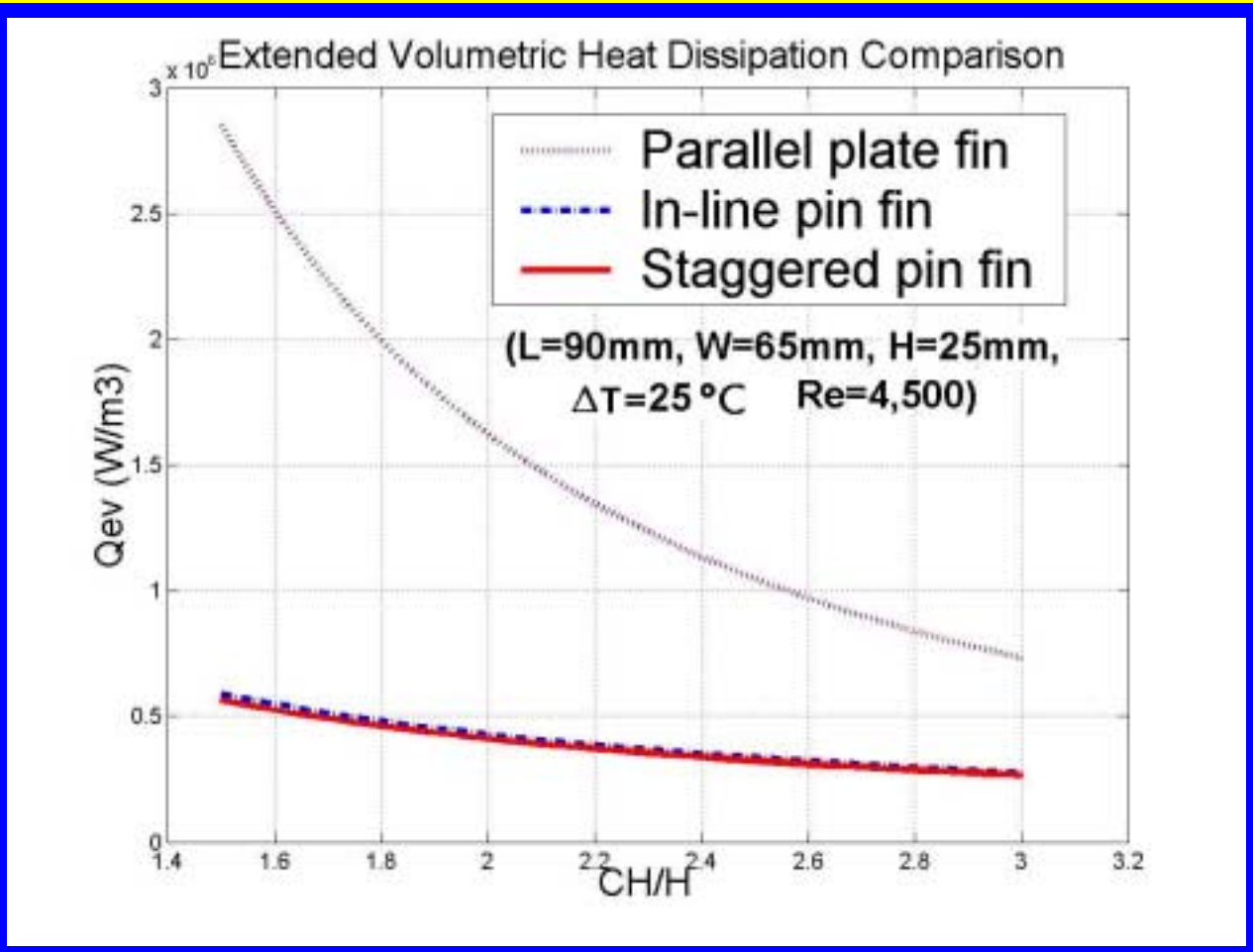
Where,

? T: array base-ambient temperature difference

Optimization Summary
(L=90mm, W=65mm, H=25mm, CH/H=3)

Heat sinks	Fin heat transfer coefficient, h_{fin}	Fin thickness d	Fin to fin spacing b	References
	[W/m^2-K]	[mm]	[mm]	
Parallel plate fin	156	0.5	1.8	Jonnson (2001)
In-line pin fin	203	3.0	4.5	Copeland (2000)
Staggered pin fin	225	3.3	5.0	Chyu (1998)

Effect of Duct Height/Heat Sink Height Ratio



Jonsson & Moshfegh (2001)

Conclusions

- With the least-volume optimization approach, we are able to optimize the choice of the heat sink design for BI air solutions.
- Previous experimental results of air-cooled heat sinks appropriate for BI solutions are not always consistent.

Future Work

- Theoretically analyze the contradiction of existing correlations of heat sinks, especially where CH/H goes to 1 (no air bypass);
- Numerically verify the existing Nusselt correlations of different kinds of heat sinks;
- Experimentally analyze the optimal volumetric heat transfer of heat sinks for BI

Questions ?

TEC

Thermo Electric Coolers, Are They for Everyone?

Giray Kaya
Reliability Inc.
Houston, TX

What do they do?

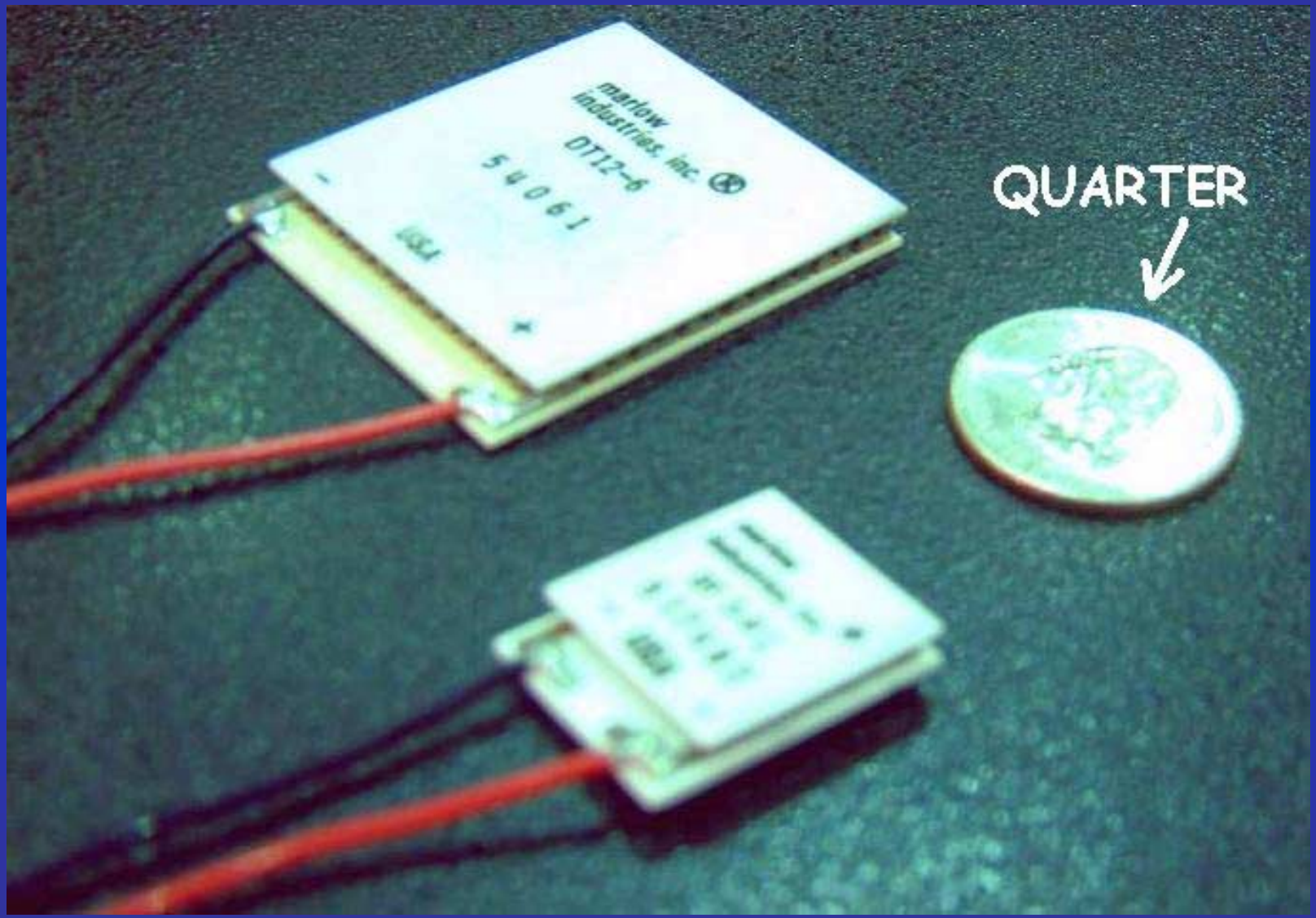
- Apply voltage across the leads
  - One side gets hot
  - Other side gets cold
- Switch polarity
  - Hot side gets cold
  - Cold side gets hot

Looks promising for control. The TEC can cool and replace the heater in the heat sink.

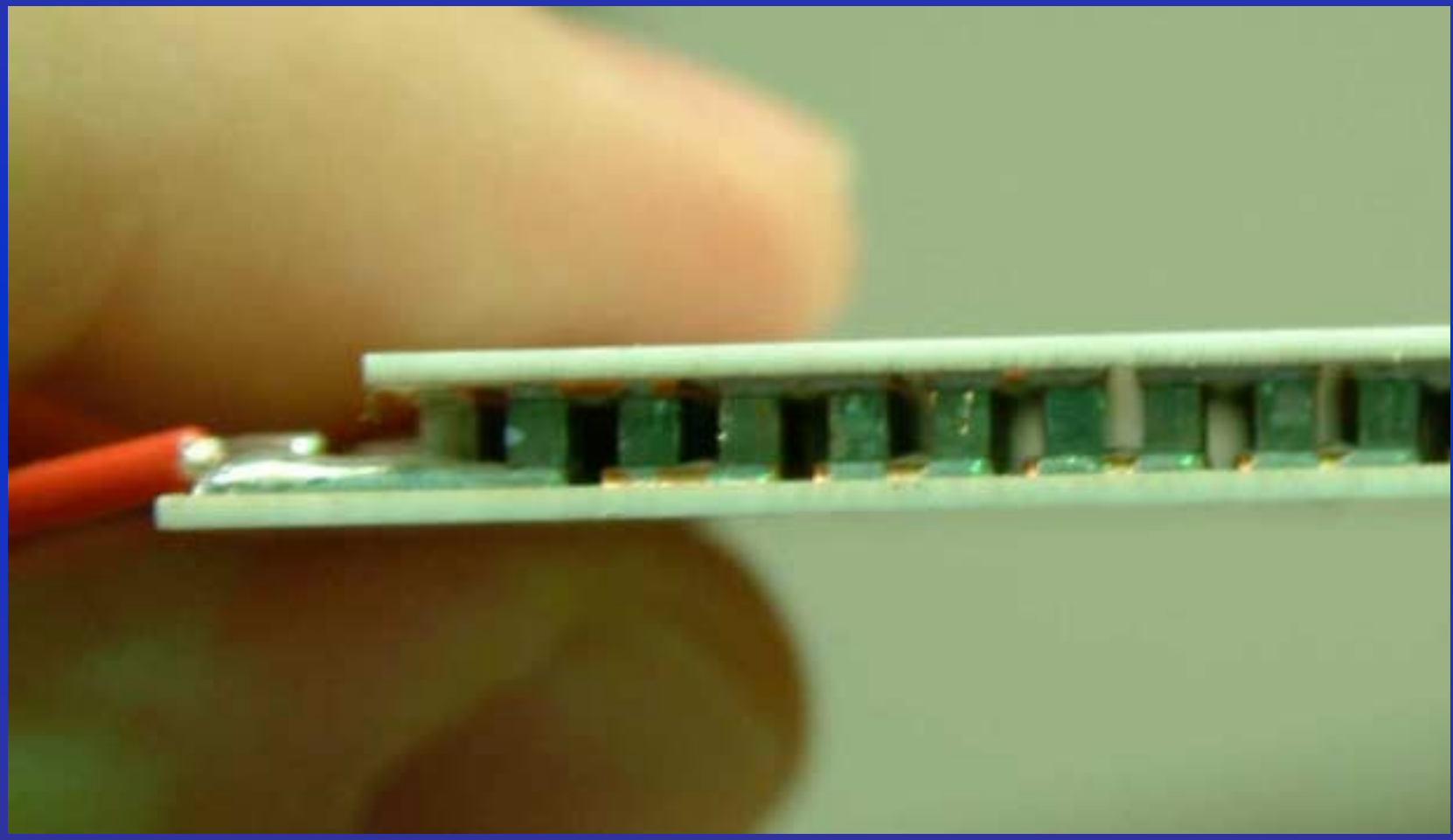
What do they look like?

- Different sizes (3 sq in to 0.5 in sq in)
- Square and rectangular
- Varying thickness (0.10 - 0.15 in)
- Two leads (**+** and **-**)
- About 43% air by volume
  - Hurts thermal path

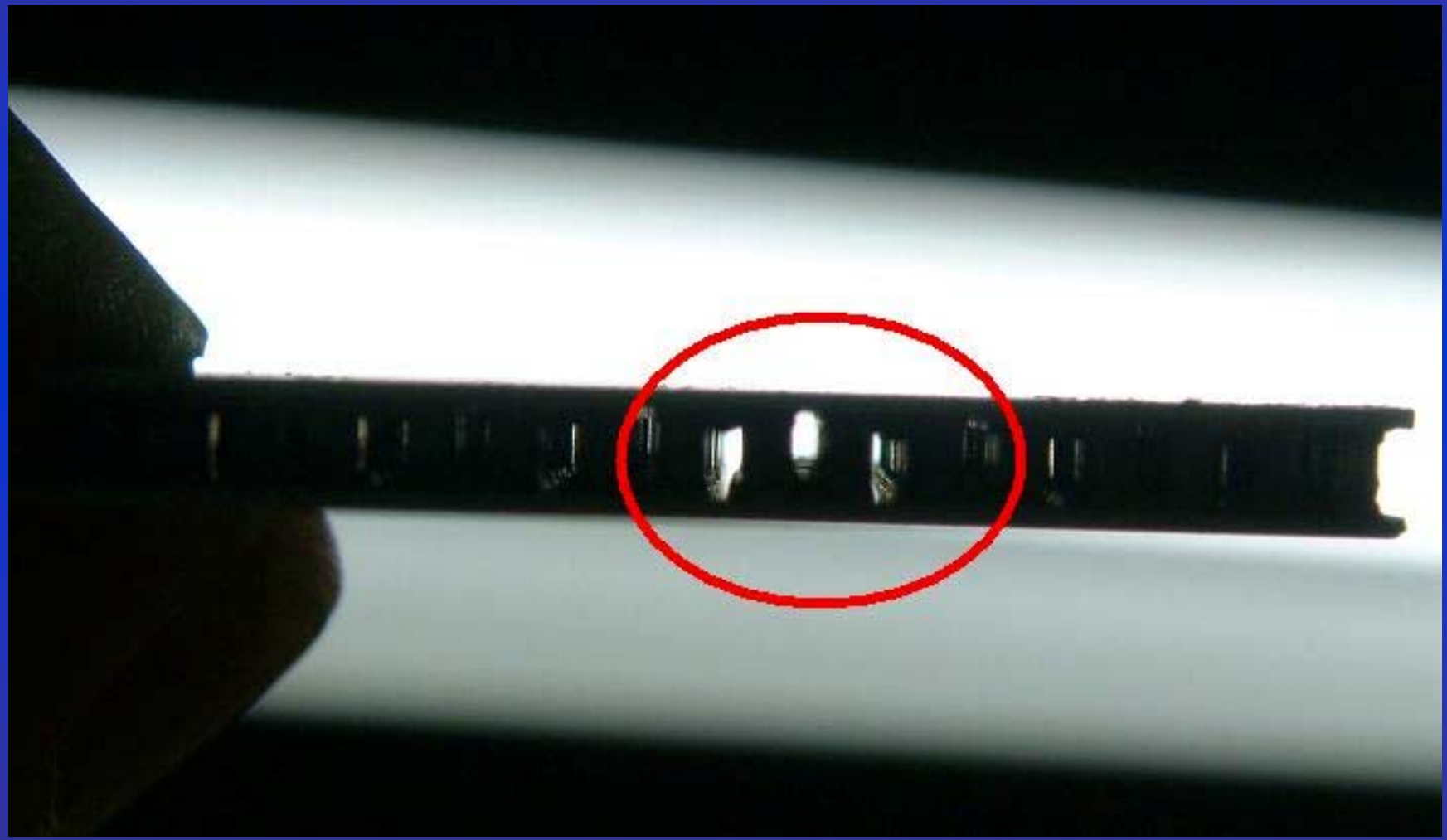
Sample Sizes



p-type and n-type pairs in series



A lot of air inside.



Who uses TECs?

Conventional Thermal System: Heat sink cools the device, but device temp never drops below ambient.

TECs are great when ambient is too hot.

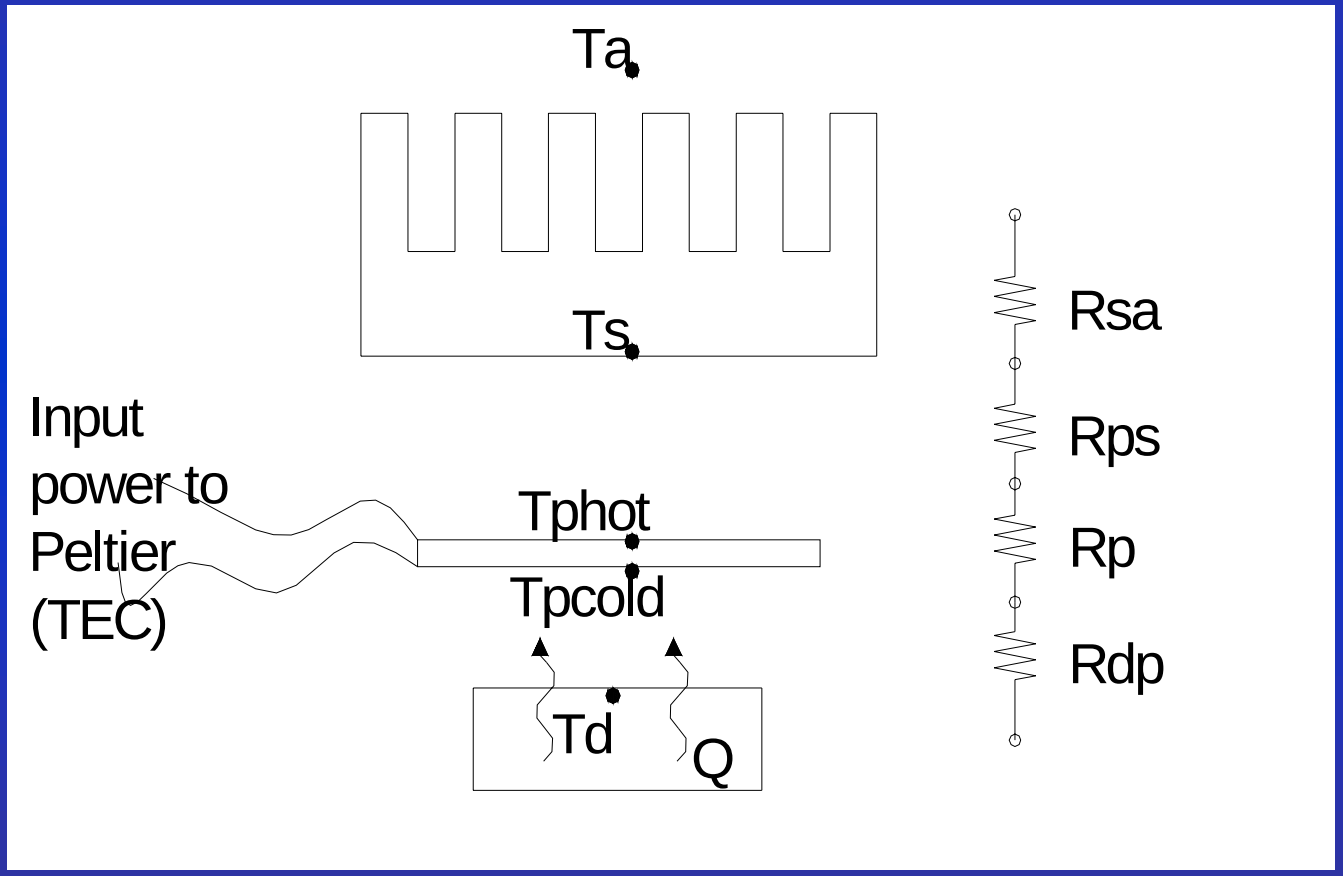
- Fancy beer coolers
- Sealed enclosures

During Burn-in:
Are devices controlled to below ambient temperature?

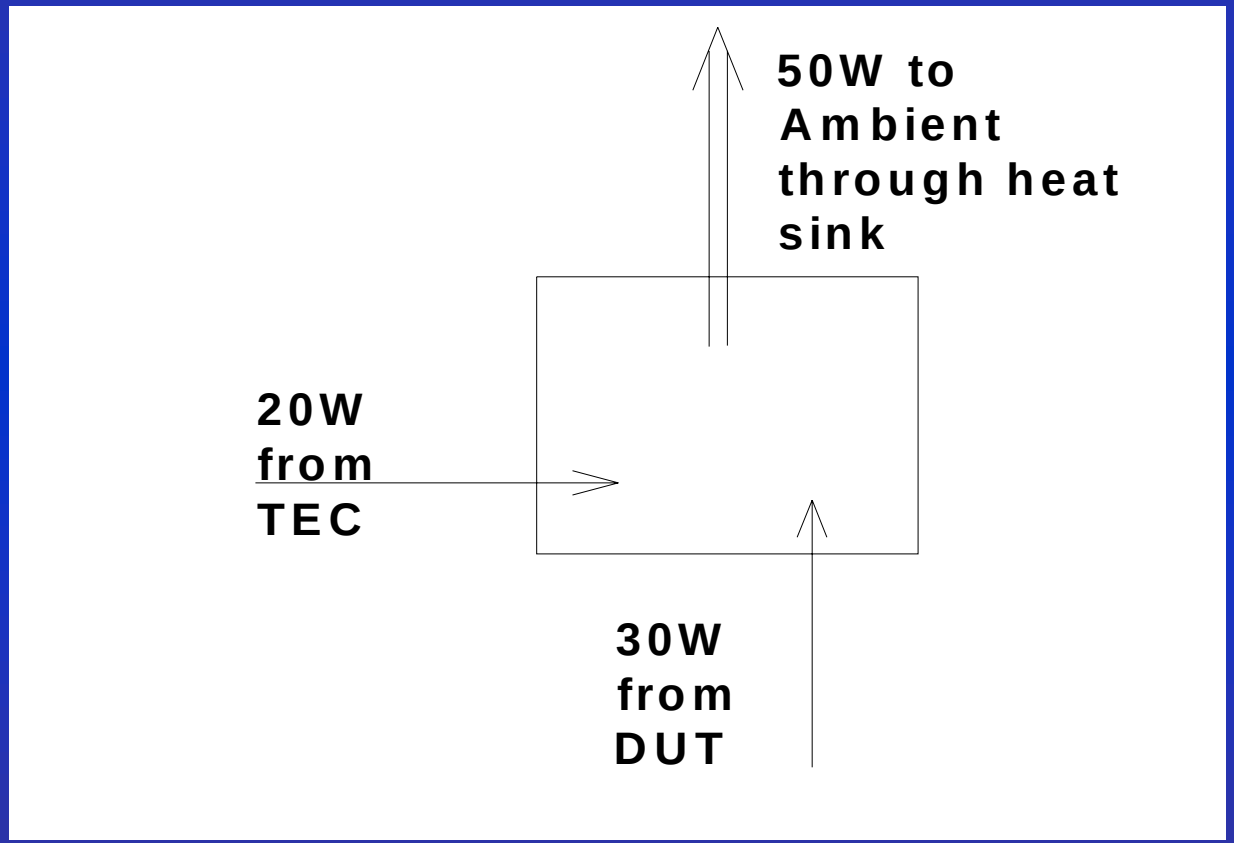
During Burn-in:
Are devices controlled to below ambient temperature?

No.

The Setup

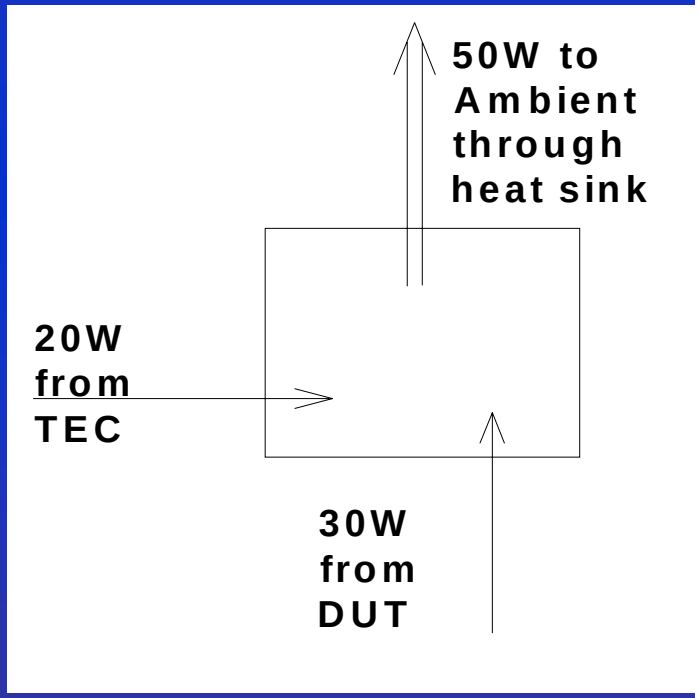

Ta
Ts
Input
power to
Peltier
(TEC)
Tphot
Tpcold
Td
Q
Rsa
Rps
Rp
Rdp

Always have a Control Volume



Disclaimers:

- Control volume is ideal case
  - Does not account for Q_{loss}
- TEC Inefficiencies
  - *You will NOT get to "dial-up" DUT power by 20W just because a 20W TEC was added.*



Power Density Levels

- Higher power TECs are 35 to 40W.
- Could not find any 200W or 300W TECs.

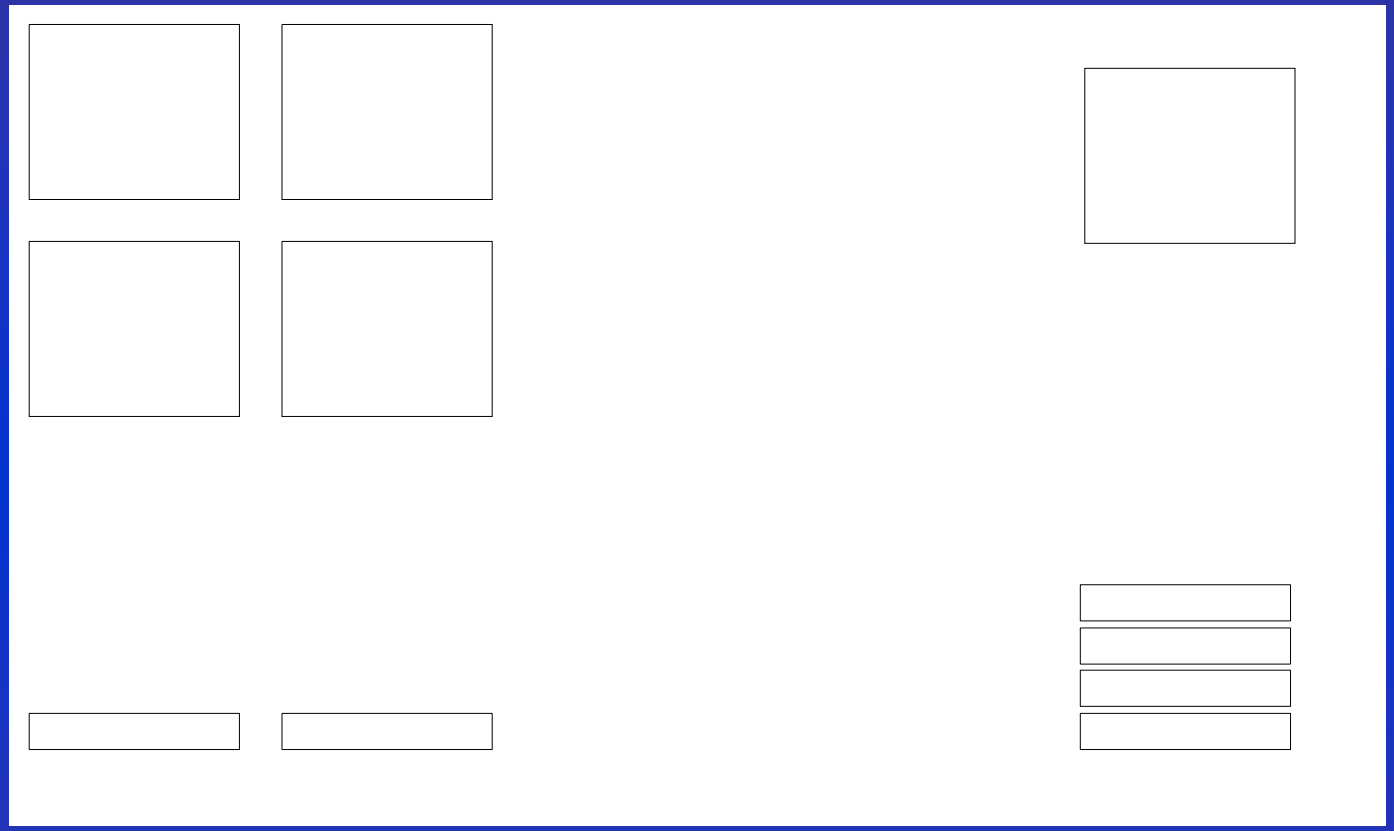
Power Density Levels

- Higher power TECs are 35 to 40W.
- Could not find any 200W or 300W TECs.

Not to fear, we can do the following….

Side by Side

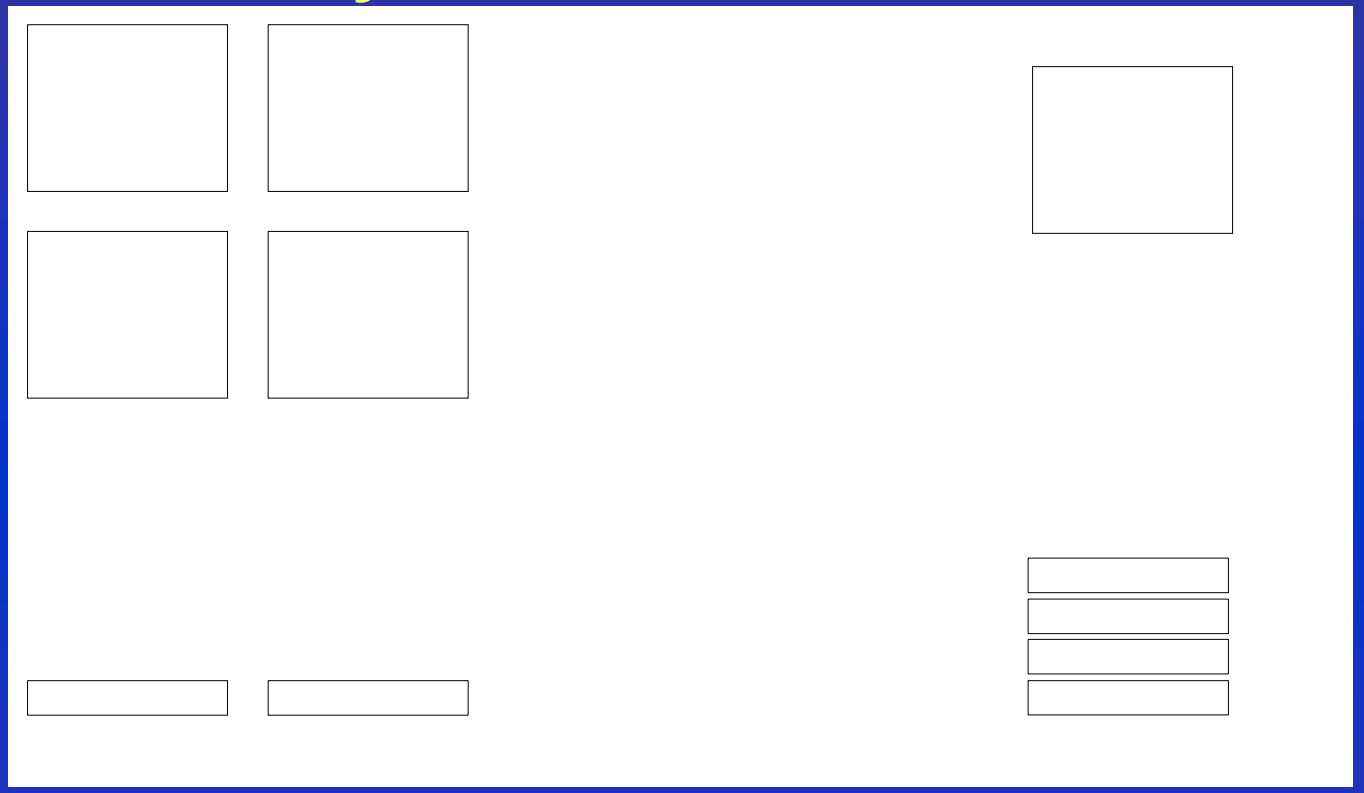
Stacked



…. Or can we?

Side by Side

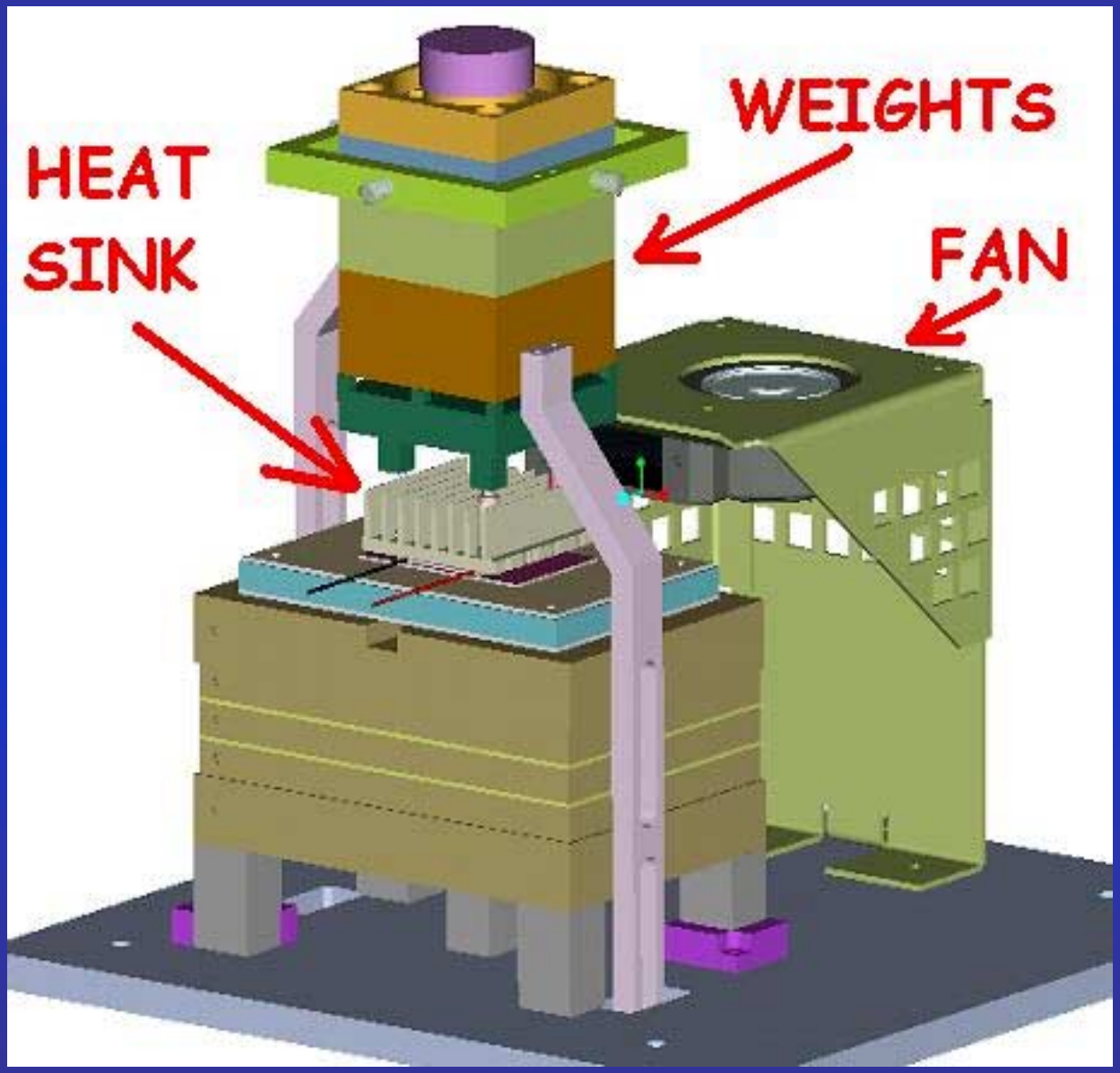
Stacked



Not enough physical room

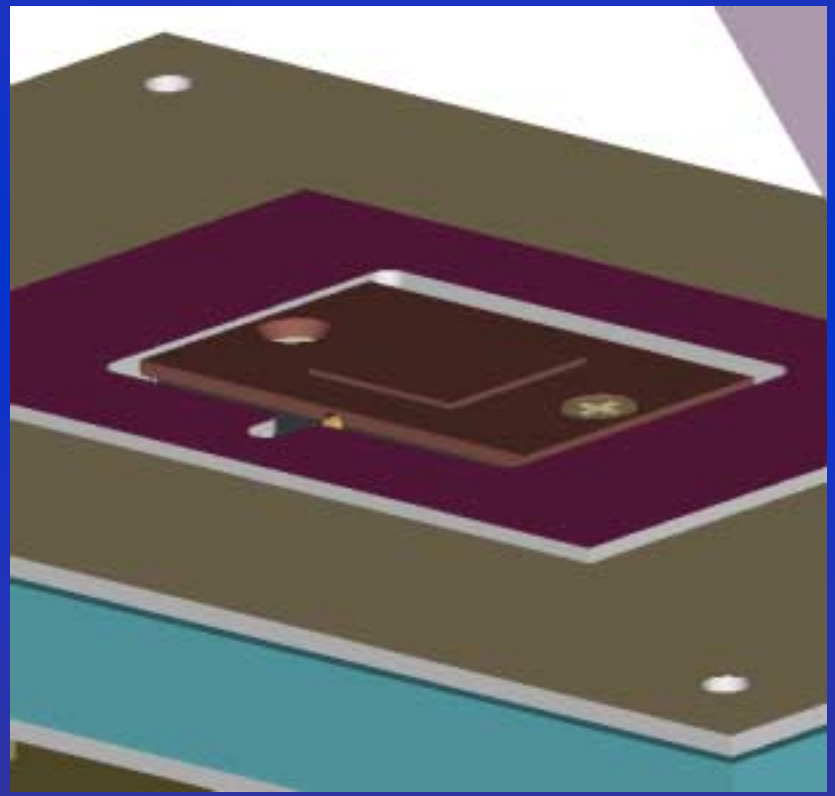
Not enough power delivery

Test Fixture

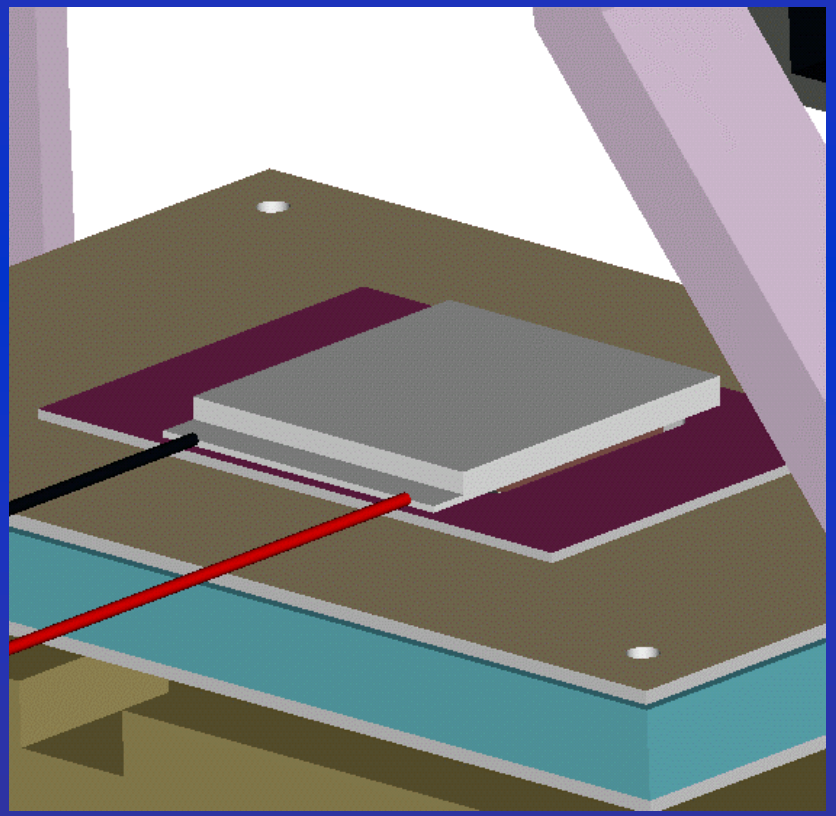


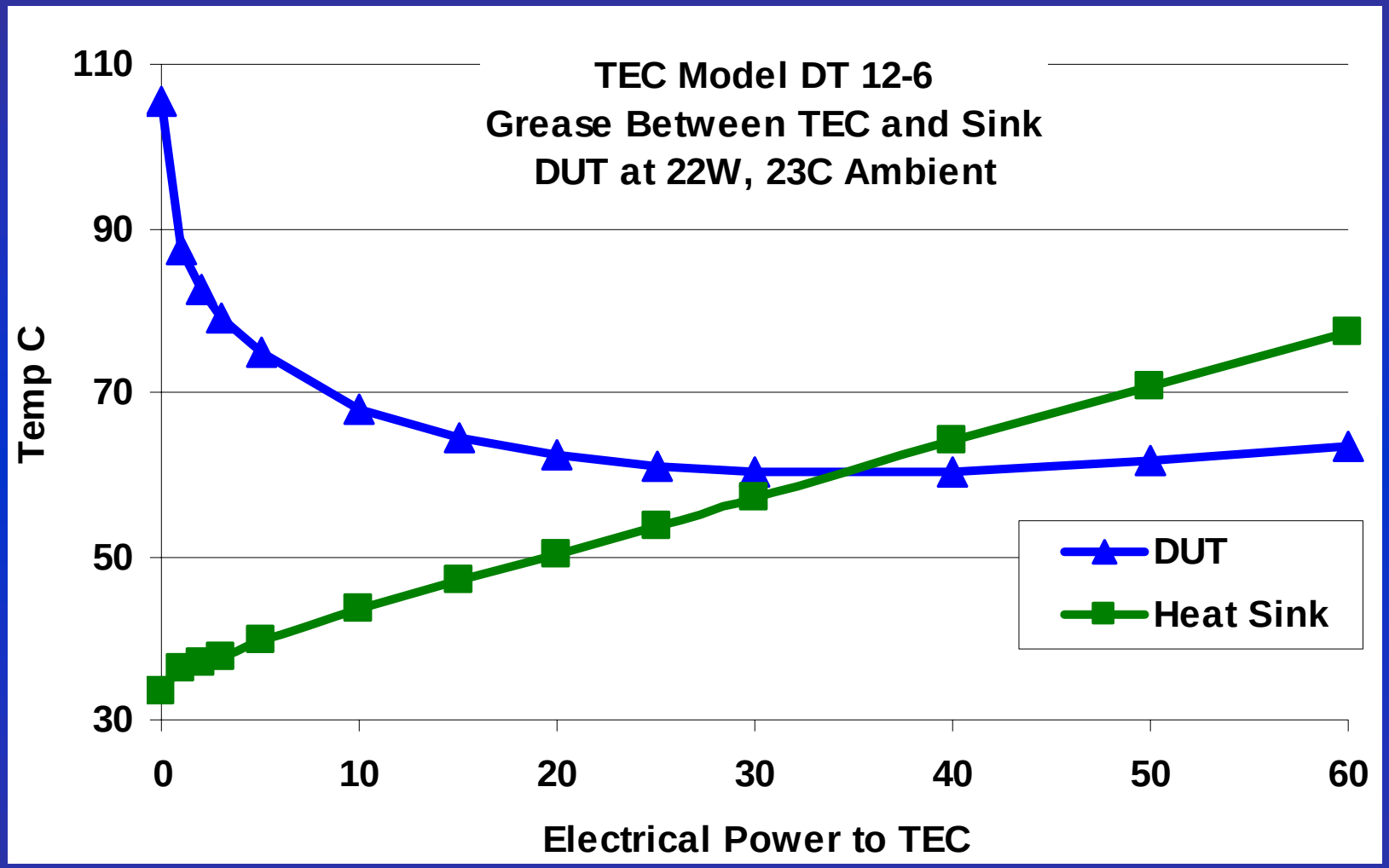
Close-up

DUT

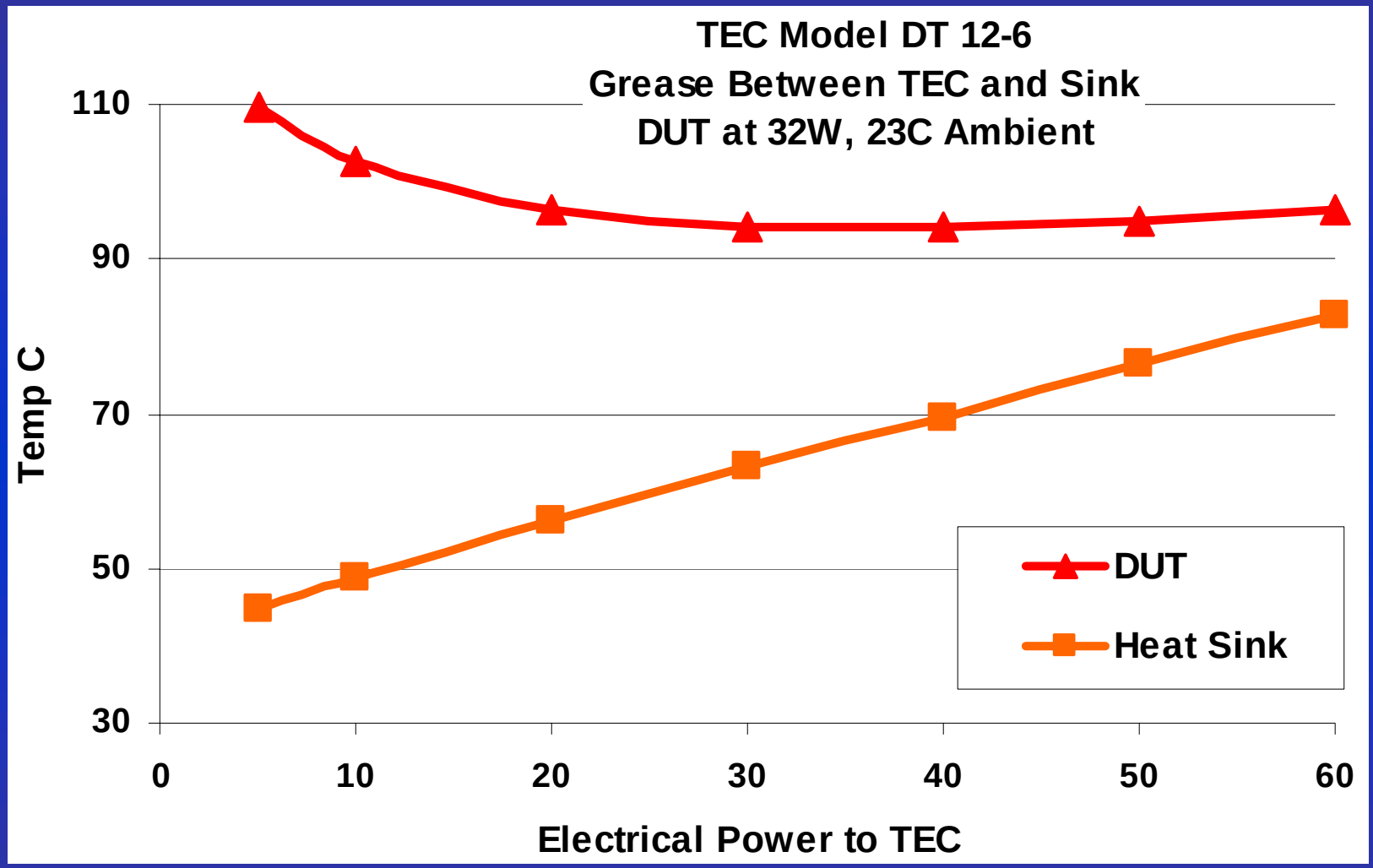


TEC on the DUT

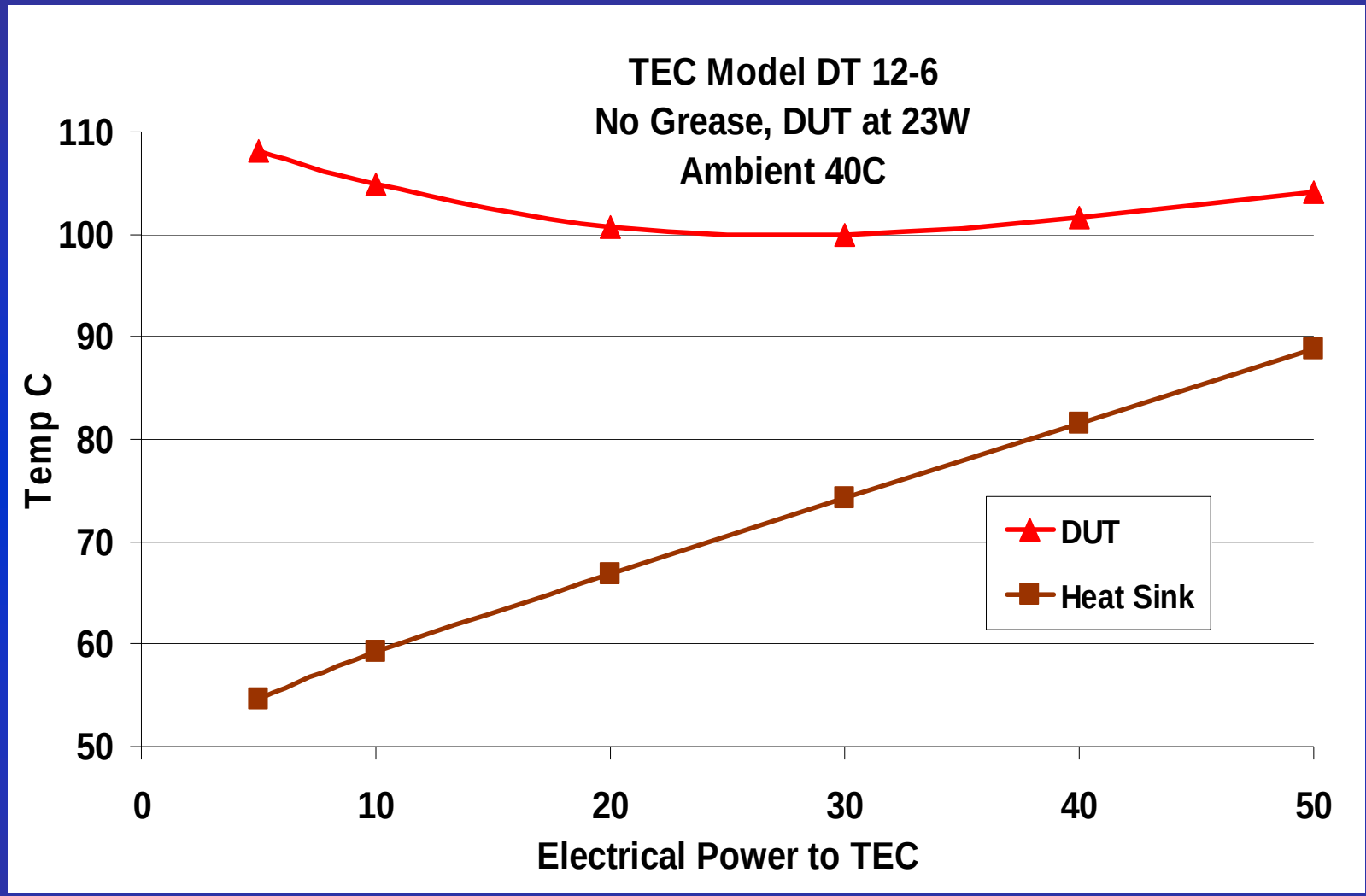




- Note the decreasing benefit as TEC power is increased.



- Note the decreasing benefit as TEC power is increased.



- Note the decreasing benefit as TEC power is increased.

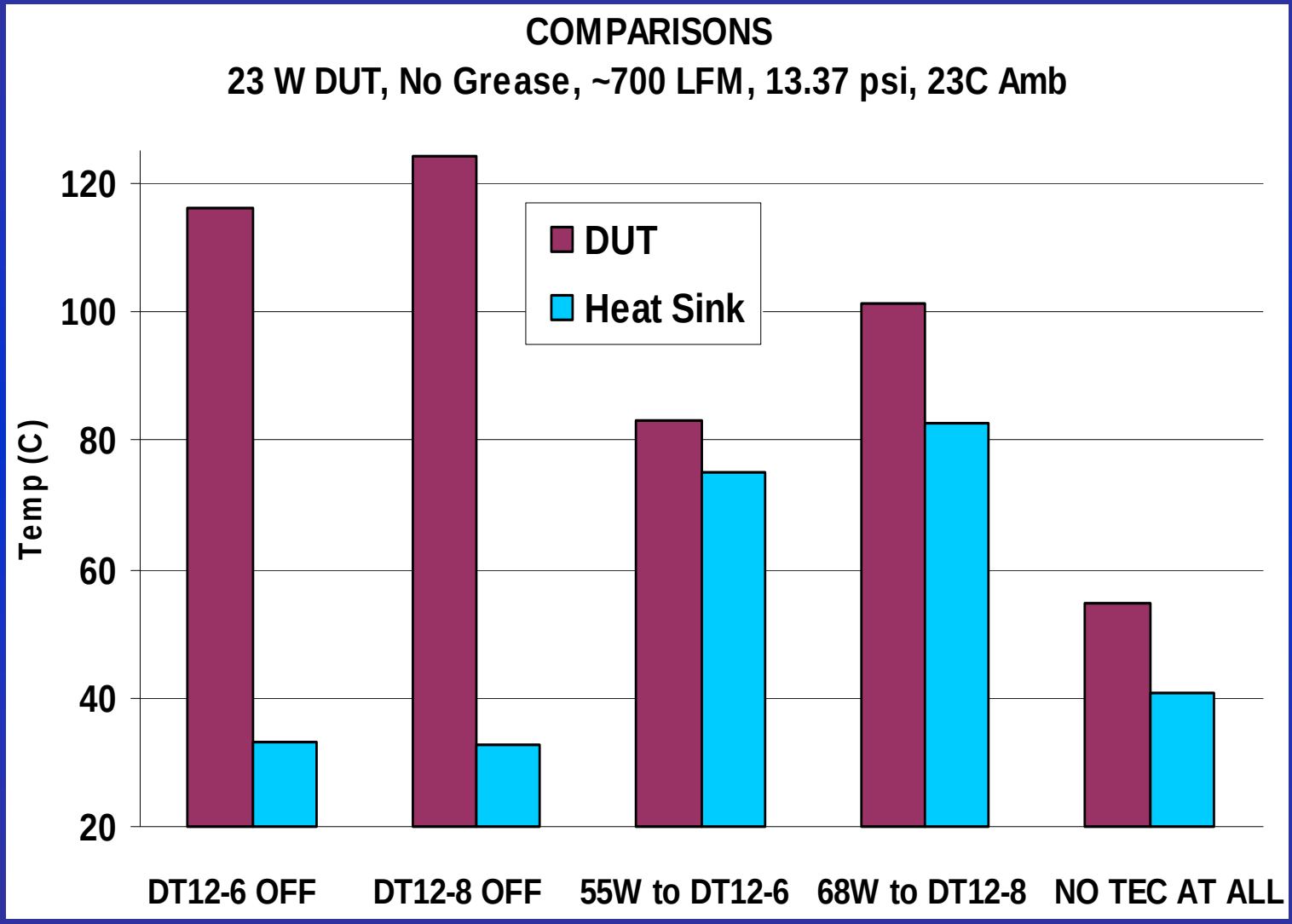
Manufacturer Recommendations

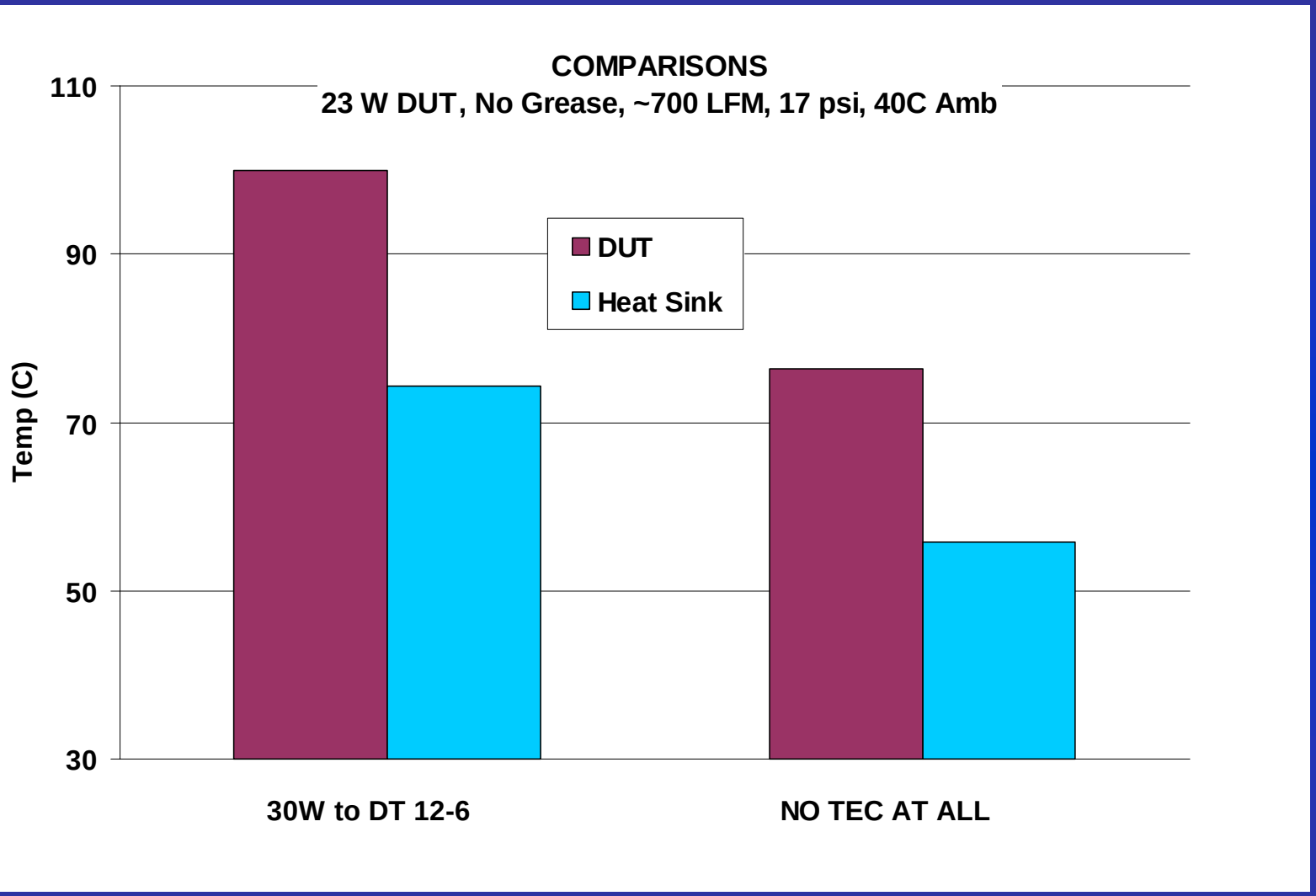
Do not power cycle (ON/OFF) the TEC excessively. But we need to control!

Maximum reliability is below 85C.

System thermal response is quicker without the TEC's mass.

Two Very Important Slides




COMPARISONS
23 W DUT, No Grease, ~700 LFM, 17 psi, 40C Amb
110
90
70
50
30
Temp (C)
DUT
Heat Sink
30W to DT 12-6
NO TEC AT ALL

Last two charts were ugly.

- Introduction of TEC into thermal path increases thermal resistance so much that we are better off without the TEC.
- Thermal resistance is so high, Thermal Control will not have the opportunity to use the TEC as a heater. Polarity will be set to “cooling mode” always.

One last point…

…almost done….

Adjust DUT power to keep DUT Temp at 110C (23C Ambient)

- With TEC model DT12-6:
  - 0W TEC means 23W DUT
  - 20W TEC means 34W DUT
- With TEC model DT12-8:
  - 0W TEC means 24W DUT
  - 20W TEC means 36W DUT

DUT power levels that keep DUT Temp at 110C (23C Ambient)

- With TEC model DT12-6:
  - 0W TEC means 23W DUT
  - 20W TEC means 34W DUT
- With TEC model DT12-8:
  - 0W TEC means 24W DUT
  - 20W TEC means 36W DUT

How do we do if the TEC is removed?

DUT power levels that keep DUT Temp at 110C (23C Ambient)

- With TEC model DT12-6:
  - 0W TEC means 23W DUT
  - 20W TEC means 34W DUT
- With TEC model DT12-8:
  - 0W TEC means 24W DUT
  - 20W TEC means 36W DUT
- **Without any TEC in the system:**
  - **65W DUT < < < W I N N E R > > >**

Efficiency Cont'd:

We have a 6W DUT and 40C Ambient.

How much TEC power is needed to keep our 6W DUT at 40C?

- **0W**
- **6W**
- **More than 6W**

Efficiency Cont'd:

We have a 6W DUT and 40C Ambient.

How much TEC power is needed to keep our 6W DUT at 40C?

- **0W** **(I haven't been listening.)**
- **6W** **(I bet this is a trick question.)**
- **More than 6W** **(My test conditions gave 8W.)**

Continued Testing

- Retest with different configurations that move the TEC away from the direct heat path.
- (TEC will need heat removal too.)