BiTS

Burn-in & Test Socket Workshop

WELCOME

March 2 - 5, 2003
Hilton Phoenix East / Mesa Hotel
Mesa, Arizona

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Test Technology Technical Council

tttc™

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Burn-in & Test Socket Workshop

Technical Program

Session 1
Monday 3/03/03 8:30AM

Test And Burn-in Operations

"Full Wafer Contact Burn-In And Test - The Ultimate In Parallelism"
Steve Steps - AEHR Test Systems

"Strategic Use Of Burn In"
Tamas Kerekes - NplusT Semiconductor Application Center S.r.l.

"A Flexible Electrical Interface Design For The Fixture Between Tester And DUT To Achieve Reduced Cost And Leadtime In ATE Toolings"
Koh Tuan Meng - Micron Semiconductor Asia
Lim Kok Lay - Micron Semiconductor Asia
(Presented by: Steve Hamren - Micron Semiconductor)

Full Wafer Contact Burn-In and Test – The Ultimate in Parallelism?

2003 Burn-in and Test Socket Workshop

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Steve Steps
Aehr Test Systems

Agenda

- Test During Burn-in Evolution
- Burn-in Process Evolution
- Test Evolution
- Convergence Point
- Conclusions

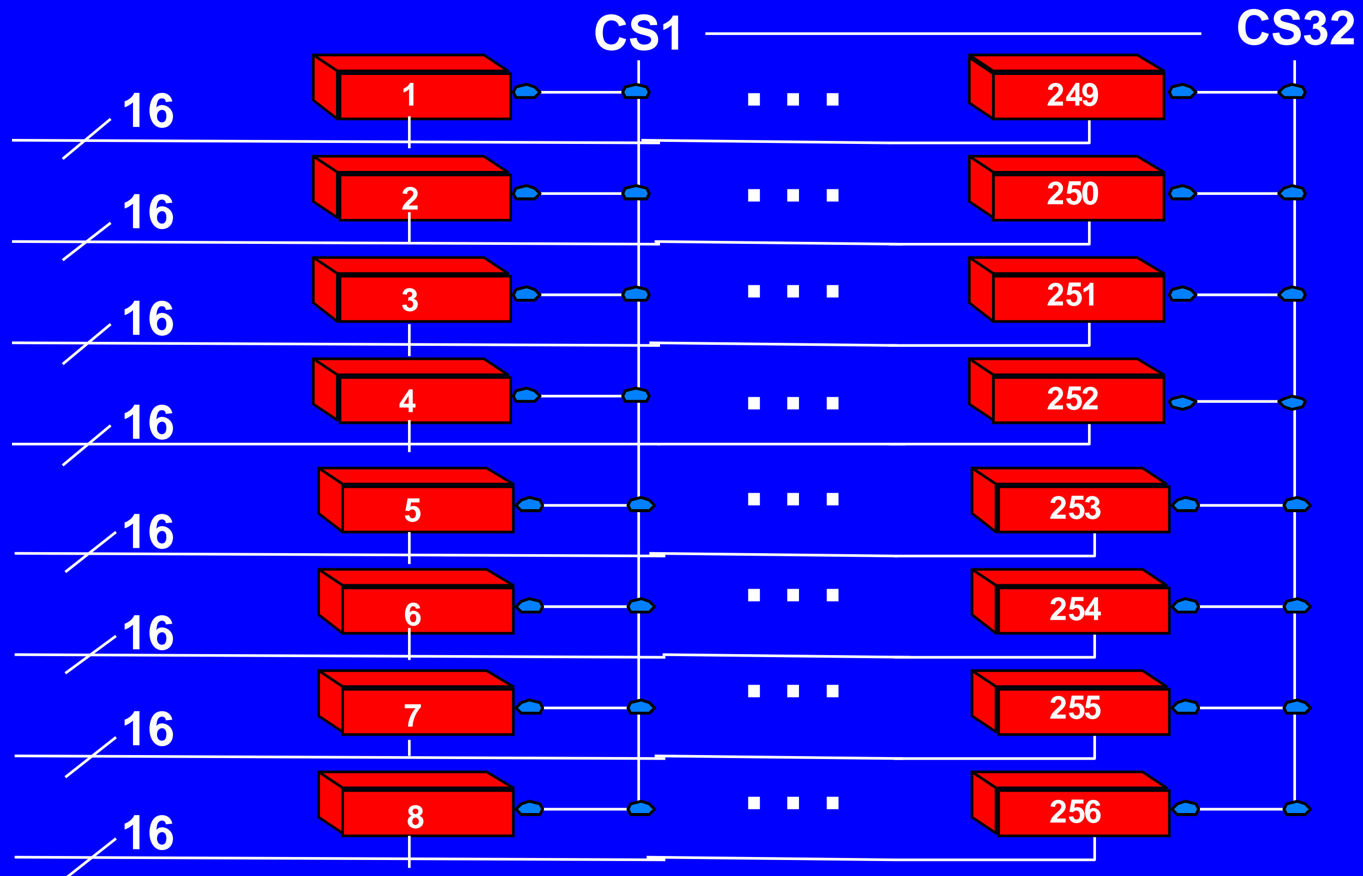
Test During Burn-in Evolution

- **Bake**
- **Static Burn-in (Power only)**
- **Dynamic Burn-in (Plus input)**
- **Output Monitoring Burn-in (Check some outputs)**
- **Burn-in and Test (Full functional test)**

All performed highly parallel

Parallel Testing

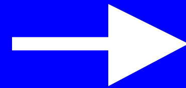
128 Tester I/O Channels X 32 CS = 4096 Total Device I/O Pins

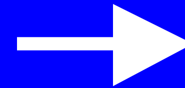


Value of Offloading Final Test

- If the burn-in system can perform a given test, it can be much cheaper
- Opportunity to perform tests at the same time as burn-in
- Experience has shown as much as 80% of final test time can be performed during burn-in

Traditional Test Process



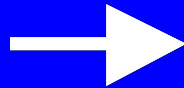


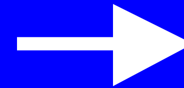
Pre Burn-in Test
- DC Parametrics Test
- Gross Functional Test

Monitored Burn-in
- Dynamic Stressing
- Long Functional Test

Final Test
- DC Parametrics Test
- AC Parametrics Test
- Speed Sort
- Pattern Sensitivity Tests
- Long Cycle Time Tests
- Data Retention Tests
- Refresh Tests

Parallel Test During Burn-in





Pre Burn-in Test
- DC Parametrics Test
- Gross Functional Test

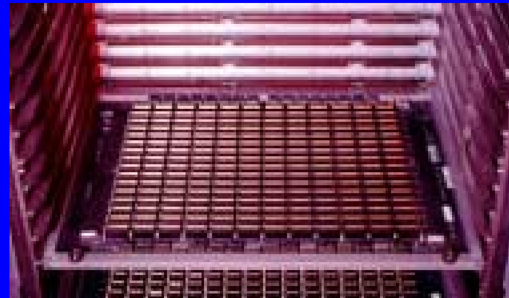
Massively Parallel Test
- Dynamic Stressing
- Long Functional Test
  - Pattern Sensitivity Tests
  - Long Cycle Time Tests
  - Data Retention Tests
  - Refresh Tests

Final Test
- DC Parametrics Test
- AC Parametrics Test
- Speed Sort

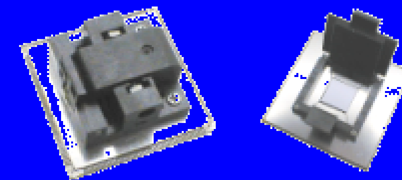
Test Offload

Burn-in Process Evolution

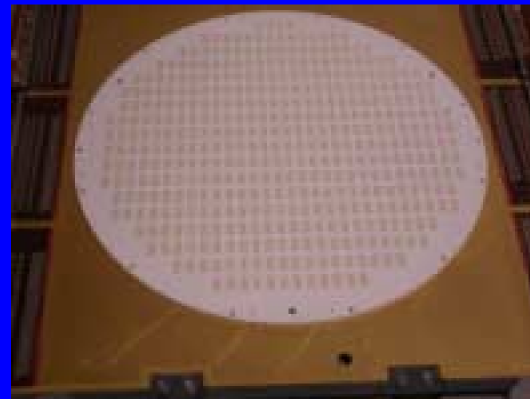
- Assembly/System
- Packaged part



- Bare die

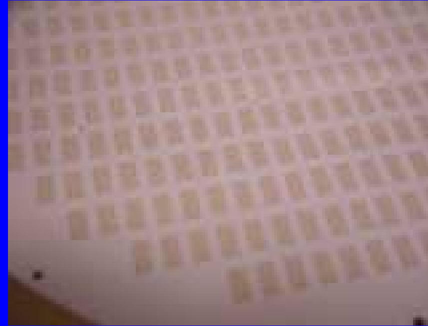


- Full Wafer

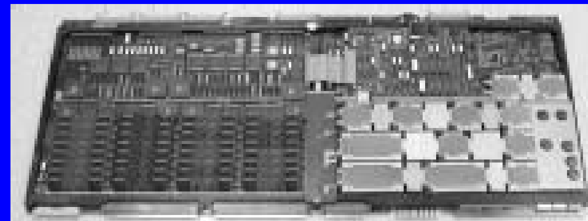


Wafer-Level Burn-In and Test

- **Full Wafer Contact**



- **Full functional test capability**



- **Thermal Stress Chamber**

Progression To Wafer-Level

- Reduce repair cost of burn-in fallout
  - More critical if assembly non-repairable
  - Reduce excessive burn-in
- Reduce wasted packaging/assembly
- Faster feedback to front-end
- KGD for SIP, MCM, etc. requires either bare die or wafer-level burn-in

Test Evolution – External Test

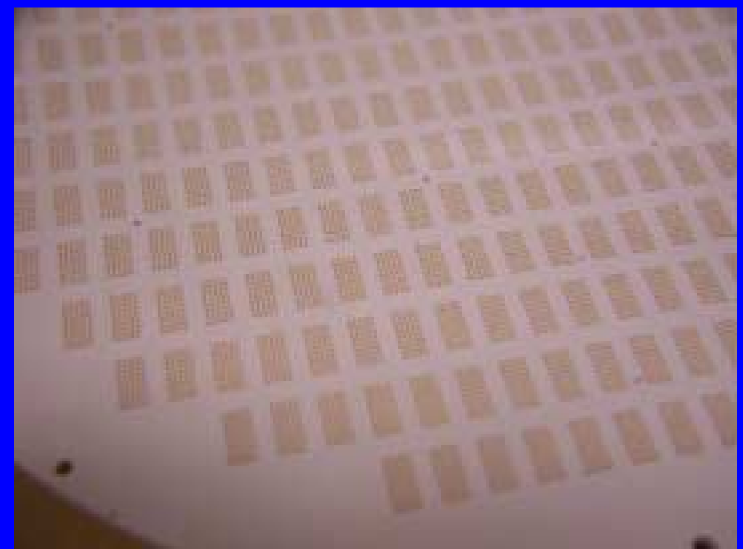
- Full I/O speed
  - Cost per channel very high ($Ks/channel)
  - Signal cable must be very short
  - GHz testing very difficult
- Full I/O width
  - One channel per device pin
  - Total device count per test very limited

Test Evolution – Structural Test

- Typically scan chain based
- External data clock speed requirements vastly reduced
- On chip ATPG
  - I/O width significantly reduced (compressed)
  - Still can have edge timing constraints
- Logic BIST
  - Device pin I/O speed << Test speed
  - Very narrow I/O (e.g., 5 pin IEEE 1149.1)
  - Lower cost channels possible (~$100/channel)
  - Paralleling devices on channels possible (<$5/device I/O)

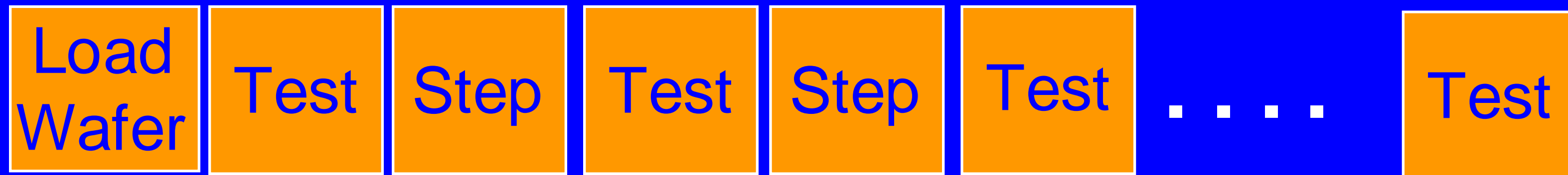
Wafer-Level Burn-in with BIST

- Logical convergence of:
  - Test During Burn-in Evolution (Full functional)
  - Burn-in Process Evolution (Wafer-level)
  - Test Evolution (Logic BIST)
- Key enabling technologies:
  - Full wafer contact
  - Massively parallel testing
  - Logic BIST



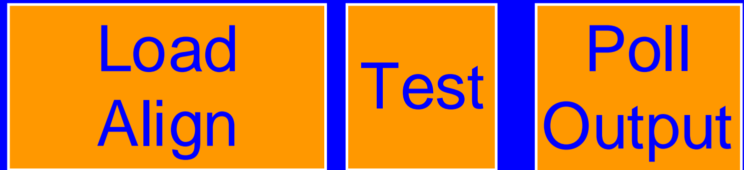
Wafer-Level Logic Test, no BIST

Using 4 site tester:

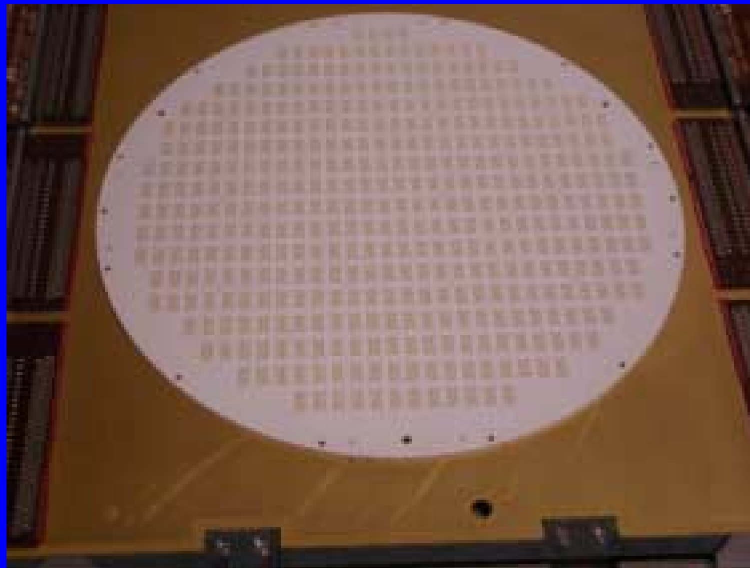


For 300 die wafer, about 80 Test cycles

Wafer-Level Logic Test, BIST



Only one test cycle required



20-40x Time Reduction!

Conclusion

- Wafer-Level burn-in and test using BIST is next step in evolution for test during burn-in
- Higher percentage of test can be performed during burn-in and thus offloaded from high speed final test

Strategic Use of Burn In

2003 Burn-in and Test Socket Workshop

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Tamas Kerekes

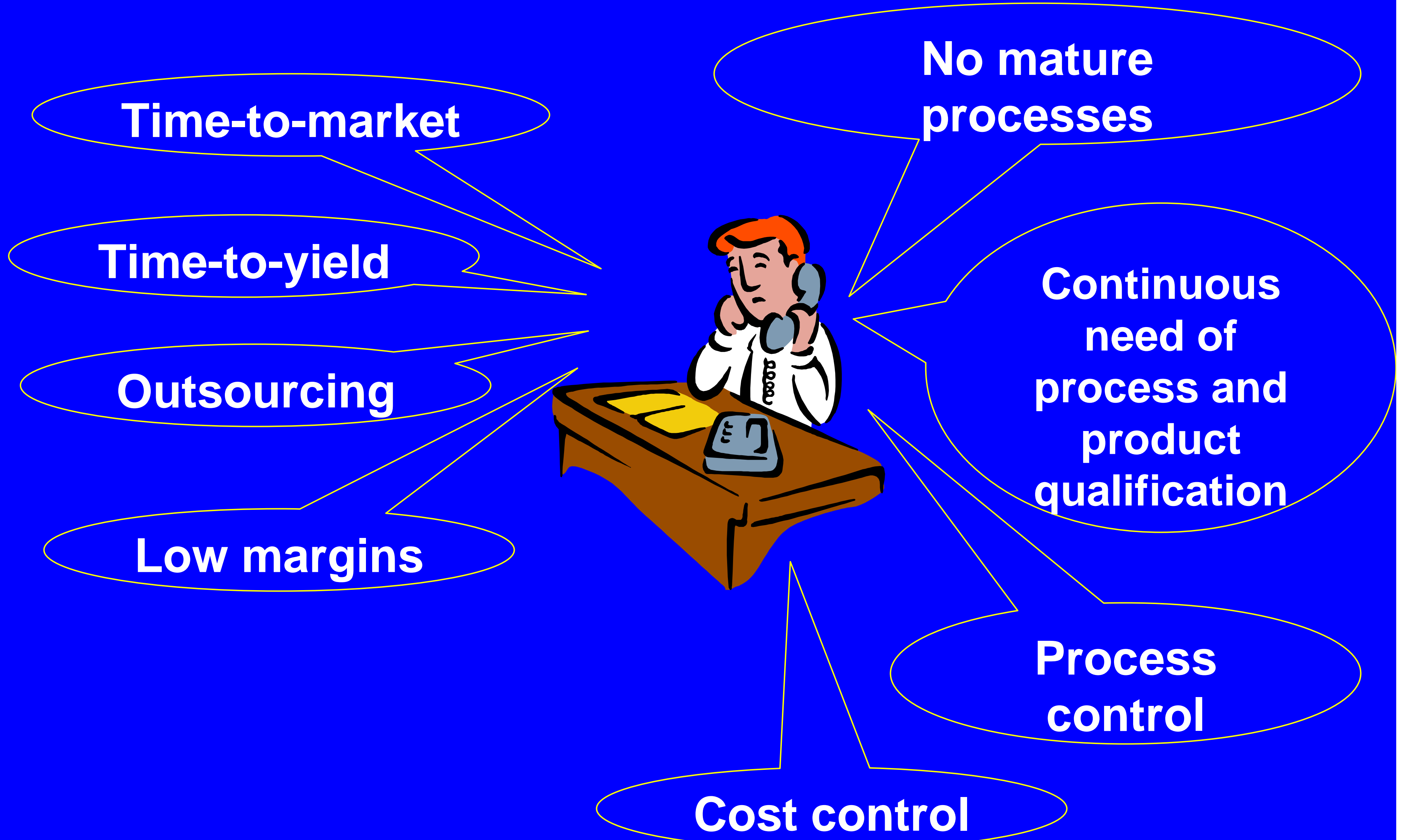
ELES Semiconductor Equipment

Agenda

- Pressure on the Burn-In
- Possibility of Adding Values
- Technical Solutions for Doing this
- Case Studies

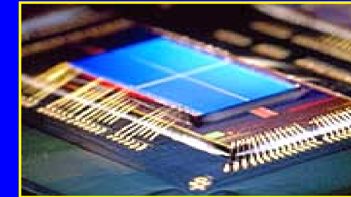
Pressure on the Burn-In

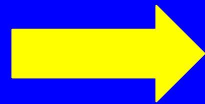
Market Trends



Technology Trends

- Low geometry
- High transistor count
- Integration, system-on-chip, analog behavior
- New packages





- High frequency
- Low voltage, high power
- Non-deterministic timing
- High IO count
- Critical reliability

- Expensive sockets
- Multi-layer, fine-pitch boards
- Thermal control
- High performance electronics
- Need of qualified engineering

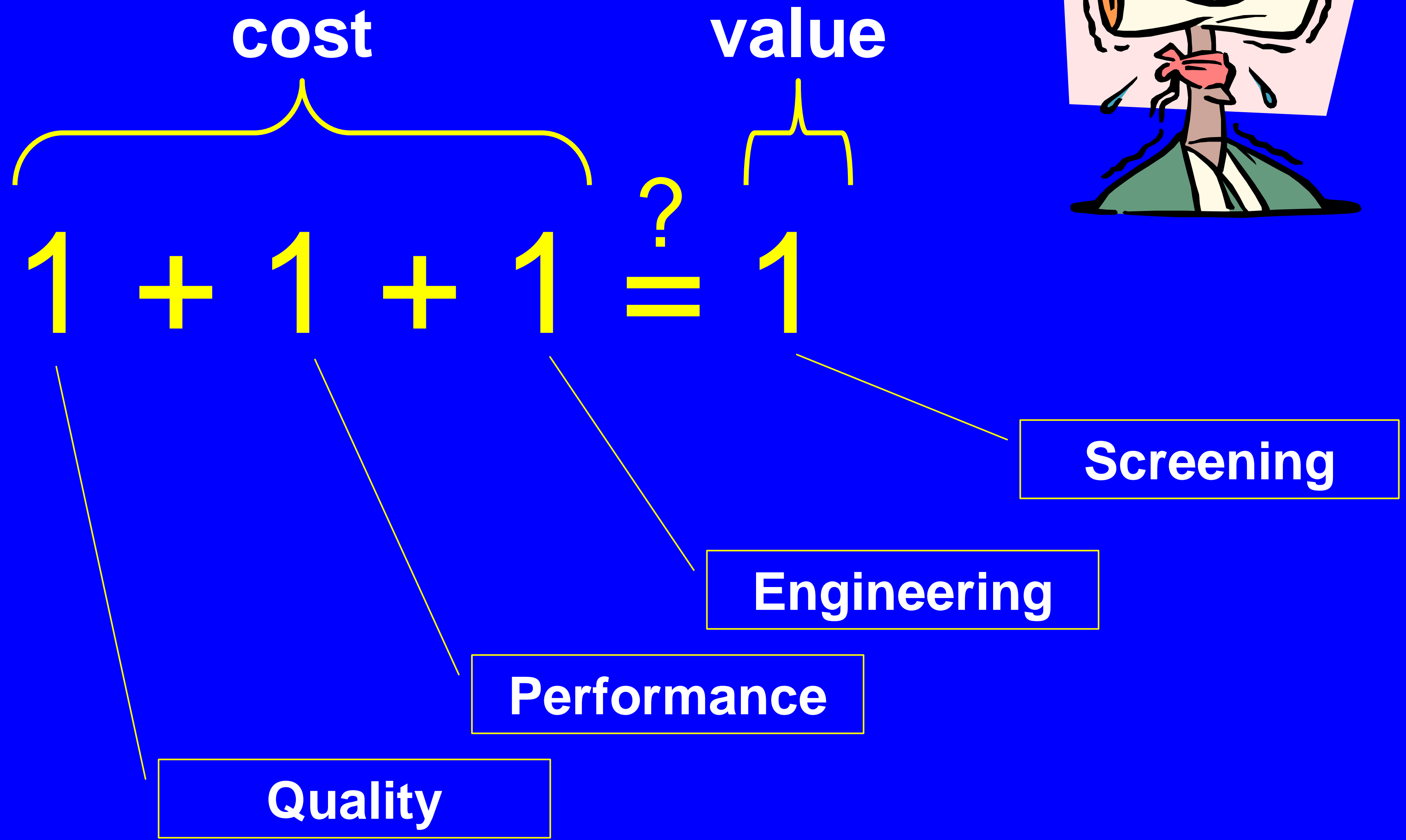
Keeping pace with the Moore law

requires huge R&D and engineering

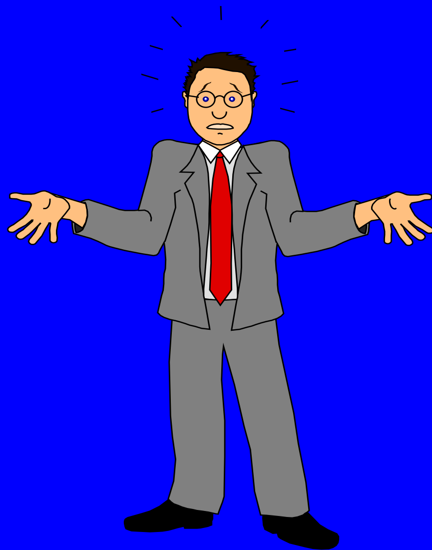
… and …

it costs !

Dilemma



Costs and complexity are strictly related to the elementary function of the burn-in:



detecting weakness of products and processes

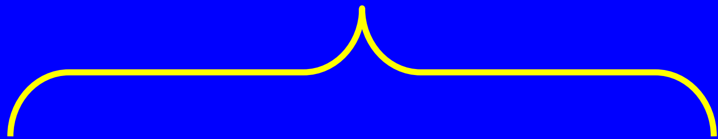
…

… thus there is no easy way to reduce or avoid these expenses

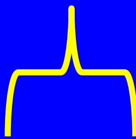
Increasing the Value of Burn-In

New Equation

cost



value



1 + 1 + 1 = 3

?

Screening +

Engineering

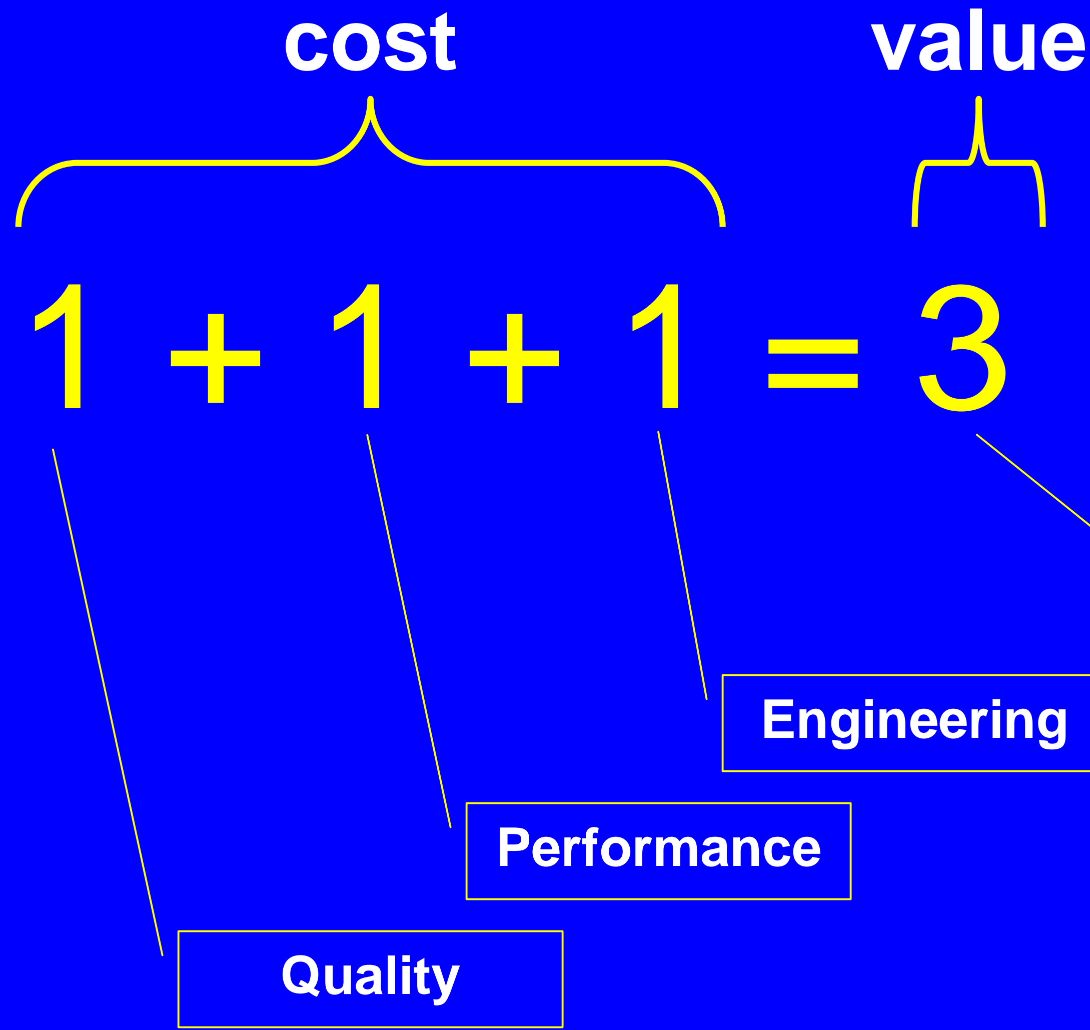
Performance

Quality

Possible Added Values

- Yield increase
- Test time saving
- Efficient management of the burn-in area

The Equation Again



Yield Increase

- During ramp-up (time-to-yield)
- During manufacturing cycle (process control)
- Requires:
  - Detailed on-line reliability data generation
  - Real-time data processing
  - Automated feedback of the data

Test Cost Saving

- Manufacturing - Goals
  - Reduced test-time on ATE
  - Better quality control in the production cycle
- Operations
  - TDBI (full burn-in)
  - Batch Testing (when no burn-in is required)
- Qualification
  - Replacement of the intermittent test on ATE with continuous in-line testing
- Not only for memories

Area Management

- Statistical Process Control
  - Utilization tracking
  - Maintenance tracking
  - Defect analysis
- Area Control
  - Lot tracking
  - Scheduling
  - Integration
- Expert System
  - “tell the operator what to do”

Technical Solutions

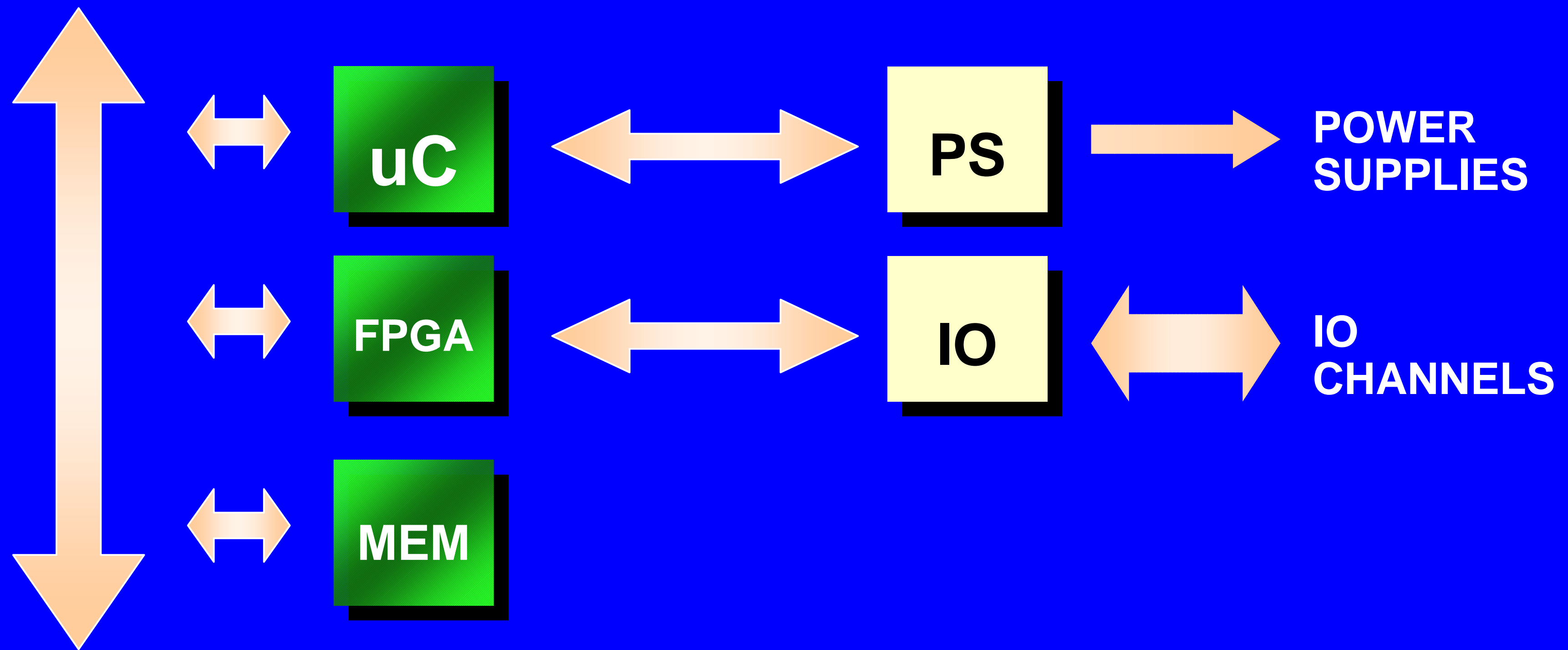
Key Factors

- Equipment
- Data management
- Organization and methodologies

Equipment

- Full use of DFT methodologies, for increased visibility
  - Scan, JTAG, SoftBIST, …
- Coverage of a wide range of devices (in the same chip)
  - Analog, digital, memory
- Flexible, programmable test flow
  - Functional tests
  - Characterizations (smoo, bitmap, …)
- Flexible, programmable data generation

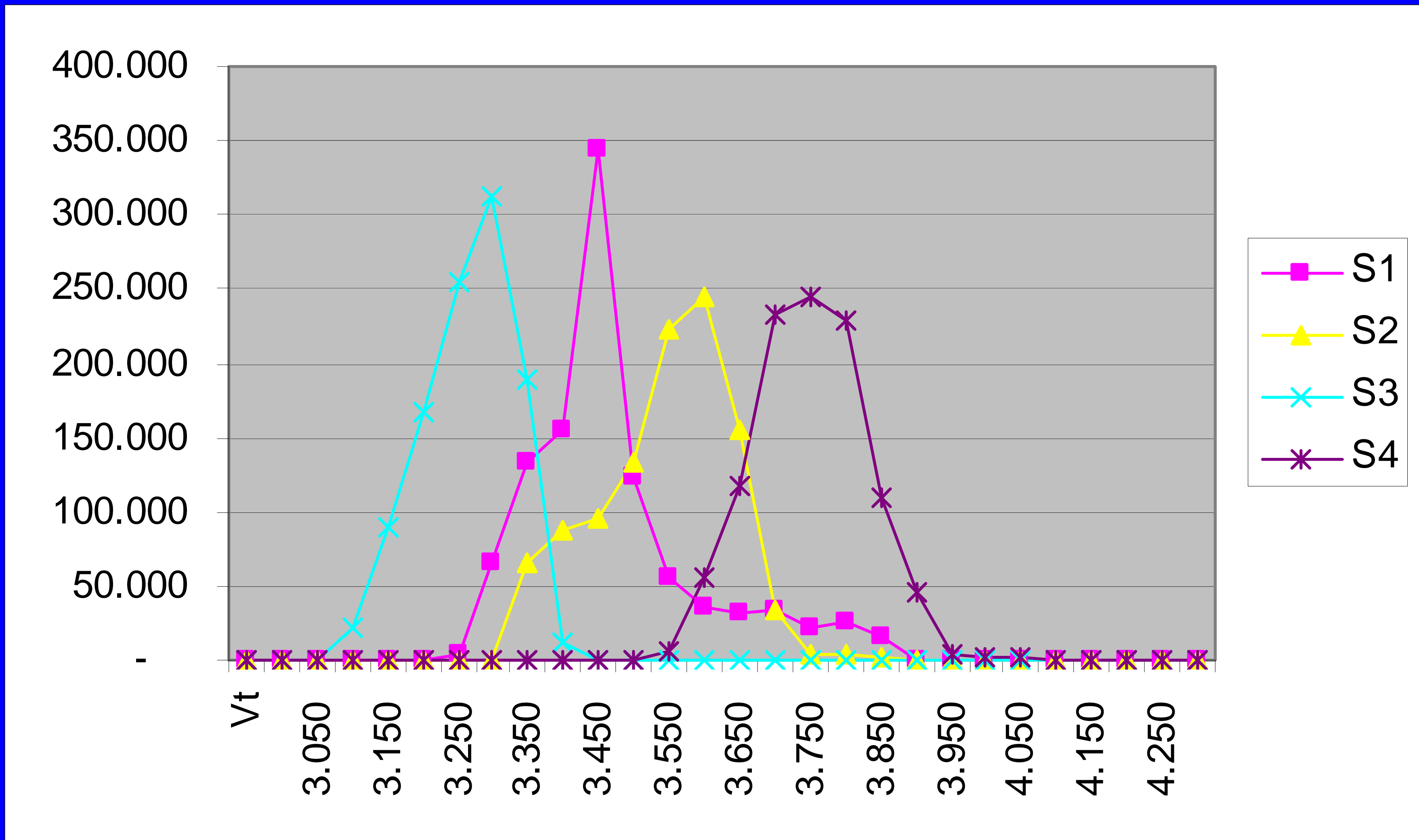
Flexible Device Management



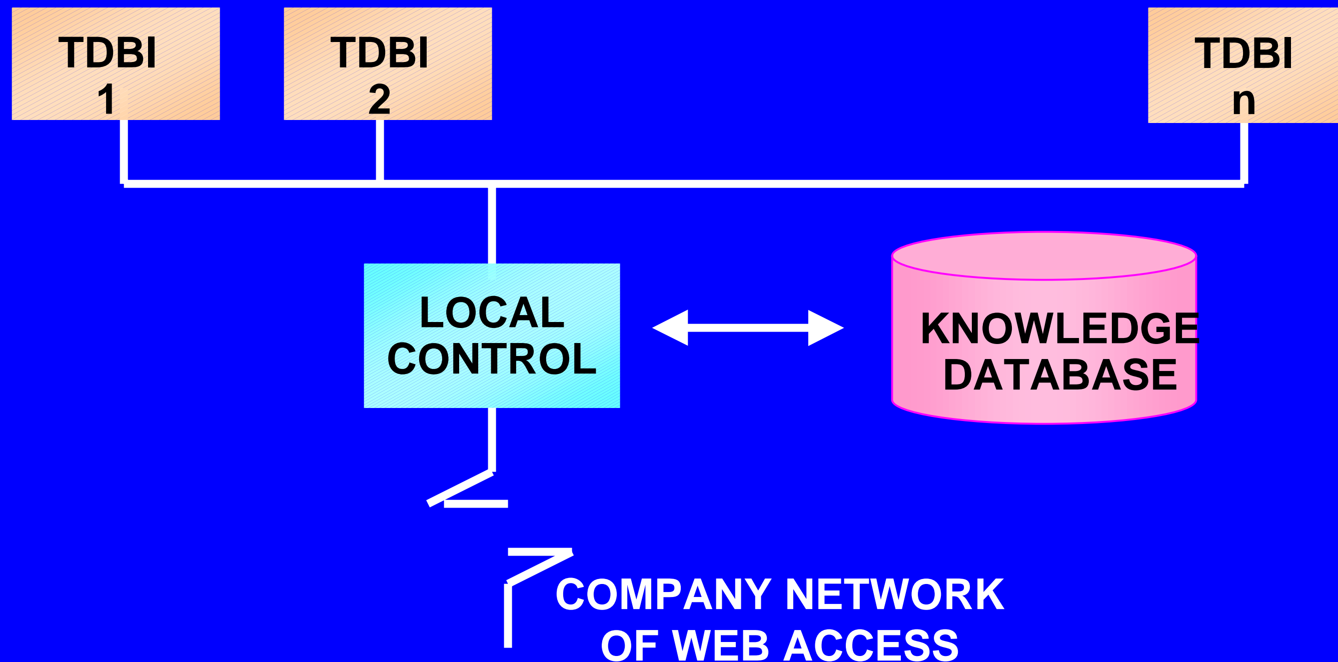
Device specific algorithms (not only flat vectors) run on the tester electronics and on the device under test

Example: Bitmap

Example: Distribution



Data Collection System



Support

- Shared recipe data base
- Remote monitor
- BLU integration
- Diagnostic tools

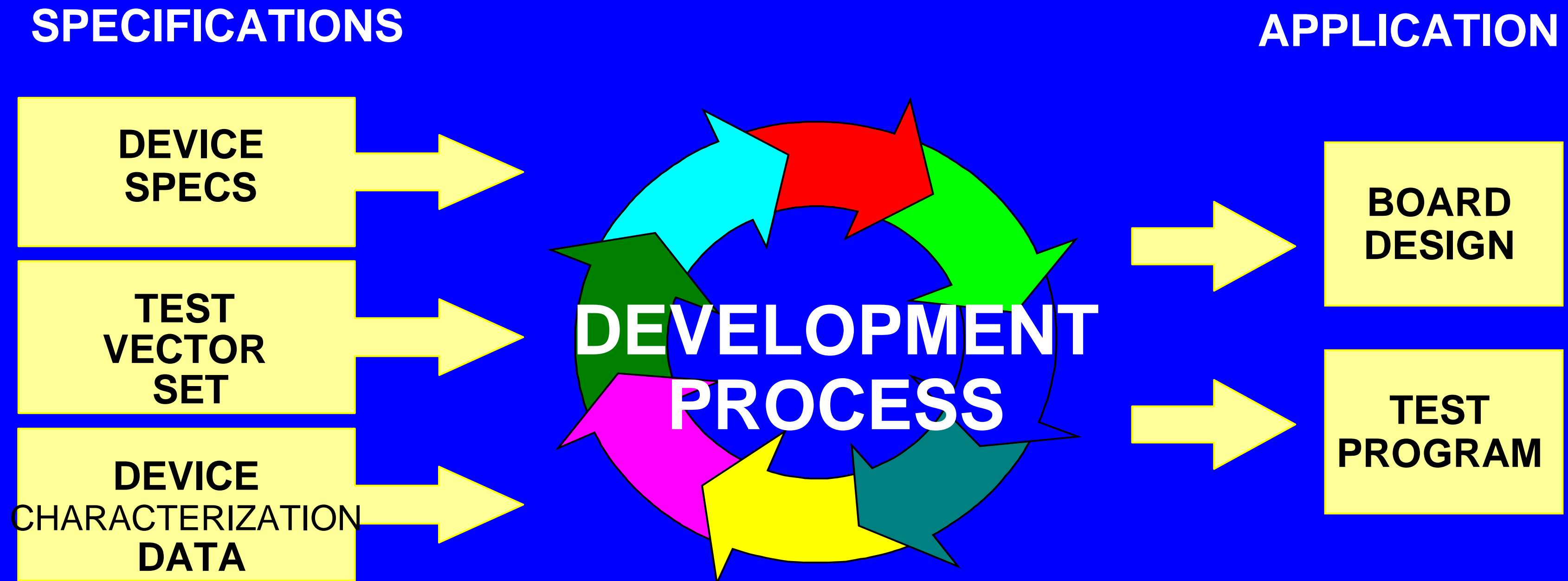
Analysis

- Summary reporting
- Correlation with knowledge data base
- Characterization tools for failure analysis

Expert system

- Utilization data
- Maintenance data
- Diagnostics data
- Fail concentration

Development Tools

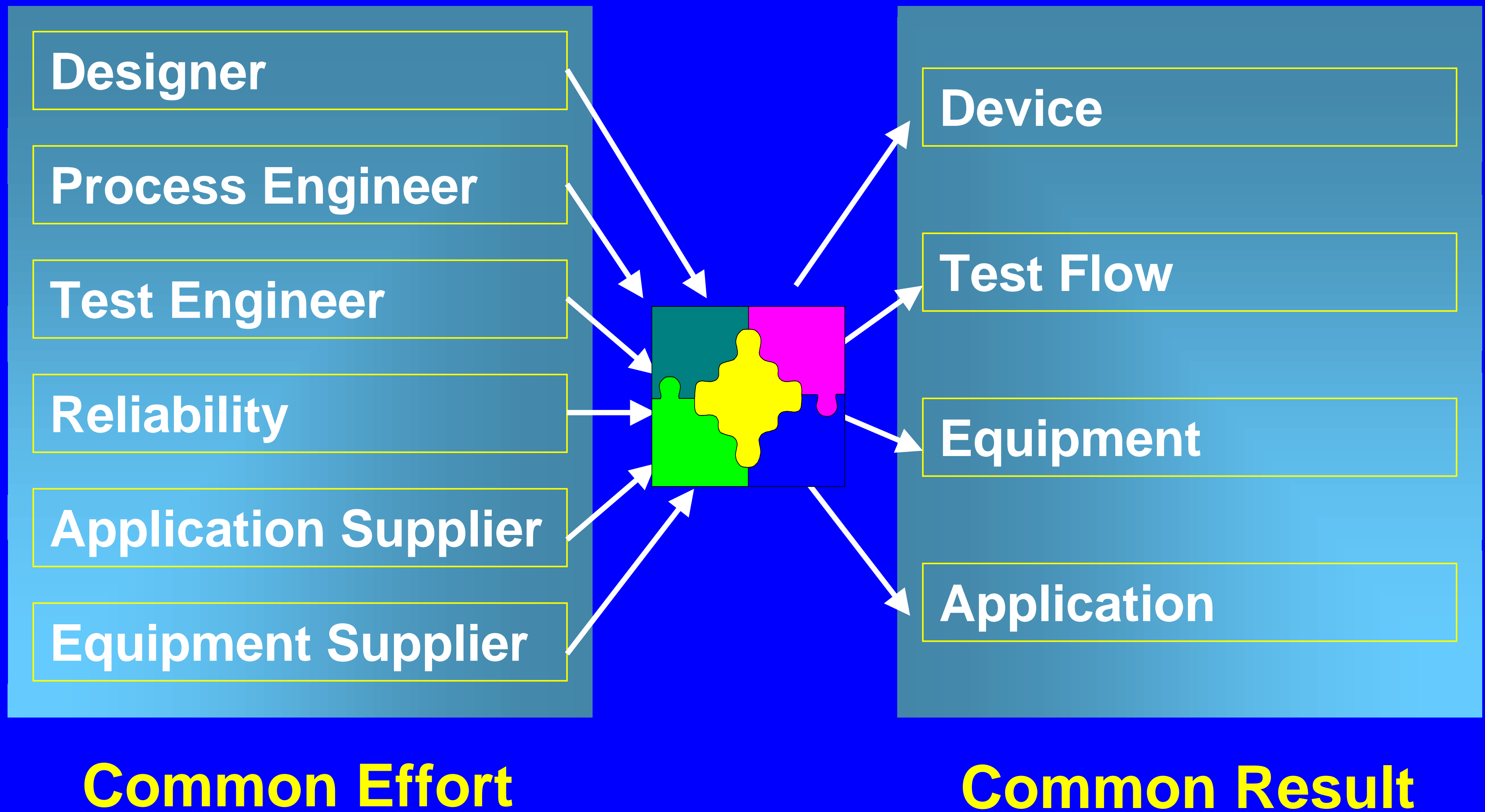


- Vector translation and IO assignment (simple case)
- Device specific algorithms (C) and test flow description (scripting)
- GUI for automated script generation

ART 200

- Flexible hardware and software structure
- High electrical performance
- Standard and user specific algorithms
- Scripting language for test flow
- Data collection and processing tools
- Area management support

Teamwork

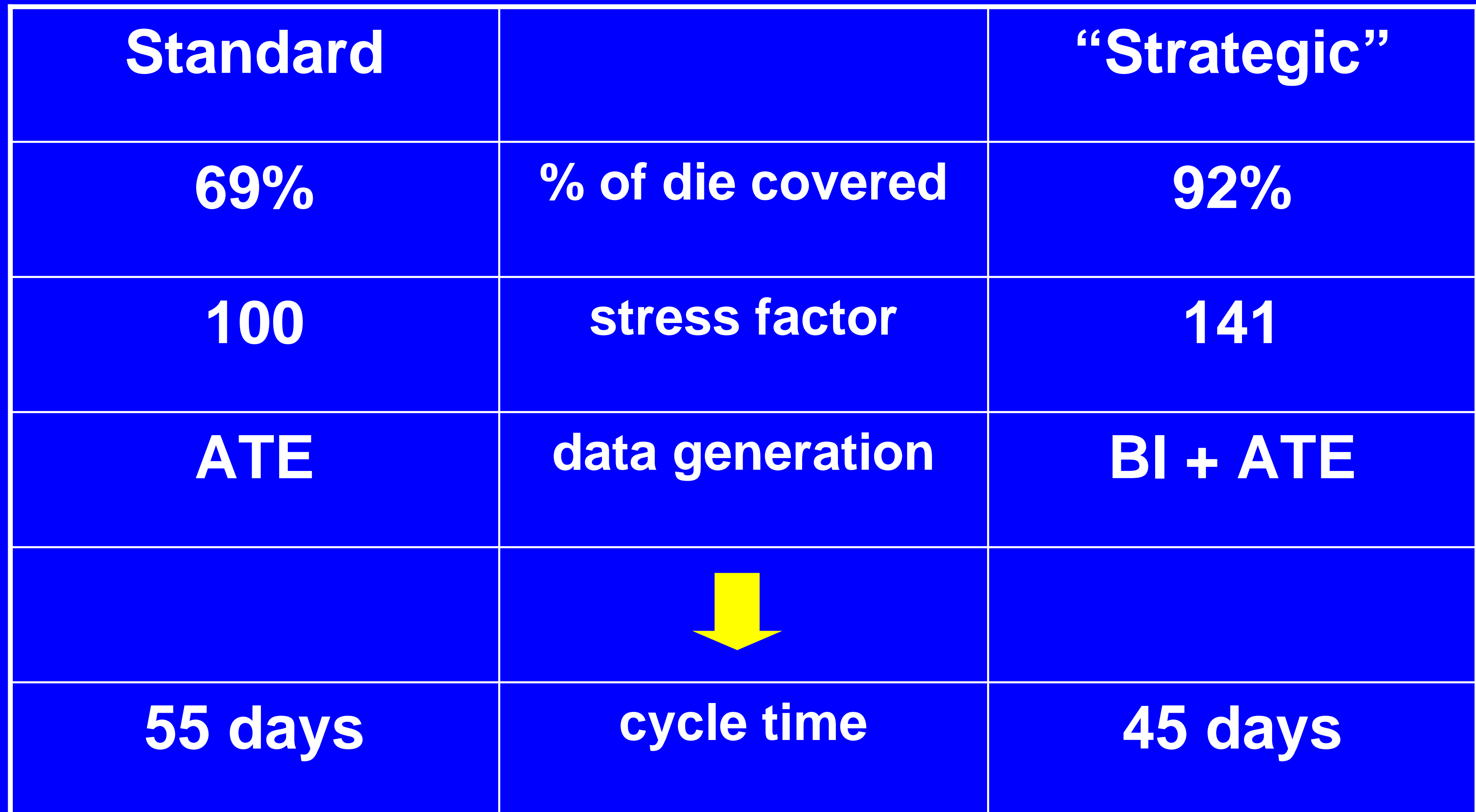


Common Effort

Common Result

Case Studies

Case Study 1: High Coverage Qualification



Standard		"Strategic"
69%	% of die covered	92%
100	stress factor	141
ATE	data generation	BI + ATE
	⬇	
55 days	cycle time	45 days

Case Study 2: New Embedded NVM Process

- Same tools used for characterization, qualification and production quality control
- Yield ramp-up from 7% to 95% in 1 WK using characterization data generated in production

Case Study 3: TDBI on Embedded NVM

- Embedded NVM tested only during burn-in
- Test result correlation proven
- Fully integrated burn-in area
- ATE test time and ATE investment reduced by 60% (6 M$)
- Total process cost reduced by 40%

Case Study 4: Fully Parallel Test on Flash

- 64 Mbit TSOP56
- All functional test steps implemented in a parallel test (“burn-in like”) environment, as an additional process step
- ATE runs only DC and AC tests (85% test time saving)
- Total process cost reduced by 50%
- Increased outgoing reliability (cycling “gratis”), value not measured yet

thank you

for your time and consideration

A FLEXIBLE ELECTRICAL INTERFACE DESIGN FOR THE FIXTURE BETWEEN TESTER AND DUT TO ACHIEVE REDUCED COST AND LEADTIME IN ATE TOOLINGS

2003 Burn-in and Test Socket Workshop

March 2 - 5, 2003

Koh Tuan Meng
Lim Kok Lay

Agenda

- Background
- Objectives
- Design Concept (Flexi-Interface)
- Prototype Evaluations Data
- Conclusions

Background

- **Device Specific Electrical Inteface**
  - **Tester channels routed to DUT (device under test) according to device pinouts.**
  - **No flexibility in toolings.**
- **High Toolings Cost**
  - **Existing toolings cannot be used if device pinouts are different.**
- **Long Leadtime For Toolings**
  - **Tpyical cycle time for building a new electrical interface is about 2 to 3 months.**

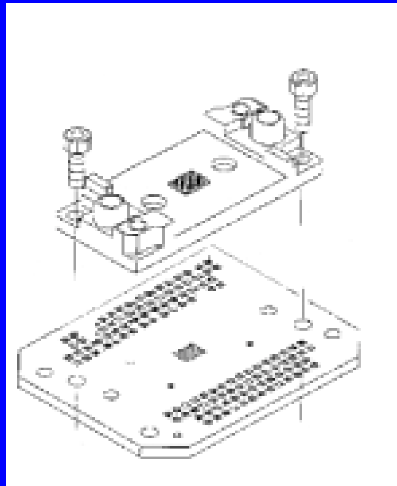
Objectives

- To have better toolings flexibility
- Reduce Test toolings cost.
- Reduce Test toolings leadtime.

Design Concept (Flexi-Interface)

Conventional Test Interface Fixture | **Flexi-Interface Test Interface Fixture**

Device Specific: Socket, Socket Board



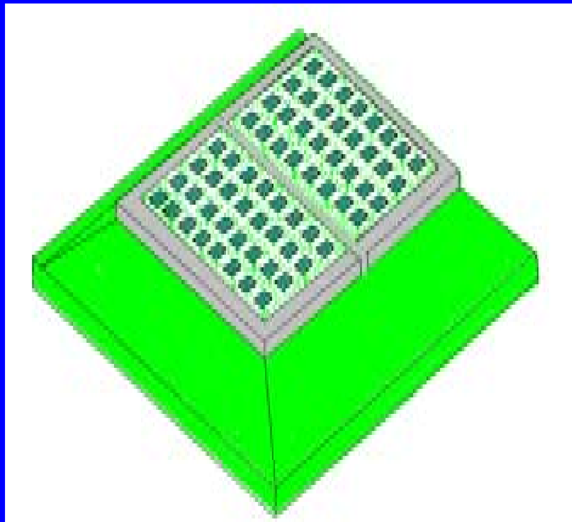
Socket

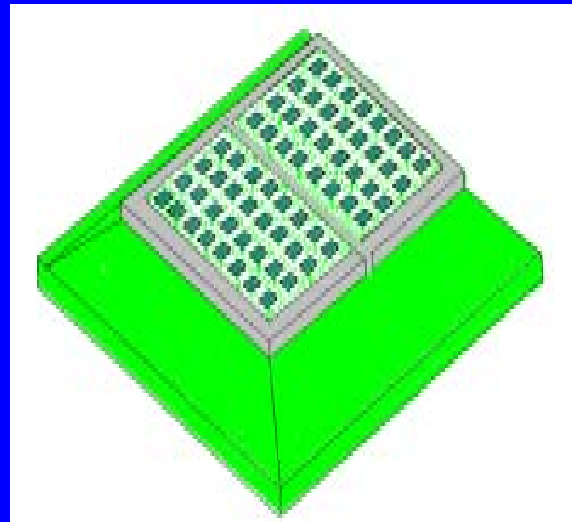
Adaptor Board

Interconnect

Socket Board

Changeover kits (Device Specific)

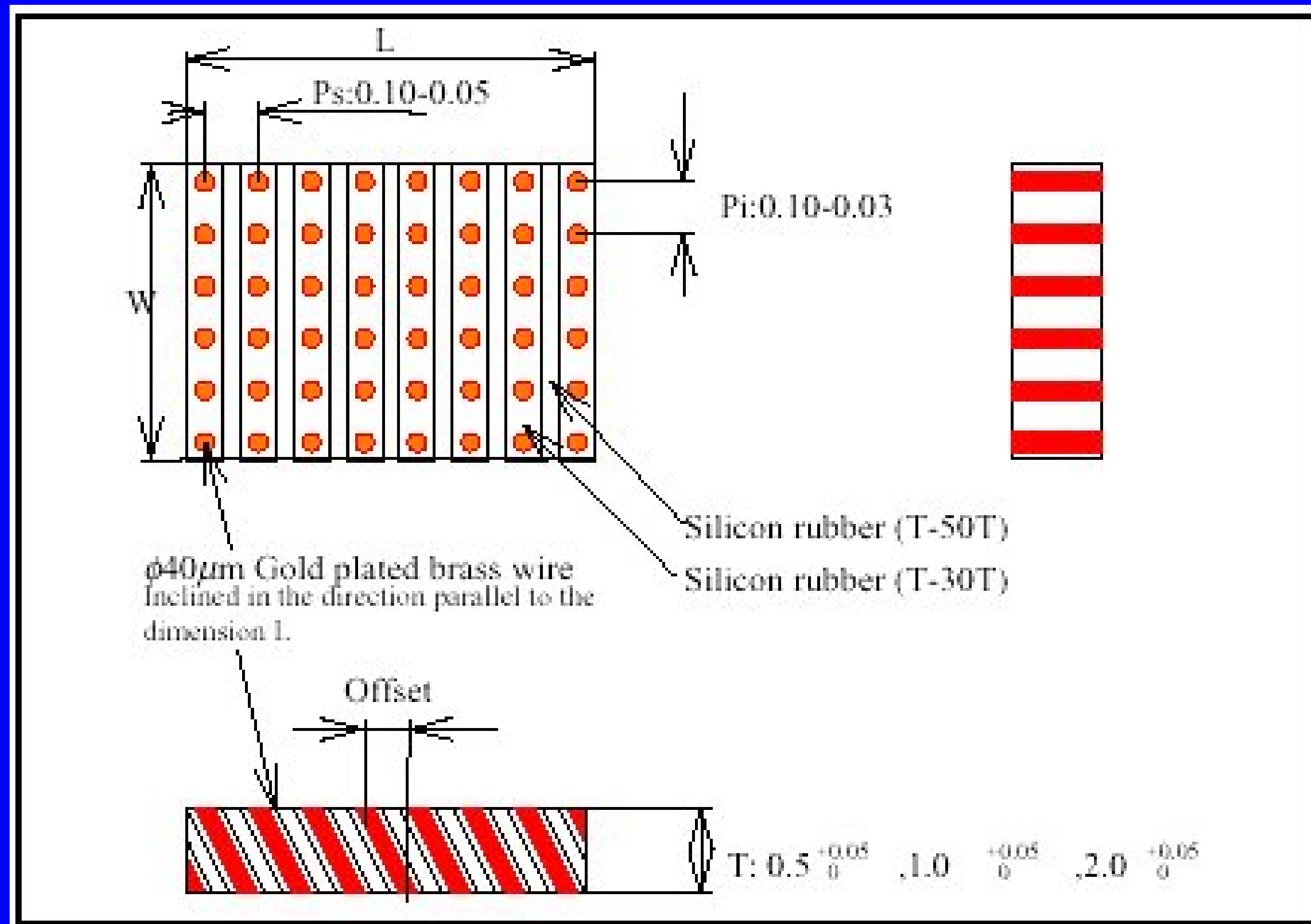




Universal Base Assembly

Interconnect Material

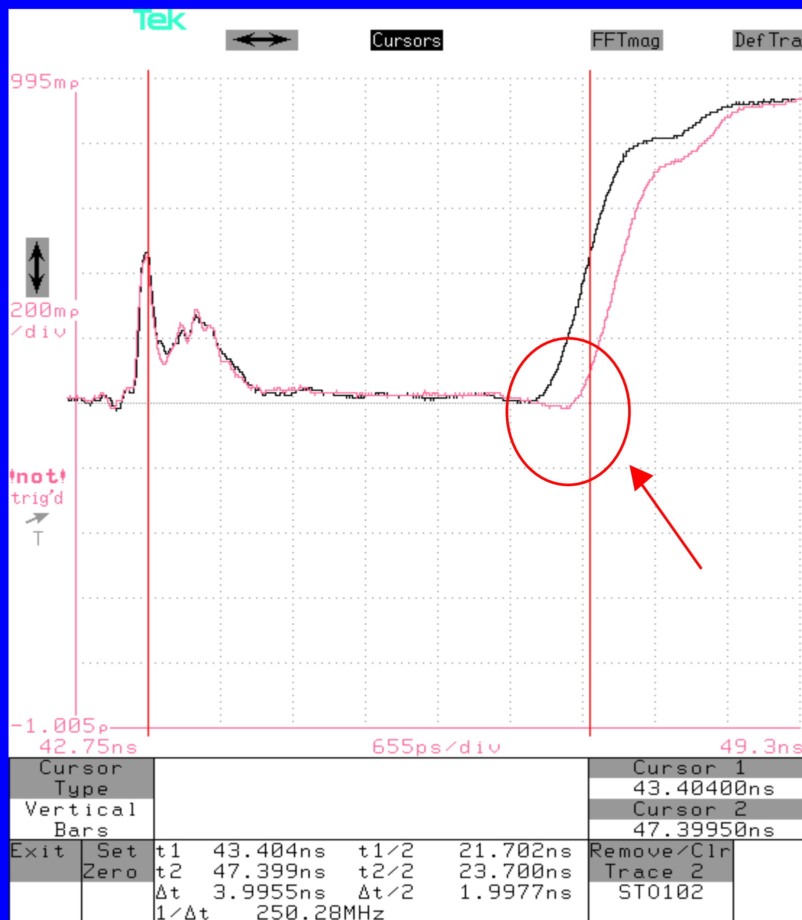
Shin-Etsu Interconnector (SMM)



Courtesy of SHIN-ETSU (http://www.shinpoly.com)

Prototype Evaluations Data

Time-Domain Measurements

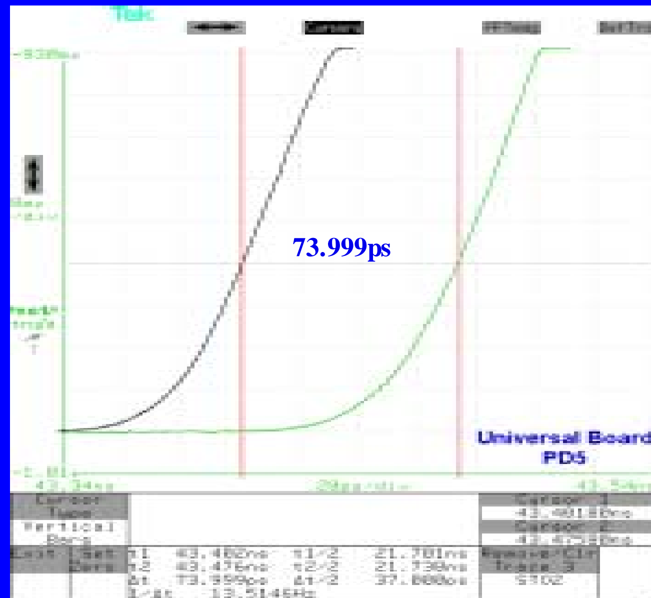


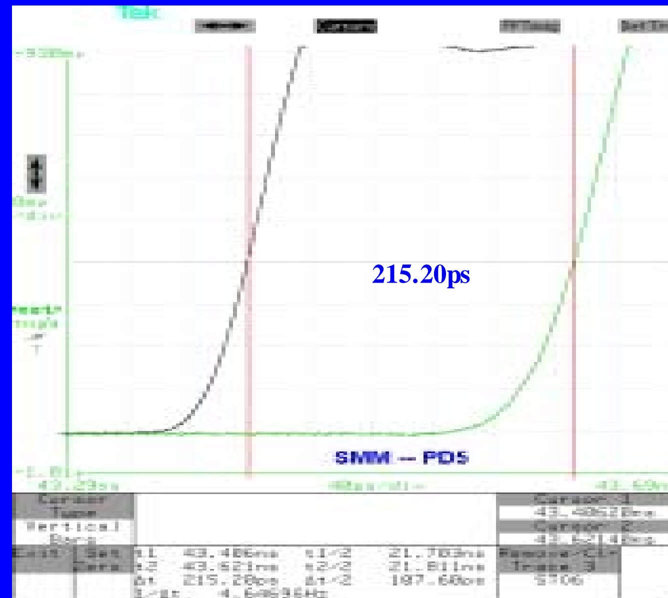
TDR (Time Domain Reflectometry) measurements were taken to capture any abnormalities on the impedance profiles for the complete signal path.

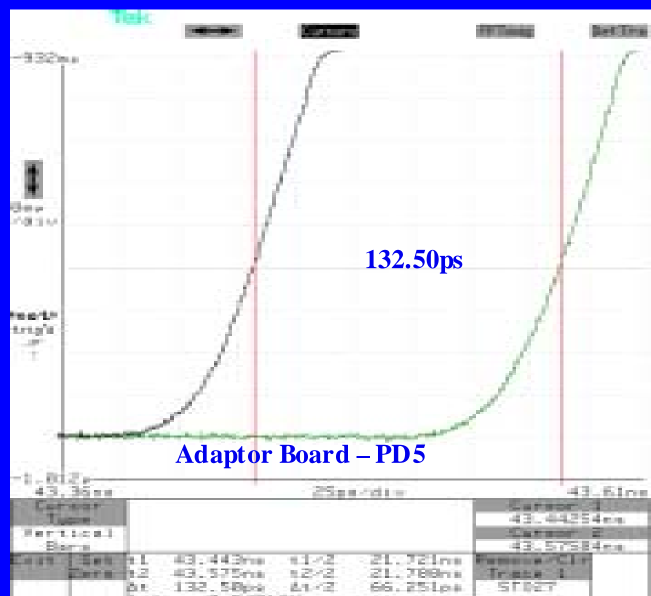
The impedance dips below 50ohms at the portion of the SMM interconnect. The SMM interconnect is not impedance control and hence causes some impedance mismatch (it has a capacitive effect).

Prototype Evaluations Data

Time-Domain Measurements





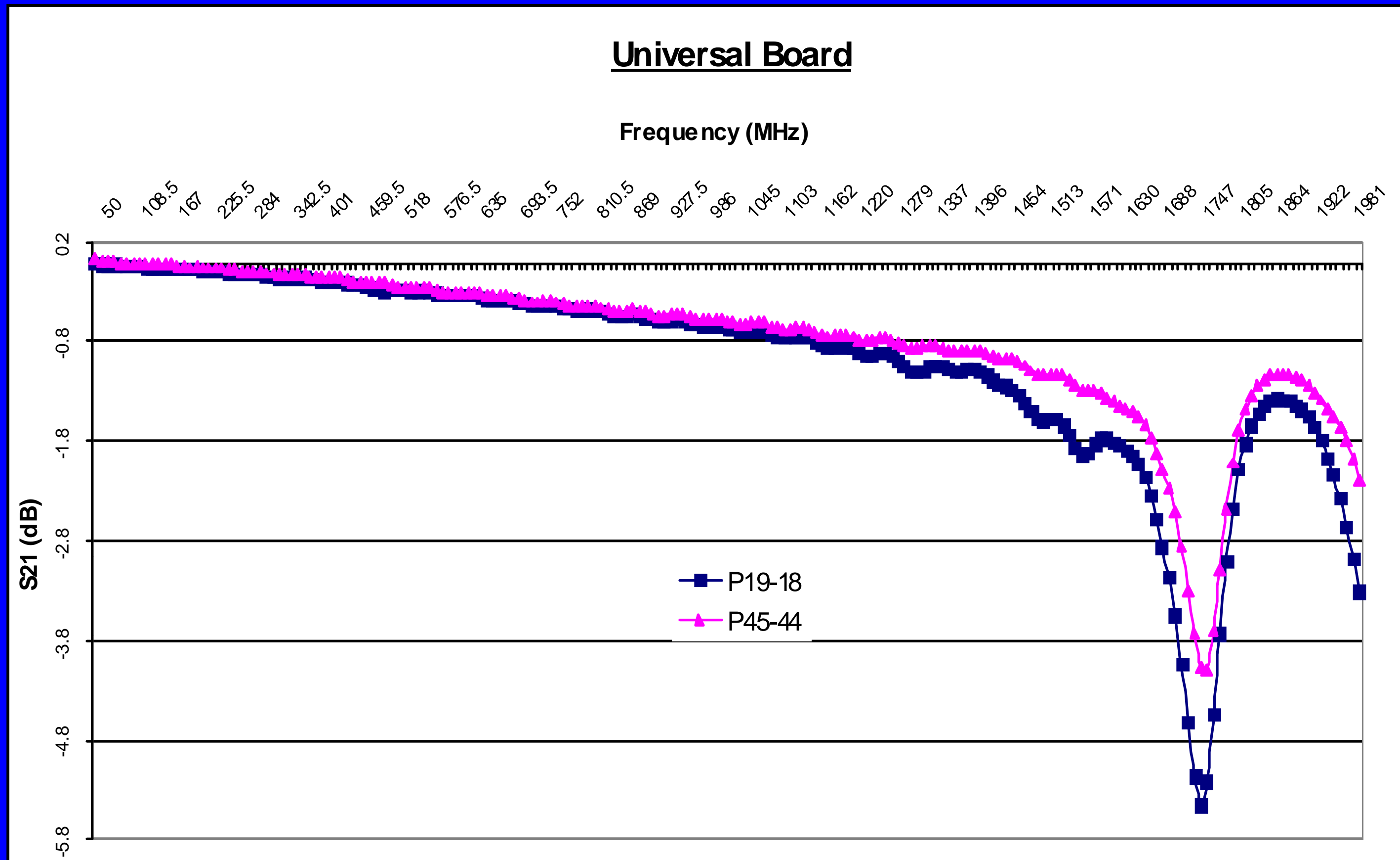


TDT (Time Domain Transmission) measurements were taken on the bare boards to derive the actual propagation delay introduced by the SMM interconnect.

The delay is only about 9ps.

Prototype Evaluations Data

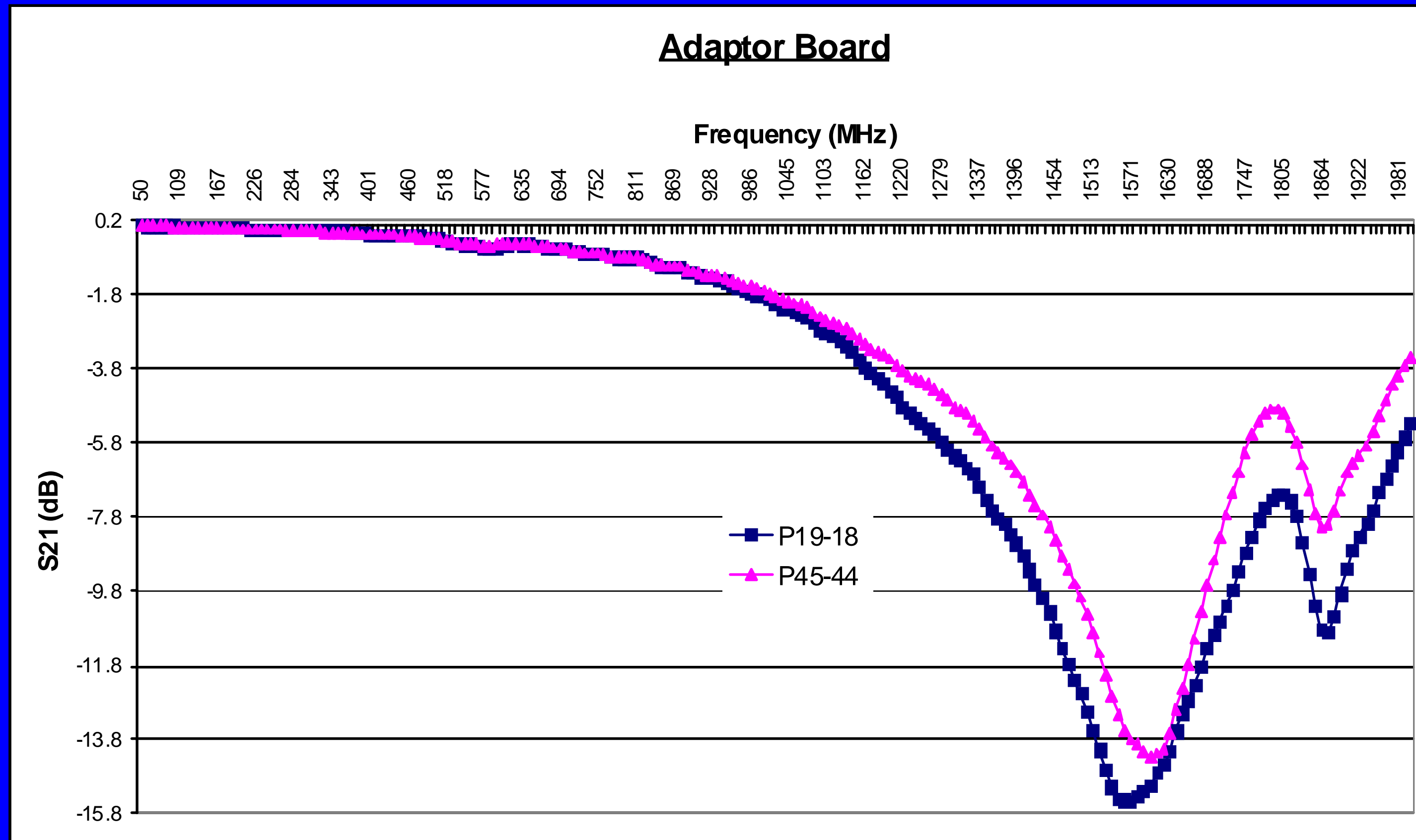
Frequency-Domain Measurements



Insertion Loss measurements were taken on the bare boards to check for the signal degradation caused by the SMM interconnect.

Prototype Evaluations Data

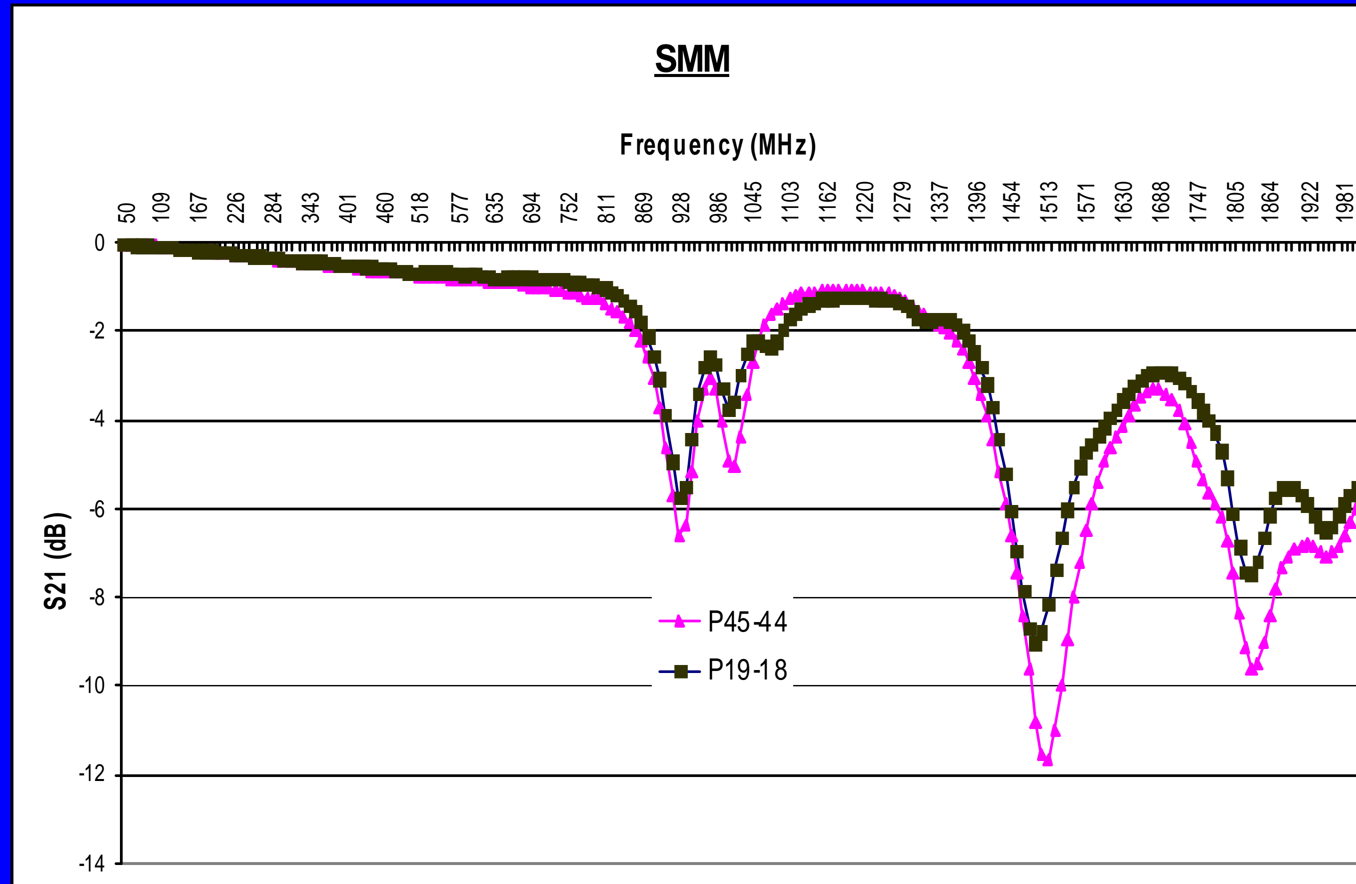
Frequency-Domain Measurements



Adaptor Board

Prototype Evaluations Data

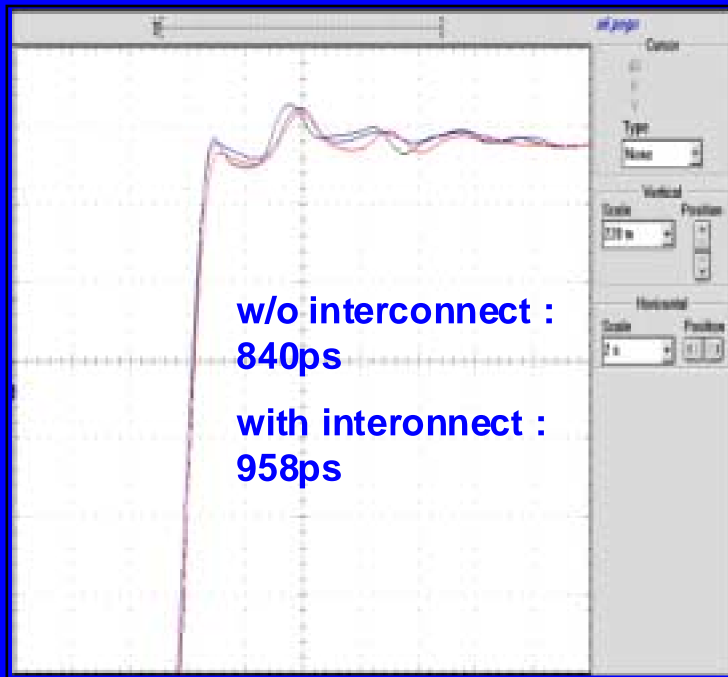
Frequency-Domain Measurements



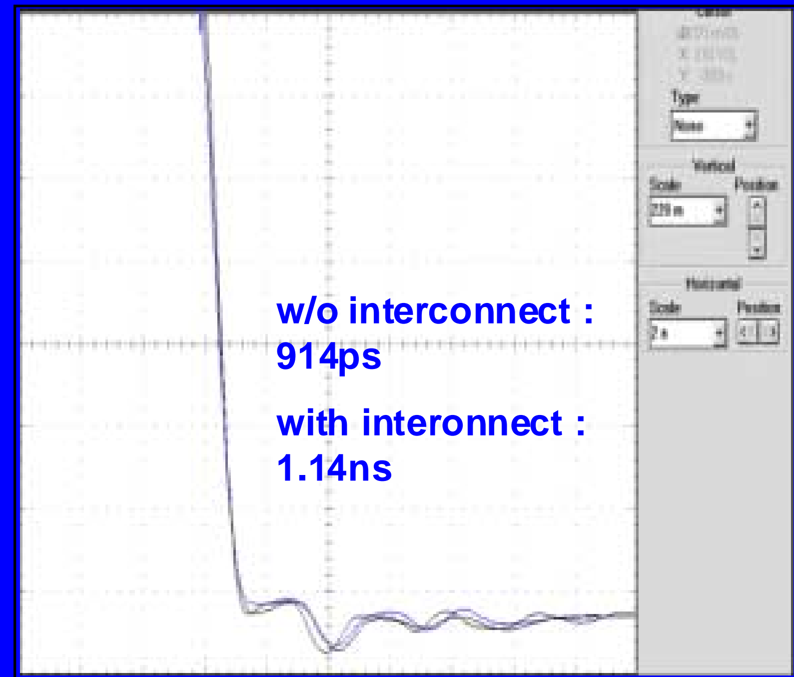
The frequency bandwidth for the complete assembly drops to 700MHz (@ 1dB insertion loss).

Prototype Evaluations Data

A short program was developed on the ATE tester to check for the rise time, cross-talk, overshoot and undershoot performance of the flexible electrical interface.



<u>Risetime</u>

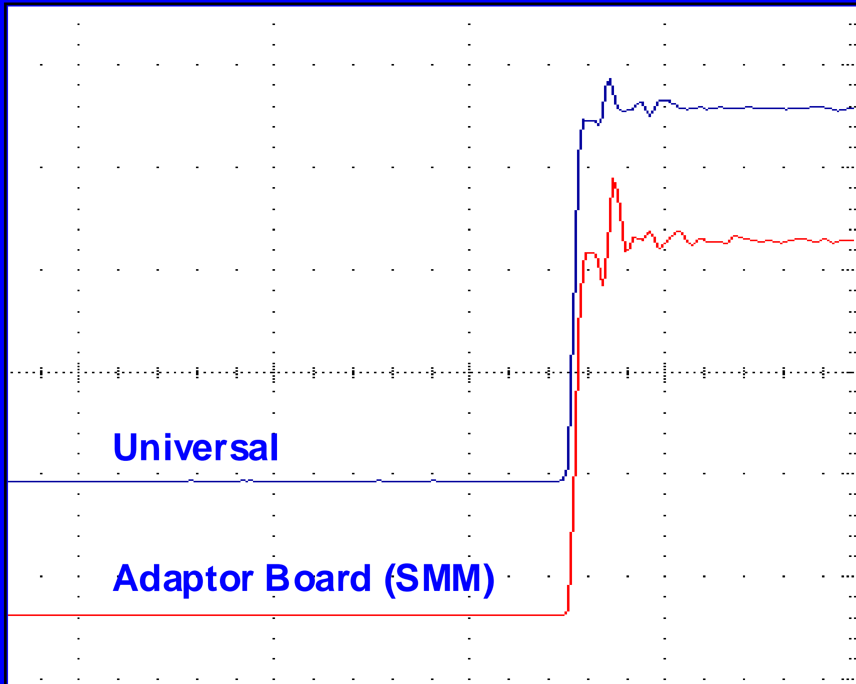


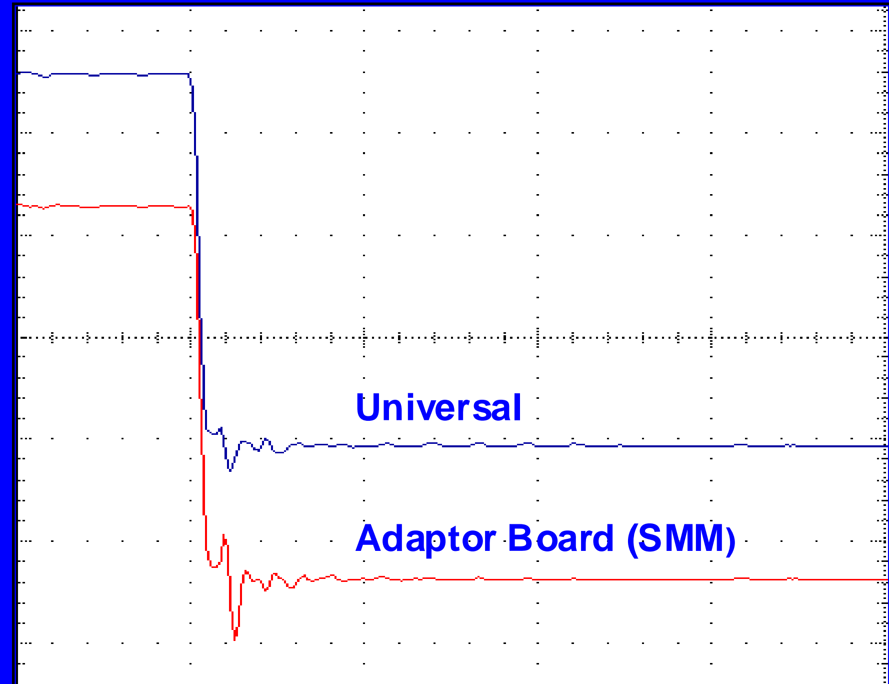
<u>Falltime</u>

With the interconnect, the risetime is degraded by about 100ps.

Prototype Evaluations Data

Crosstalk Measurements





Board Type	Overshoot / Undershoot
Universal Board	125mv / 40mv
Adaptor Board (SMM)	292mv / 60mv

Board Type	Overshoot / Undershoot
Universal Board	80mv / 65mv
Adaptor Board (SMM)	317mv / 85mv

The interconnect causes about 10% overshoot voltage.

Conclusions

- **With the data collected in both the Time & Frequency domains, the flexible electrical interface concept has been proven to be viable for device testing (for SDRAM). There is, however, still room for improvements on the interface between board to board.**

- **The next challenge would be to prove out the Flexi-interface concept for higher speed device testings (DDR II & beyond).**