Burn-in & Test Socket Workshop

March 3-6 , 2002
Hilton Phoenix East/Mesa Hotel
Mesa, Arizona

IEEE

IEEE COMPUTER SOCIETY

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Test Technology Technical Council

Burn-in & Test Socket Workshop

Technical Program

Invited Address
Sunday 3/03/02 8:00PM

"The International Technology Roadmap For Semiconductors

(ITRS) - Guidance for Global Technology and Manufacturing R&D Resources in the New Millenium"

Alan K. Allan
Staff Engineer
Intel Corporation

The International Technology Roadmap for Semiconductors

[ITRS] - Guidance for Global Technology and Manufacturing R&D Resources in the New Millennium

03/03/02

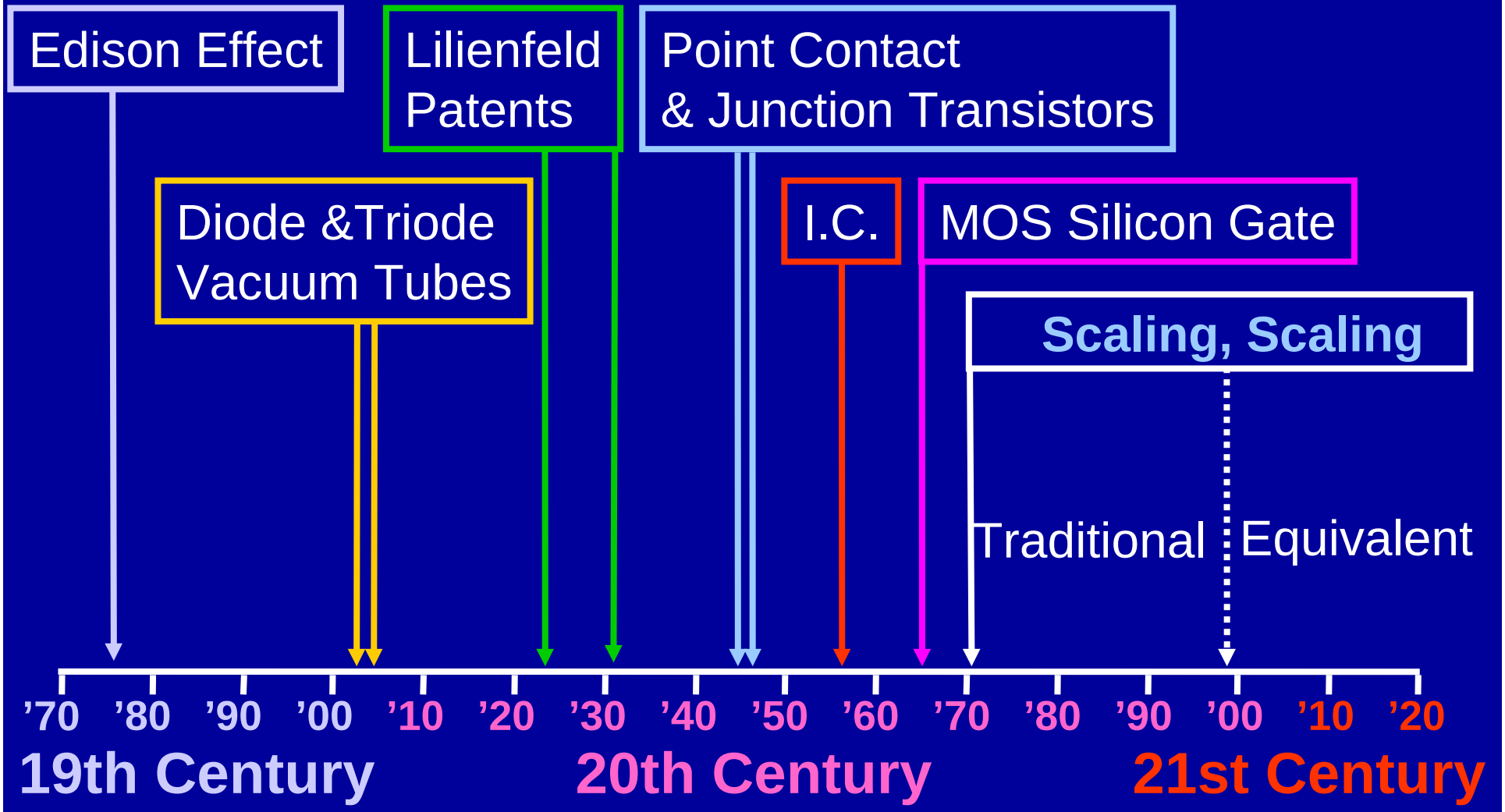
BiTS Workshop – Hilton/Mesa, AZ

Alan Allan / Intel Corporation

Agenda

- ITRS Overview
- Scaling Benefits/Definition
- 1999 ITRS vs. 2001 ITRS
- Review of Some Challenge Examples
  - ORTC (Scaling, Cell Size, Frequency)
  - Lithography
  - Test
  - Factory Integration
- Summary/Q&A

150 Years of Electronics



Source: Intel/P.Gargini

THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS) GOALS:

• Present an **industry-wide consensus** on the "best current estimate" of our future research and development needs out to a 15-year horizon.

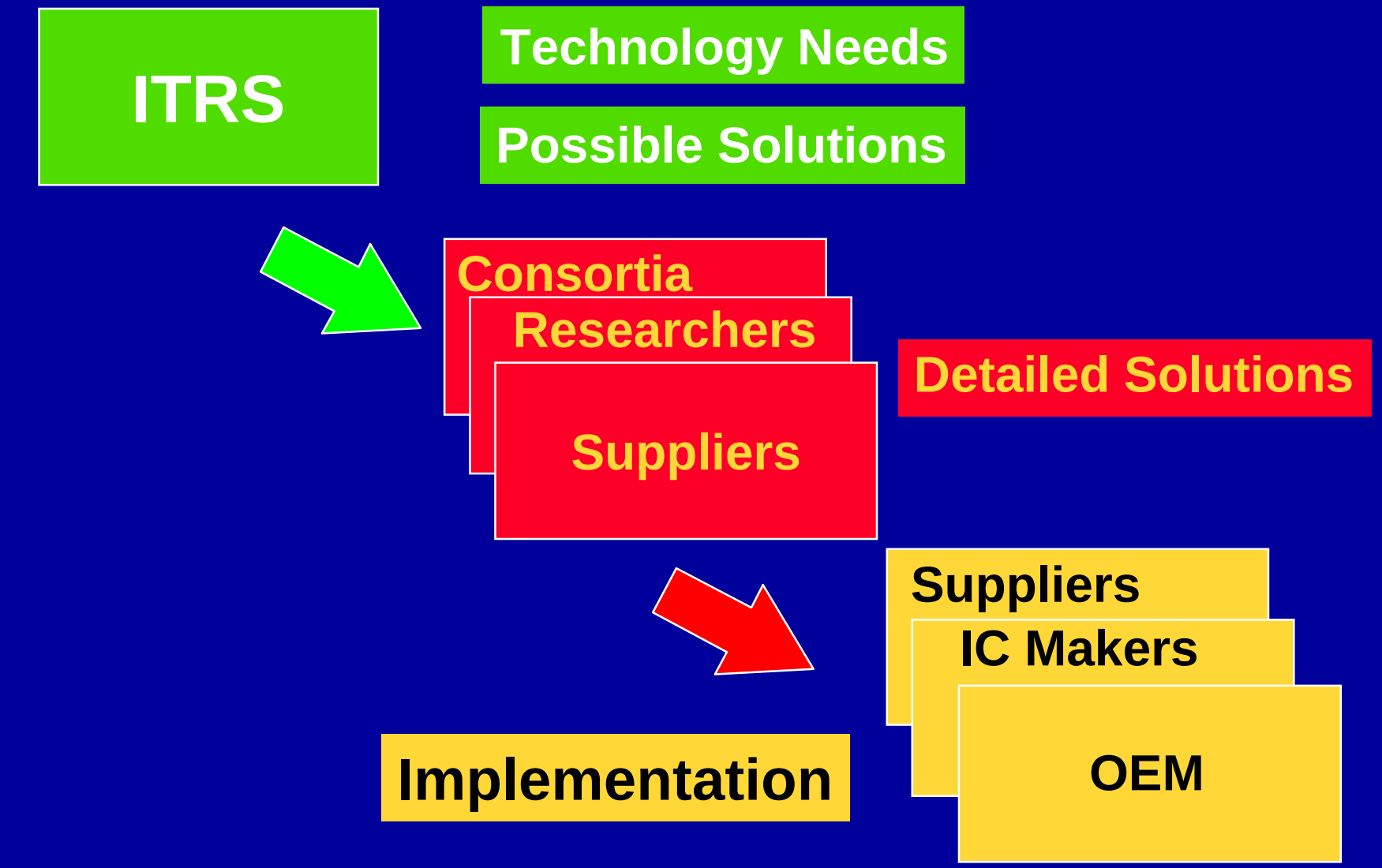
• Provide a **guide** to the efforts of research organizations/sponsors (industry, government, and universities.)

...Based on **premise** of continuing the four-decade-long trends of an industry that has distinguished itself by:

- rapid pace of improvement in its **products**
- exponential improvement of manufacturing capability and productivity to reduce the minimum **feature sizes[SCALING]** and **cost/function** used to fabricate integrated circuits.

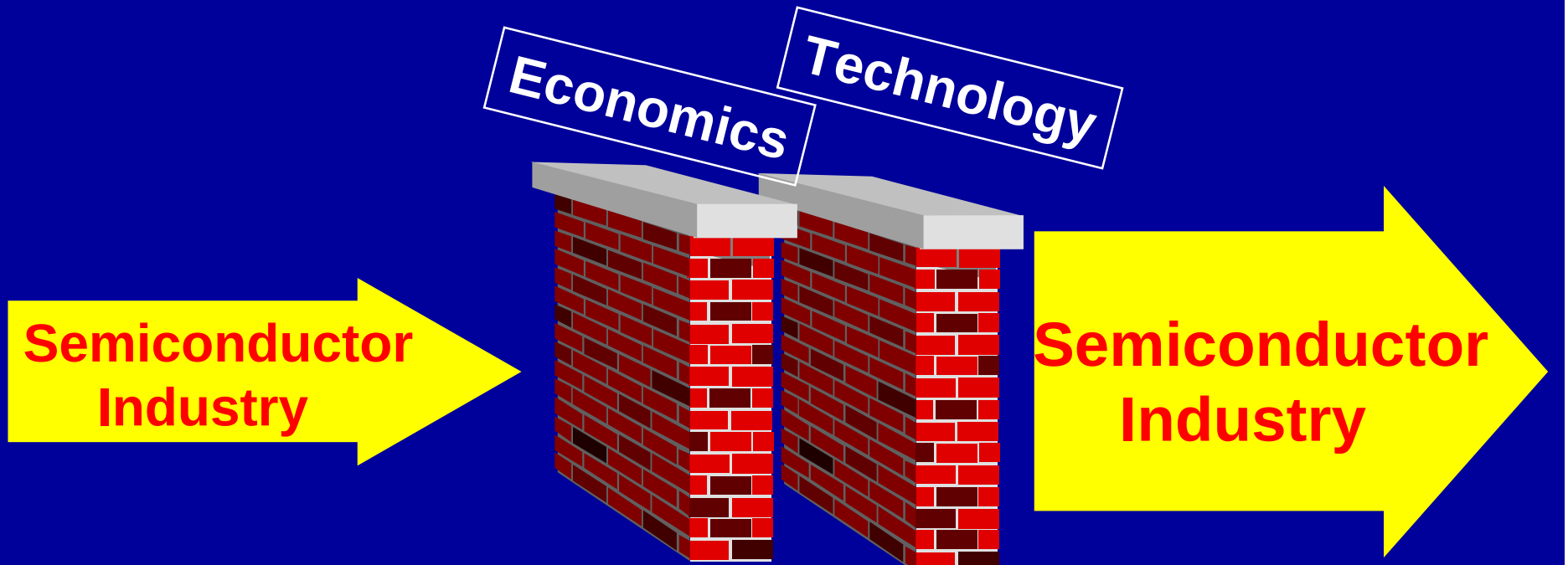
Source: 1999 ITRS, 11/99

From Strategy to Implementation

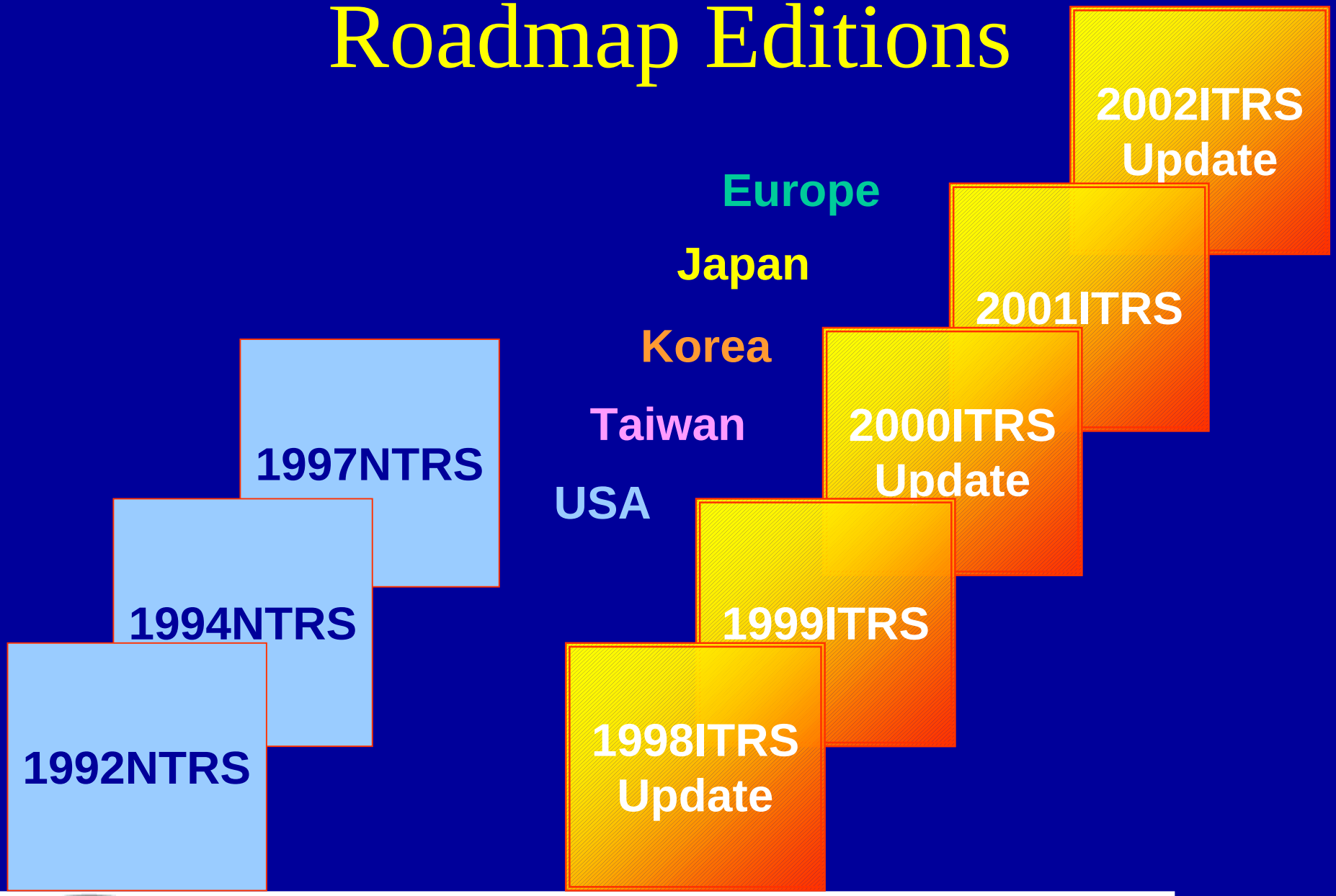


The Need for Globalization

90's	21st Century



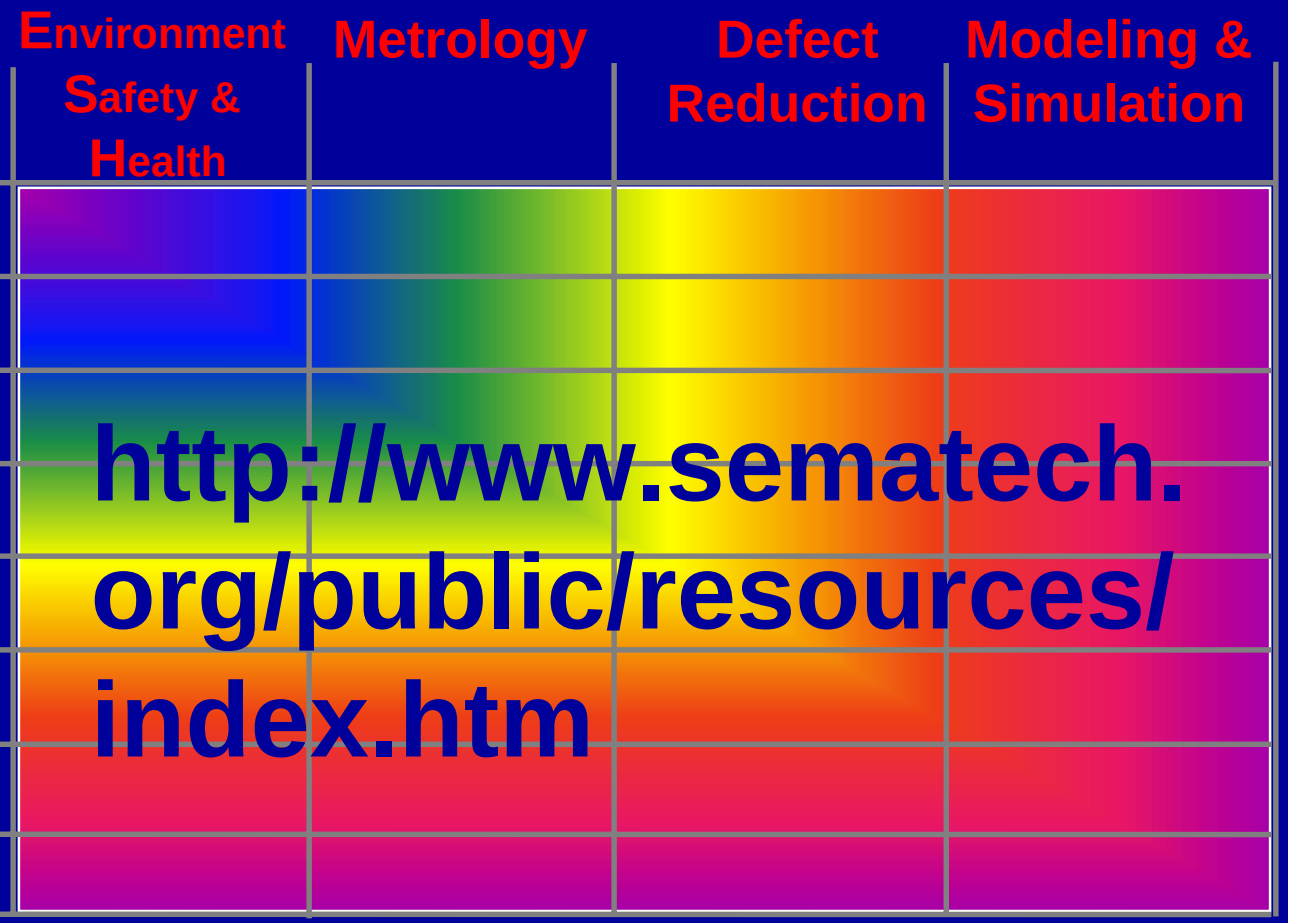
Roadmap Editions



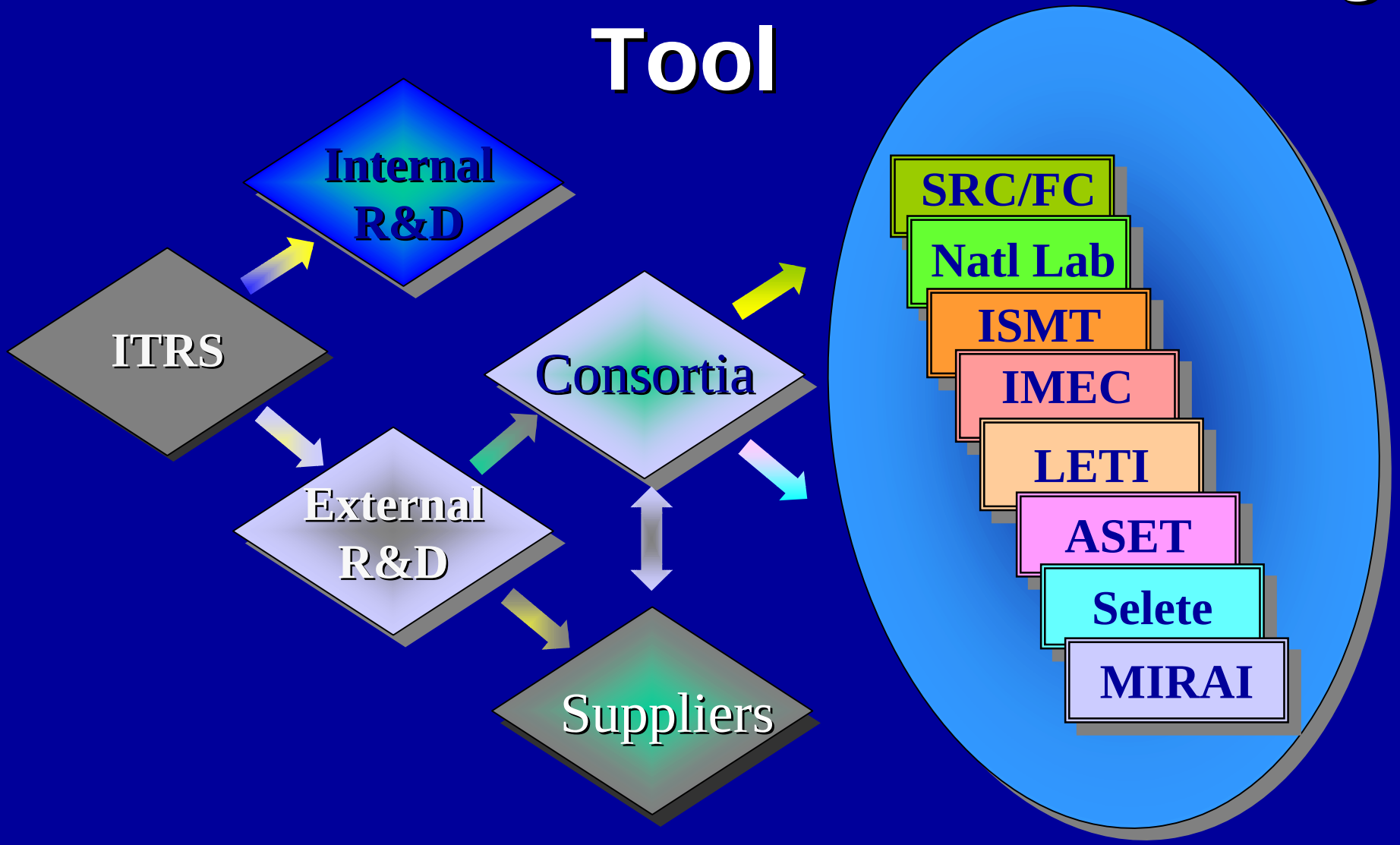
The Plan for Globalization - ITRS Working Groups

International Technology Working Groups (ITWG)

International Crosscut Technology Working Group (ICCT WG)

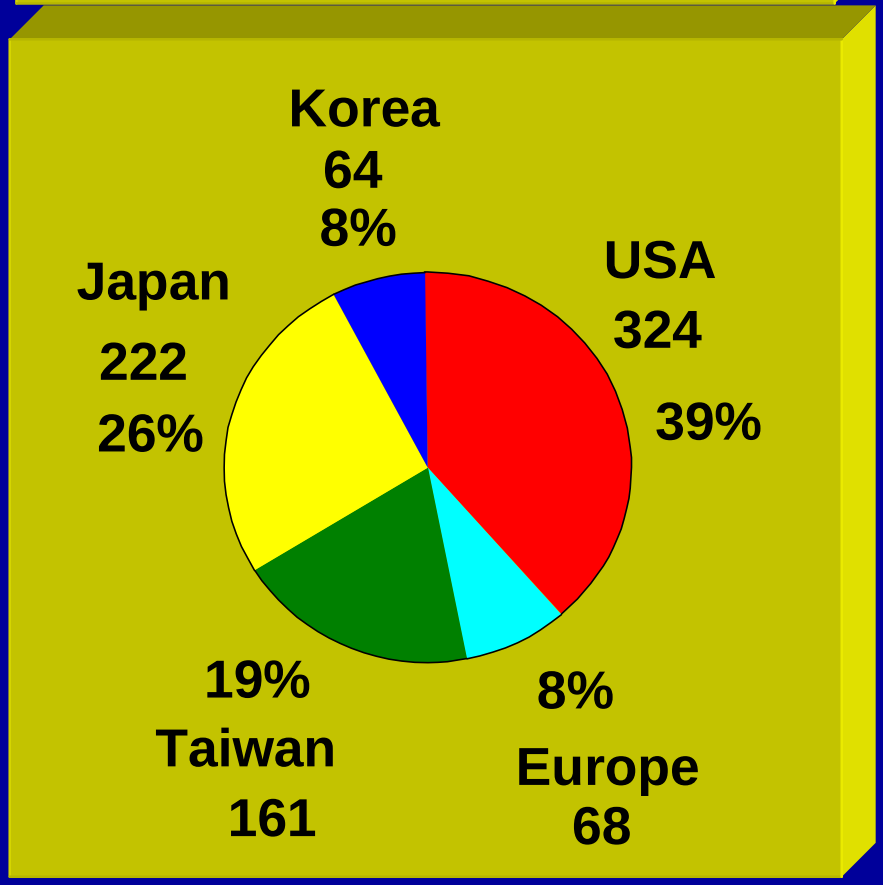


Use of ITRS as a Global Planning Tool

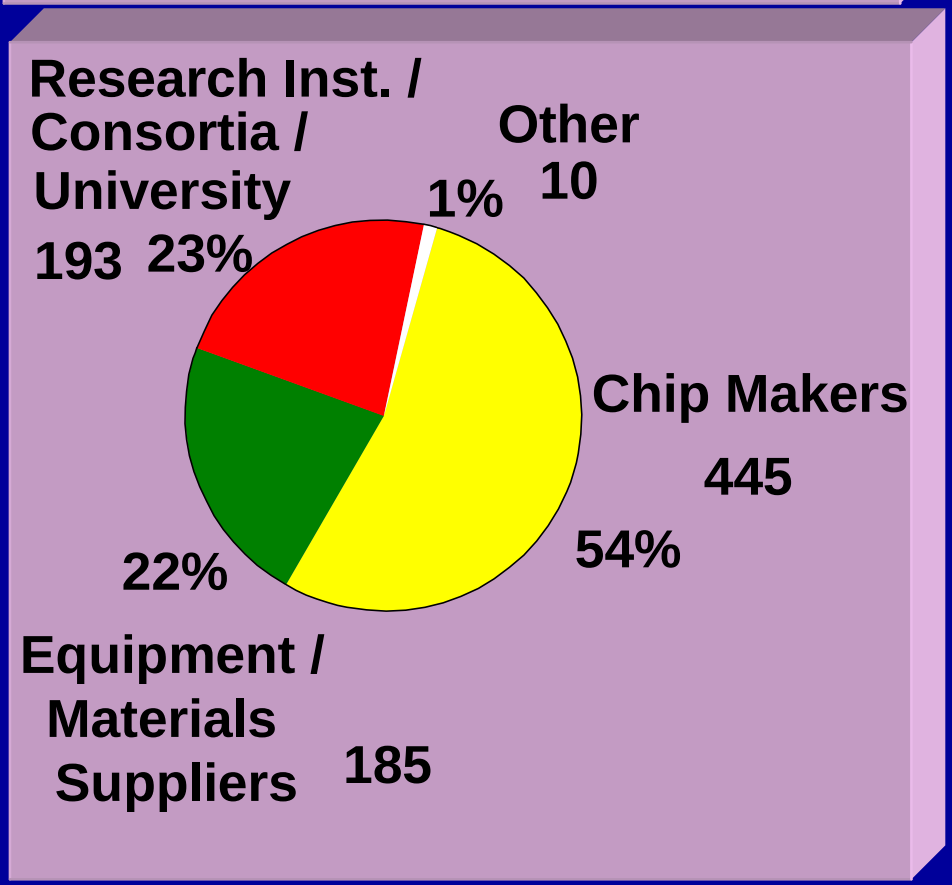


Composition of the Technology Working Group (ITWG) in 2001

TWG Members by Regions



TWG Members by Affiliations



Source: 2001 ITRS - Exec. Summary

2001 ITRS Renewal
Key Accomplishments

- 130nm node 1-year pull-in to 2001 (2-yr cycle), validating the 1999 ITRS "Best Case")
- 90nm trend rate (0.7x/node) correction to 2004 (3-yr cycle), vs 2006 in 1999 ITRS
- Added detail to DRAM Cell design improvement rate limitations
- Affordable Lithography Field Size/Reticle limitations identified/supported
- MPU Physical Gate Length Performance Trend Identified
- Published full Renewal Online (order CDs)
  http://www.sematech.org/public/resources/index.htm

MOS Transistor Scaling Impacts Everything!

Parameter	Scaled Voltage	Constant Voltage
Supply Voltage (Vdd)	S	1
Channel Length (Lg, Le)	S	S
Channel Width (W)	S	S
Gate Oxide Thickness (Tox)	S	S
Substrate Doping (N)	1/s	1/s
* Drive Current (Id)	S	1/s
Gate Capacitance (Cg)	S	S
Gate Delay	S	S^2
Active Power	S^3	S

S < 1

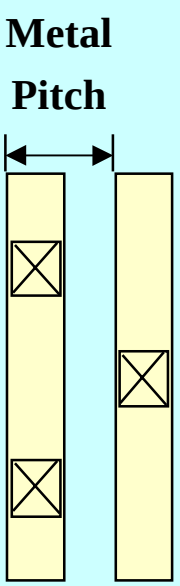
* Does Not Include Carrier Velocity Saturation

MOS Transistor Scaling (1974 to present)

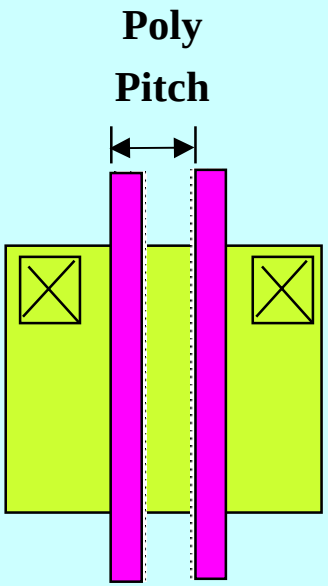
S=0.7

[0.5x per 2 nodes]

Half Pitch (= Pitch/2) Definition



(Typical DRAM)

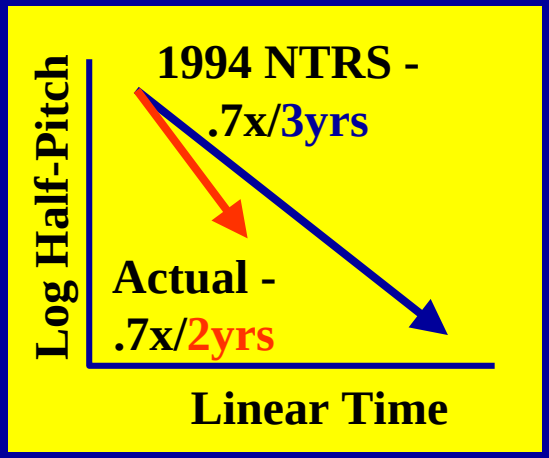


(Typical MPU/ASIC)

Source: 2001 ITRS - Exec. Summary

Scaling Calculator +

Node Cycle Time:



0.7x 0.7x

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5x

N N+1 N+2

* CARR(T) = Compound Annual Reduction Rate (@ cycle time period, T)

Node Cycle Time (T yrs):

*CARR(T) =

[(0.5)^(1/2T yrs)] - 1

CARR(3 yrs) = -10.9%

CARR(2 yrs) = -15.9%

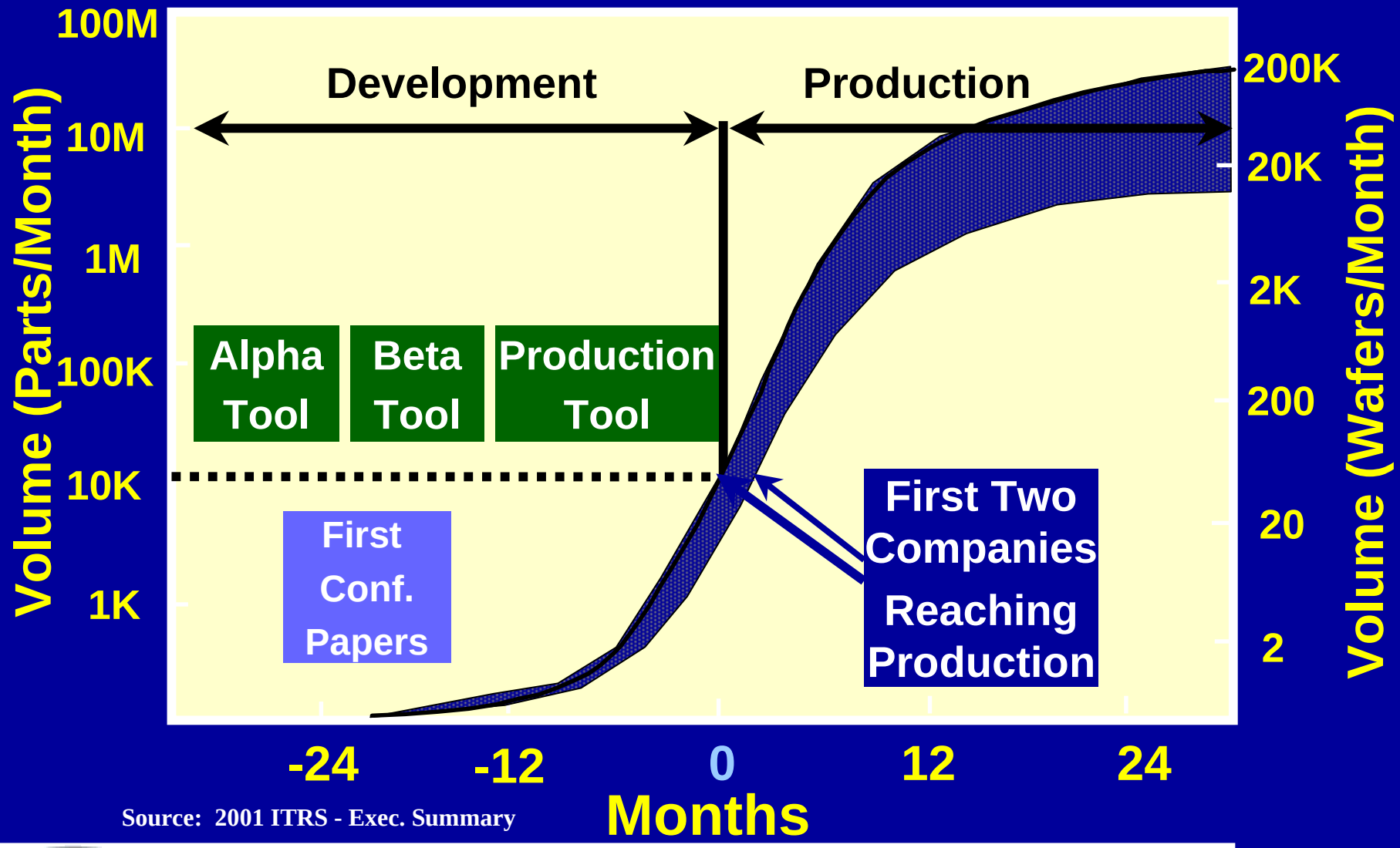
Source: 2001 ITRS - Exec. Summary

2001 ITRS

SCALING Timing Highlights

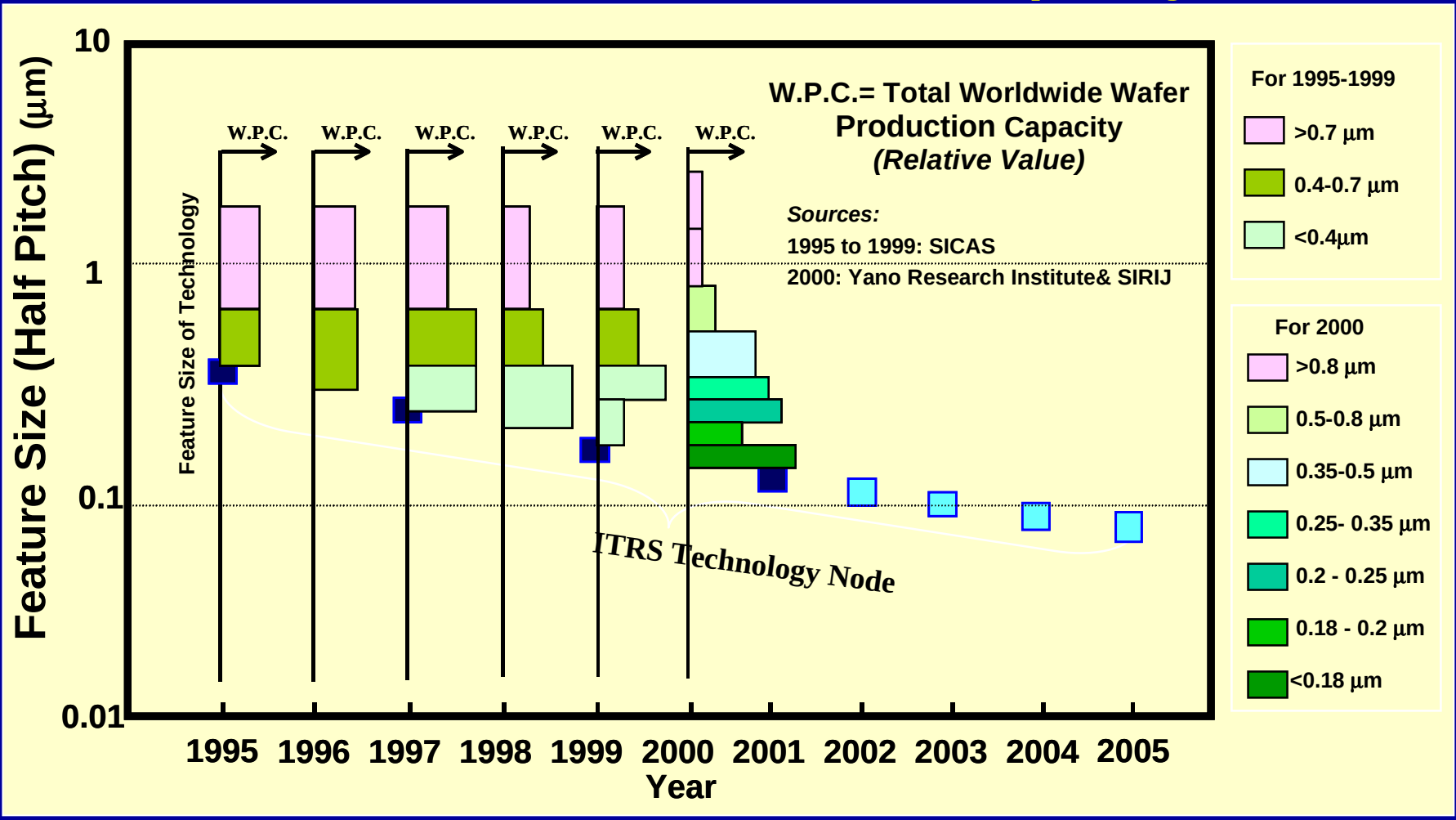
- **The DRAM Half-Pitch (HP) remains on a 3-year-cycle trend after 130nm/2001**
- **The MPU/ASIC HP remains on a 2-year-cycle trend until 90nm/2004, and then remains equal to DRAM HP (3-year cycle)**
- **The MPU Printed Gate Length (Pr GL) and Physical Gate Length (Ph GL) will be on a 2-year-cycle until 45nm and 32nm, respectively, until the year 2005**
- **The MPU Pr GL and Ph GL will proceed parallel to the DRAM/MPU HP trends on a 3-year cycle beyond the year 2005**
- **The ASIC/Low Power Pr/Ph GL is delayed 2 years behind MPU Pr/Ph GL**
- **ASIC HP equal to MPU HP**

Production Ramp-up Model and Technology Node



Source: 2001 ITRS - Exec. Summary

Technology Node vs Actual Wafer Production Capacity



Source: 2001 ITRS - Exec. Summary

Some Key Challenges

- **"Red Brick Wall Shifts"** 1999 vs 2001
- ORTC **Scaling** Goals
- Device **Scaling** Challenges
- **ITWG** Challenges - Examples

The "Red Brick Wall" - 2001 ITRS vs 1999

Table 1. 2001 Status of Red Brick Wall

Year of production	2001	2003	2005		2007	2010	2016
DRAM half-pitch (nm)	130	100	80		65	45	22
Overlay accuracy (nm)	46	35	28		23	18	9
MPU gate length (nm)	90	65	45		35	25	13
CD control (nm)	8	5.5	3.9		3.1	2.2	1.1
T_{ox} (equivalent) (nm)	1.3-1.6	1.1-1.6	0.8-1.3		0.6-1.1	0.5-0.8	0.4-0.5
Junction depth (nm)	48-95	33-66	24-47		18-37	13-26	7-13
Metal cladding thickness (nm)	16	12	9		7	5	2.5
Intermetal dielectric constant, k	3.0-3.6	3.0-3.6	2.6-3.1		2.3-2.7	2.1	1.8

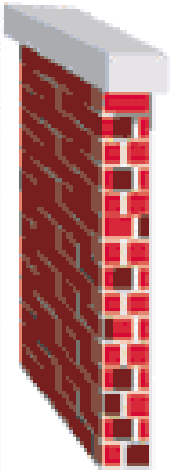
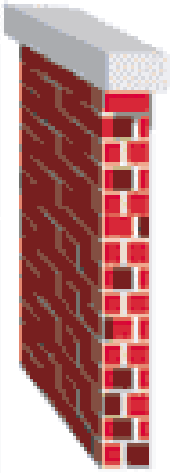


Table 2. 1999 Status of Red Brick Wall

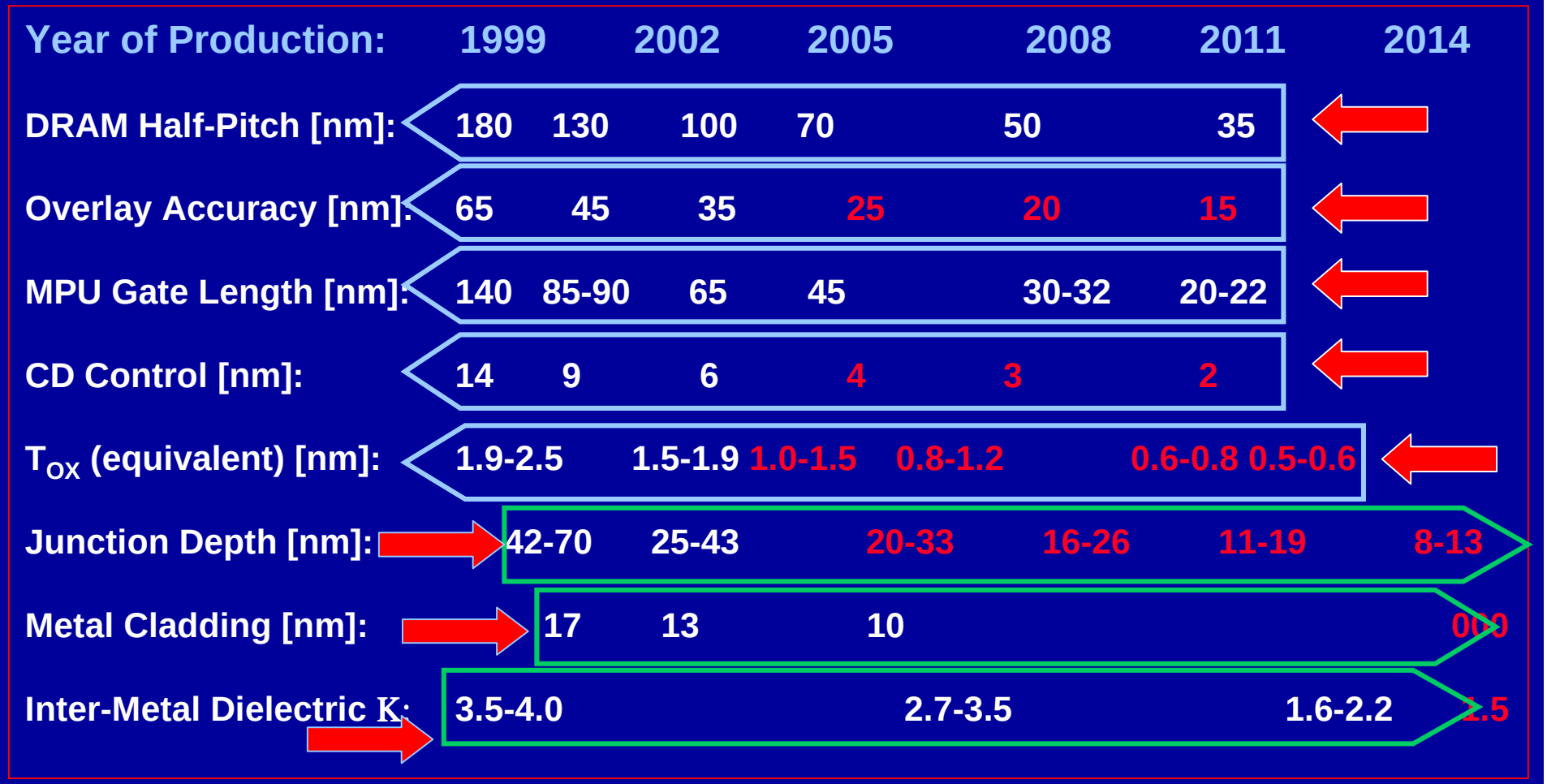
Year of production	1999	2002	2005		2008	2011	2014
DRAM half-pitch (nm)	180	130	100		70	50	35
Overlay accuracy (nm)	65	45	35		25	20	15
MPU gate length (nm)	140	85-90	65		45	30-32	20-22
CD control (nm)	14	9	6		4	3	2
T_{ox} (equivalent) (nm)	1.9-2.5	1.5-1.9	1.0-1.5		0.8-1.2	0.6-0.8	0.5-0.6
Junction depth (nm)	42-70	25-43	20-33		16-26	11-19	8-13
Metal cladding thickness (nm)	17	13	10		0	0	0
Intermetal dielectric constant, k	3.5-4.0	2.7-3.56	1.6-2.2		1.5	<1.5	<1.5



Source: Semiconductor International - http://www.e-insite.net/semiconductor/index.asp?layout=article&articleId=CA187876

Roadmap Acceleration and Deceleration

2001 versus 1999 Results



2001 ITRS ORTC Node Tables – w/Node Cycles

[Node = DRAM Half-Pitch (HP)] **[3-Year Node Cycle]**

Table 1a Product Generations and Chip Size Model Technology Nodes—Near-term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm) ††	90	75	65	53	45	40	35
MPU Physical Gate Length) (nm)	65	53	45	37	32	28	25
ASIC/Low Power Printed Gate Length (nm) ††	130	107	90	75	65	53	45
ASIC/Low Power Physical Gate Length) (nm)	90	75	65	53	45	37	32

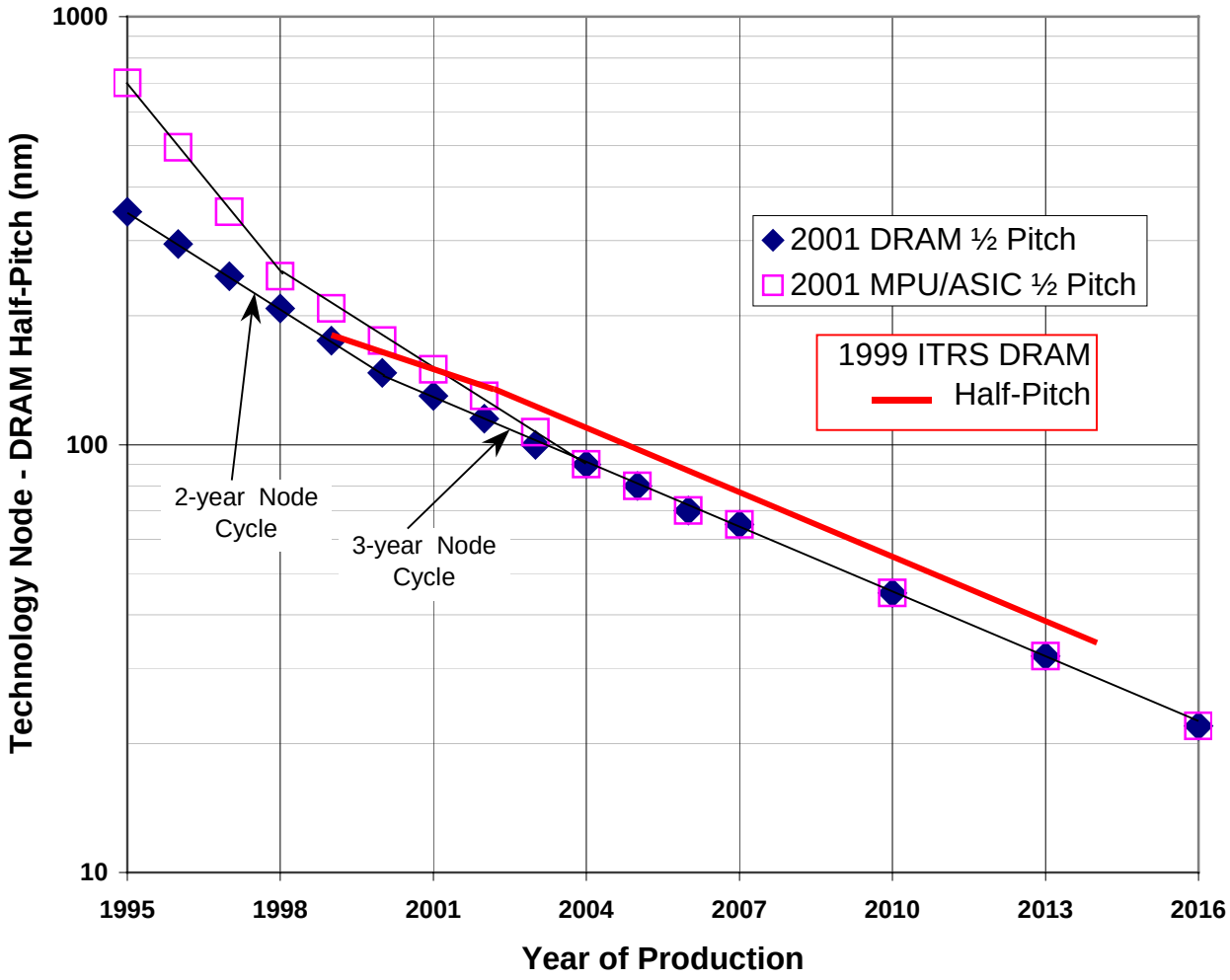
[MPU Gate Length Cycle (GL)]: [2-year cycle] [3-year cycle]

Table 1b Product Generations and Chip Size Model Technology Nodes—Long-term years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm) ††	25	18	13
MPU Physical Gate Length) (nm)	18	13	9
ASIC/Low Power Printed Gate Length (nm) ††	32	22	16
ASIC/Low Power Physical Gate Length) (nm)	22	16	11

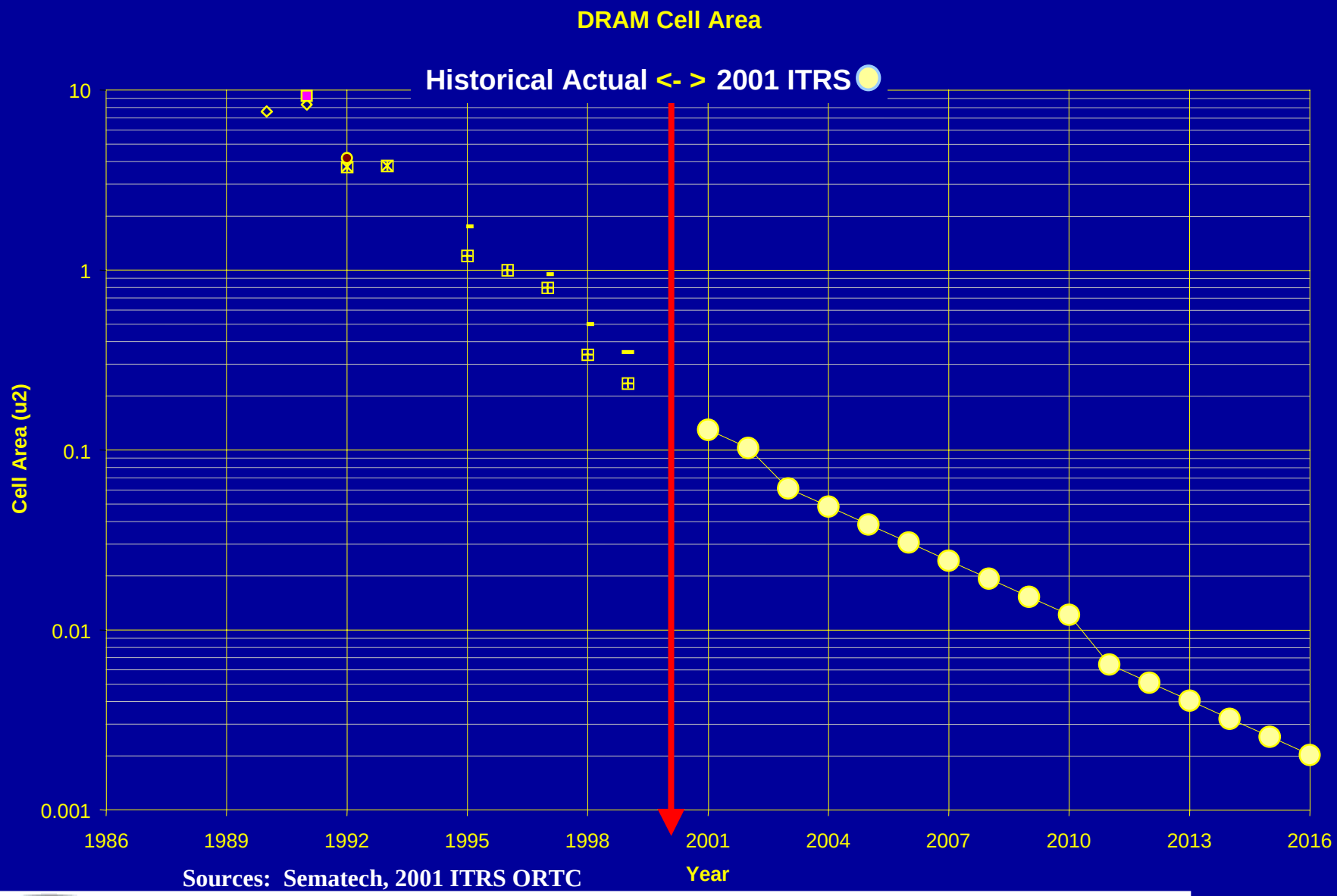
[MPU HP/GL Cycle]: [3-year cycle]

ITRS Roadmap Acceleration Continues...Half Pitch



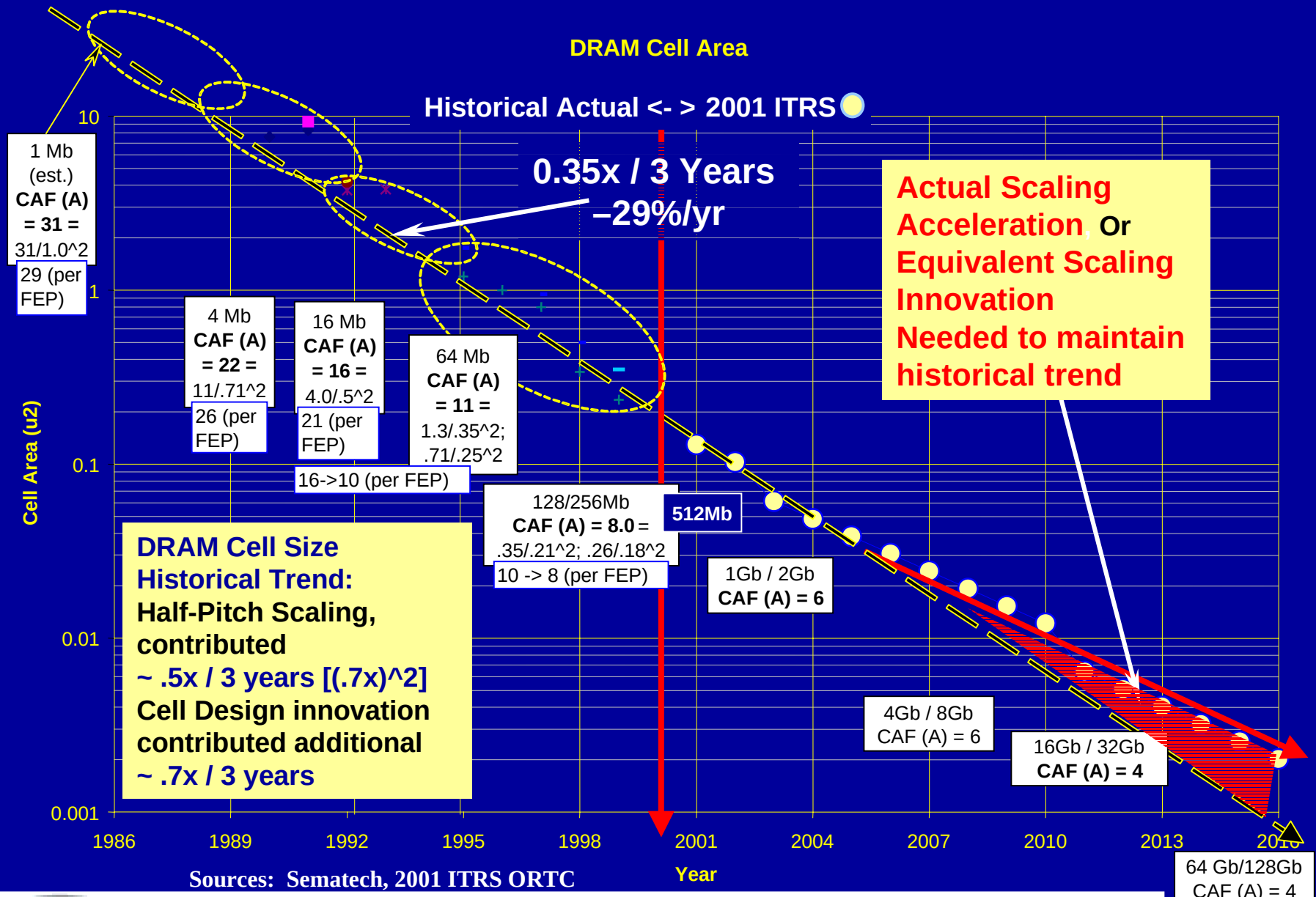
Source: 2001 ITRS - Exec. Summary, ORTC

DRAM Cell Area History / 2001 ITRS Model

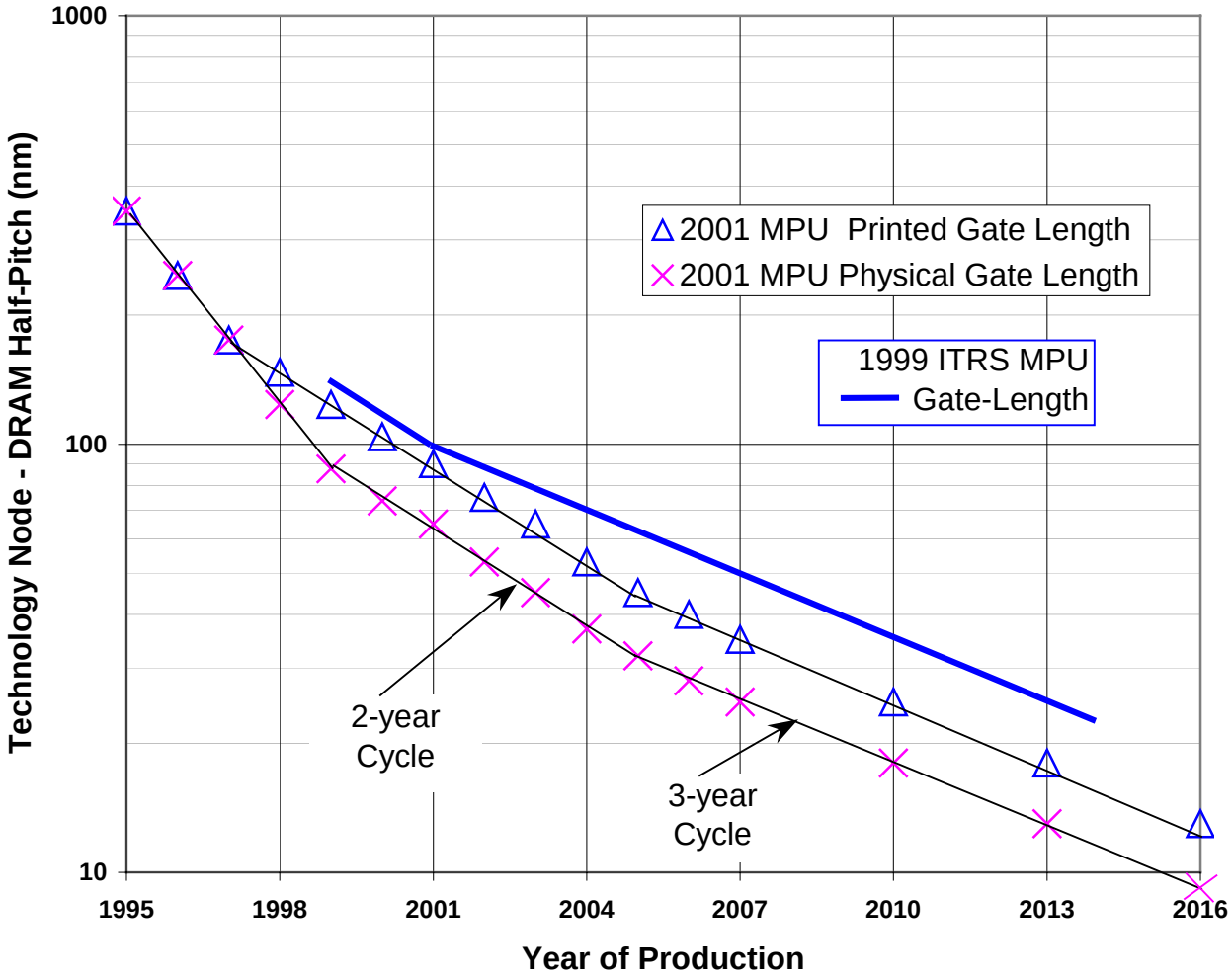


Sources: Sematech, 2001 ITRS ORTC

DRAM Cell Area History / 2001 ITRS Model



ITRS Roadmap Acceleration Continues…Gate Length



Source: 2001 ITRS - Exec. Summary, ORTC

2001 ITRS ORTC MPU Frequency Tables – w/Node Cycles

Table 4c Performance and Package Chips: Frequency On-Chip Wiring Levels— Near-Term Years

YEAR OF PRODUCTION	2001	2002	2003	2004	2005	2006	2007
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU/ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Chip Frequency (MHz)							
On-chip local clock	1,684	2,317	3,088	3,990	5,173	5,631	6,739
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	1,684	2,317	3,088	3,990	5,173	5,631	6,739
Maximum number wiring levels—maximum	7	8	8	8	9	9	9
Maximum number wiring levels—minimum	7	7	8	8	8	9	9

[2-Yr GL Cycle; then 3-Yr]

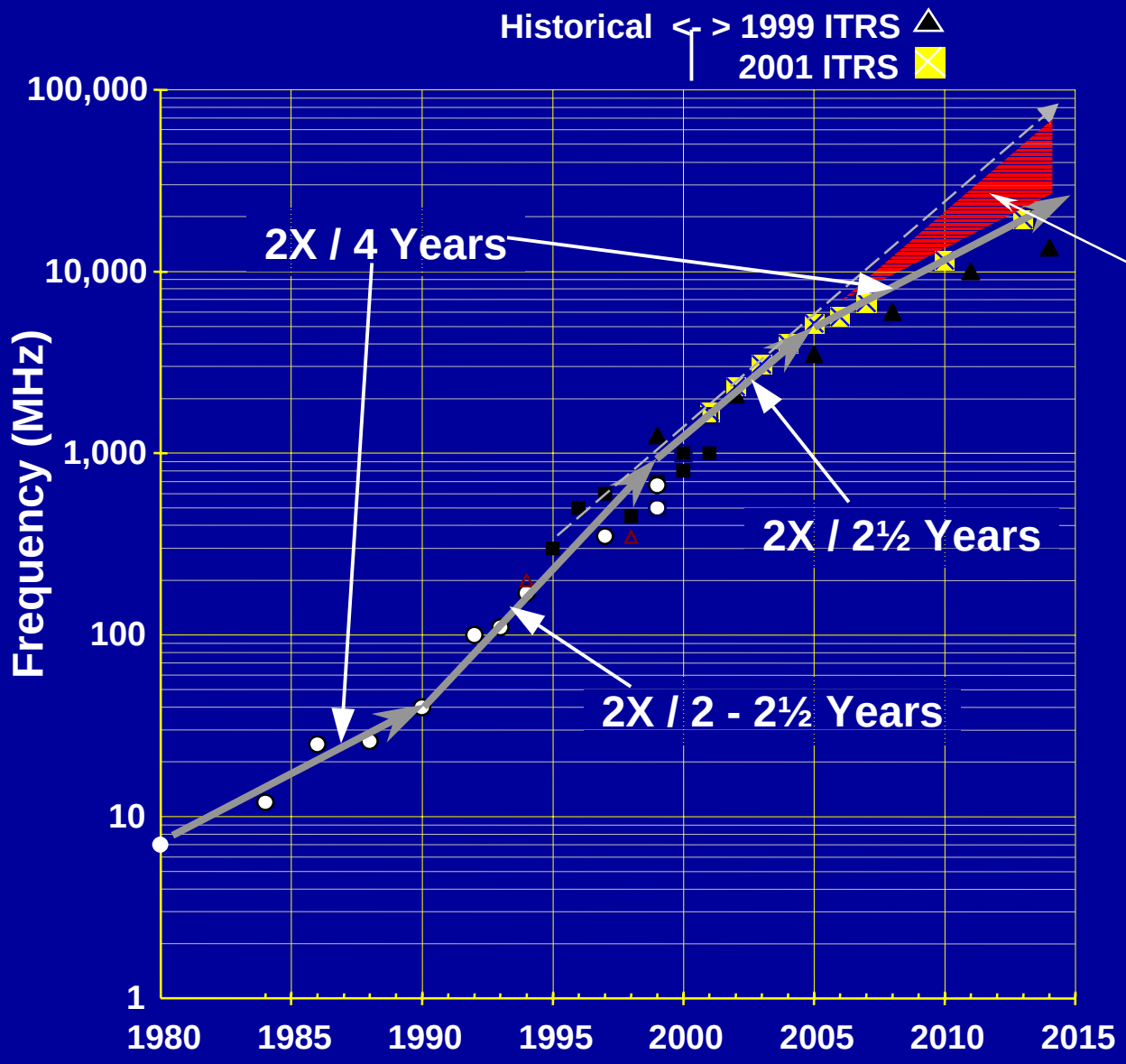
Table 4d Performance and Package Chips: Frequency, On-Chip Wiring Levels—Long-term Years

YEAR OF PRODUCTION	2010	2013	2016
DRAM ½ Pitch (nm)	45	32	22
MPU/ASIC ½ Pitch (nm)	45	32	22
MPU Printed Gate Length (nm)	25	18	13
MPU Physical Gate Length (nm)	18	13	9
Chip Frequency (MHz)			
On-chip local clock	11,511	19,348	28,751
Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[1]	11,511	19,348	28,751
Maximum number wiring levels—maximum	10	10	10
Maximum number wiring levels—minimum	9	9	10

[3-year cycle]

Sources: 2001 ITRS ORTC

MPU Clock Frequency Actual vs ITRS



Actual Scaling Acceleration, Or Equivalent Scaling Innovation Needed to maintain historical trend

MPU Clock Frequency Historical Trend:

Gate Scaling, Transistor Design contributed ~ 17-19%/year

Architectural Design innovation contributed additional ~ 21-13%/year

Sources: Sematech, 2001 ITRS ORTC

Some Examples of ITWG Major Challenges

ITWG

- Design
- ***Lithography***
- ***Test***
- Front End Process
- Interconnect
- PIDS, Emerging Devices
- Assembly & Packaging
- ***Factory Integration***

Cross ITWG

- Environment, Safety, Health
- Metrology
- Modeling and Simulation
- Yield Enhancement

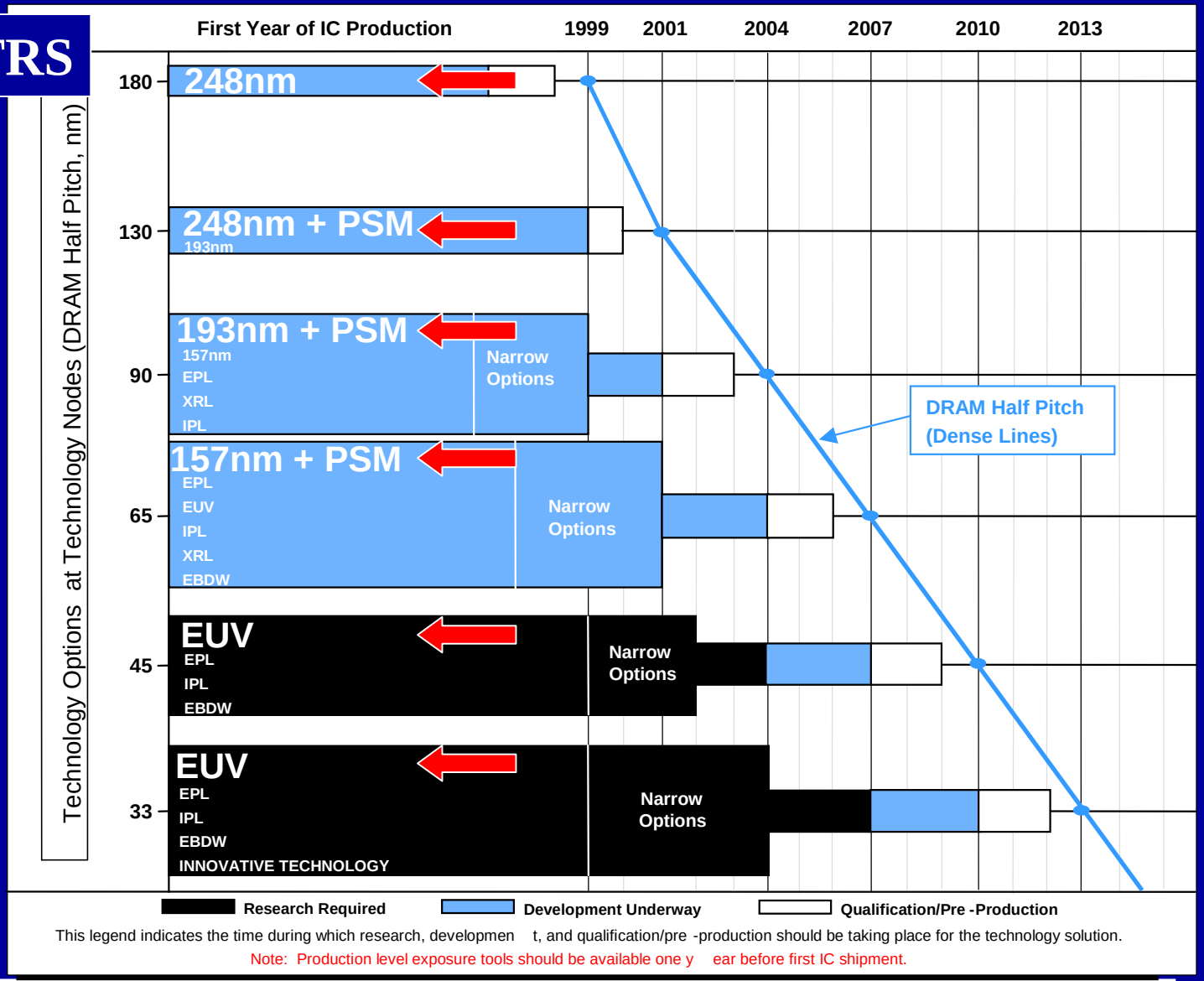
Lithography ITWG Report

ITRS Conference

November 29, 2001
Santa Clara, CA

Lithography Exposure Tool Potential Solutions

2001 ITRS



Difficult Challenges: Near Term

Five difficult challenges ≥ 65 nm before 2007.	Summary of issues
Optical and post-optical mask fabrication	• **Registration, CD control, defectivity, and 157 nm films; defect free multi-layer substrates or membranes.** • **Equipment infrastructure (writers, inspection, repair).**
Cost control and return-on-investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput over time. • Cost-effective masks. • Sufficient lifetimes for the technologies,
Process control	• Processes to control gate CDs to less than 2 nm (3σ) • Alignment and overlay control to < 23 nm overlay.
Resists for ArF and F_2	• Outgassing, LER, SEM induced CD changes, defects ≤ 32 nm.
CaF_2	• **Yield, cost, quality.**

Difficult Challenges: Long Term

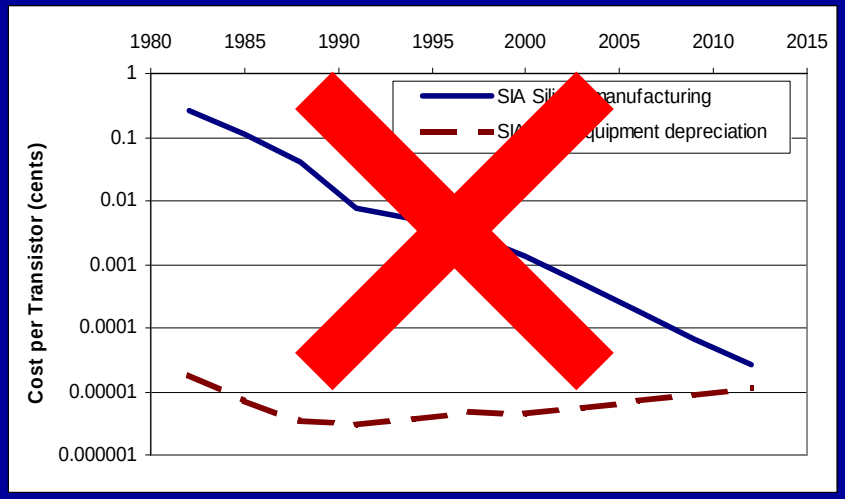
Five difficult challenges < 65 nm beyond 2007.	Summary of issues
Mask fabrication and process control	• **Defect-free NGL masks.** • **Equipment infrastructure (writers, inspection, repair).** • **Mask process control methods.**
Metrology and defect inspection	• Capability for critical dimensions down to 9 nm and **metrology for overlay down to 9 nm, and patterned** wafer defect inspection for defects < 32 nm.
Cost control and return on investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput. • Development of cost-effective post-optical masks. • Achieving ROI for industry with sufficient lifetimes for the technologies.
Gate CD control improvements; process control; resist materials	• Processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness. • Alignment and overlay control methods to < 9 nm overlay.
Tools for mass production	• **Post optical exposure tools capable of meeting requirements of the Roadmap.**

2001 ITRS Test Chapter

ITRS Test ITWG

Don Edenfeld

Scaling Component Test Cost



- Recent steps have enabled test cost to begin to scale across technology nodes
  - Equipment reuse across nodes
  - Increasing test throughput
- Challenge remains in most segments, especially ***high speed and high integration products***

Dismantling the Red Brick Walls

- Design For Test enabling has begun to remove many of the roadblocks that appeared in the 1997 and 1999 roadmaps
  - Test is becoming integrated with the design process
  - Improvements demonstrated in capability and cost
- Continued research is needed into new and existing digital logic fault models toward identification of true process defects
- ***Development of Analog DFT methods must advance***
  - Formalization of analog techniques and development of fault models

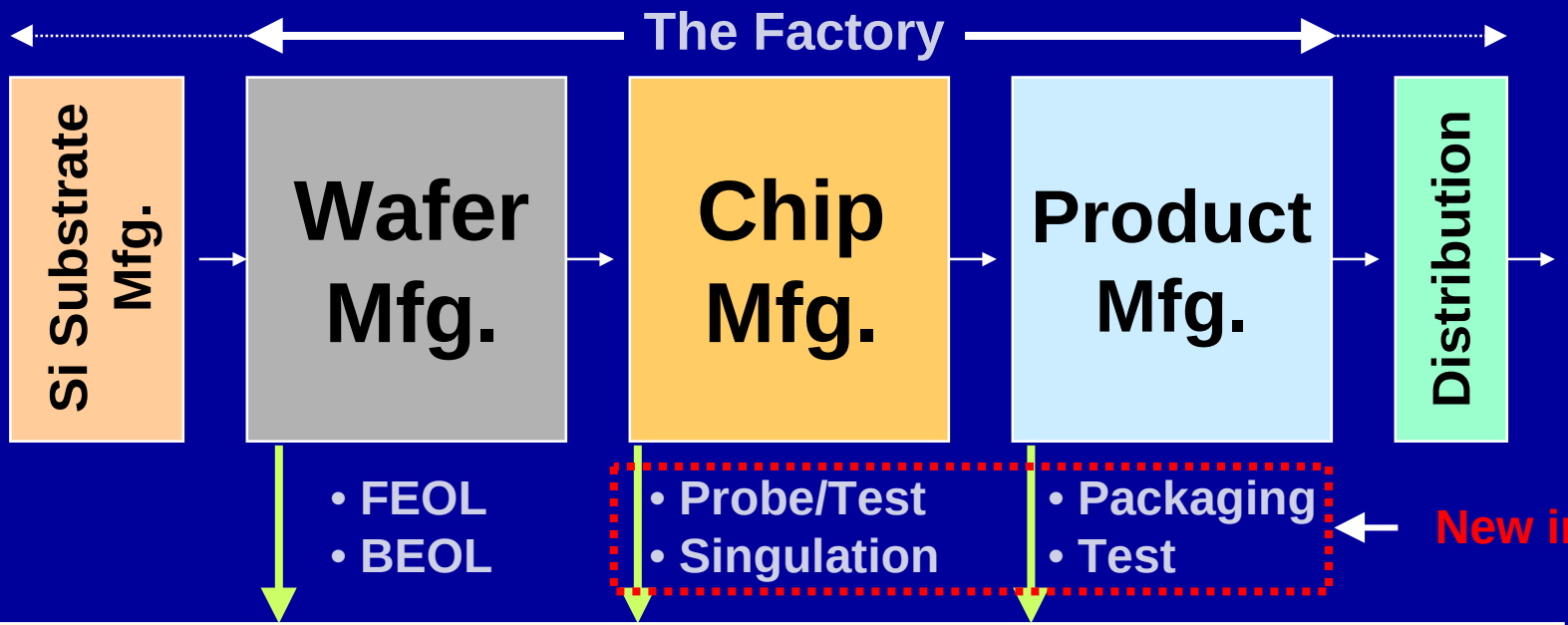
Test Software Standards Focus

- **Standards** for test equipment interface & communication are needed to decrease equipment factory integration time
  - Improve equipment interoperability to reduce factory systems integration time
  - e.g, built into 300mm equipment specifications
- **Standards** for ATE software and test program generation are needed to decrease test development effort and improve time to market
  - Lower the barrier for selecting the optimal equipment
- Increased focus for **standards** development and adoption of existing standards

2001 ITRS
Factory Integration ITWG

Jeff Pettinato

2001 Factory Integration Scope Includes Wafer, Chip and Product Manufacturing



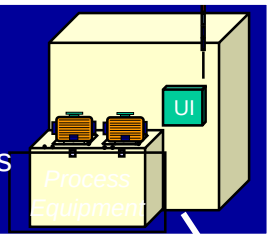
The Factory is driven by Cost and Productivity:

- Reduce factory capital and operating costs per function
- Enable efficient high-volume production with operational models for varying product mixes (high to low) and other business strategies
- Increase factory and equipment reuse, reliability, and overall efficiency
- Quickly enable process technology shrinks and wafer size changes

Factory Integration Requirements and Solutions are Expressed through 6 Functional Areas

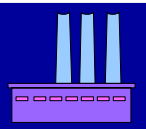
Production Equipment

- Process and Metrology equipment
- Mainframe and process chambers
- Wafer Handling Robots, Load Ports
- Internal software & computers



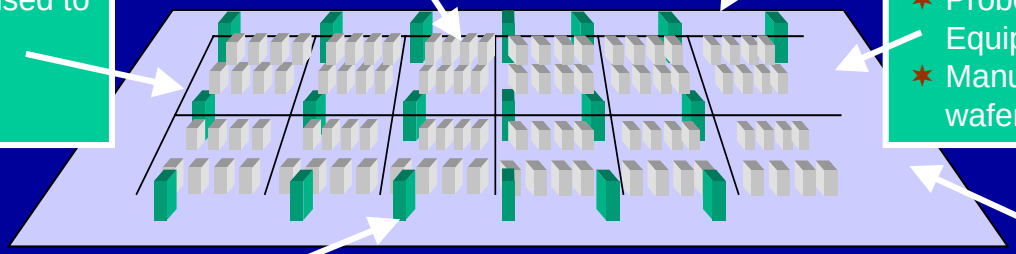
Facilities

- Cleanroom, Labs, Central Utility Building
- Facilities Control and Monitoring Systems
- Power, Plumbing, HVAC, Utilities, Pipes, UPS
- Life safety systems, waste treatment



Factory Operations

- Policies and procedures used to plan, monitor and control production
- Direct factory labor

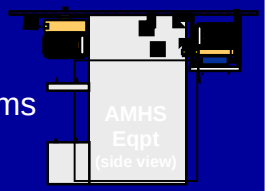


Test Manufacturing

- Prober, Handler, and Test Equipment
- Manufacturing processes to test wafers and chips

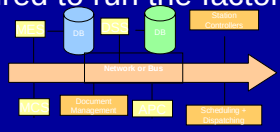
Material Handling Systems

- Wafer and Reticle Carriers
- Automated storage systems
- Interbay & intrabay transport systems
- Personnel guided vehicles
- Internal Software & computers



Factory Information & Control

- Data and Control systems required to run the factory
- Decision support
- Process control
- Plan, Schedule, Dispatch
- Computers, databases, software outside equipment



2001 Difficult Challenges

> 65nm through 2007

- ***Managing Complexity***
  - Quickly and effectively integrating rapid changes in semiconductor technologies and market conditions
- Factory Optimization
  - Productivity increases are not keeping pace with needs
- ***Flexibility, Extendibility, Scalability***
  - Ability to quickly convert to new semiconductor technologies while reusing equipment, facilities, and skills

< 65nm after 2007

- ***Post CMOS Manufacturing Uncertainty***
  - Inability to predict factory requirements associated with post CMOS novel devices
- ***450mm Wafer Size Conversion***
  - Timing and manufacturing paradigm for this wafer size conversion

Summary

- **Technology acceleration continued with 2001 ITRS**
- **DRAM half-pitch is expected to return to a 3-year cycle after 2001 but….*so we have said before***
- **The Red Brick Wall is still there but it has become permeable**
- **Innovation will be necessary, in addition to technology acceleration, to maintain historical performance trends**

Summary(cont.)

- **Major challenges have been identified by each of the ITWGs – many opportunities for innovative R&D**
- **Many material transitions are needed, but not sufficient, in the next few years to maintain the scaling pace**
- **Close coordination of design, process integration and packaging is required to meet system requirements in the future**
- **Please visit the online resources at:** http://www.sematech.org/public/resources/index.htm

Words to the Wise…

- "Word.. without Action.. is Dead" – James ca 1st Century
- "Simplest..is Best" – William of Ockham, ca 13th Century
- **"Better..Faster..Cheaper"** – Craig Barrett, ca 21st Century (and also daily)
- "Talk..is Cheap" – Semiconductor Suppliers

Backup

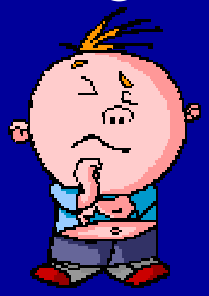
[Test] Summary

How can we improve manageability of the divergence between validation and manufacturing equipment?

Can ATE instruments catch up and keep up with high speed serial performance trends?

Can DFT mitigate analog test cost as does in the digital domain?

What is the cost and capability optimal SOC test approach?



What happens when high speed serial interfaces become buses?

How can we make test of complex SOC designs more cost effective?

Will market dynamics justify development of next generation functional test capabilities?

Can DFT and BIST mitigate the mixed signal tester capability treadmill? What other opportunities exist?

Will increasing test data volume lead to increased focus on Logic BIST architectures? What are the other solutions?