Burn-in & Test Socket Workshop

March 3-6 , 2002
Hilton Phoenix East/Mesa Hotel
Mesa, Arizona

IEEE

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Test Technology Technical Council

Burn-in & Test Socket Workshop

Technical Program

Session 4
Tuesday 3/05/02 10:30AM

Burn-in Methodology

“Alternatives For Burning In Bare Die”

Steve Steps - Aehr Test Systems

“Strip Burn-in For Fine Pitch Semiconductor Devices”

Hon Lee Kon - Intel Corporation
Hongfei Yan - Intel Corporation
(Presented By: KW Low - Intel Corporation)

“High Performance Burn-in In Low Cost Environment"

Tamas Kerekes - ELES Semiconductor Equipment
Giampiero Trupia - STMicroelectronics

Alternatives for Burning in Bare Die

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Steve Steps
Aehr Test Systems

AEHR TEST SYSTEMS

Agenda

- Why is bare die burn-in important?
- What are bare die burn-in and test alternatives?
- What is Wafer-Level Burn-in and Test?
- Cost Comparison Charts
- Conclusions

Market Demands

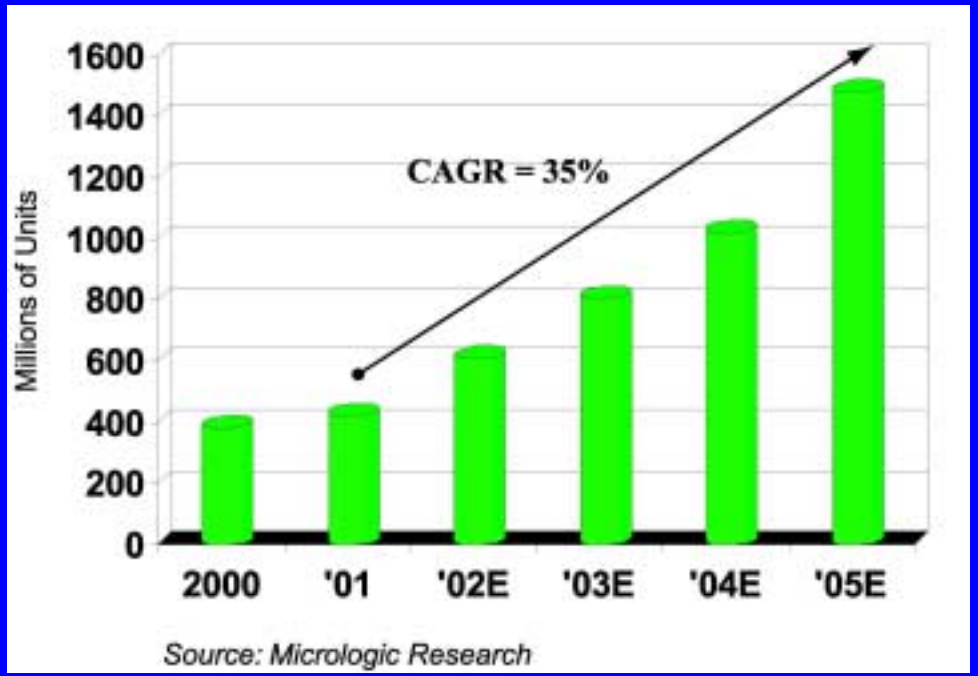
- Higher capability cellular telephones, PDAs, portable music
- Lighter weight
- Smaller size
- Willing to pay a premium price





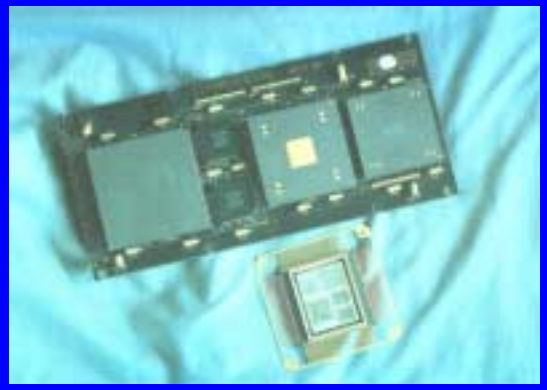
Market Trends

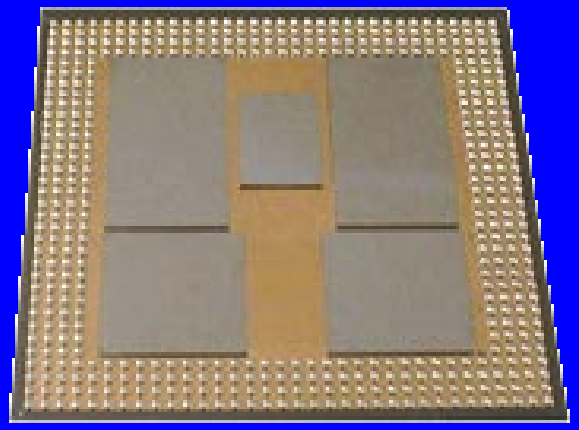
- Demand for these devices is growing rapidly
- Market for new devices is also growing



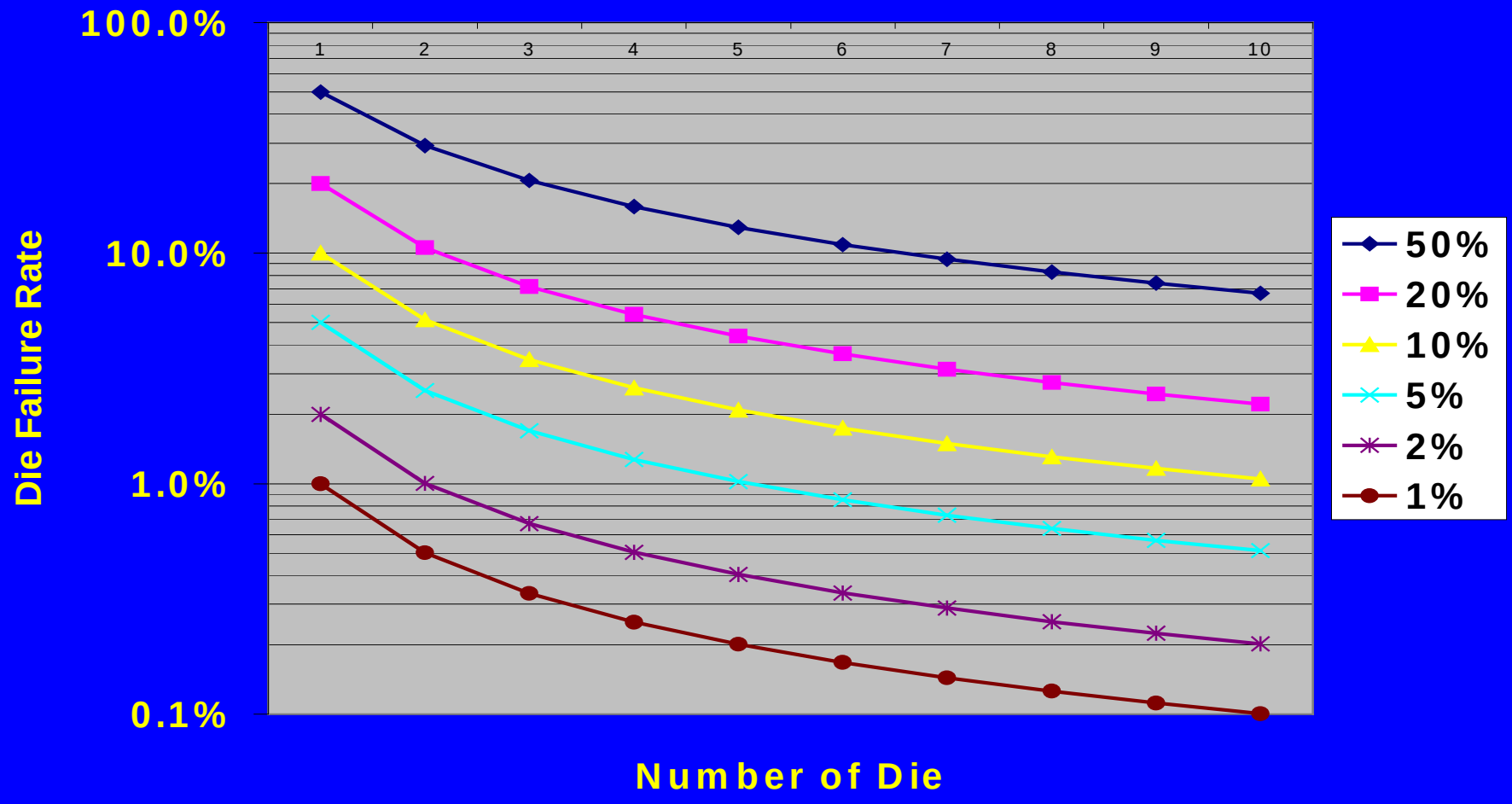
Technology Solution

- Miniaturization is the solution
- System On a Chip (SOC) has mixed technology issues
- Multiple, bare die on a substrate (MCM, SIP, SOP, etc.)





Highly Reliable Die Required



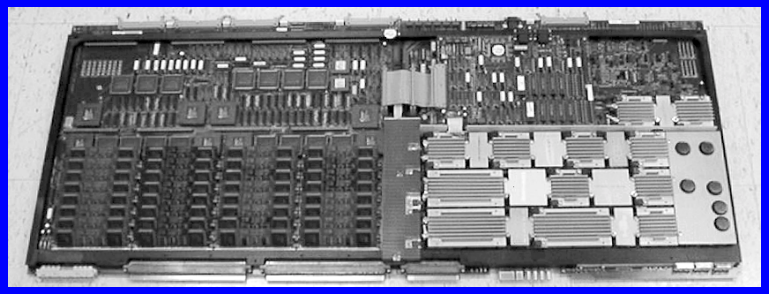
KGD Die Burn-In Alternatives

- Wafer-Level Burn-in and Test (WLBT)
- Bare die temporary package (e.g., DiePak®)
- Wafer Probing
- Minimal packaging (e.g., CSP)

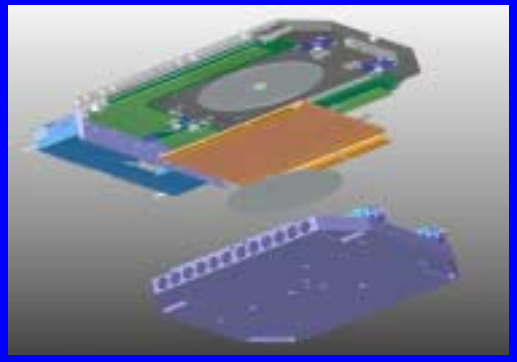
Wafer Level Burn-In System

FOX™ FULL WAFER CONTACT

Oven



System Electronics



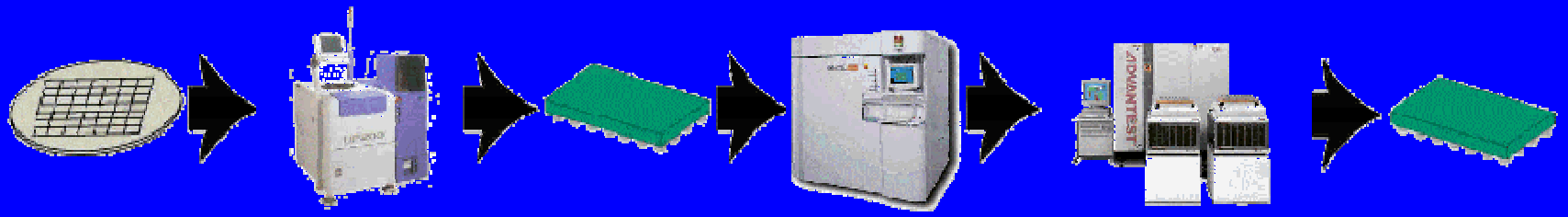
WaferPak™

Load Station

AEHR TEST SYSTEMS

Traditional Back-end vs. WLBT

Traditional Back-end



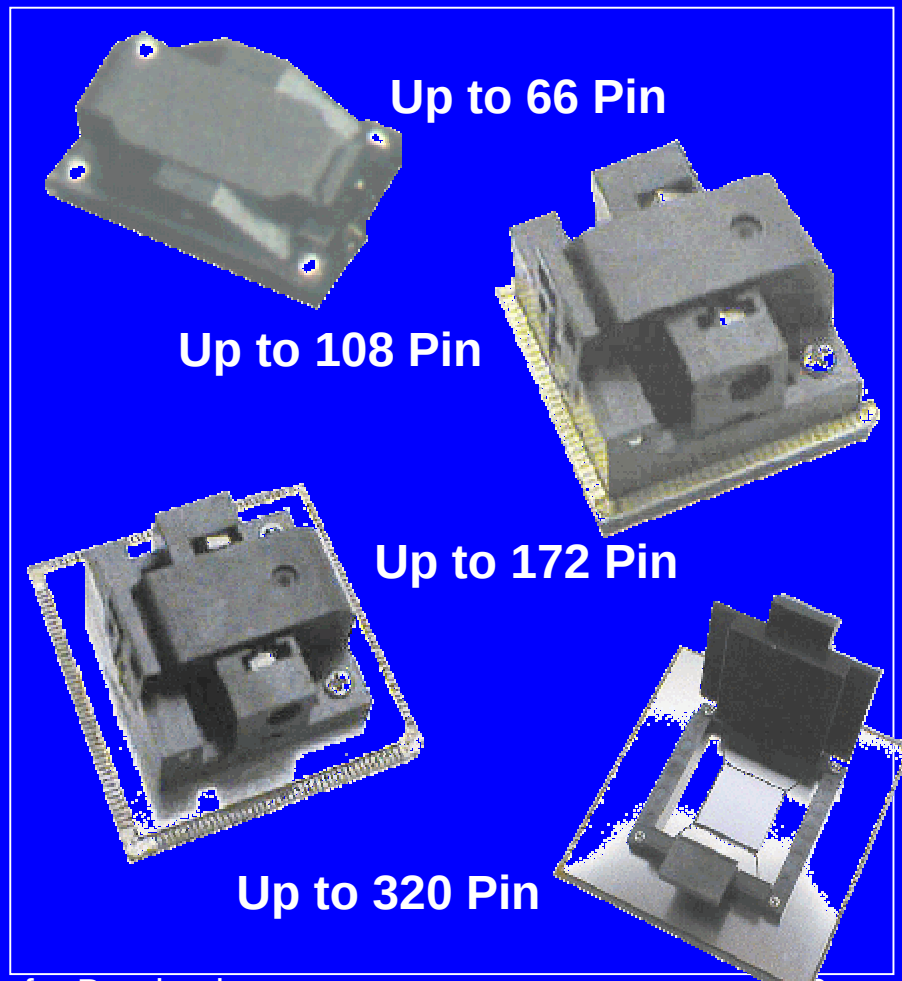
Wafer | Wafer Probe | Package | Burn-in | Final Test | Known-Good Package

Wafer-Level Burn-in and Test

Wafer | Wafer-Level Burn-in and Test | Wafer Final Test | KGD Wafer

DiePak® Carrier Products

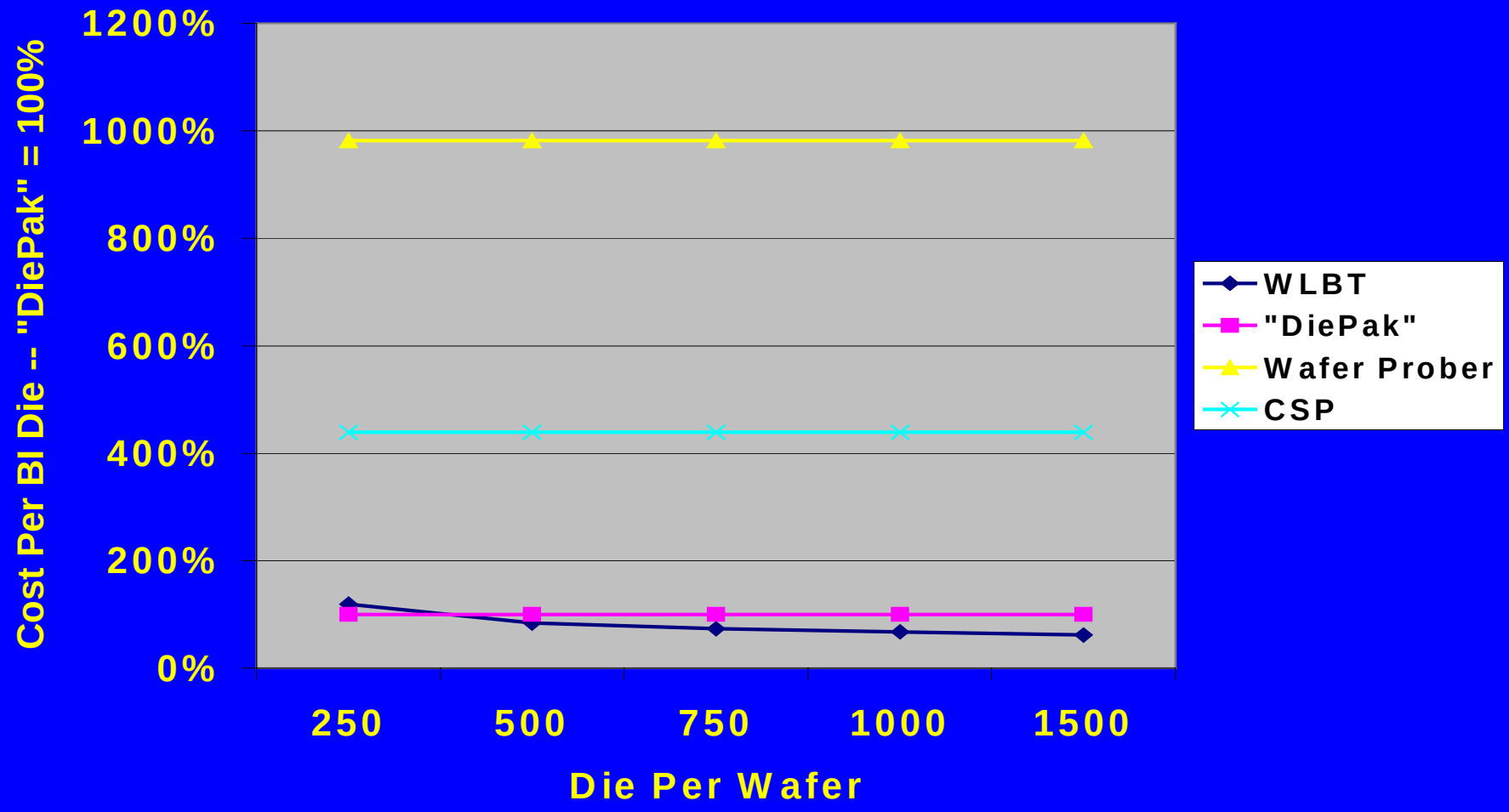
- A family of reusable temporary packages
- Enables burn-in and test of bare die
- Improves yield and lowers cost of SiPs and MCMs



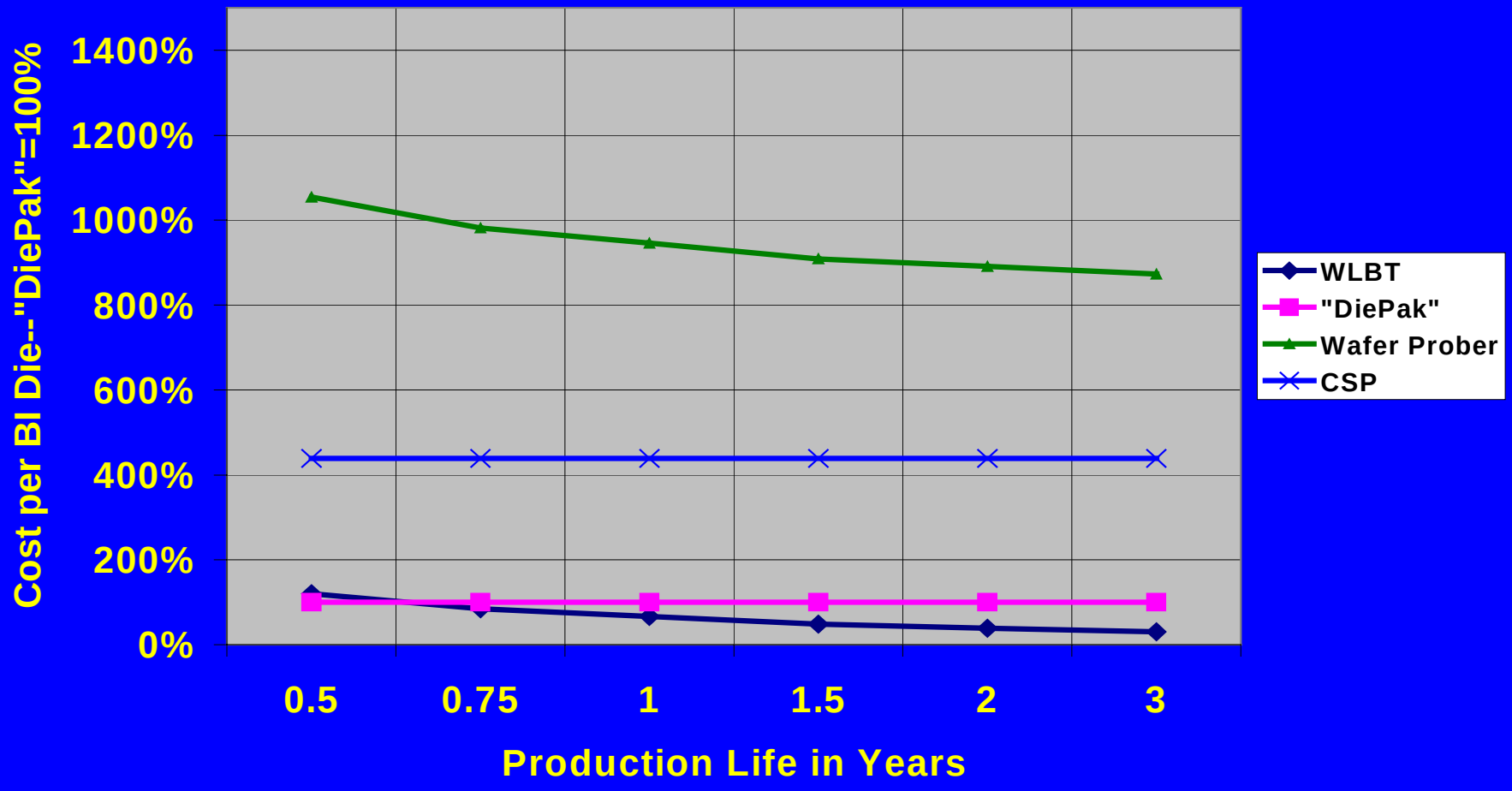
Cost Per Burned-In Die

- Versus die per wafer
- Versus production life
- Versus burn-in time
- Cost breakdowns

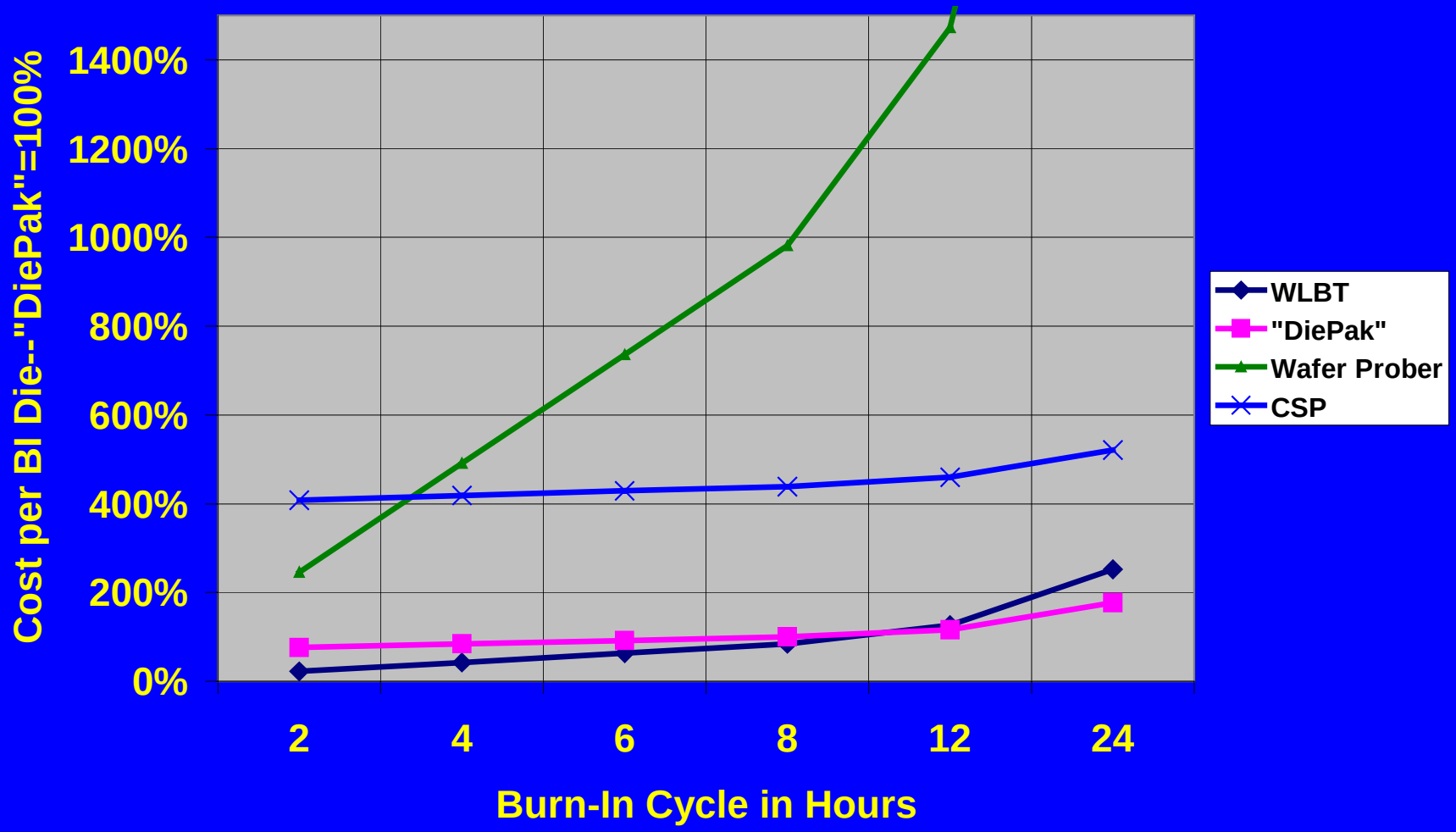
Affect of Die Per Wafer



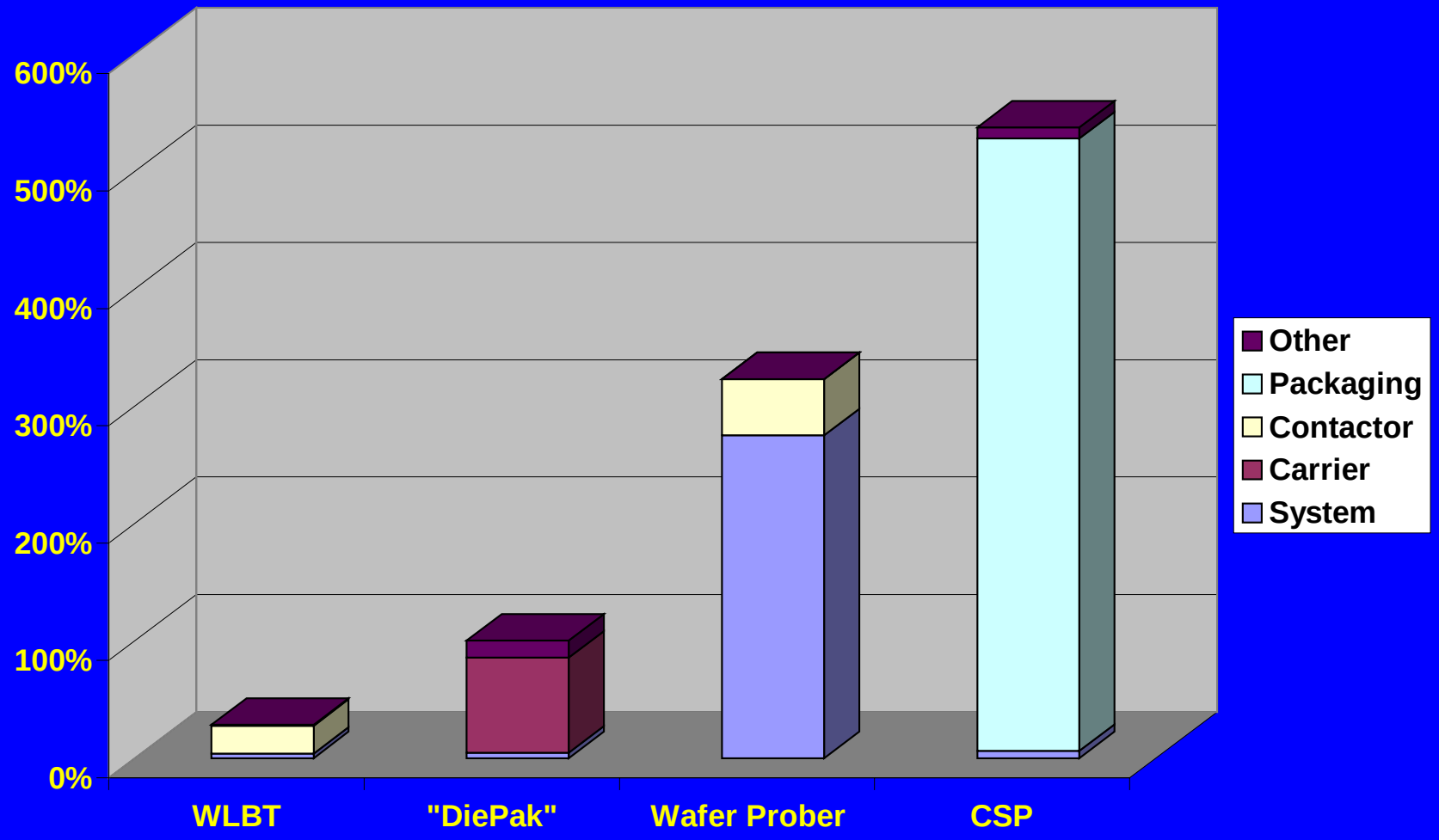
Affect of Production Life



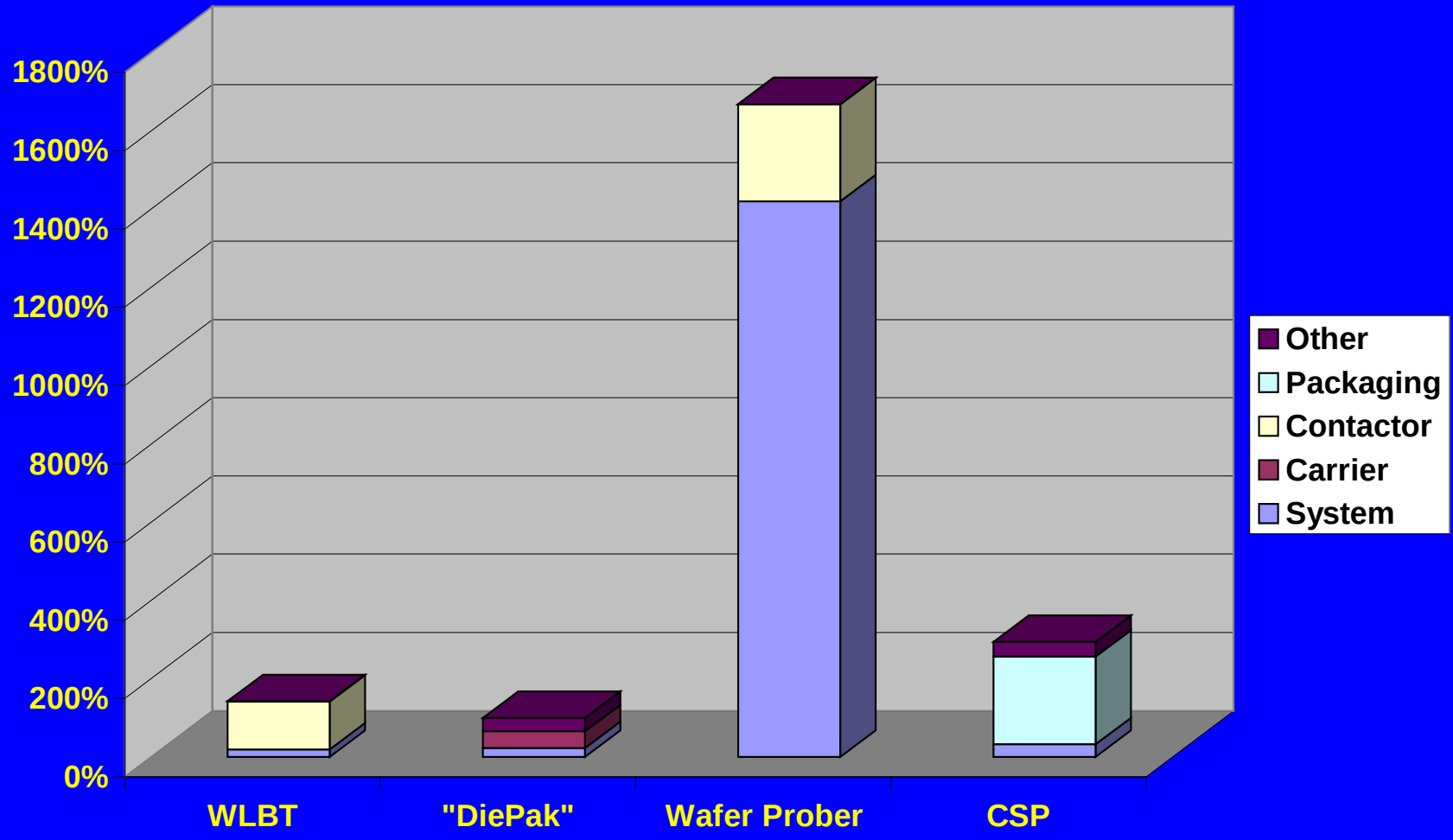
Affect of Burn-In Hours



Cost Breakdown – 2 Hour BI



Cost Breakdown – 24 Hour BI



Conclusions

- The optimal solution varies by die per wafer.
  - Fewer die per wafer favors “DiePak”
  - More die per wafer favors WLBT
- The optimal solution varies by burn-in time.
  - For short burn-in, WLBT is preferred
  - For longer burn-in, “DiePak” is preferred

Conclusions

- The cost drivers vary by burn-in time.
  - Shorter burn-in cycles dominated by "consumables"; e.g., packaging and carriers.
  - Longer burn-in cycles are dominated by "system" costs; e.g., system hardware, operating costs, contactors
- The optimal solution varies by Production Life
  - Longer Production Life stronger favors WLBT

Conclusions

- Volume cost factors
  - Very low volume favors prober
  - Low volume favors DiePak and CSP
  - High volume favors WLBT
- Future trends
  - Cost will trend down over time for all choices
  - WLBT will have the steepest trend

Strip Burn-in For Fine-Pitch Semiconductor Packages

Hon Lee Kon/ Hongfei Yan

intel

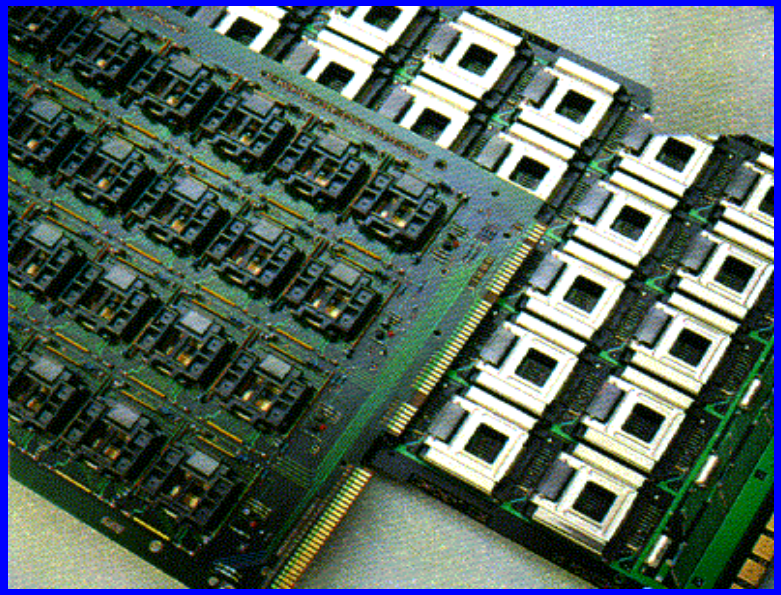
BiTS
BURN-IN & TEST SOCKET WORKSHOP

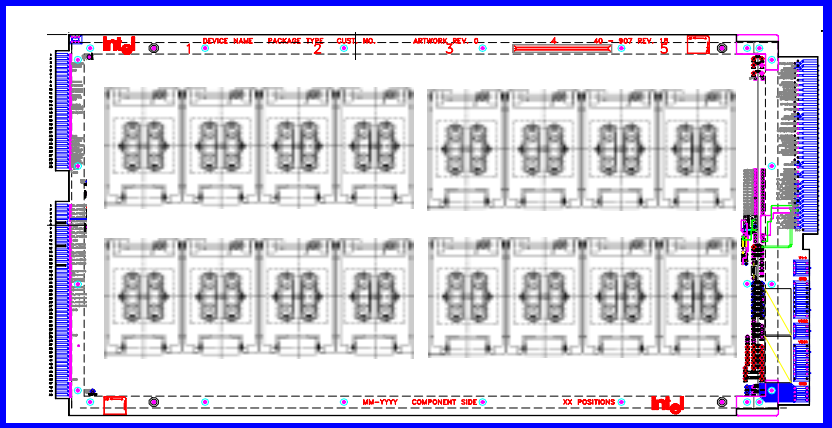
2002 Burn-in and Test Socket Workshop

Agenda

- Introduction – What Is Strip Burn-In (BI) ?
- Advantages
- Technology Challenges & Consideration for BI Board/Socket
- Areas of Concern
- Conclusions
- Acknowledgement

What Is Strip BI ?





Conventional Burn-in

- Singulated DUT / BI Socket
- Post assembly process

Strip Burn-in

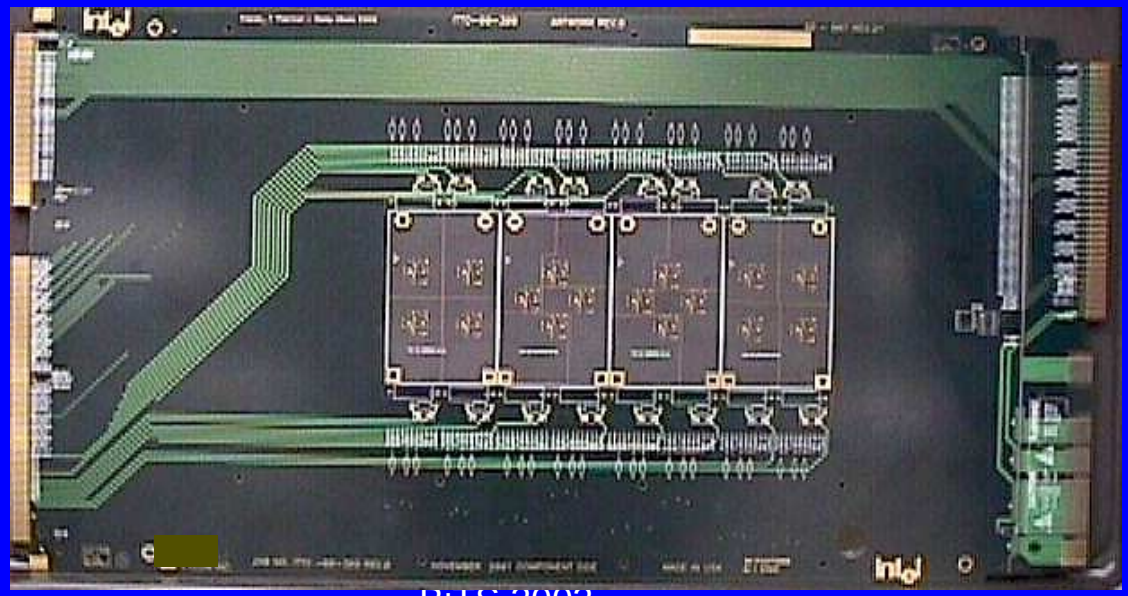
- Strip Panel prior to singulation
- CSP Packages
- Semi-completed assembly process

Burn-in Form Factor Changed Dramatically !

How does this impact us?

Why Strip BI ?

- **Improve Burn-in efficiency for fine pitch devices**
  - Provide massive parallel test capability
  - Improved Tj control for speed test/improved bin split
  - Weed out any assembly related defects prior to unit singulation
  - Improved handling for small form-factor packages eg. µBGA CSP



Technology Challenges

- Provide accurate, reliable and repeatable contact pin alignment to surface contact and contact pin to package alignment. (industry standard : ±0.002”)
- Utilize existing PCB fabrication process for fine pitch design (<0.8mm) [Current conventional PCB fab is at its limit for fine pitch design]
- Minimize positional error for contact pads to socket guide pins
- Stable and capable process in high volume manufacturing
- PCB material selection and design routing
- Interaction between CTE of silicone die and PCB
- Cost effective (cost target $?)

Strip Burn-In Board Design Consideration

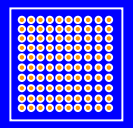
- Fine pitch, high density design
- PCB Material Selection

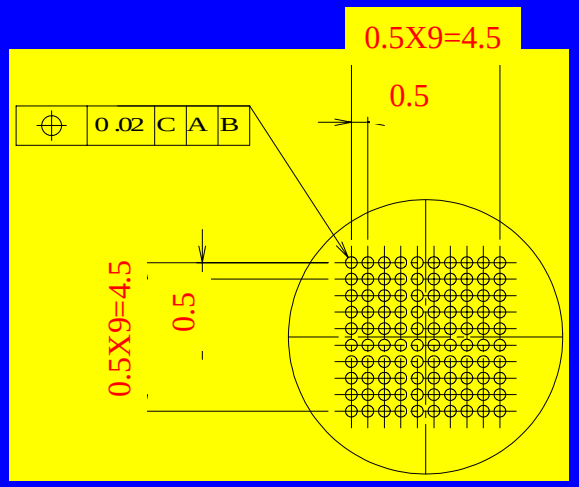
1) Fine Pitch, High Density Design

Typical 35 x 35mm package

8x8 mm

7x7 mm





- **Form Factor Comparison**
  - **Each strip has multiple die on the substrate**
  - **Each substrate has more than >30 die.**

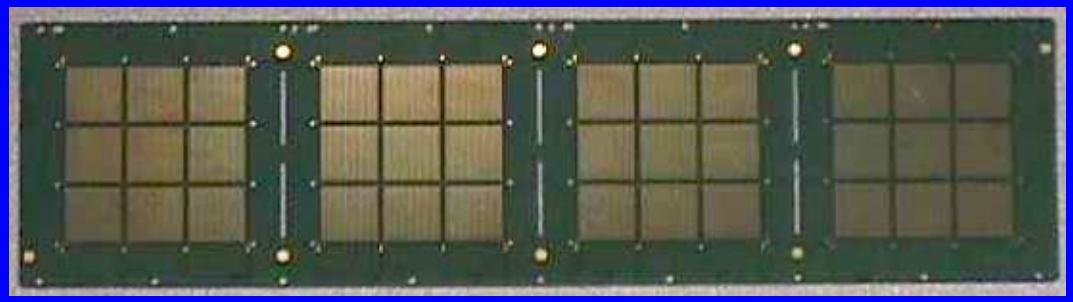
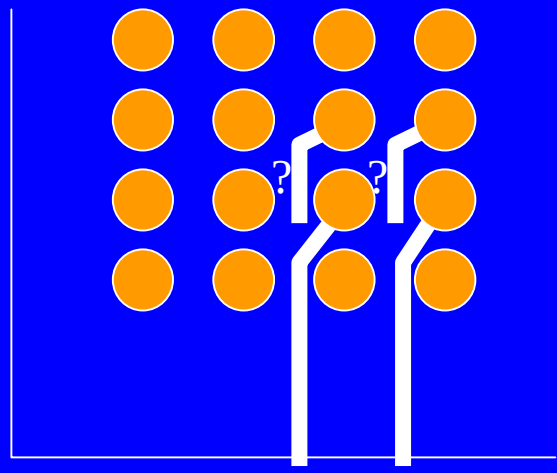


Photo illustration are not to scale. They are for relative size comparison.

PCB trace routing

- smaller via drilling aspect ratio violate current PCB mfg. spec (for 62mils board)
- Array inner pad trace fanout problem:- double/triple tracks difficult to achieve
- Small trace width (~ 3mils) is hard to manufacture



Design & Mfg. issues

- very low PCB yield (percentage)
- assembly wave soldering capability unknown
- cost & TPT increases exponentially (graph)

2) PCB Material Selection Consideration

PCB Laminates

- Non-Woven vs Woven laminates
  - For fine pitch, copper migration along the glass bundles causing shorts between adjacent holes, or holes and conductors

Conductive Anodic Filament (CAF) Phenomenon

- Advantages of Non-Woven material
  - Minimal / No warpage, extremely flat finished bare board.
  - Excellent dimensional stability.
  - Improved drilling locational accuracy, (less deflection, drill wander), less drill breakage on microdrills .

Strip Burn-In Socket Design Consideration

- Socket to strip package contact alignment
- Handling issue and strip damage control
- Socket Contact Alignment to PCB

1) Contact Alignment between Socket and Pkg

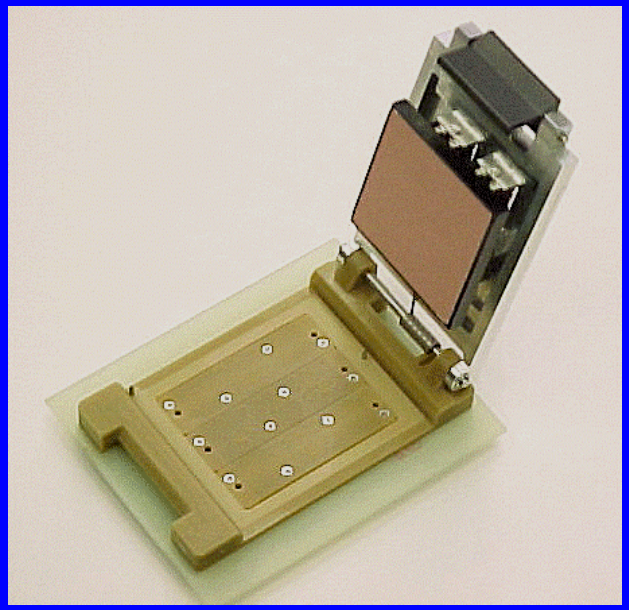
- **Form Factor Consideration**
  - **Each strip has multiple die on the substrate**
  - **Each substrate has more than >30 die**
  - **Long dimensions**
  - **Fine pitch**
- **No optical alignment feature available/feasible in BI**
  - **Mechanical tooling holes for alignment**
- **CTE mismatch**

2) Handling Issue and Strip Damage Control

- **Load and unload strip Pkg to socket**
  - **Long and thin substrate**
  - **Thin die**
- **Engaging Pkg to socket contact**
  - **Warpage issue**
  - **Avoid die damage**

3) Contact Alignment to PCB

- Socket design for long dimension
  - Modular concept vs. single piece concept
- Fine pitch of contacts
- Alignment features of socket contacts to PCB
  - Positional tolerance of contacts
  - Tolerance of Alignment pin size and position



Areas of Concern

Socket to Package:

- Insufficient travel of package and warpage – which leads to insufficient contact force and consequently, high / unstable resistance or electrical open
- Package to socket pocket alignment – need fine adjustment from finger to press on package to make contact
- Sensitive to foreign material on contact points

Socket to PCB:

- X-Y alignment between socket contact to PCB pads is off incrementally from X-axis and decrement-ally from Y-axis.
- The effect is accumulative for the difference between drill hole and pads, as they are from 2 different processes; drilling and etching.
- Different datum / reference point used in both processes.
- Z-stack up between socket contact to PCB is sensitive to traces / routings / solder mask on PCB substrate
- Sensitive to foreign material

Conclusion

- Strip BI improve burn-in efficiency for fine pitch devices
- Process stability, dimensional with respect to the accuracy and PCB selected are key challenges for fine pitch design.
- Smaller vias, trace fanout topology, trace width and mechanical alignment are main design considerations for fine pitch.
- Paradigm shift in burn-in socket design – modular concept vs single piece concept
- Alignment of socket to PCB and strip panel to socket are critical factors and need to be addressed up front during development.

Acknowledgement

The Authors would like to acknowledge the contribution from their colleagues to this BiTS paper.

- **Intel Test Tooling Organization**
- **Paul Schubring, Michael Carroll**
- **KW Low**

High Performance Burn-In in Low Cost Environment

Tamás Kerekes - ELES
Giampiero Trupia - STMicroelectronics

2002 Burn-in and Test Socket Workshop
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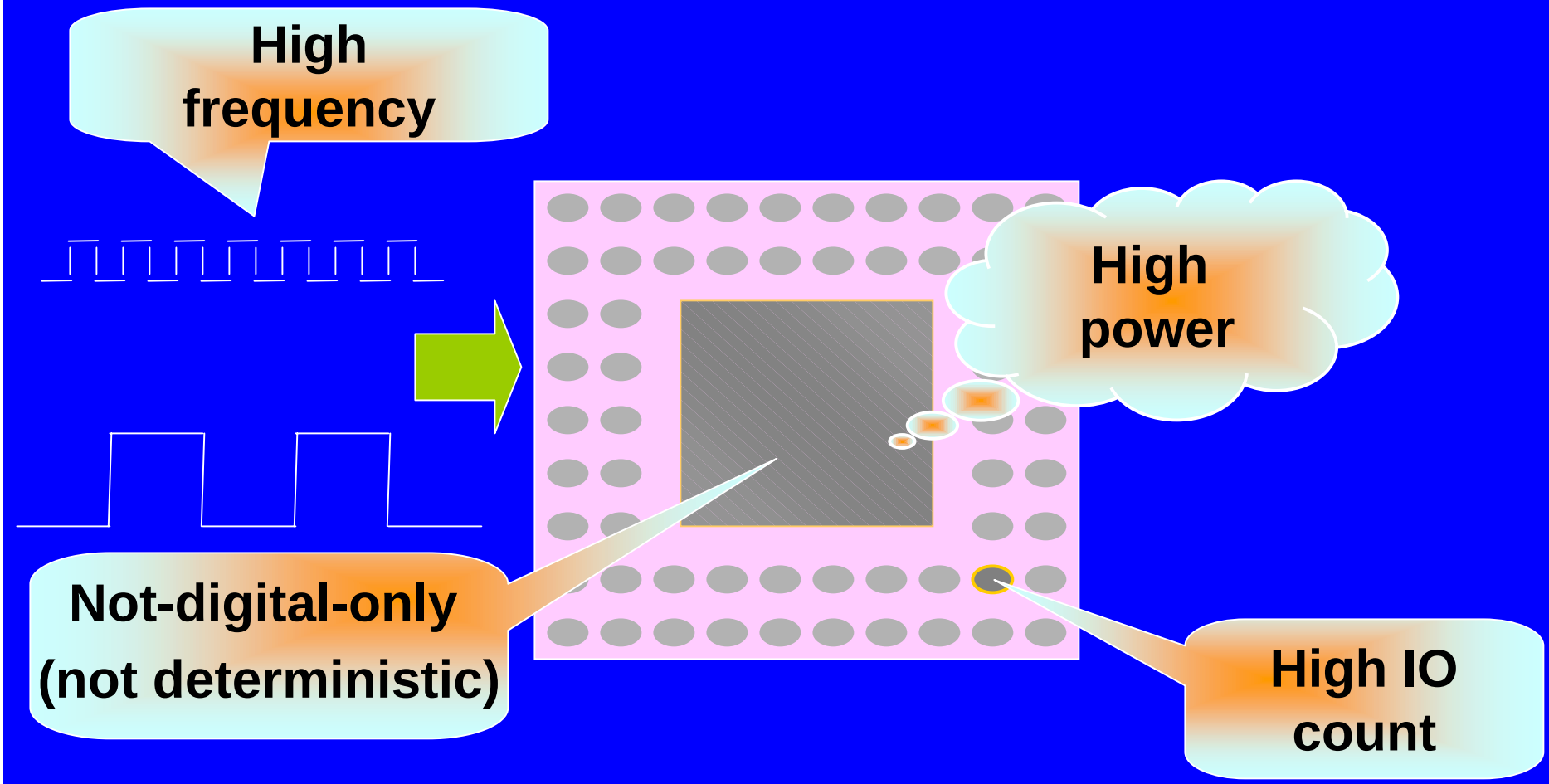
Agenda

- Burn-In on µC and SOC
- Design For Test in Burn-In
- The SOFT-BIST concept
- Extended data acquisition
- The benefits of SOFT-BIST
- Conclusions

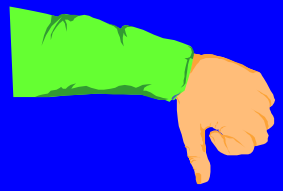
SOC Burn-In Challenges

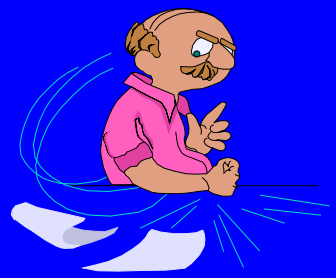


Increased complexity and cost of equipment and board

In Order to Save

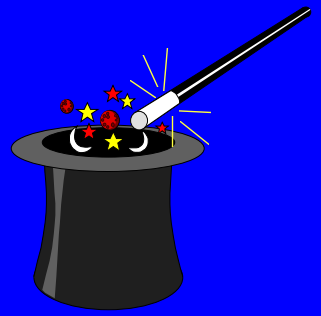
Make simple device





Reduce test complexity

Apply DFT and DFpT



DFT in Burn-In

- **The only way to ensure testability and "burninability"**
- **Drawbacks (scan-chain, BIST):**
  - larger silicon surface
  - longer time-to-market
  - low flexibility
  - scan-chain: long vector sequences (memory, time)

The Dream DFT

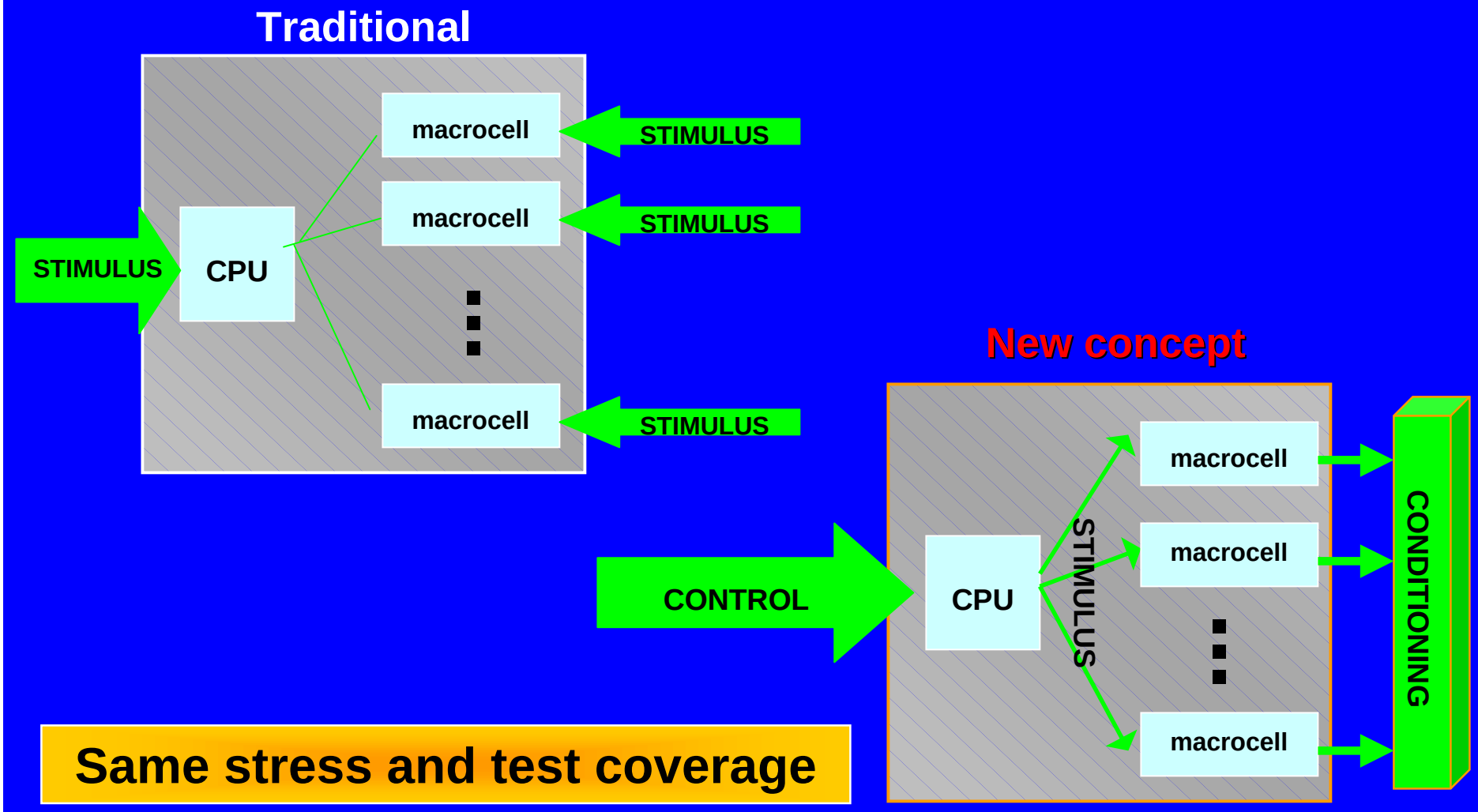
- No additional silicon surface
- High flexibility
- High test and stress coverage
- Burn-in at max. speed
- Simplified equipment and boards

Dreams and Reality

- **The dream can turn into reality through:**
  - Fully programmable test engine
  - Simple interface (few low speed IOs and clock)

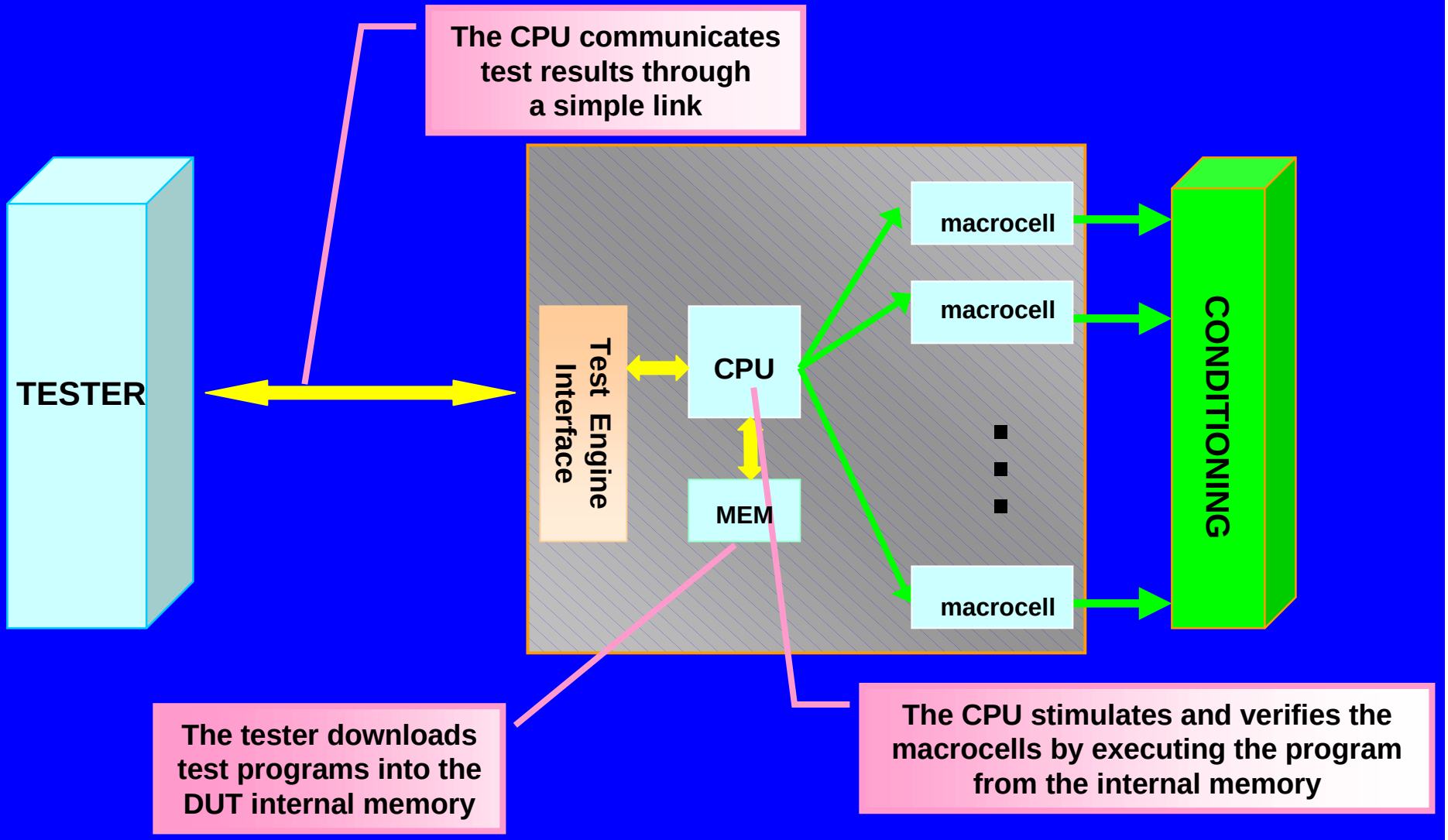
➔ **In µC and SOC the test engine may be the same as the application CPU (applying a few simple design rules)**

Change of the Burn-In Concept

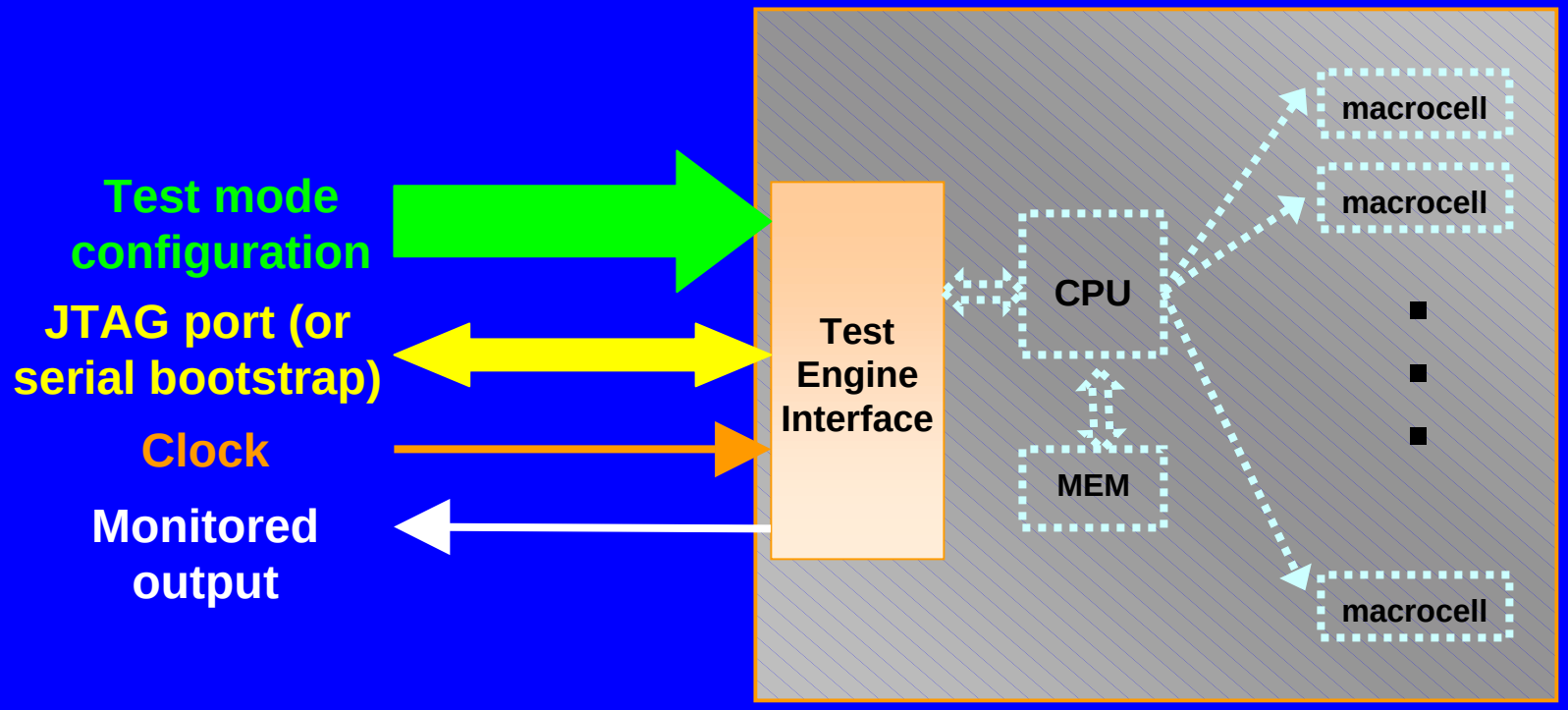


Same stress and test coverage

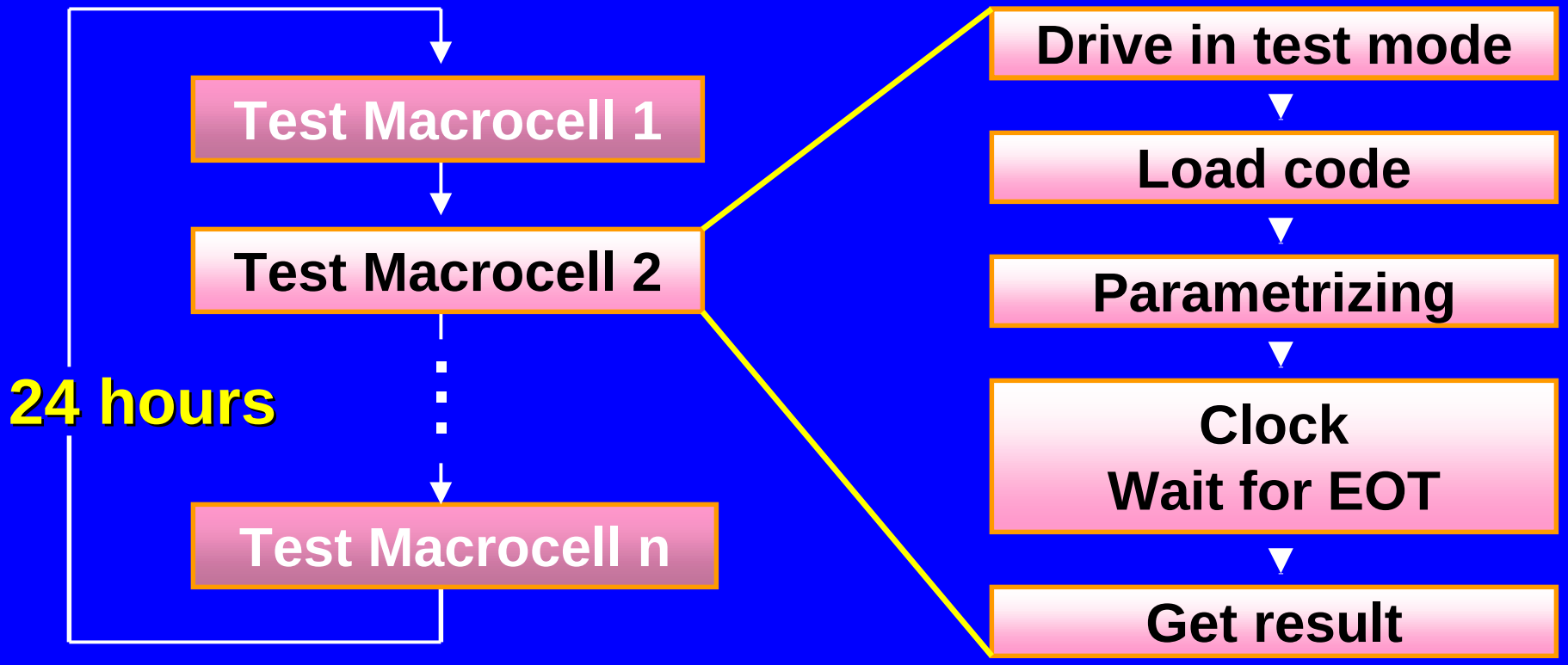
SOFT-BIST Concept



Test Engine Interface



Test Execution



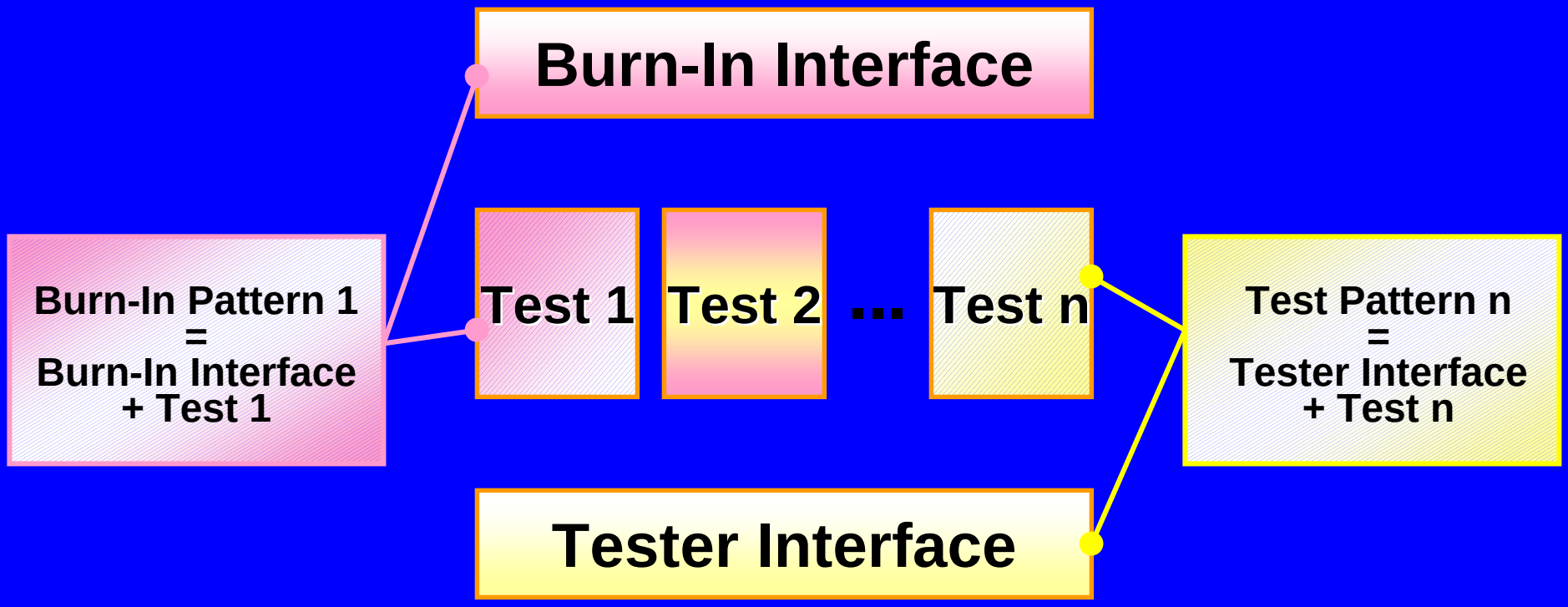
…or more complex sequence, in a completely programmable way

Feedback of test results to the tester
allows to modify the program's flow 'on the fly'

Code Loading

- **Short vector sequence**
  - **Only for loading and not for execution**
  - **Dramatically reduces vector memory depth** [100 test patterns 1k each ⇒ 100x1000x10 = 1M vectors, 8-32 lines]
  - **Code loading overhead typically < 0.1%**
- **Fragmented and sequenced**
  - **Because of the DUT internal memory limitation**
- **Test program is a merge of**
  - **Macrocell test**
  - **Burn-in interface**

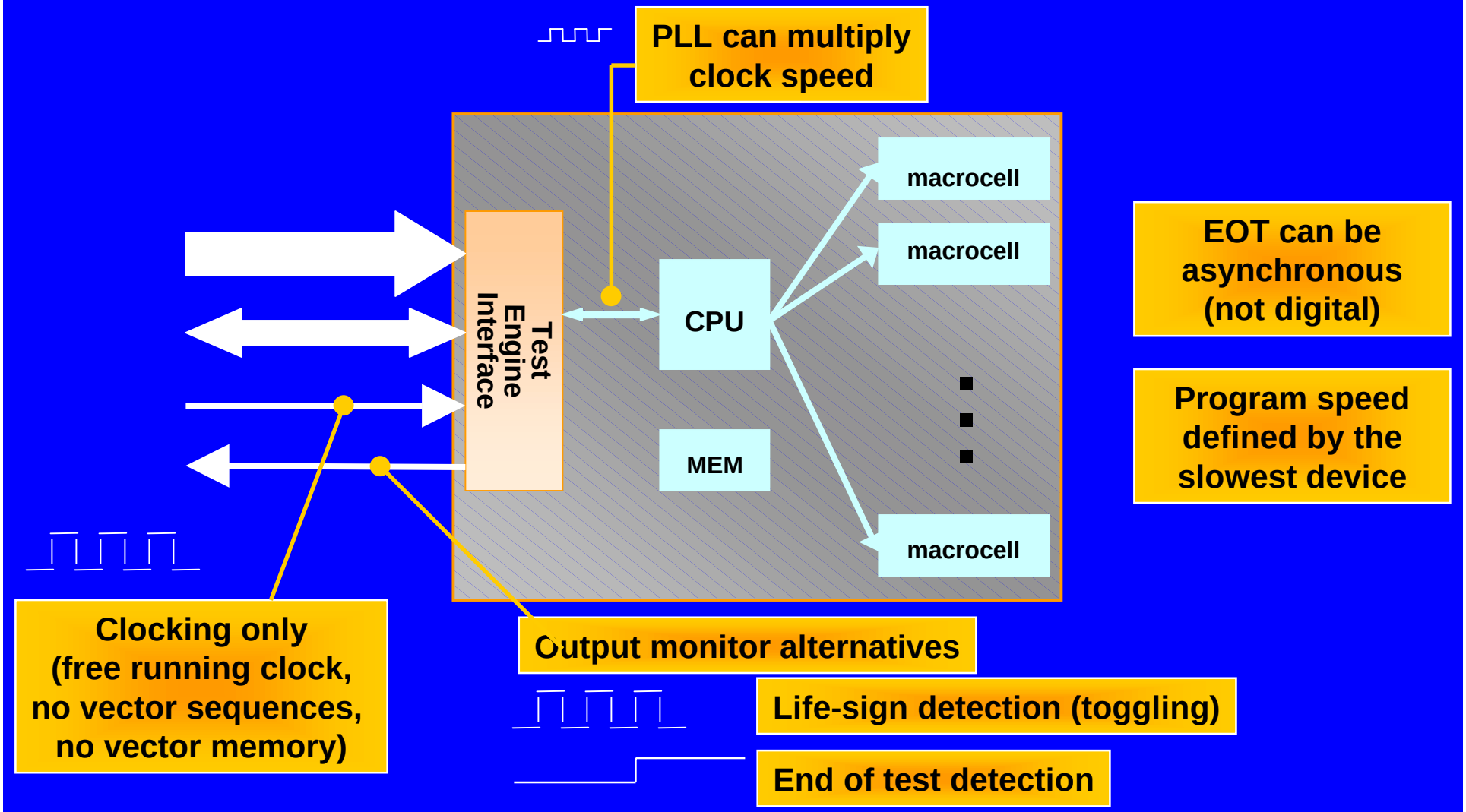
Burn-In and Test Library



Test Program Parameters

- **Test programs can be parameterized run-time**
- **Utilization**
  - Same test code in different conditions (saves memory)
  - Parameters calculated run-time
- **Example: write good or fail results in the non-volatile memory**

Test Program Execution



Acquisition of Test Results

Option 1: good/fail

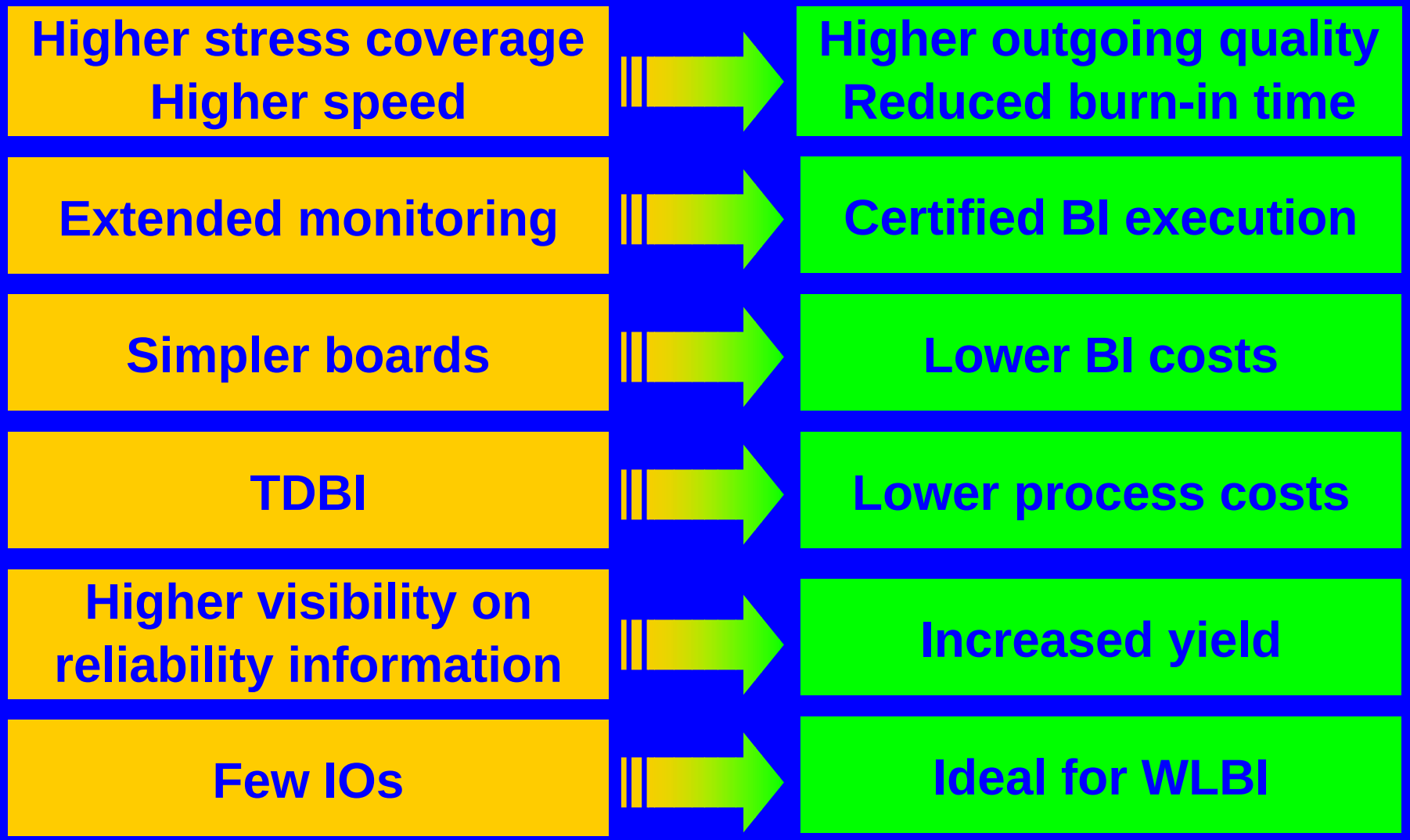
- Bin classification based on which test pattern fails

Option 2: detailed data exchange

- Bin classification based on which test program fails and what the test pattern says

- Additional information
  - how good
  - why does it fail

Benefits


Higher stress coverage
Higher speed
Higher outgoing quality
Reduced burn-in time
Extended monitoring
Certified BI execution
Simpler boards
Lower BI costs
TDBI
Lower process costs
Higher visibility on reliability information
Increased yield
Few IOs
Ideal for WLBI

Increased Engineering?

- Once methodology is set, transferring the test library in the burn-in environment is straightforward
- Hardware design and verification of signal quality require less engineering time
- Management of changes is dramatically simpler

Drawbacks

- **Limited application range**
  - CPU
  - Internal executable RAM
  - Bootstrap capability

In some cases it is convenient to design-in this kind of test engine to get the advantages of the SOFT-BIST concept

Conclusions

- **SOFT-BIST is an efficient way to test SOC, uC and other device families**
- **Advantages include:**
  - Higher stress
  - More extensive test coverage
  - Simplified hardware
  - Sharing of the test library with ATE

Acknowledgments

- Nuccio Mastrogiacomo
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