Burn-in & Test Socket Workshop

March 3-6 , 2002
Hilton Phoenix East/Mesa Hotel
Mesa, Arizona

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Burn-in & Test Socket Workshop

Technical Program

Session 3
Tuesday 3/05/02 8:00AM

Thermal Management Methods

"Thermal Modeling Of Burn-in System"

Liu Baomin - Advanced Micro Devices

"Burn-in System And Driver Board Technology Advances"

Mike Niederhofer - - Incal Technology, Inc.

Bruce Simikowski - Incal Technology, Inc.

Thermal Modelling of Burn In System

Liu Baomin

Senior Engineer, Advanced Micro Devices

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Agenda

- Background
- Objective
- Brief Introduction of CFD Thermal Simulation
- Road Map of BI system level simulation
- Model Development & Validation
- Prediction of a new design
- Hotspot and Solution
- Conclusions
- Acknowledgement

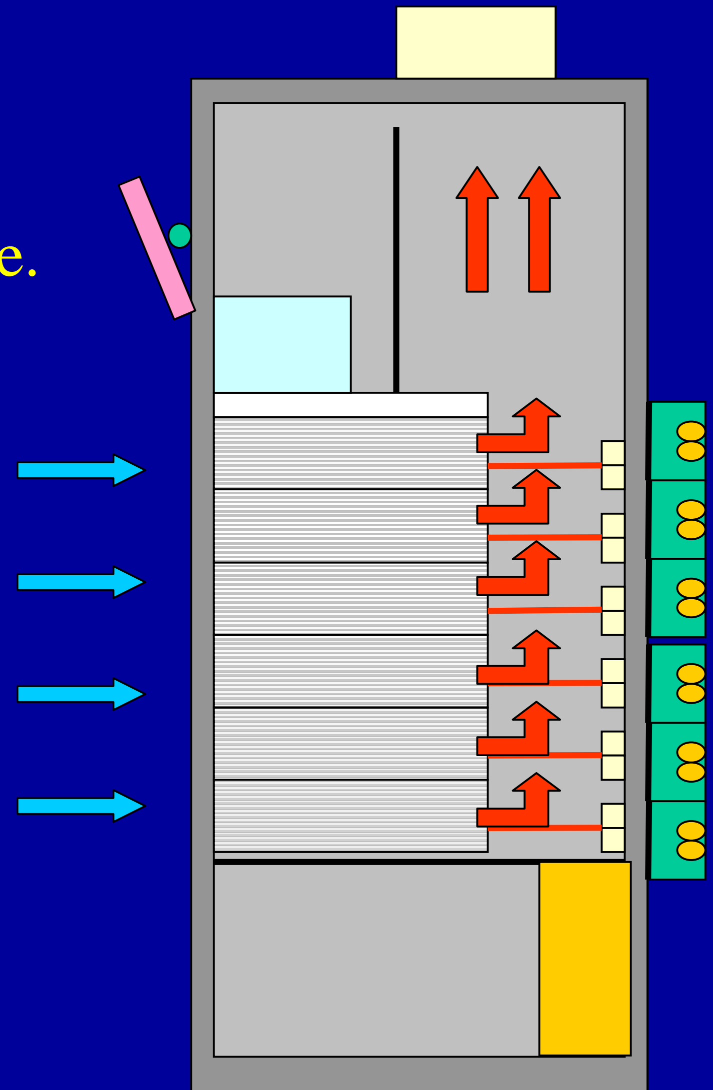
Background

BI System Features:

- To Handle Device at high power levels.
- Active thermal control of DUT temperature.
- Forced air flow to move heat out of rack.
- PSU is placed outside main rack.

Thermal Issues to be concerned:

- Large Heat Load: around 1 KW/tray.
- Passive thermal control of critical cables & components.
- New devices



Objectives

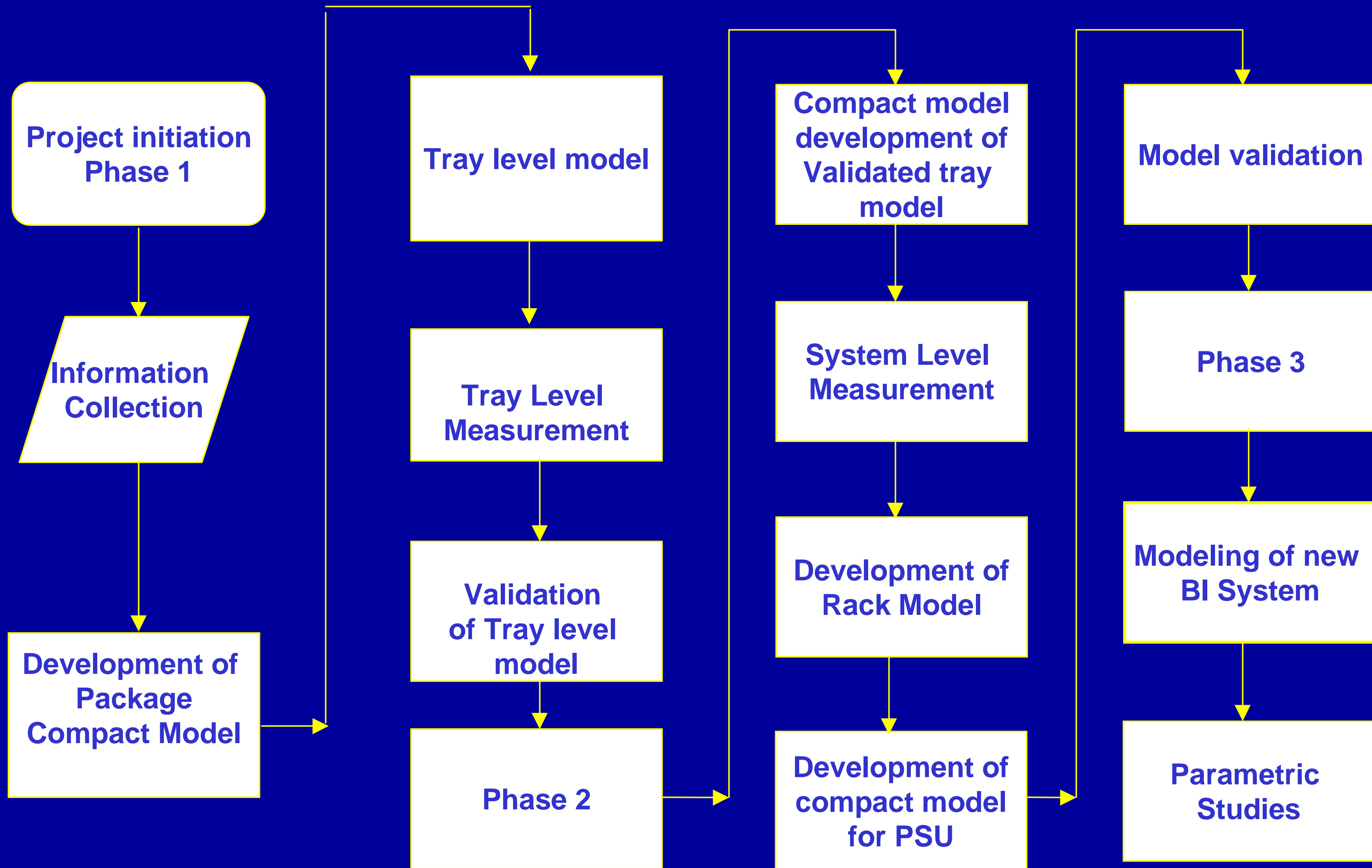
With the prediction of the thermal and air flow profiles in the BI system, the present CFD thermal simulation is to

- Verify the thermal performance of new BI system design
- Parametric studies on device power, rack flow, ambient temperature etc.
- Predict hot spots and develop the thermal solution
- Assist to develop new innovative BI systems.

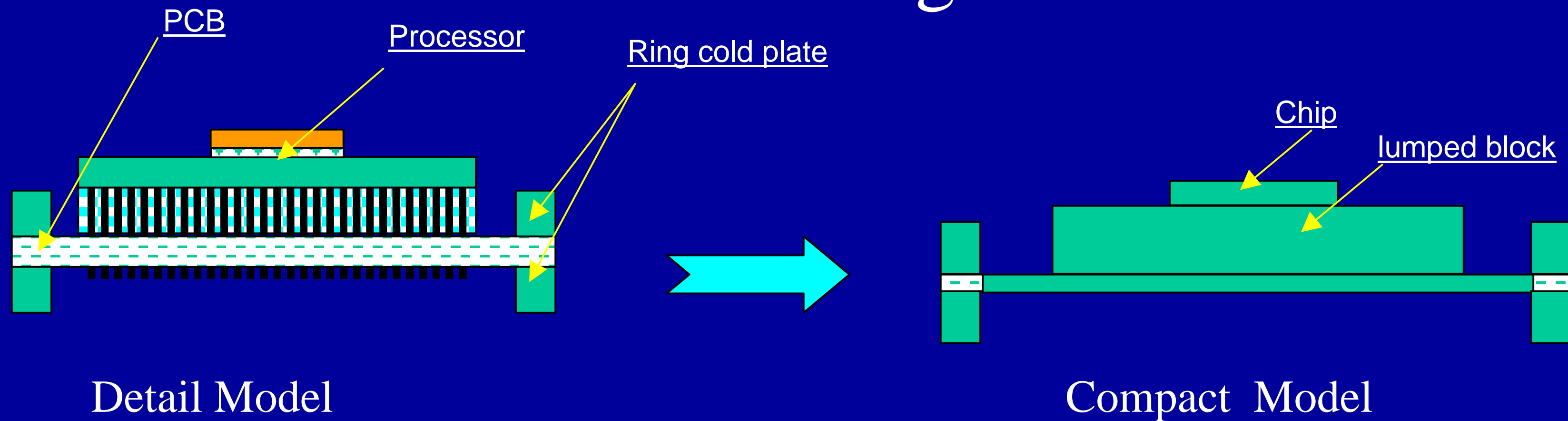
Review of CFD

- Computational Fluid Dynamics, also handle heat transfer
- Solve the governing equation sets of fluid flow & heat transfer
- Input parameters: Geometry, material properties, heat sources and flow sources (fan, pumps, etc), boundary conditions.
- Output: Velocity & temperature field
- Commercial Software for electronic system: Flotherm, Icepak, Paksi, etc.
- Flotherm V3.2 has been used in the present work.

Road Map



Detail & Compact Modeling of A CPGA Package



Power dissipation	Theta JB in detailed model °C/W	Theta JB in Compact model °C/W	% differecne w.r.t detailed model
10 watts	5.38	5.43	0.9%
40 Watts	5.6	5.48	2%

Compact model is accepted!

AMD

Detail Modeling of HBI Tray

Tray Fans

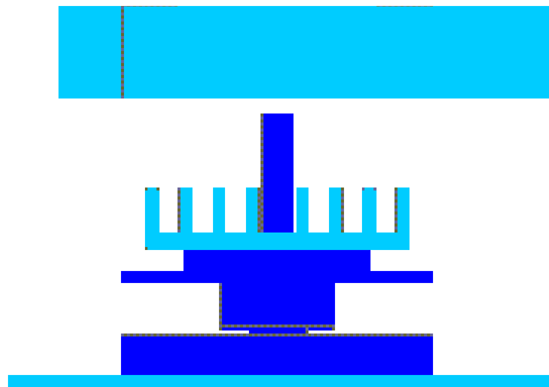
T Board

Processor heat sink

Processor

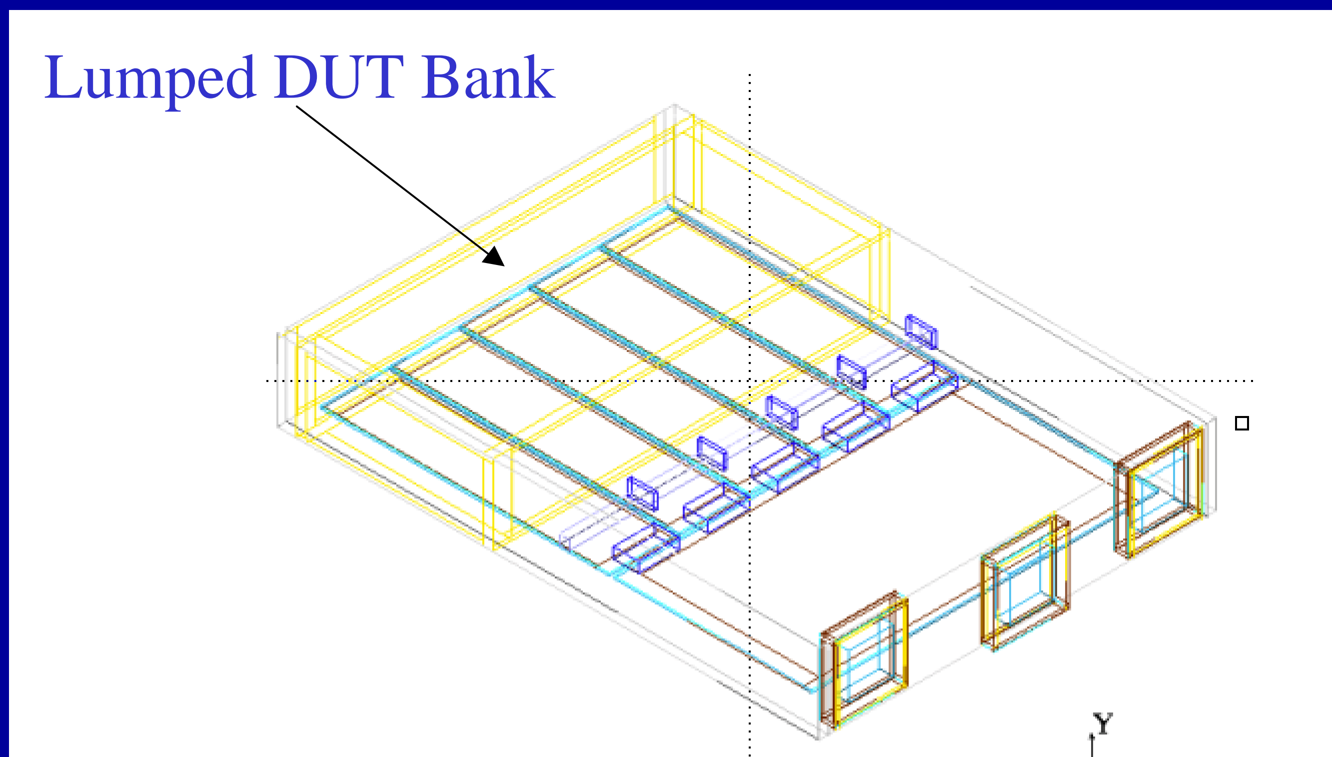
(Compact model)

Front Panel

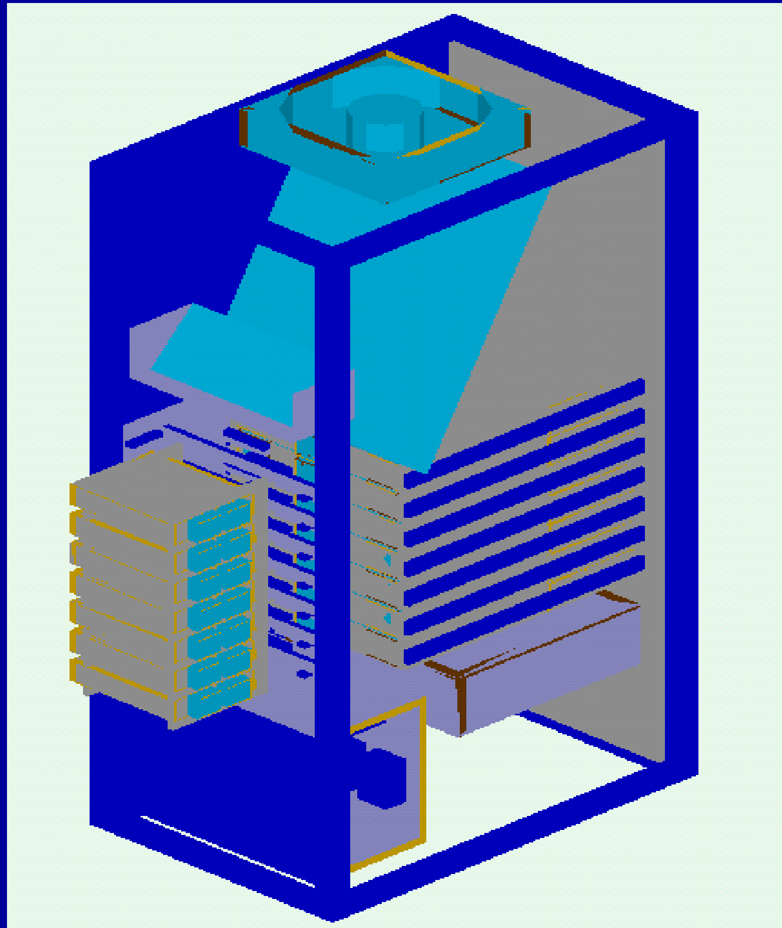


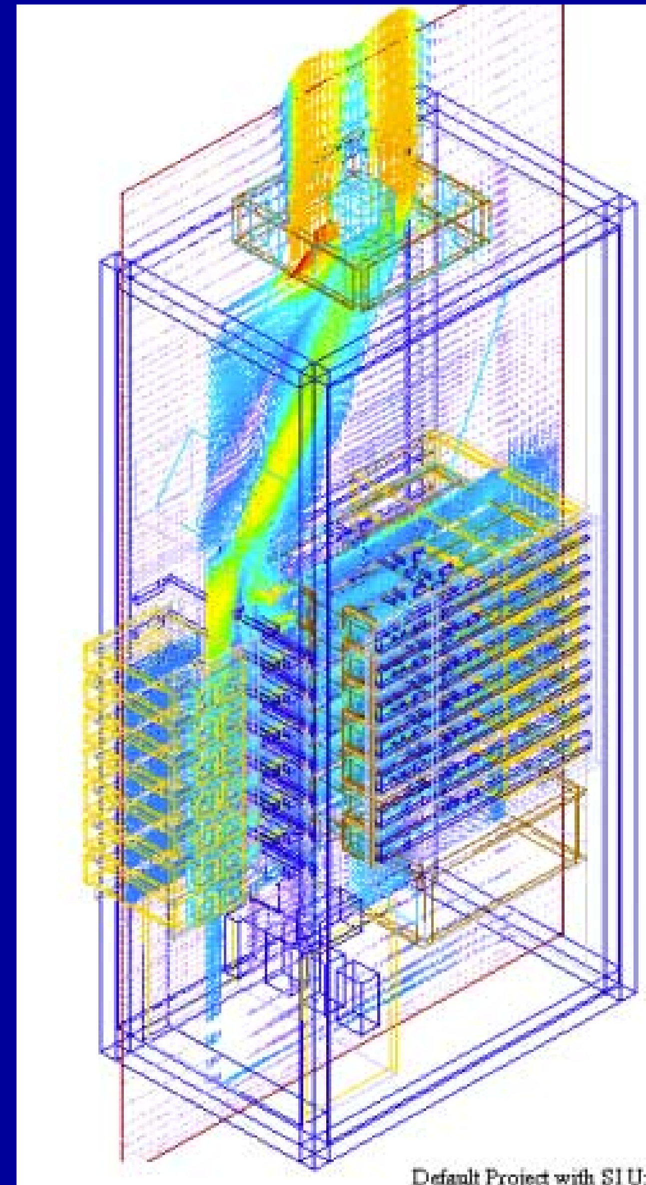
Compact Modeling of HBI Tray

- To control mesh number in each tray for system model.
- Represent detail model in air flow & temperature through tray.
- Processor, heat sink and fan assembly are lumped together.



Modeling of BI System



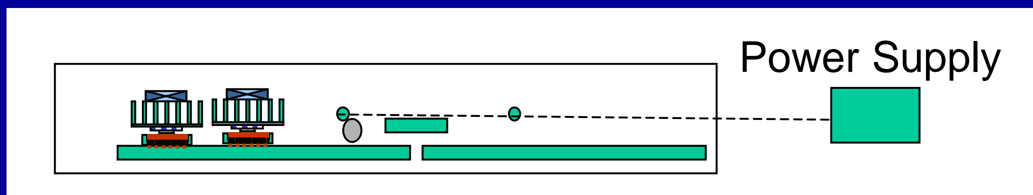


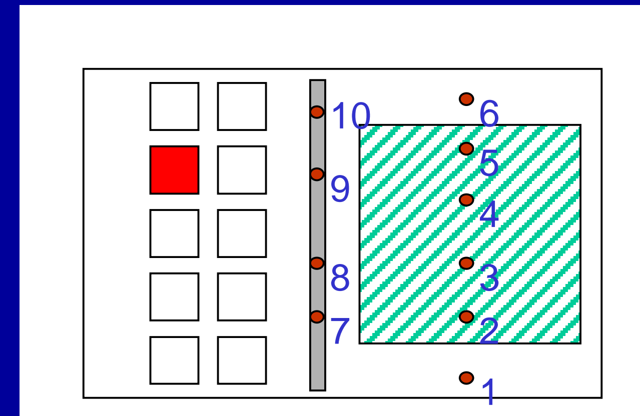
- Exhaust fan, baffle,7 compact model of trays, power supply unit (PSU),
- Power supply exhaust fan, power sequence,PC,cable extenders

AMD

Tray Level Validation

- **Power measurement** of TEC, DUT, Fans, & PCB.
- **Air Temperature measurement** at 10 locations.





Position	Simulation Results with inlet air temperature = 25°C	Extrapolated results for inlet air temperature = 20.8°C	Measured air temperature with inlet air temperature = 20.8°C	% deviation w.r.t measured air temperature
P1	38.2	34	29	17.2%
P2	45.2	41	32.4	26.5%
P3	42.1	37.9	31.7	19.5%
P4	38.3	34.1	32	6.5%
P5	42.4	38.2	33.4	14.3%
P6	37	32.8	32.3	1.5%
P7	30.9	26.7	27.4	2.5%
P8	28.9	24.7	28.3	12.7%
P9	29.1	24.9	27.4	9.1%
P10	29.6	25.4	27.3	6.9%

At most positions, the deviation is less than 15%.

Tray model is accepted.

Rack Level Validation with CPGA Package

- **Power rates** into rack, 7 PSU, PC, and 7 trays
- **Air temperature** at 20 critical locations.
- **Measured 7 times** under different conditions

At all positions, the deviation is less than 12%.

Locations	Thermal Couples	Measurement, °C	Simulation, °C	Difference, %
Air guide Left	**TC1, TC2**	**26.9**	**27.1**	**0.7**
Air guide Right	**TC3, TC4**	**27.5**	**27.1**	**-1.5**
Above sequencer	**TC5**	**25.3**	**24.2**	**-4.3**
Below baffle	TC6	27.6	27.8	**0.7**
Tray 7 Exit	TC7	26.4	24.8	**-6.1**
Tray 4 Exit	TC8	28.6	27.0	**-5.6**
Tray 1 Exit	TC9	26.4	27.6	**4.5**
Tray 1 inlet	TC10	22.1	-	**Ambient Temp**
Tray 3 inlet	TC11	21.8	-	**Ambient Temp**
Tray 6 inlet	TC12	22.1	-	**Ambient Temp**
Tray 1 Temp	TC13	27.9	26.9	**-3.6**
Tray 2 Temp	TC14	28.7	27.9	**-2.8**
Tray 3 Temp	TC15	28.4	28.0	**-1.4**
Tray 4 Temp	TC16	25.6	28.6	**11.7**
Tray 5 Temp	TC17	28.7	29.3	**2.1**
Tray 6 Temp	TC18	28.2	28.6	**1.4**
Tray 7 Temp	TC19	22.9	23.6	**3.1**
Rack side	TC20	22.7	-	Ambient

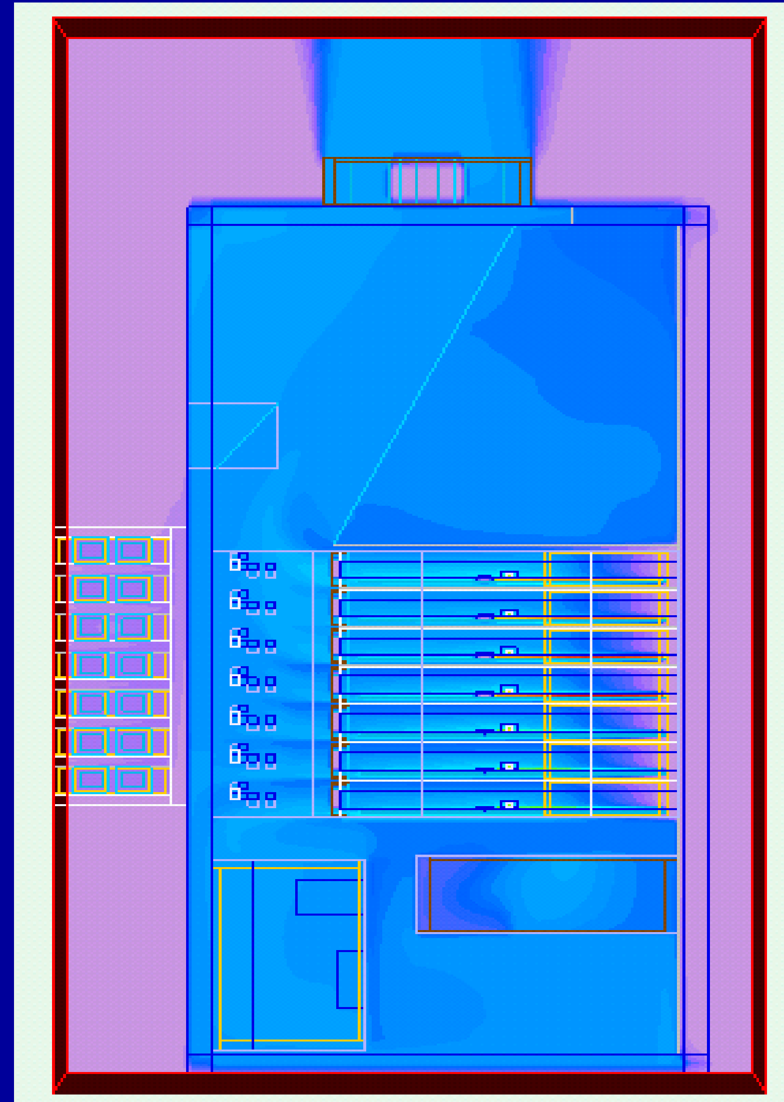
Rack Level Validation by Electric Heaters

Condition

- Ambient Temperature – 30 Deg C
- Exhaust Fan Speed - 1300cfm
- Thermal Load per tray – 1200watts
- Number of Trays per rack - 7

Result

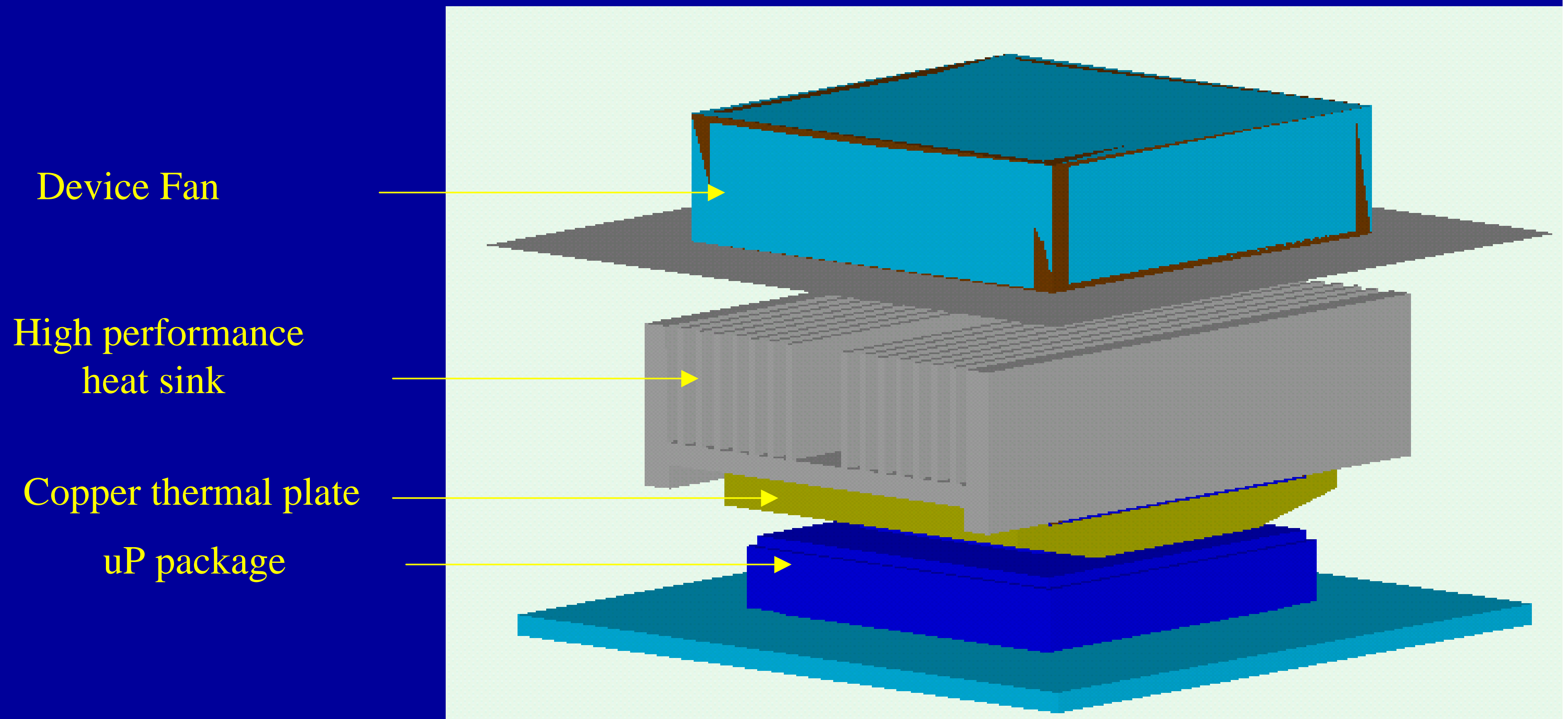
Tray Numbering	Measurement	Simulation	Diff %
Tray 1	54.3	51.1	6.24%
Tray 2	48.5	47.1	3.04%
Tray 3	45.5	48.1	-5.34%
Tray 4	48.0	49.3	-2.57%
Tray 5	43.9	49.6	-11.40%
Tray 6	47.3	51.6	-8.25%
Tray 7	46.6	50.5	-7.70%



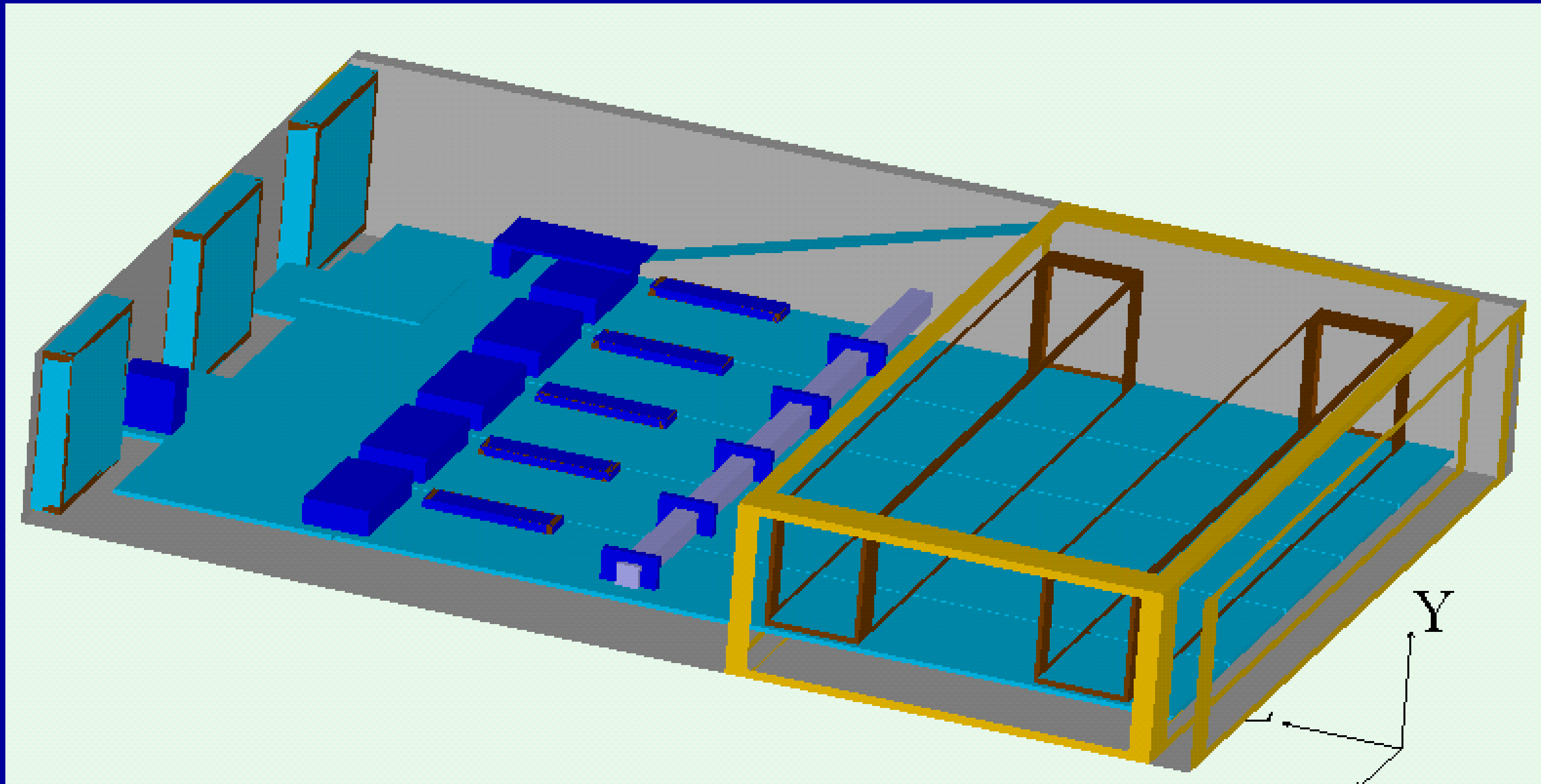
Simulation agrees with measurement at difference less than 12%.

Rack level model is accepted!

Application to New BI Design: DUT Unit

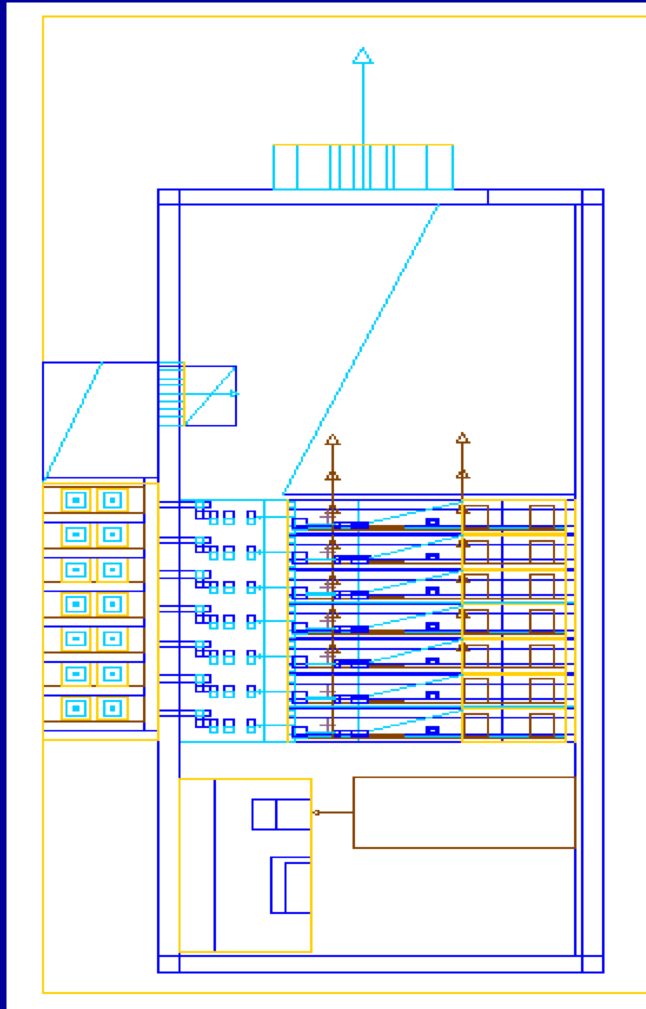


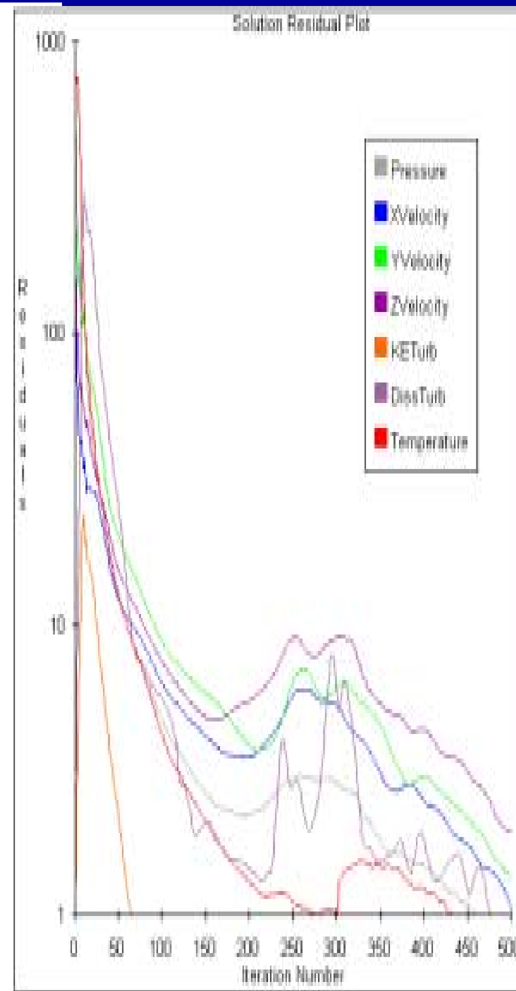
Modeling of New BI Tray

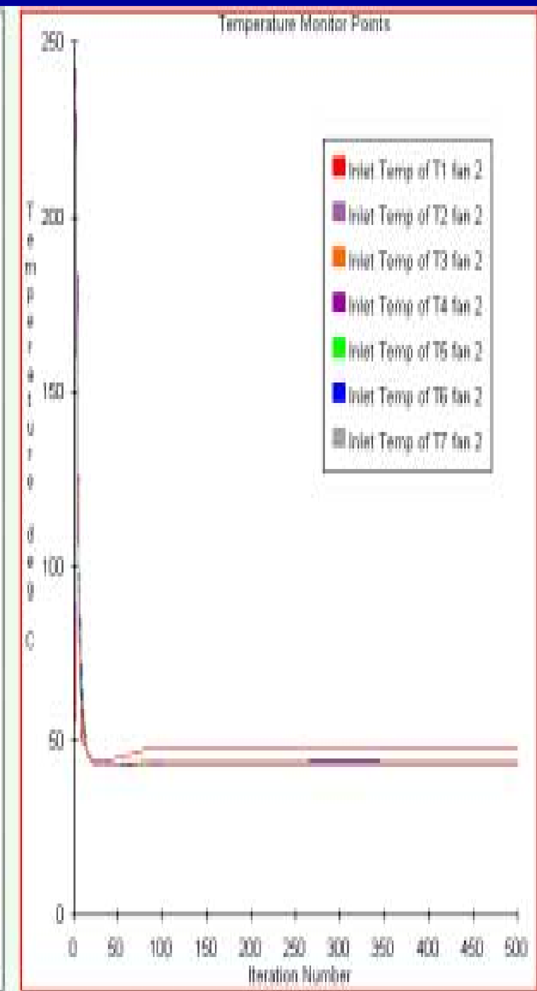


- PCBs: V board, F-Board, S-board & T board.
- Components: Voltage Regulator Modules (VRMs), Convert block
- 3 Tray Fans, Cable & its connector

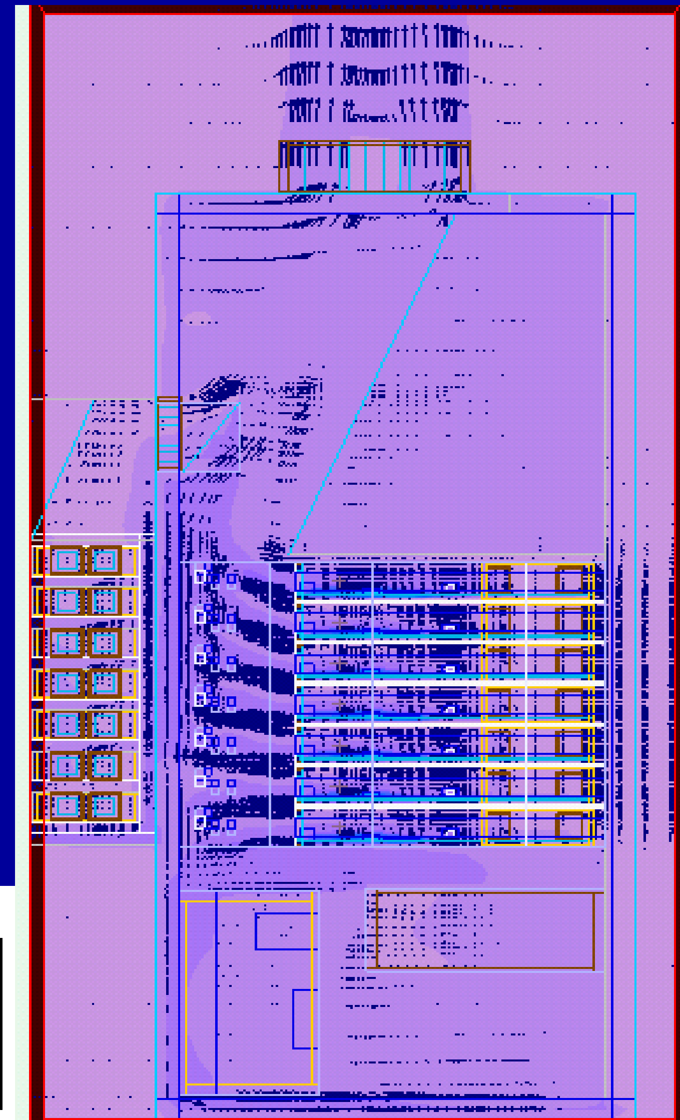
Modeling of New BI Rack







Typical Flow & Thermal Distributions



Design conditions:

uP = 45W; TEC=30W

VRM = 15.6W

Totally, 1.25KW/tray, 11.65W/rack.

Ambient: 25'C

Rack Fan: 1392 CFM

Predictions:

Tray Temperature, 'C:						
Tray 7	Tray 6	Tray 5	Tray 4	Tray 3	Tray 2	Tray 1
44.7	44.6	44.5	44.3	43.9	43.6	48.0

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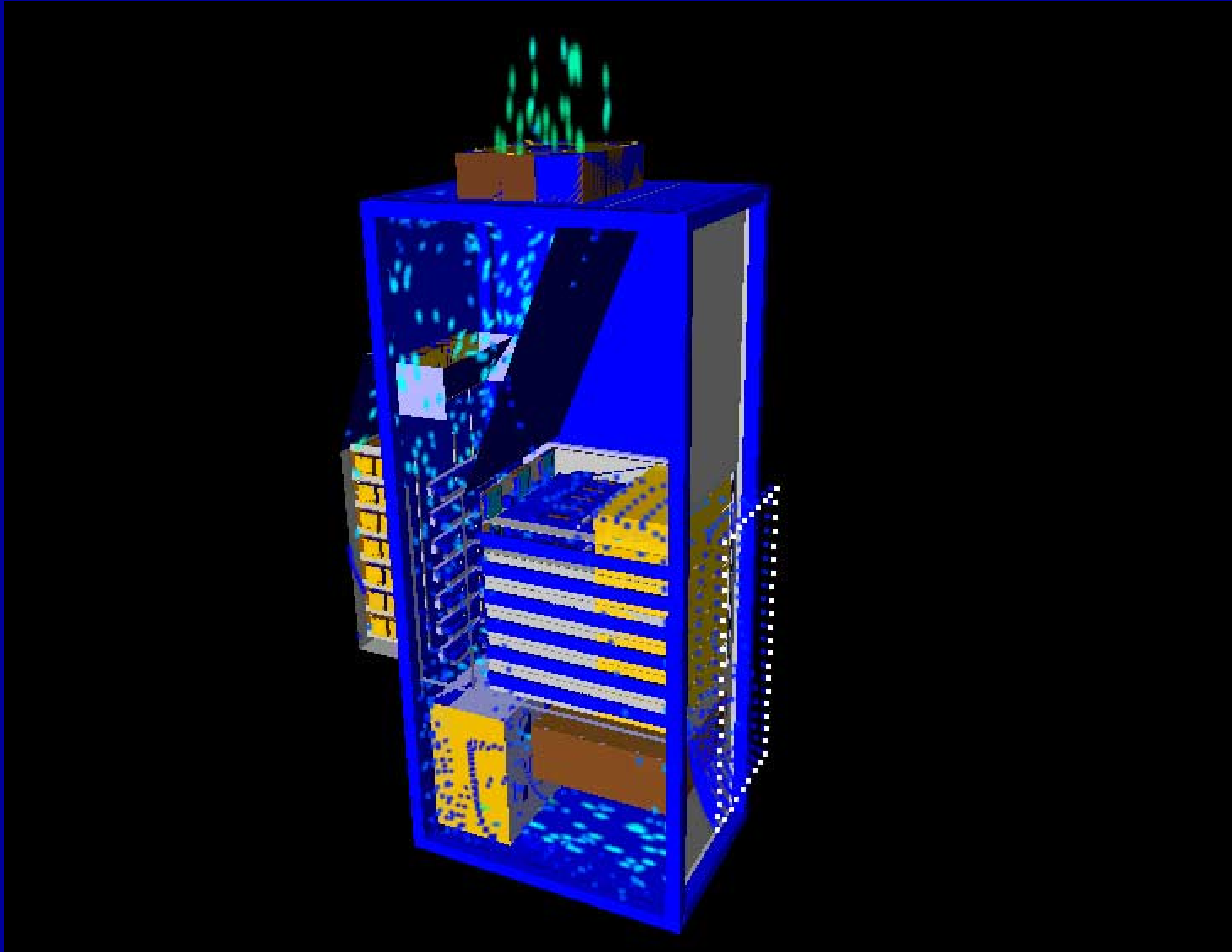
Animation of Air Flow in BI Rack



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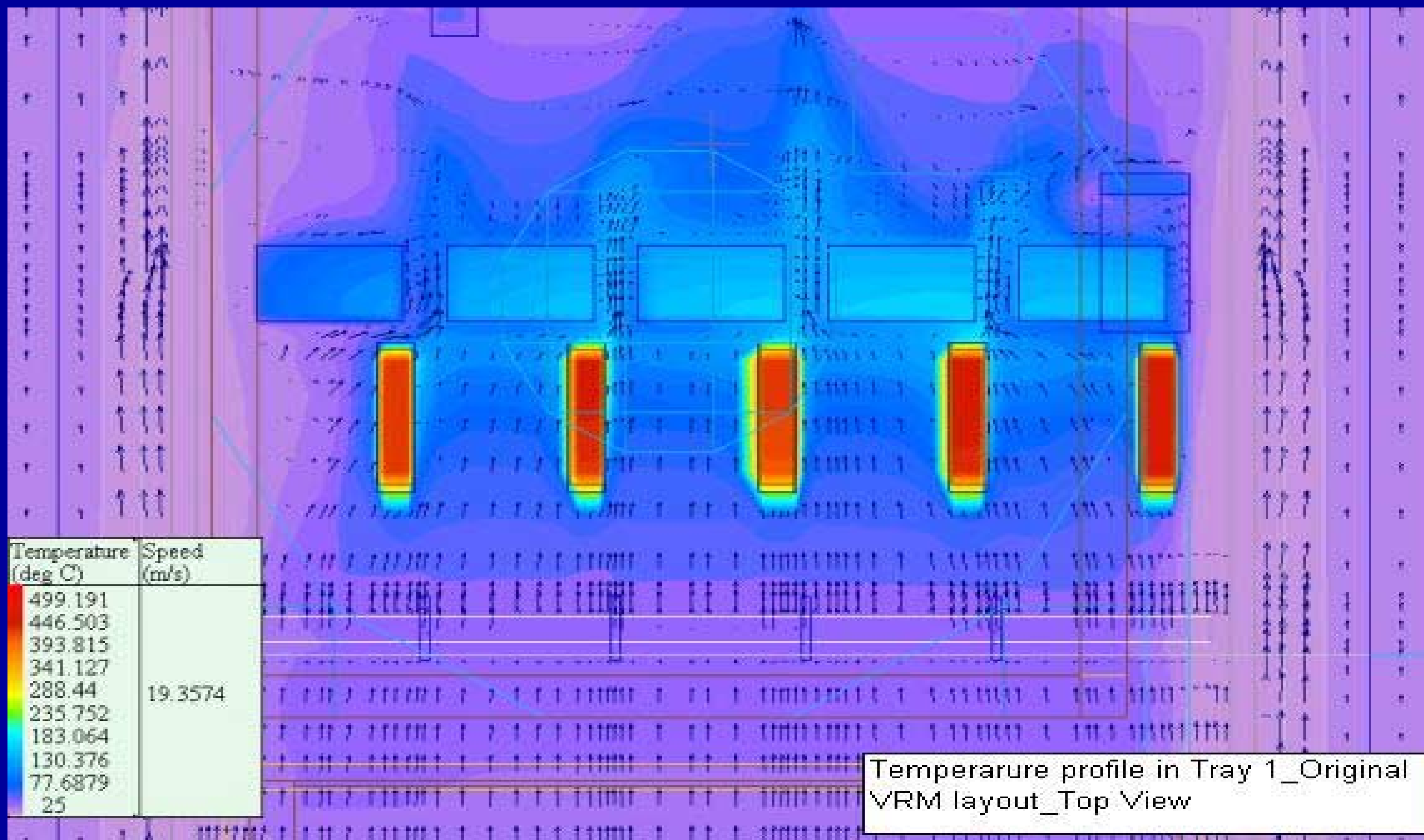
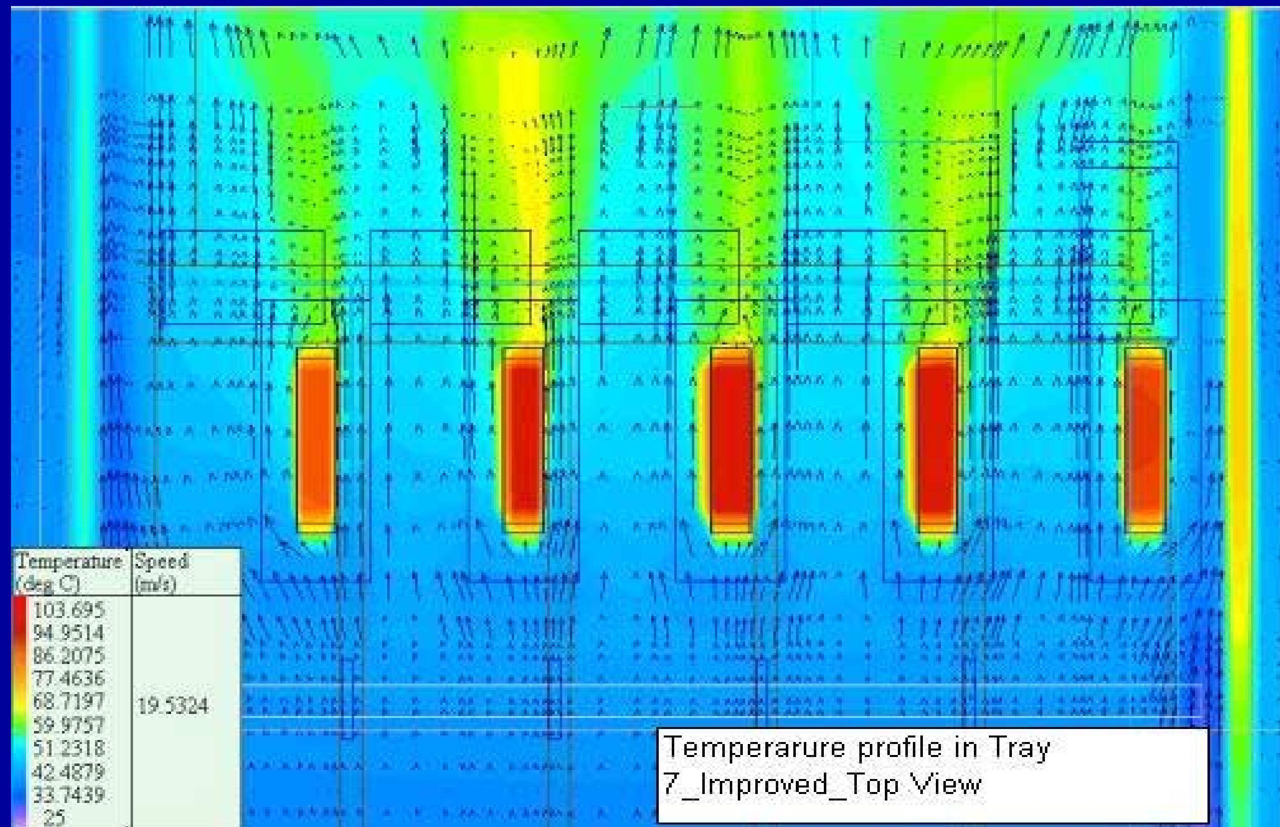
Hot Spots in the Present Design



Tray 1	VRM1	VRM2	VRM3	VRM4	VRM5
Temp, 'C	458	468	448	474	498

VRMs are at about 500’C, Hot spots in the rack!

Thermal Solution to Hot Spots by Heat Bridge



Tray 7	VRM1	VRM2	VRM3	VRM4	VRM5
Temp, 'C	94	101	103	103	96

Tray Temperature, 'C:						
Tray 7	Tray 6	Tray 5	Tray 4	Tray 3	Tray 2	Tray 1
43.7	43.8	43.7	43.6	43.2	43.0	45.4

Achievement: VRM Temp < 150'C, Tray Temp reduced by about 1'C.

Conclusions

- Thermal simulation methodology for BI system have been developed with validations.
- New BI system design have been modeled and hot spots were detected on VRMs.
- Methods has been developed to solve the thermal issues.
- CFD modeling can be used to evaluate, improve the system design, and prevent the thermal issues before manufacturing and production and thus time-saving and cost-saving.

Benefits of Thermal Simulation

- Procedures to develop and validate the CFD models for complicated systems.
- Compact model development methodology for component and sub-system.
- Validation experiment at subsystem and full system level
- Experience and knowledge can be used to simulate other testing equipment and systems.

Acknowledgement

The following persons are acknowledged for their respective contributions and support to the project:

- Bay Gim Leng, Rathin Mandal, Mui Yew Cheong, Rafiq Hussain, Maung, MS, James Hayward, Raj Master, AW CK and CS Chan from AMD.
- D.Pinjala, O.K.Navas from Institute of Microelectronics (Singapore)

Support of AMD management is also appreciated.

BiTS 2002
Burn-in System
and
Driver Board
Technology Advances

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Mike Niederhofer, & Bruce Simikowski
INCAL Technology, Inc.

Burn-in System Minimum Requirements

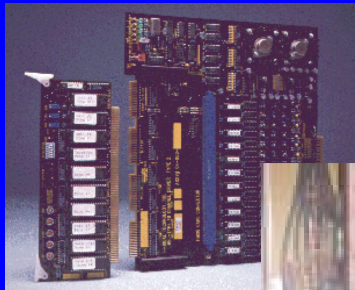
- Temperature control
- Power supply control and sequencing
- Dynamic drive signal capabilities
- Downloadable pattern file structures

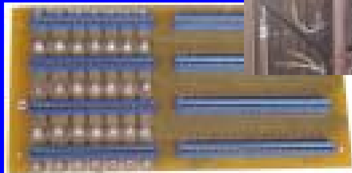
Past Burn-in system technology

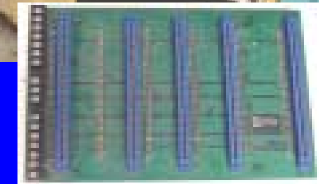
- Static Burn-in
- Dynamic drivers with binary counter or EEProm based drivers
- No output monitoring - manual operator measurement
- Manual power supply sequencing or thumb-wheel switches
- Temperature monitor via chart recorder

Early Burn-in systems

- **The OLD way**





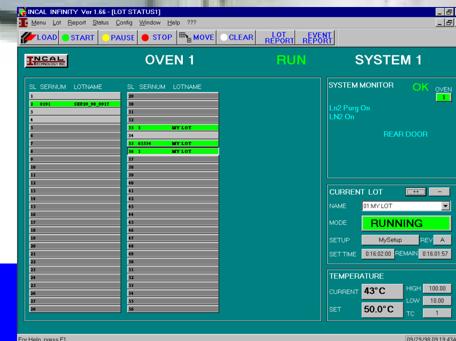


Today's customers demand

- Flexible system tooling for different board types
- Windows based op system - Windows NT
- Network access - Desktop Emulation
- Output monitoring
- Lower voltage levels - .5 volts for <.13 micron tech.
- Higher frequencies - to 33 MHz
- BIST test functions
- DUT Status, failure data analysis
- Pattern editors
- Tester vector converters

Modern Burn-in Systems

- **Computerized**
- **Low Voltages**
- **DUT Monitoring**

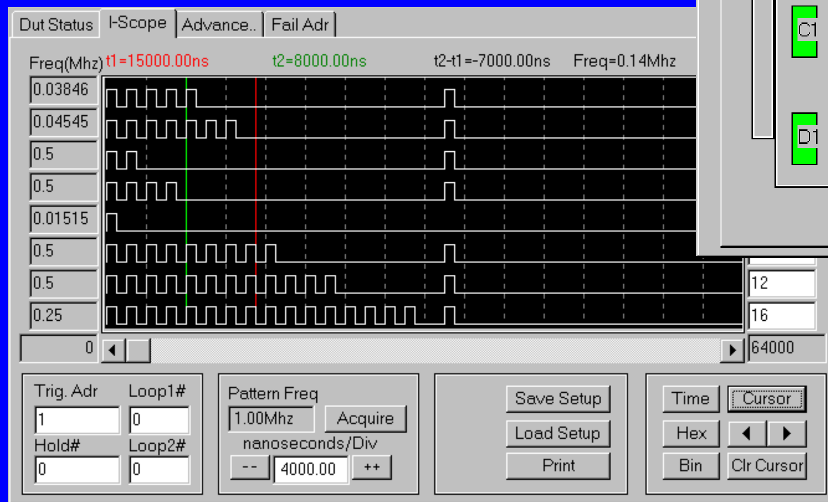


Windows Op sys

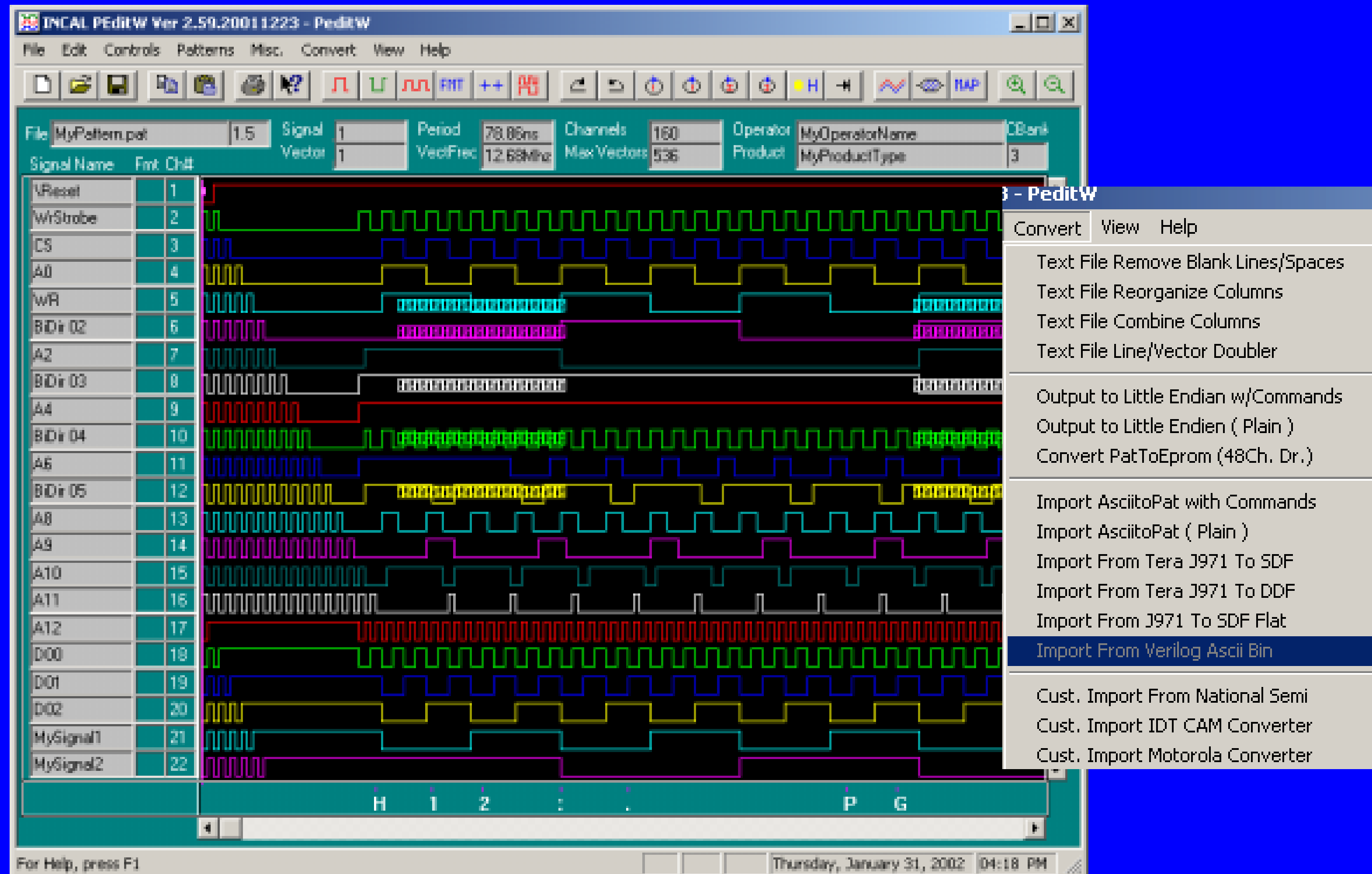
- **Vertical**
  - **or**
- **Horizontal**

Slot Information

- **DUT Mapping**
- **Waveform retrieval example**
- **Advanced fail information**



Pattern Editor Program



Tester Vector conversions

- A Difficult Challenge

PeditW

Convert View Help

Text File Remove Blank Lines/Spaces
Text File Reorganize Columns
Text File Combine Columns
Text File Line/Vector Doubler
Output to Little Endian w/Commands
Output to Little Endien (Plain)
Convert PatToEprom (48Ch. Dr.)
Import AsciitoPat with Commands
Import AsciitoPat (Plain)
Import From Tera J971 To SDF
Import From Tera J971 To DDF
Import From J971 To SDF Flat
Import From Verilog Ascii Bin
Cust. Import From National Semi
Cust. Import IDT CAM Converter
Cust. Import Motorola Converter

Enter File Format In
Number of lines befor
Number of char left of
Number of columns o
Frequency in Mhz
3 Control Banks
2 Control Banks
Little Endien (LSB to MSB)
Big Endien (MSB to LSB)
Bk4 Bk5 Bk6 Bk7 Bk8 Bk12 Bk13 Bk14 Bk15 Bk16
Cancel OK

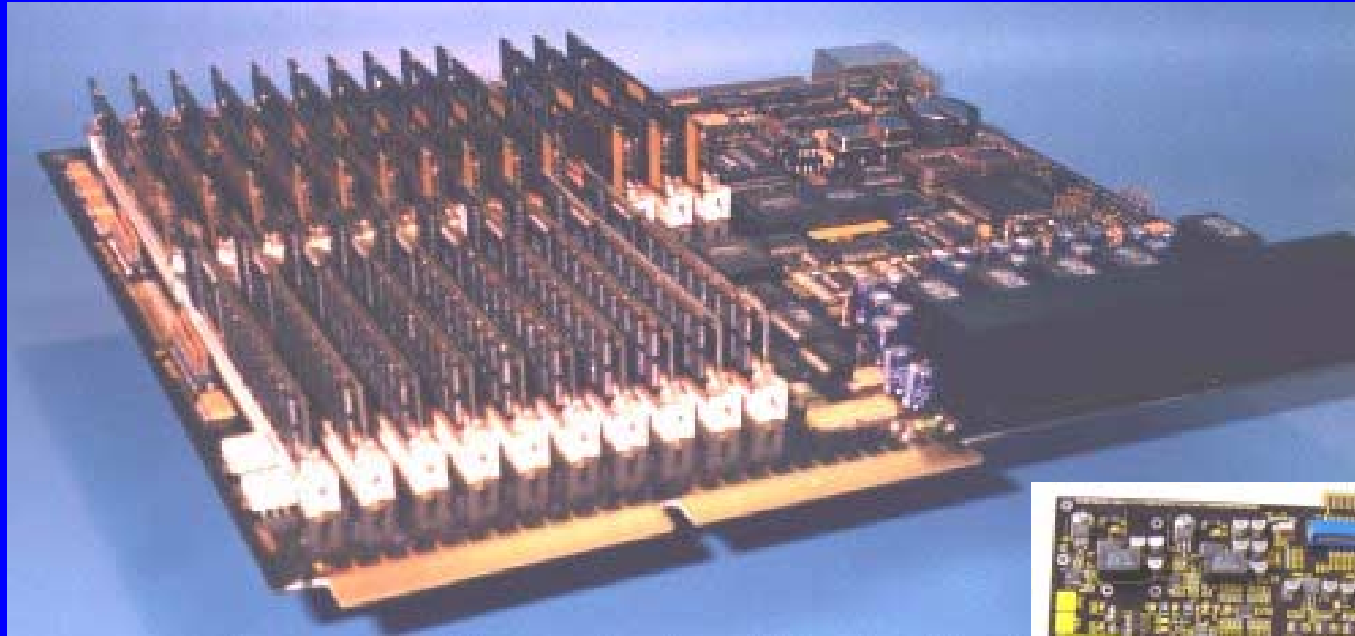
Previous Driver capabilities

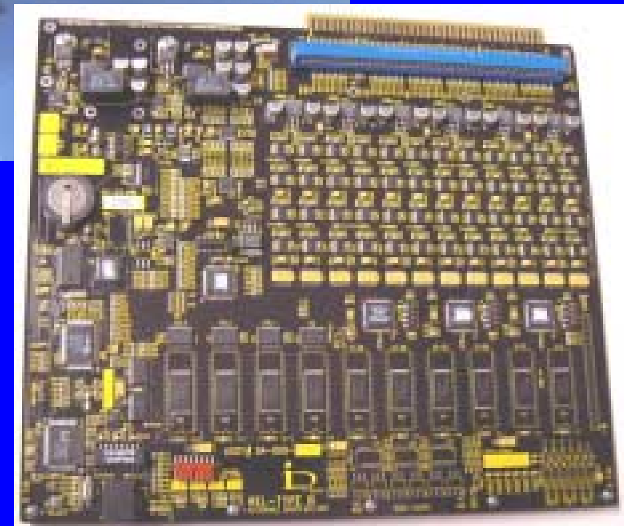
- 16 address lines / eight clocks
- Clock outputs in ranges of 5 to 10 volts
- Maximum frequency of 2 to 10 MHz
- No on-board memory. Pattern Generators configured on a zone basis.
- 96 channels maximum
- Discrete Output channels

Latest driver board technology requirements

- Computer controlled
- Tester file Compatibility
- Configurable Drive and Monitor channels
- Speeds of > 25 MHz
- Memory pattern depth 2 to 16 Meg
- Monitor of DUT outputs
- 128 to 256 channels
- Compatible to many signal types: TTL, LVTTL, LVDS, PECL, GTL, GTL+, CML

Modern Drivers



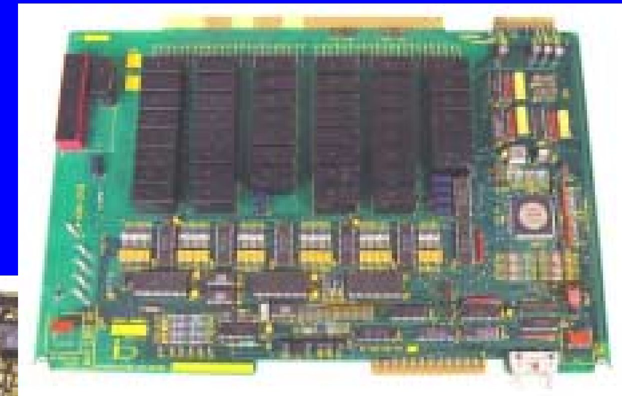
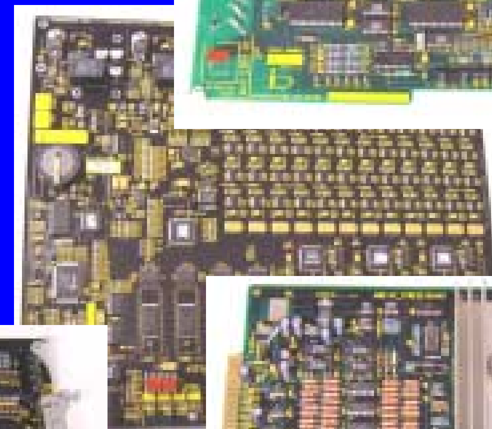


Dedicated driver boards

- Application specific or
- Industry specific
- Surface mount technology
- High production volumes
- Lower unit cost

Dedicated driver boards

- Application specific Drivers
  - HTRB/HTGS
  - HYBRID
  - Electro Migration
  - Soft-Error

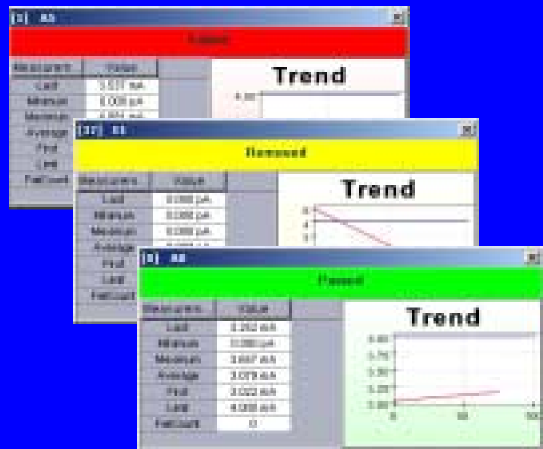



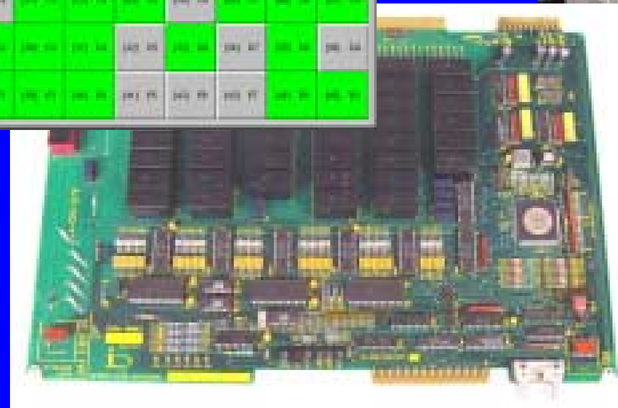
High Power System & Driver requirements

- Designed specifically for Hi-Voltage FET, IGBT, SSR testing
- High voltage capabilities
- Individual DUT power Control/Monitoring
- Automotive market
- Industrial Controls Market

Specialty B/I system specifications

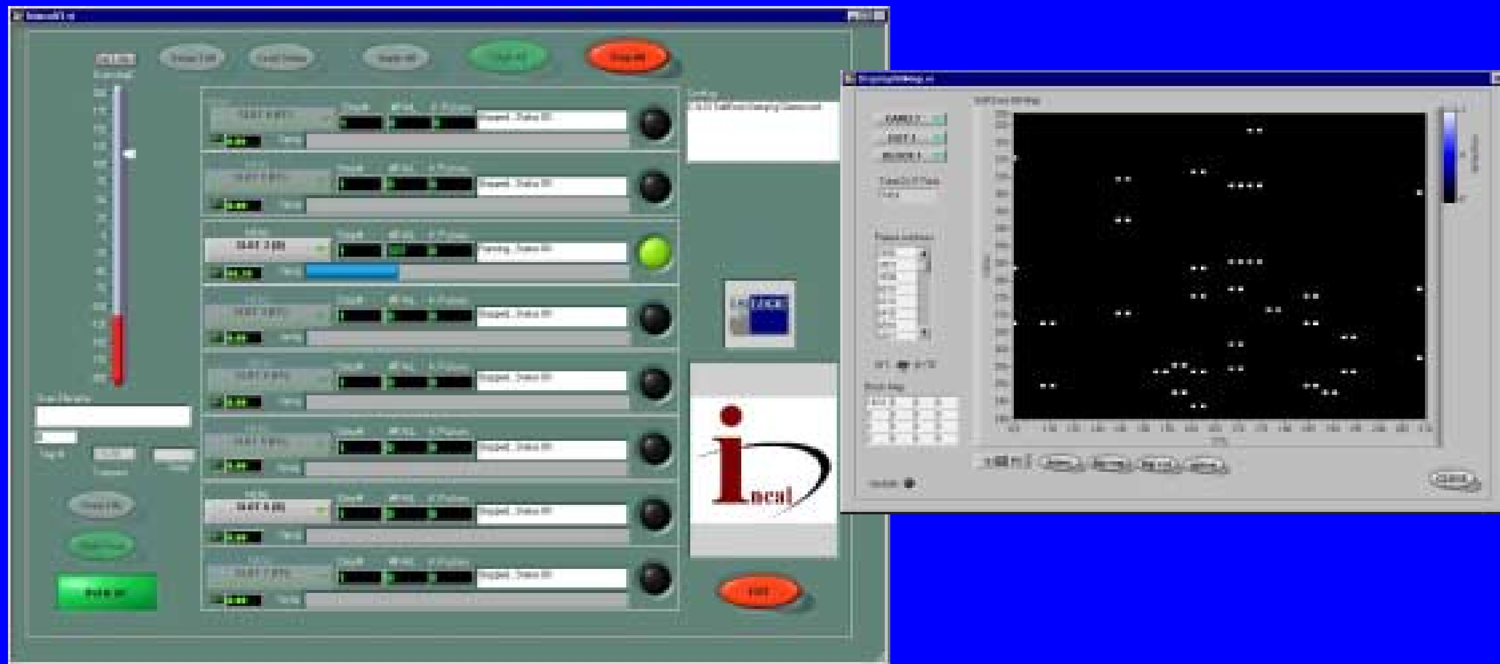
- Computer controlled
- Individual DUT monitoring





New emerging test methodologies

- Soft Error testing
- Test memory locations with neutron or proton sources present



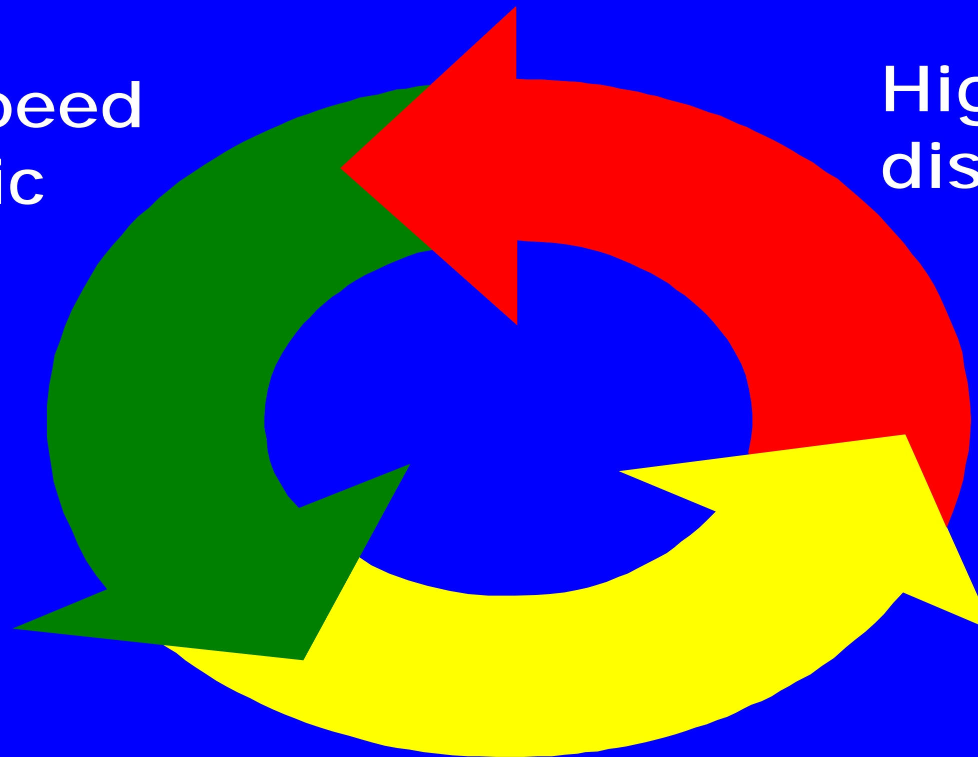
Today's Industry markets and requirements

MARKET	REQUIREMENTS
• Commercial IC market	Low cost / delivery
• Automotive market	High power
• Memory market	Speed /error detect
• Medical / Military	Custom hardware
• Test Lab market	Cost / flexibility

Today's industry demands

High speed dynamic drive

High power dissipation



Deeper pattern requirements

Specialty and Hybrid market specifications

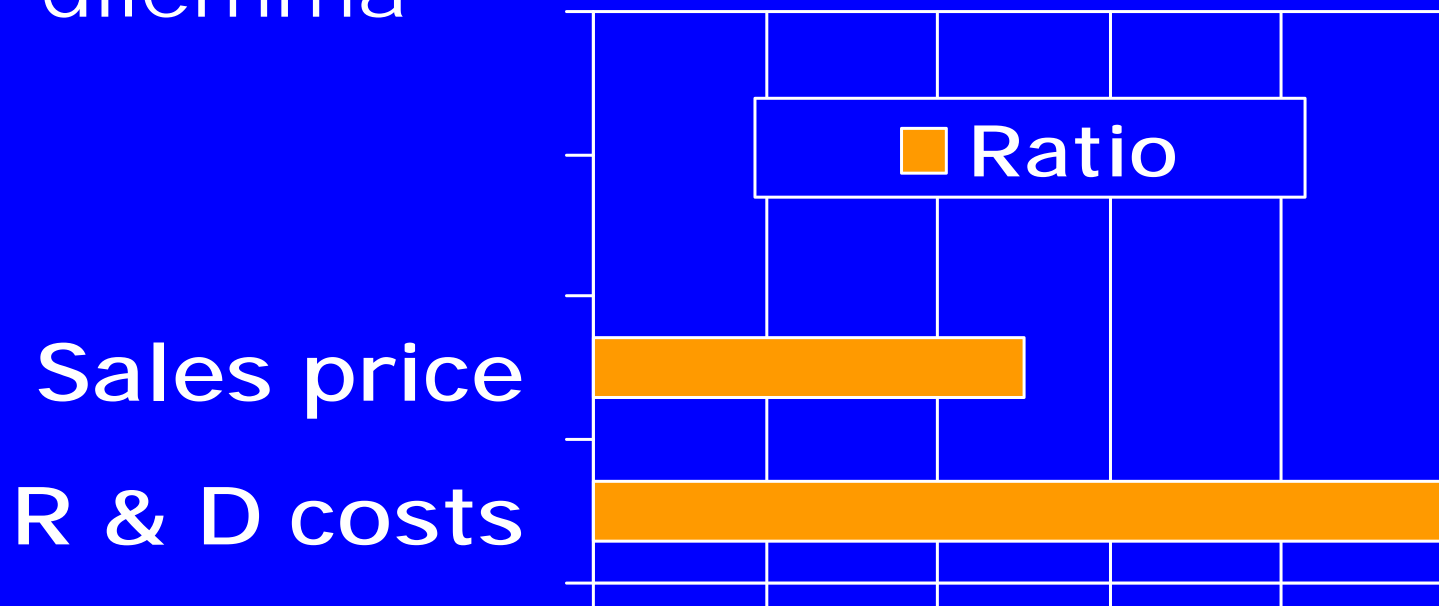
- Implantable Devices
- High Quality levels required
- Custom Hybrids and sockets
- High Voltage Power and Signals
- Monitor capabilities required

Test Lab market

- Low cost, universal hardware
- Adapter trays to utilize existing BIBS
- Flexibility
- Ease of Pattern Generation & Conversion

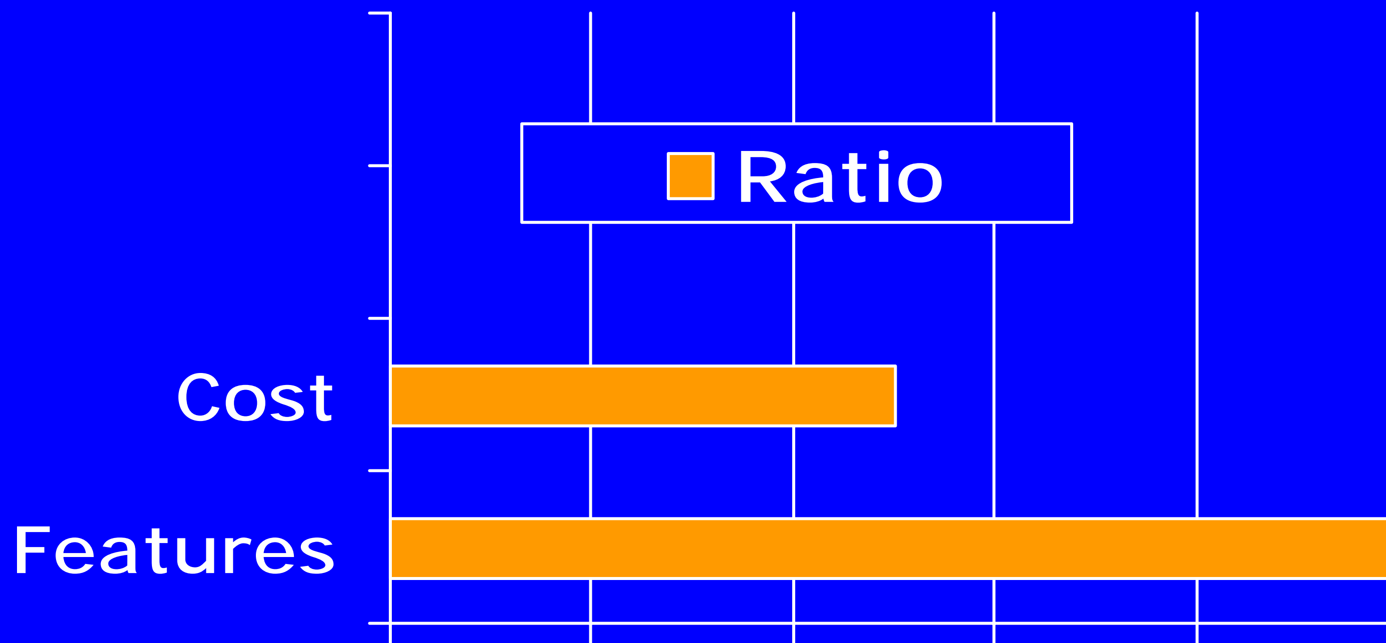
System vendor's plight

- A typical System engineering dilemma



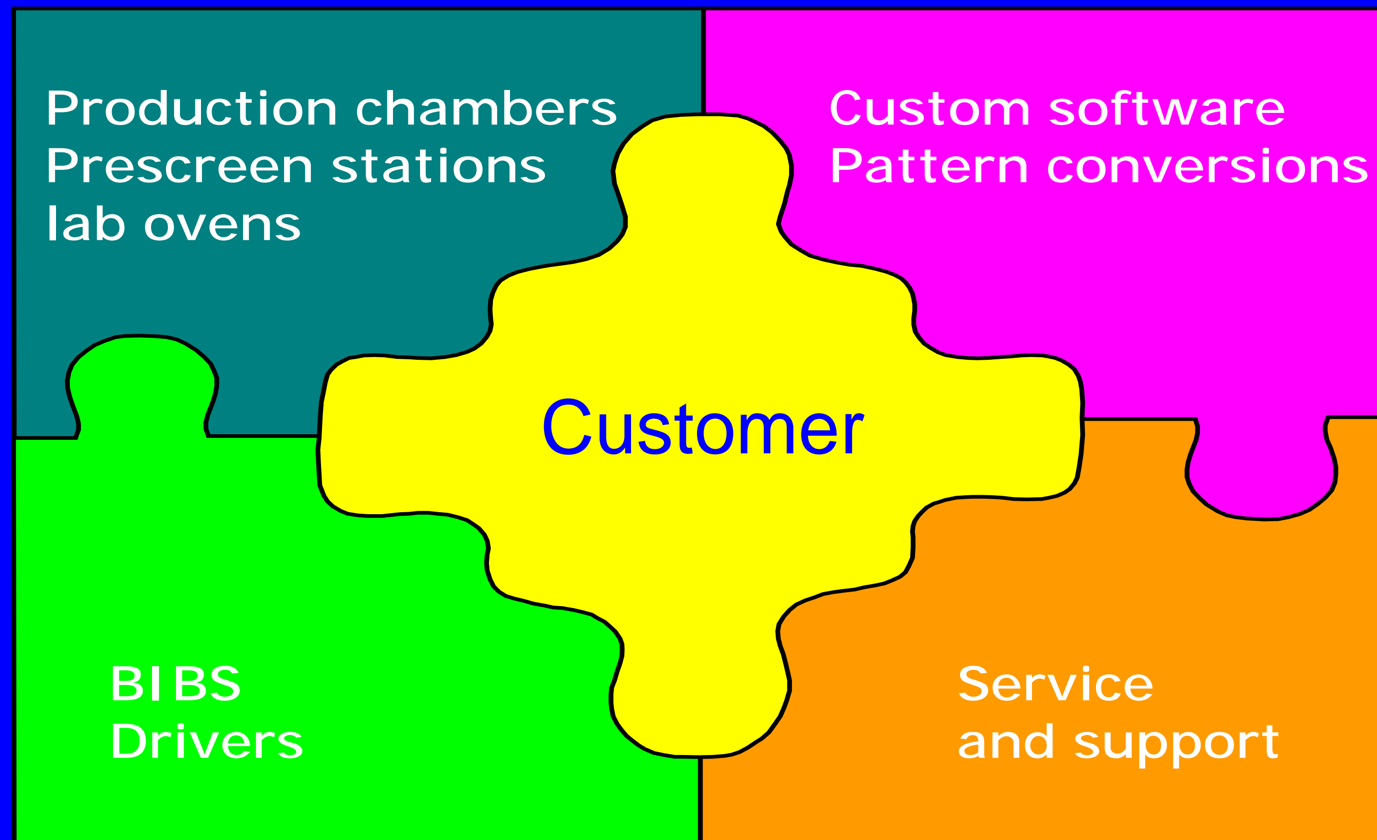
Customer's requirements

- A perfect solution for the customer



Burn-in system vendor

- One stop shopping



Conclusion

- Vendors and customers work towards common goal of improving technology while lowering costs
- Standardization of hardware
- Sharing of R & D costs
- Discuss technology advancements and technical requirements up-front
- Service multiple markets with present technology
- Industry consolidation inevitable

Conclusion

- Today we see Production systems that offer the flexibility to test and burn-in different product types and technologies for many different markets
- The cost of these Burn-in systems can approach those of high-end VLSI testers

Conclusion

- A working relationship between the system vendor and the customer at all stages of the purchase and utilization cycle will reduce R & D costs, thus lowering system costs

- NRE charges, design costs, custom hardware, and custom software ...

  WILL ALWAYS EXIST

Conclusion

- Minimizing these costs , while providing the customer cost effective technical solutions

  Is the CHALLENGE system vendors face today