

## Burn-in & Test Socket Workshop

March 3-6 , 2002 Hilton Phoenix East/Mesa Hotel Mesa, Arizona

Computer Society





# BITS

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#### **Technical Program**

Session 3 Tuesday 3/05/02 8:00AM

**Thermal Management Methods** 

"Thermal Modeling Of Burn-in System"

Liu Baomin - Advanced Micro Devices

"Burn-in System And Driver Board Technology Advances"

Mike Niederhofer - - Incal Technology, Inc. Bruce Simikowski - Incal Technology, Inc.



## Thermal Modelling of Burn In System

#### Liu Baomin

#### Senior Engineer, Advanced Micro Devices

Email: bao-min.liu@amd.com

### Agenda

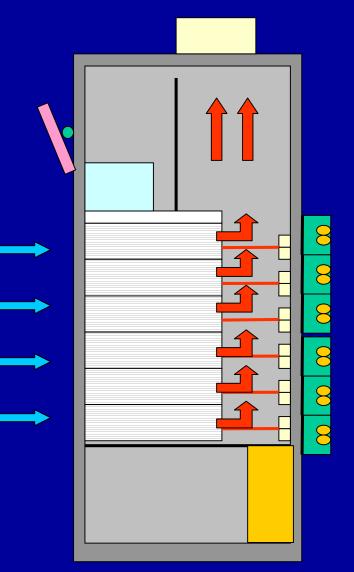
- Background
- Objective
- Brief Introduction of CFD Thermal Simulation
- Road Map of BI system level simulation
- Model Development & Validation
- Prediction of a new design
- Hotspot and Solution
- Conclusions
- Acknowledgement

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### Background

- **BI System Features:**
- To Handle Device at high power levels.
- Active thermal control of DUT temperature.
- Forced air flow to move heat out of rack.
- PSU is placed outside main rack.
- Thermal Issues to be concerned:
- Large Heat Load: around 1 KW/tray.
- Passive thermal control of critical cables & components.
- New devices





### Objectives

With the prediction of the thermal and air flow profiles in the BI system, the present CFD thermal simulation is to

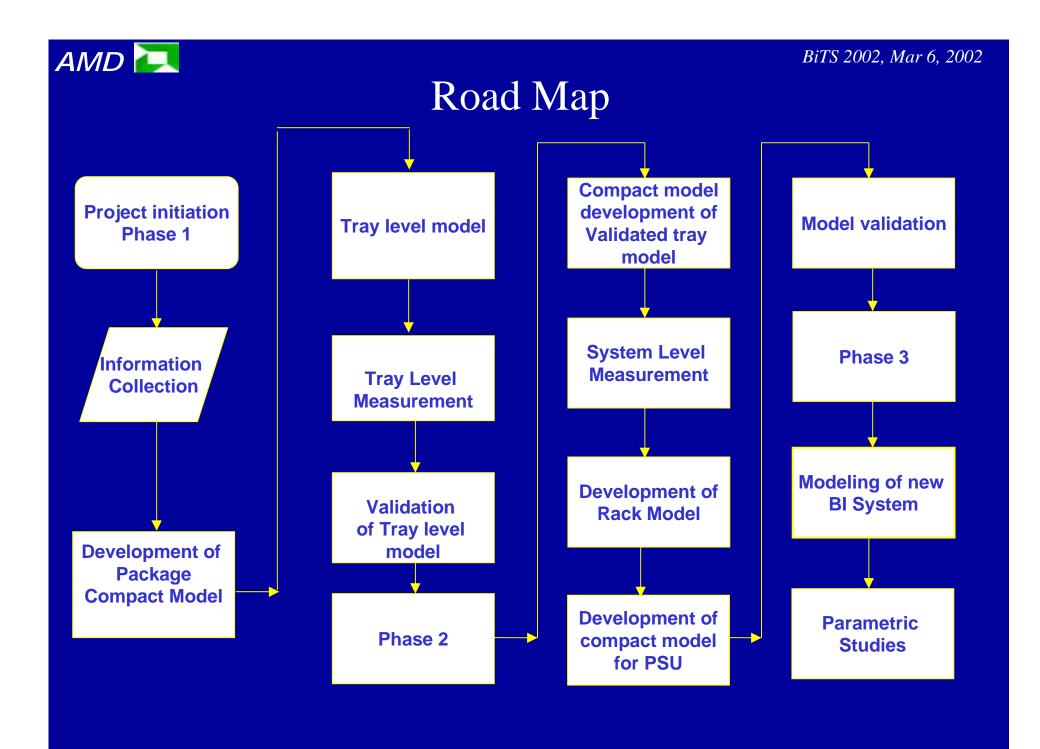
• Verify the thermal performance of new BI system design

• Parametric studies on device power, rack flow, ambient temperature etc.

- Predict hot spots and develop the thermal solution
- Assist to develop new innovative BI systems.

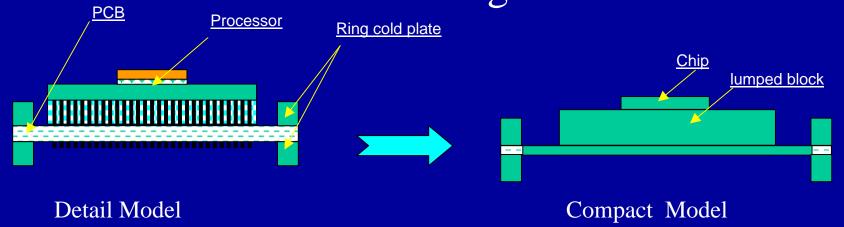
### Review of CFD

- Computational Fluid Dynamics, also handle heat transfer
- Solve the governing equation sets of fluid flow & heat transfer
- Input parameters: Geometry, material properties, heat sources and flow sources (fan, pumps, etc), boundary conditions.
- Output: Velocity & temperature field
- Commercial Software for electronic system: Flotherm, Icepak, Paksi, etc.
- Flotherm V3.2 has been used in the present work.



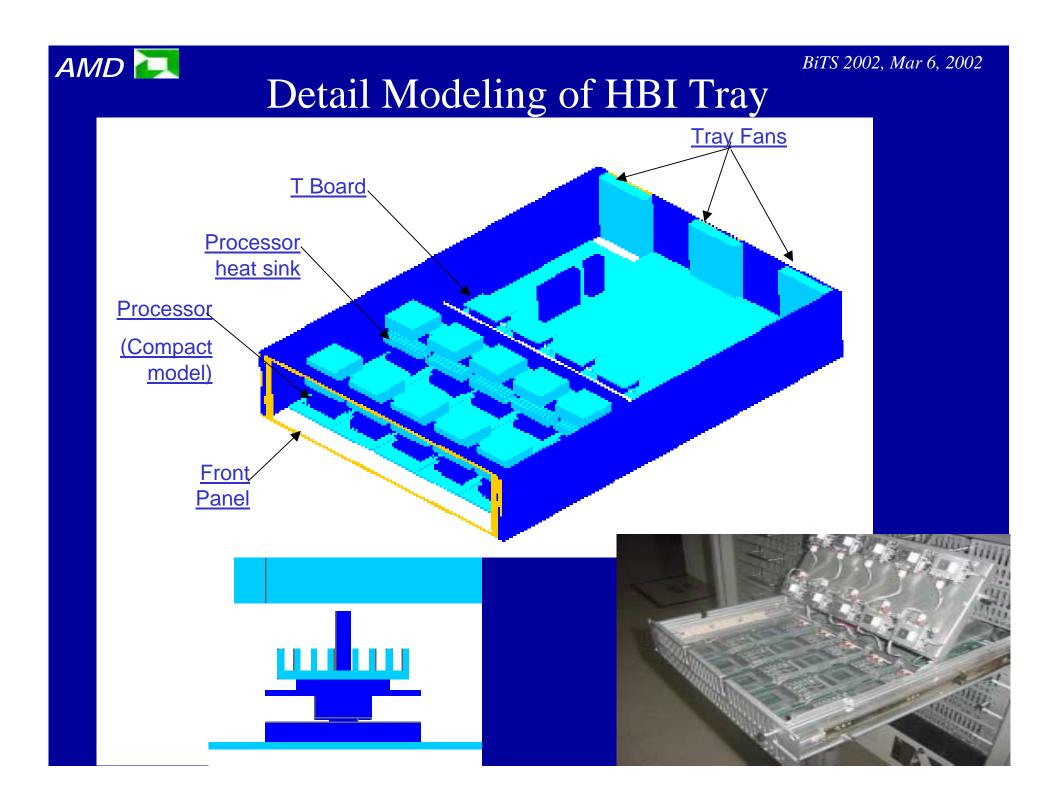


### Detail & Compact Modeling of A CPGA Package



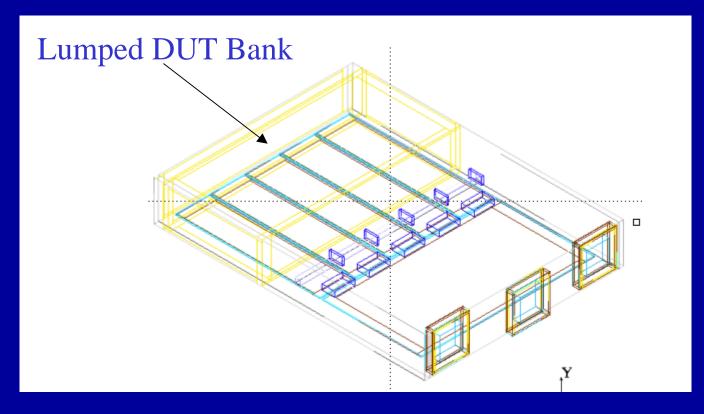
Power dissipation	Theta JB in detailed model °C/W	Theta JB in Compact model °C/W	% differecne w.r.t detailed model
10 watts	5.38	5.43	0.9%
40 Watts	5.6	5.48	2%

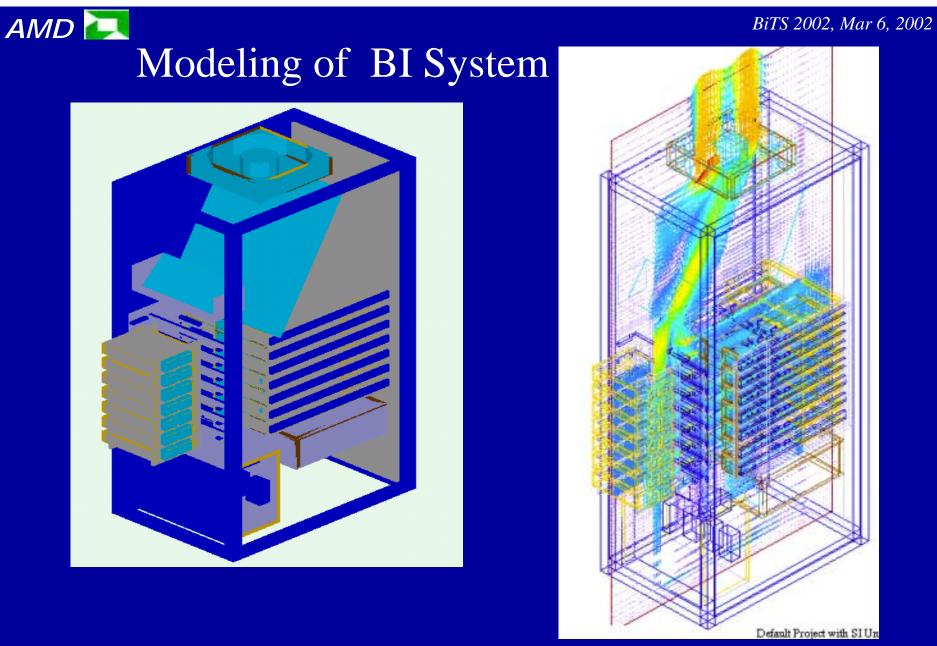
Compact model is accepted!



### Compact Modeling of HBI Tray

- To control mesh number in each tray for system model.
- Represent detail model in air flow & temperature through tray.
- Processor, heat sink and fan assembly are lumped together.





OExhaust fan, baffle,7 compact model of trays, power supply unit (PSU),

OPower supply exhaust fan, power sequence, PC, cable extenders



% deviation

w.r.t

#### Tray Level Validation

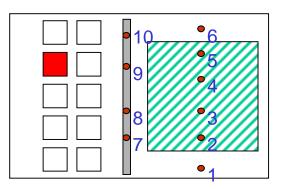
- **Power measurement** of TEC, DUT, Fans, & PCB.
- Air Temperature measurement at 10 locations.



Position

Simulation

**Results with** 



Measured

air temperature

	inlet air	inlet air	with inlet air	measured air
	temperature =	temperature =	temperature =	temperature
	25°C	20.8°C	20.8°C	
P1	38.2	34	29	17.2%
P2	45.2	41	32.4	26.5%
P3	42.1	37.9	31.7	19.5%
P4	38.3	34.1	32	6.5%
P5	42.4	38.2	33.4	14.3%
P6	37	32.8	32.3	1.5%
P7	30.9	26.7	27.4	2.5%
P8	28.9	24.7	28.3	12.7%
P9	29.1	24.9	27.4	9.1%
P10	29.6	25.4	27.3	6.9%
	P2 P3 P4 P5 P6 P7 P8 P9	temperature = 25°CP138.2P245.2P342.1P438.3P542.4P637P730.9P828.9P929.1	temperature = 25°Ctemperature = 20.8°CP138.234P245.241P342.137.9P438.334.1P542.438.2P63732.8P730.926.7P828.924.7P929.124.9	temperature = 25°Ctemperature = 20.8°Ctemperature = 20.8°CP138.23429P245.24132.4P342.137.931.7P438.334.132P542.438.233.4P63732.832.3P730.926.727.4P828.924.728.3P929.124.927.4

Extrapolated

results for

At most positions, the deviation is less than 15%.

Tray model is accepted.

#### Rack Level Validation with CPGA Package

- **Power rates** into rack, 7 PSU, PC, and 7 trays
- Air temperature at 20 critical locations.
- Measured 7 times under different conditions

At all positions, the deviation is less than 12%.

Locations	Thermal Couples	Measuremen t,	Simulati on,	Difference, %
Air guide Left	TC1, TC2	26.9 °C	27.1 <sup>°C</sup>	0.7
Air guide Right	TC3, TC4	27.5	27.1	-1.5
Above sequencer	TC5	25.3	24.2	-4.3
Below baffle	TC6	27.6	27.8	0.7
Tray 7 Exit	TC7	26.4	24.8	-6.1
Tray 4 Exit	TC8	28.6	27.0	-5.6
Tray 1 Exit	TC9	26.4	27.6	4.5
Tray 1 inlet	TC10	22.1	-	Ambient Temp
Tray 3 inlet	TC11	21.8	-	Ambient Temp
Tray 6 inlet	TC12	22.1	-	Ambient Temp
Tray 1 Temp	TC13	27.9	26.9	-3.6
Tray 2 Temp	TC14	28.7	27.9	-2.8
Tray 3 Temp	TC15	28.4	28.0	-1.4
Tray 4 Temp	TC16	25.6	28.6	11.7
Tray 5 Temp	TC17	28.7	29.3	2.1
Tray 6 Temp	TC18	28.2	28.6	1.4
Tray 7 Temp	TC19	22.9	23.6	3.1
Rack side	TC20	22.7	_	Ambient

#### Rack Level Validation by Electric Heaters

#### **Condition**

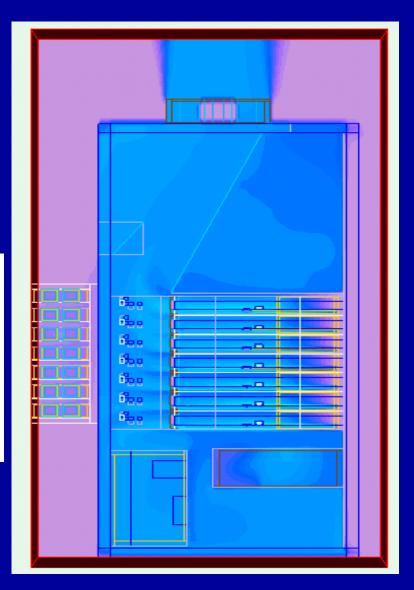
- Ambient Temperature 30 Deg C
- Exhaust Fan Speed 1300cfm
- Thermal Load per tray 1200watts
- Number of Trays per rack 7

#### **Result**

Tray			
Numbering	Measurement	Simulation	Diff %
Tray 1	54.3	51.1	6.24%
Tray 2	48.5	47.1	3.04%
Tray 3	45.5	48.1	-5.34%
Tray 4	48.0	49.3	-2.57%
Tray 5	43.9	49.6	-11.40%
Tray 6	47.3	51.6	-8.25%
Tray 7	46.6	50.5	-7.70%

Simulation agrees with measurement at difference less than 12%.

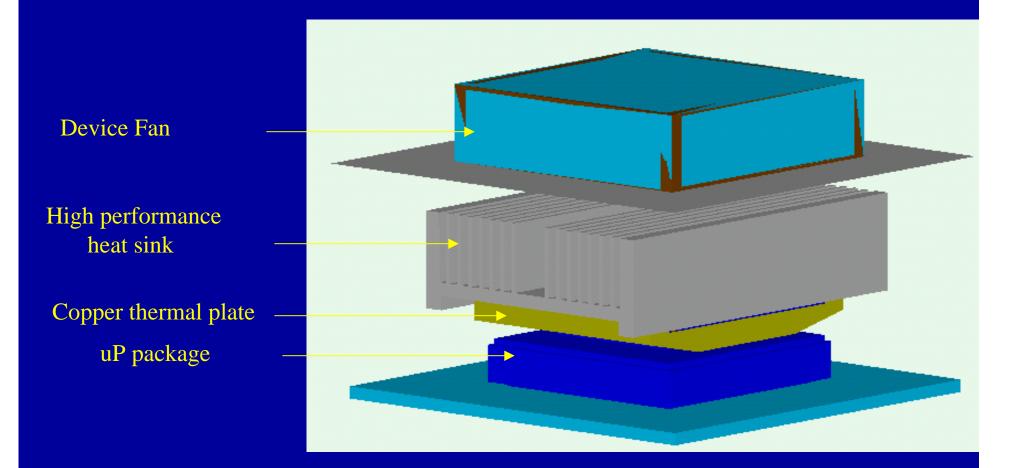
**Rack level model is accepted!** 





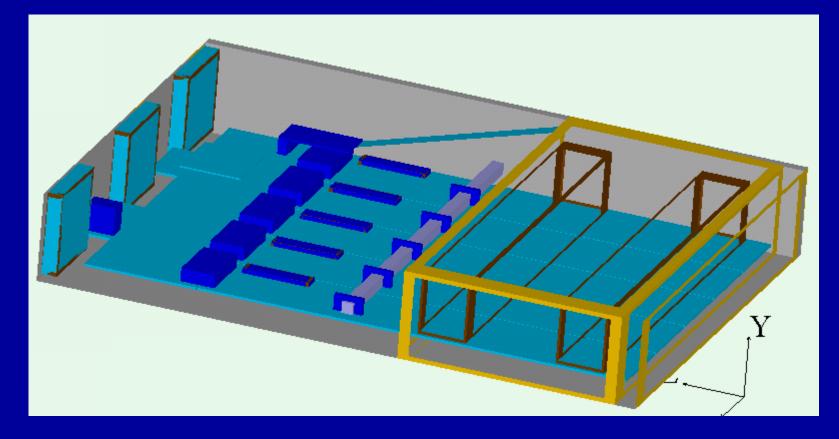
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### Application to New BI Design: DUT Unit





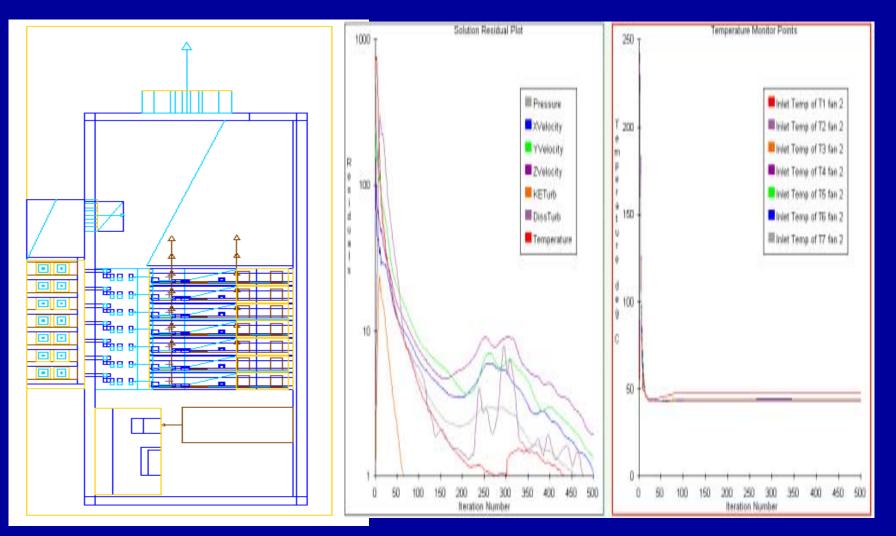
#### Modeling of New BI Tray



- PCBs: V board, F-Board, S-board & T board.
- Components: Voltage Regulator Modules (VRMs), Convert block
- 3 Tray Fans, Cable & its connector

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#### Modeling of New BI Rack



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#### Typical Flow & Thermal Distributions

Design conditions:

uP = 45W; TEC = 30W

VRM = 15.6W

Totally, 1.25KW/tray, 11.65W/rack.

Ambient: 25'C

Rack Fan: 1392 CFM

#### **Predictions:**

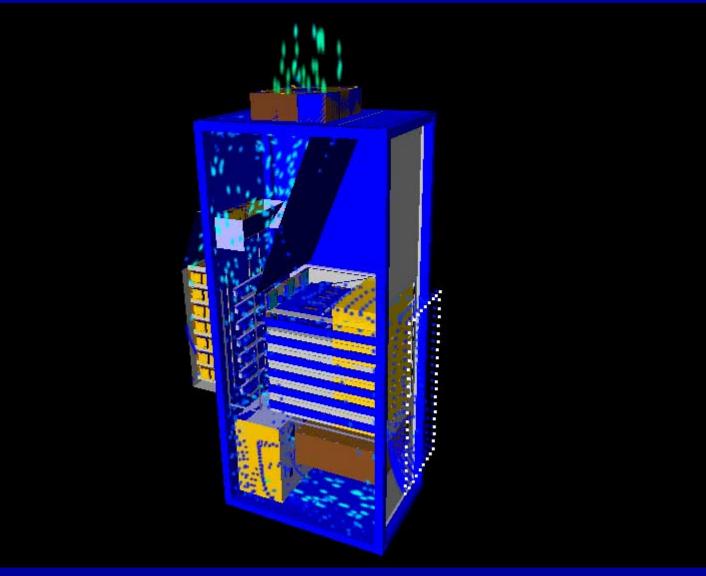
Tray Te	mperatu	re, 'C:				
Tray 7	Tray 6	Tray 5	Tray 4	Tray 3	Tray 2	Tray 1
44.7	44.6	44.5	44.3	43.9	43.6	48.0





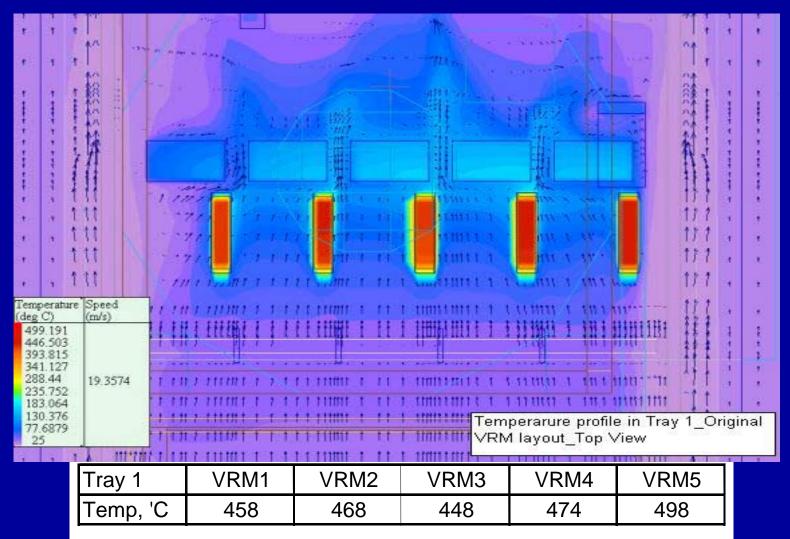
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#### Animation of Air Flow in BI Rack





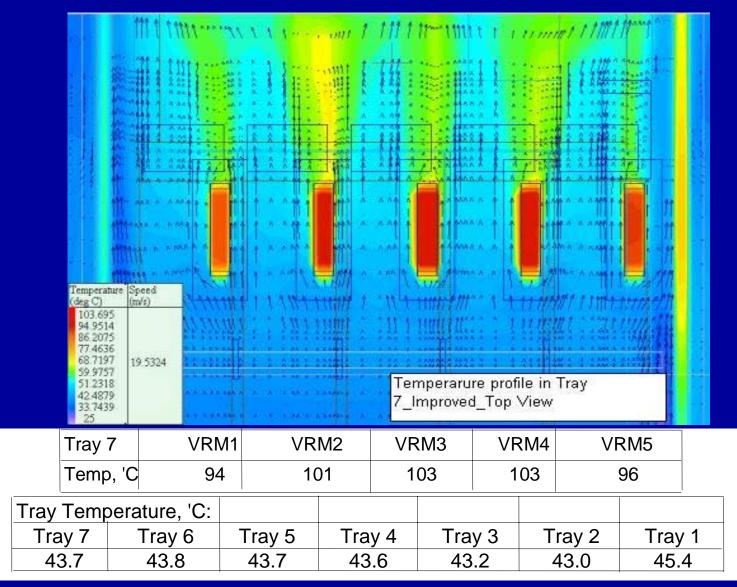
#### Hot Spots in the Present Design



#### VRMs are at about 500'C, Hot spots in the rack!



#### Thermal Solution to Hot Spots by Heat Bridge



Achievement: VRM Temp < 150'C, Tray Temp reduced by about 1'C.

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### Conclusions

- Thermal simulation methodology for BI system have been developed with validations.
- New BI system design have been modeled and hot spots were detected on VRMs.
- Methods has been developed to solve the thermal issues.
- CFD modeling can be used to evaluate, improve the system design, and prevent the thermal issues before manufacturing and production and thus time-saving and cost-saving.

#### **Benefits of Thermal Simulation**

- Procedures to develop and validate the CFD models for complicated systems.
- Compact model development methodology for component and sub-system.
- Validation experiment at subsystem and full system level
- Experience and knowledge can be used to simulate other testing equipment and systems.

### Acknowledgement

The following persons are acknowledged for their respective contributions and support to the project:

•Bay Gim Leng, Rathin Mandal, Mui Yew Cheong, Rafiq Hussain, Maung, MS, James Hayward, Raj Master, AW CK and CS Chan from AMD.

• D.Pinjala, O.K.Navas from Institute of Microelectronics (Singapore)

Support of AMD management is also appreciated.



## BITS 2002 Burn-in System and Driver Board Technology Advances

2002 Burn-in and Test Socket Workshop March 3 - 6, 2002



Mike Niederhofer, & Bruce Simikowski INCAL Technology, Inc.

## Burn-in System Minimum Requirements

- Temperature control
- Power supply control and sequencing
- Dynamic drive signal capabilities
- Downloadable pattern file structures

## Past Burn-in system technology

- Static Burn-in
- Dynamic drivers with binary counter or EEProm based drivers
- No output monitoring manual operator measurement
- Manual power supply sequencing or thumb-wheel switches
- Temperature monitor via chart recorder

## Early Burn-in systems

#### • The OLD way



1/30/2002

### Today's customers demand

- Flexible system tooling for different board types
- Windows based op system Windows NT
- Network access Desktop Emulation
- Output monitoring
- Lower voltage levels .5 volts for <.13 micron tech.</li>
- Higher frequencies to 33 MHz
- BIST test functions
- DUT Status, failure data analysis
- Pattern editors
- Tester vector converters

## Modern Burn-in Systems

- Computerized
- Low Voltages
- DUT Monitoring

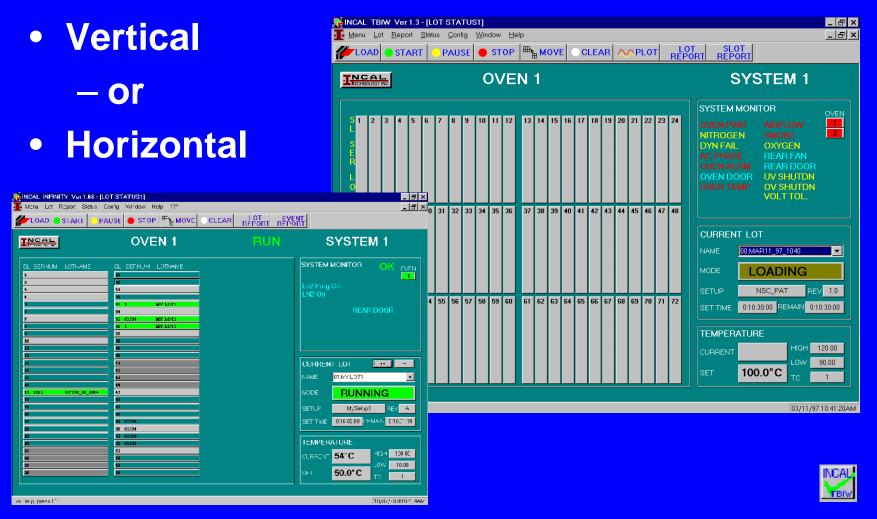




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## Windows Op sys

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## **Slot Information**

Mon

- DUT Mapping
- Waveform retrieval example
- Advanced fail information

Dut Status I-Scope Advance Fail Adr			
Freq(Mhz) t1=15000.00ns t2=8000.00	)ns t2-t1=-7(	000.00ns Freq=0	.14Mhz
0.01515			
	Л		
			12
			16
			▶ 64000
Trig. Adr     Loop1#       1     0       Hold#     Loop2#       0     0	xcquire /Div ++	Save Setup Load Setup Print	Time     Cursor       Hex     Image: Cursor       Bin     Clr Cursor

itoring Oven# 1, Slot# 1, Lot# JUL10_99_1454	×
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Dut Status I-Scope Advance   Fail Adr	
A1         A2         A3         A4         A5         A6         A7         A8         A9         A10         A11         A12         A13         A14         A15         A16	
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16	
Dut Status   PScope   Advance   Pail Adr         D1       D2       Signal Pass/Fail Status       Fail Addr , Loop1, Loop2, Hold	
001         002         003         004         005         006         007         41         15         016           017         018         019         020         021         022         023         44         15         15         016           033         034         035         036         037         038         039         49         15         17         048	
12       033       034       035       036       037       038       039       49        47       048         16       049       050       051       052       053       054       055       57        53       064         16       065       066       067       068       069       070       071       19        79       080         16       081       082       083       084       085       086       087       26        35       096	
Cursor         097         098         099         100         101         102         103         104         105         106         107         108         109         110         111         112           113         114         115         116         117         118         119         120         121         122         123         124         125         126         127         128           129         130         131         132         133         134         135         136         137         138         139         140         141         142         143         144	
Instruction         Instruction	

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### Pattern Editor Program

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D01 D02 MySignal1 MySignal2	19 20 21 22 44 17 18 19 19 19 10 10 10 10 10 10 10 10 10 10	Cust. Import From National Semi Cust. Import IDT CAM Converter Cust. Import Motorola Converter
For Help, press F1	Thursday, January 31, 2002 04:	18 PM //

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### **Tester Vector conversions**

#### • A Difficult Challenge

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		the BUB there based Provide Help		
🖉 SampleAscilCommunds - Notispiel		DERGANTER	Output to Little Endien ( Plain ) Convert PatToEprom (48Ch. Dr.)	
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3 - PeditW

Convert View Help

Text File Remove Blank Lines/Spaces

Text File Reorganize Columns Text File Combine Columns Text File Line/Vector Doubler

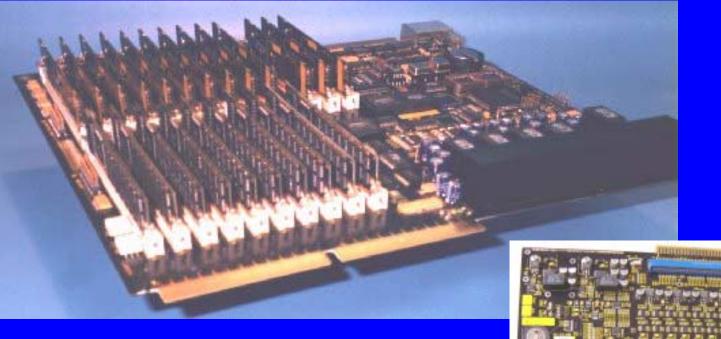
### **Previous Driver capabilities**

- 16 address lines / eight clocks
- Clock outputs in ranges of 5 to 10 volts
- Maximum frequency of 2 to 10 MHz
- No on-board memory. Pattern Generators configured on a zone basis.
- 96 channels maximum
- Discrete Output channels

## Latest driver board technology requirements

- Computer controlled
- Tester file Compatibility
- Configurable Drive and Monitor channels
- Speeds of > 25 MHz
- Memory pattern depth 2 to 16 Meg
- Monitor of DUT outputs
- 128 to 256 channels
- Compatible to many signal types: TTL, LVTTL, LVDS, PECL, GTL, GTL+, CML

### **Modern Drivers**





### **Dedicated driver boards**

- Application specific or
- Industry specific
- Surface mount technology
- High production volumes
- Lower unit cost

### **Dedicated driver boards**

- Application specific Drivers
  - HTRB/HTGS
  - HYBRID
  - Electro Migration
  - Soft-Error







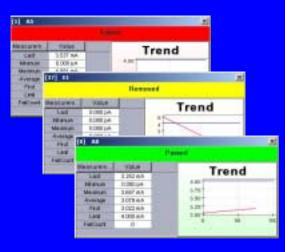
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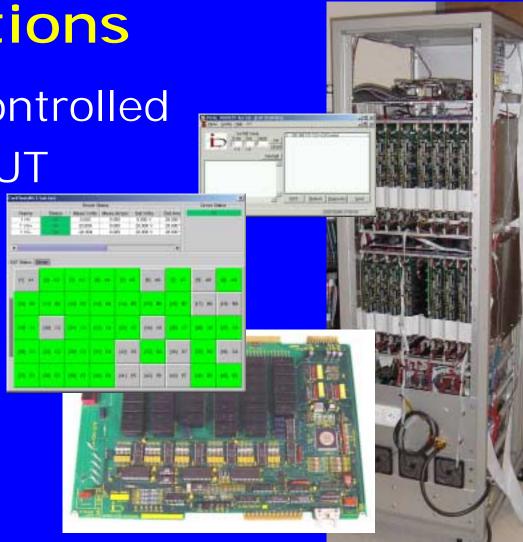
# High Power System & Driver requirements

- Designed specifically for Hi-Voltage FET, IGBT, SSR testing
- High voltage capabilities
- Individual DUT power Control/Monitoring
- Automotive market
- Industrial Controls Market

# Specialty B/I system specifications

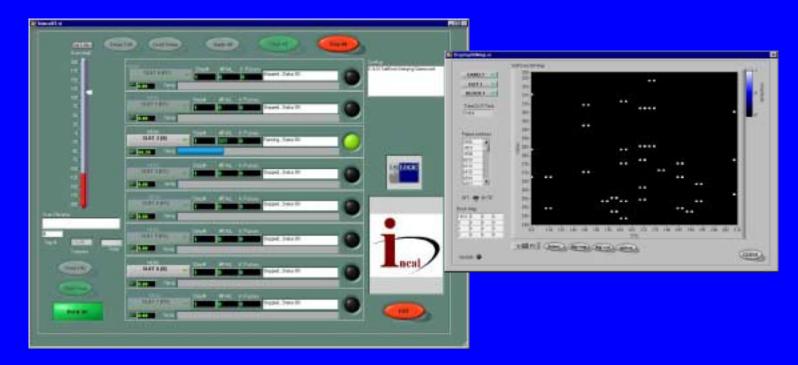
- Computer controlled
- Individual DUT monitoring





### New emerging test methodologies

- Soft Error testing
- Test memory locations with neutron or proton sources present



## Today's Industry markets and requirements

#### MARKET

- Commercial IC market
- Automotive market
- Memory market
- Medical / Military
- Test Lab market

#### **REQUIREMENTS**

Low cost / delivery High power Speed /error detect Custom hardware Cost / flexibility

### Today's industry demands

High speed dynamic drive High power dissipation

Deeper pattern requirements

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# Specialty and Hybrid market specifications

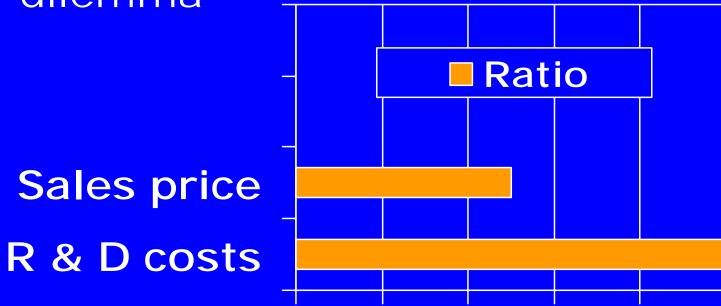
- Implantable Devices
- High Quality levels required
- Custom Hybrids and sockets
- High Voltage Power and Signals
- Monitor capabilities required

### Test Lab market

- Low cost, universal hardware
- Adapter trays to utilize existing BIBS
- Flexibility
- Ease of Pattern Generation & Conversion

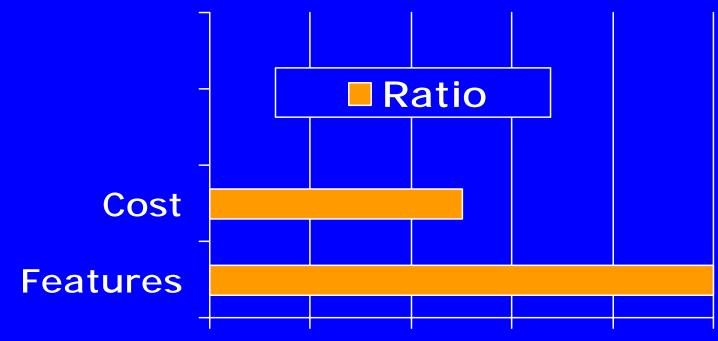
### System vendor's plight

 A typical System engineering dilemma



### Customer's requirements

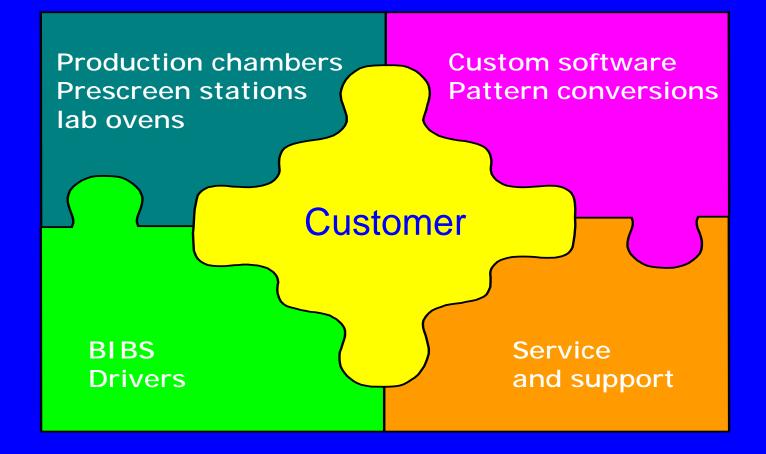
 A perfect solution for the customer



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### **Burn-in system vendor**

#### One stop shopping



- Vendors and customers work towards common goal of improving technology while lowering costs
- Standardization of hardware
- Sharing of R & D costs
- Discuss technology advancements and technical requirements up-front
- Service multiple markets with present technology
- Industry consolidation inevitable

- Today we see Production systems that offer the flexibility to test and burn-in different product types and technologies for many different markets
- The cost of these Burn-in systems can approach those of high-end VLSI testers

- A working relationship between the system vendor and the customer at all stages of the purchase and utilization cycle will reduce R & D costs, thus lowering system costs
- NRE charges, design costs, custom hardware, and custom software ...

WILL ALWAYS EXIST

• Minimizing these costs , while providing the customer cost effective technical solutions

Is the CHALLENGE system vendors face today