Burn-in & Test Socket Workshop

March 3-6 , 2002
Hilton Phoenix East/Mesa Hotel
Mesa, Arizona

IEEE

IEEE COMPUTER SOCIETY

Sponsored By The IEEE Computer Society Test Technology Technical Council

BiTS Burn-in & Test Socket Workshop

Technical Program

Session 2
Monday 3/04/02 10:30AM

Managing High Frequency Requirements

"Optimizing Load Board Design And Modeling For High Frequency Contactors"
Jeff Sherry - Johnstech International Corporation

"The New YieldPro Array Series Contactor"
Julius Botka - Agilent Technologies

"Electrical And Mechanical Performance Characterization Of High Frequency Test Sockets"
Lisa Steckley - IBM Microelectronics
Dr. Hanyi Ding - IBM Microelectronics

Optimizing Load Board Design and Modeling for High Frequency Contactors

Jeff Sherry, RF Engineer
Johnstech International

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Discussion Topics

- Modeling & its importance
- Designing load boards for optimal performance
- Load board effects
- Grounding schemes
- Crosstalk improvements
- Load board pad size and placement
- Model validation & performance examples

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Modeling & Its Importance

- Determine potential problems before building hardware
- Determine expected performance
- Determine trends and sensitivity of circuits
- Determine effects of tolerances
- Determine interaction between components in system (device, contactor, handler, etc.)
- Design for the device, form, fit, and function of the end application

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Designing Load Boards for Optimal Performance

Microstrip and Coplanar Effects

- Substrate thickness ↓ — Impedance ↓
- Trace width ↓ — Impedance ↑
- Permittivity (ε_r) ↓ — Impedance ↑
- Trace thickness ↓ — Impedance ↑

Coplanar Waveguide Effects

- Spacing (pitch) ↓ — Impedance ↓
- Adding ground plane — Impedance ↓

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Load Board Effects

- Loss tangent affects insertion loss more at higher frequencies
- Uniformity of ε_r and loss tangent vs. frequency
- Substrate thickness affects inductance to ground
- Increased frequency means thinner substrates
- Substrate thickness and dielectric constant (ε_r), along with line width, are major parameters in controlling impedance
- Plating thickness has the biggest effect on load board life

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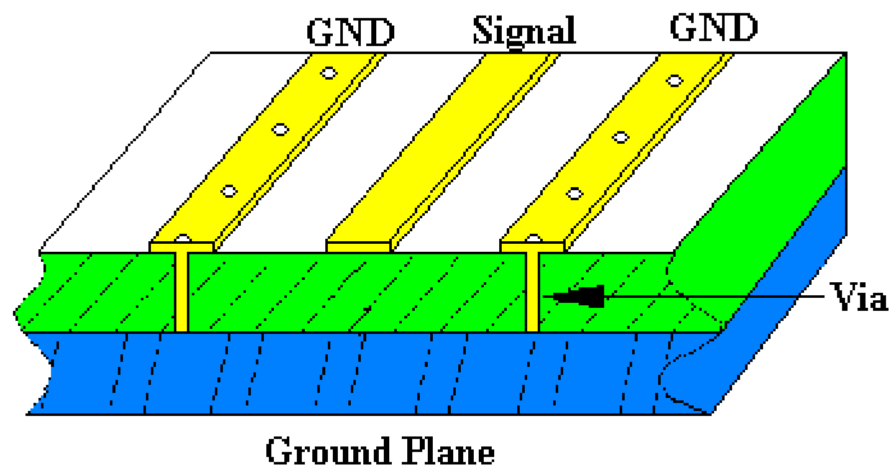
Load Board Effects

- Things to improve load board design
  - Eliminate right angles
  - Eliminate changes in line width
  - Separate high frequency traces with ground
  - Move clock traces away from other signal lines
  - Place decoupling components close to the device
  - Use matched impedance traces up to the device or test contactor

Johnstech

Grounding Schemes

- Length and area of the ground path is very important
- Ground inductance should be minimized
- Resistance of ground should be low (to minimize power supply voltage drop)
- Grounding controls crosstalk between signals



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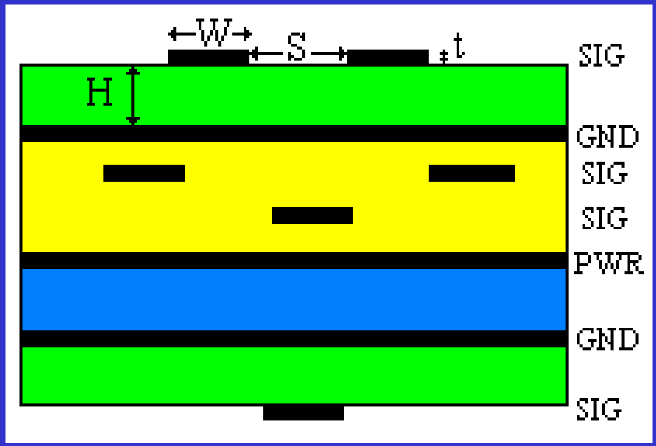
Crosstalk Improvements

- Increase the spacing (S) between traces
- Minimize substrate height (H) while achieving matched impedance
- Route signals orthogonally between layers
- Minimize parallel run lengths between signals
- Use differential routing for clock or critical nets



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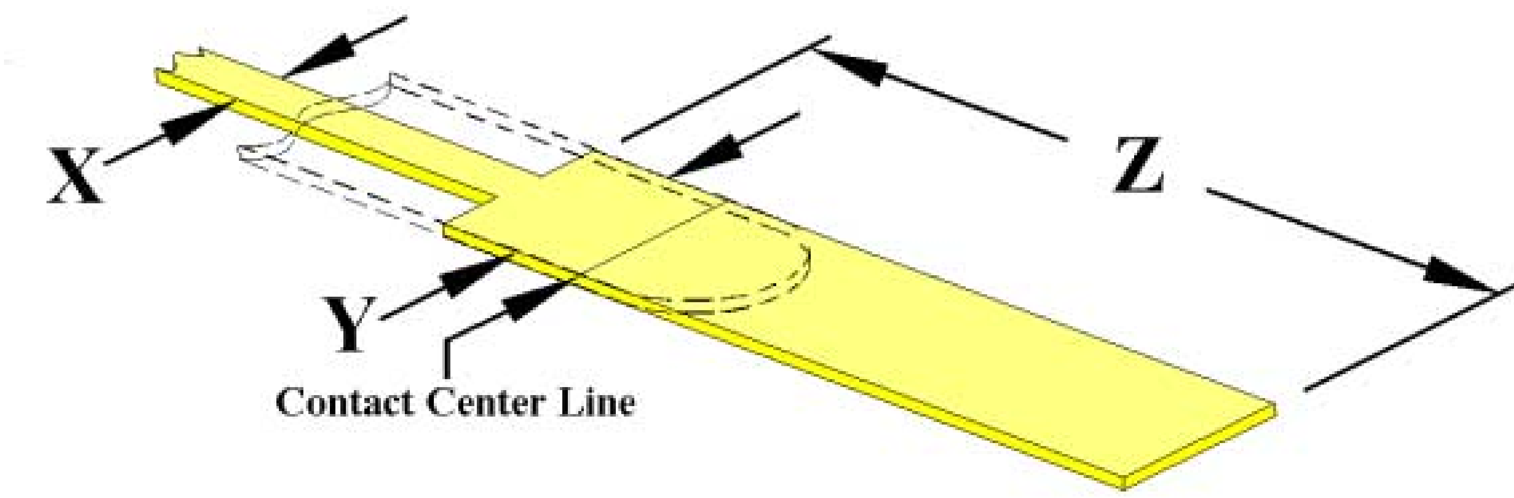
Load Board Pad Size and Placement



X = Y = 50 ohms = Optimal Performance
Z = Optimal Pad Length

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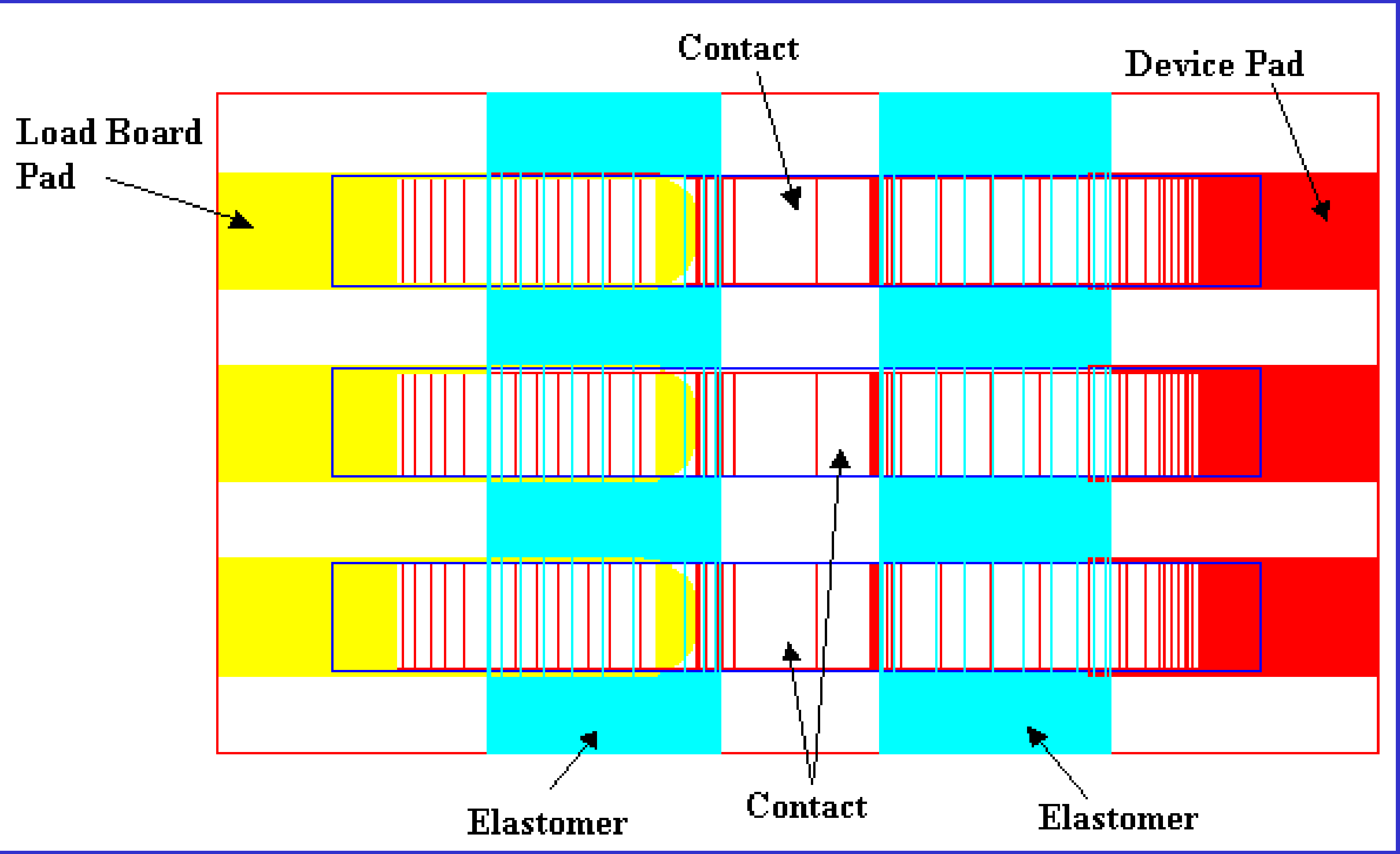
Load Board Pad Size and Placement



Model Validation & Performance Examples

- Validating the Model
  - Explain test results
  - Confirm if contactor will meet customer needs
  - Identify improvements to contactor
  - Identify improvements to load board (i.e. pad sizes)
  - Determine equivalent circuits
  - Investigate changes to contactors to meet customer specific needs

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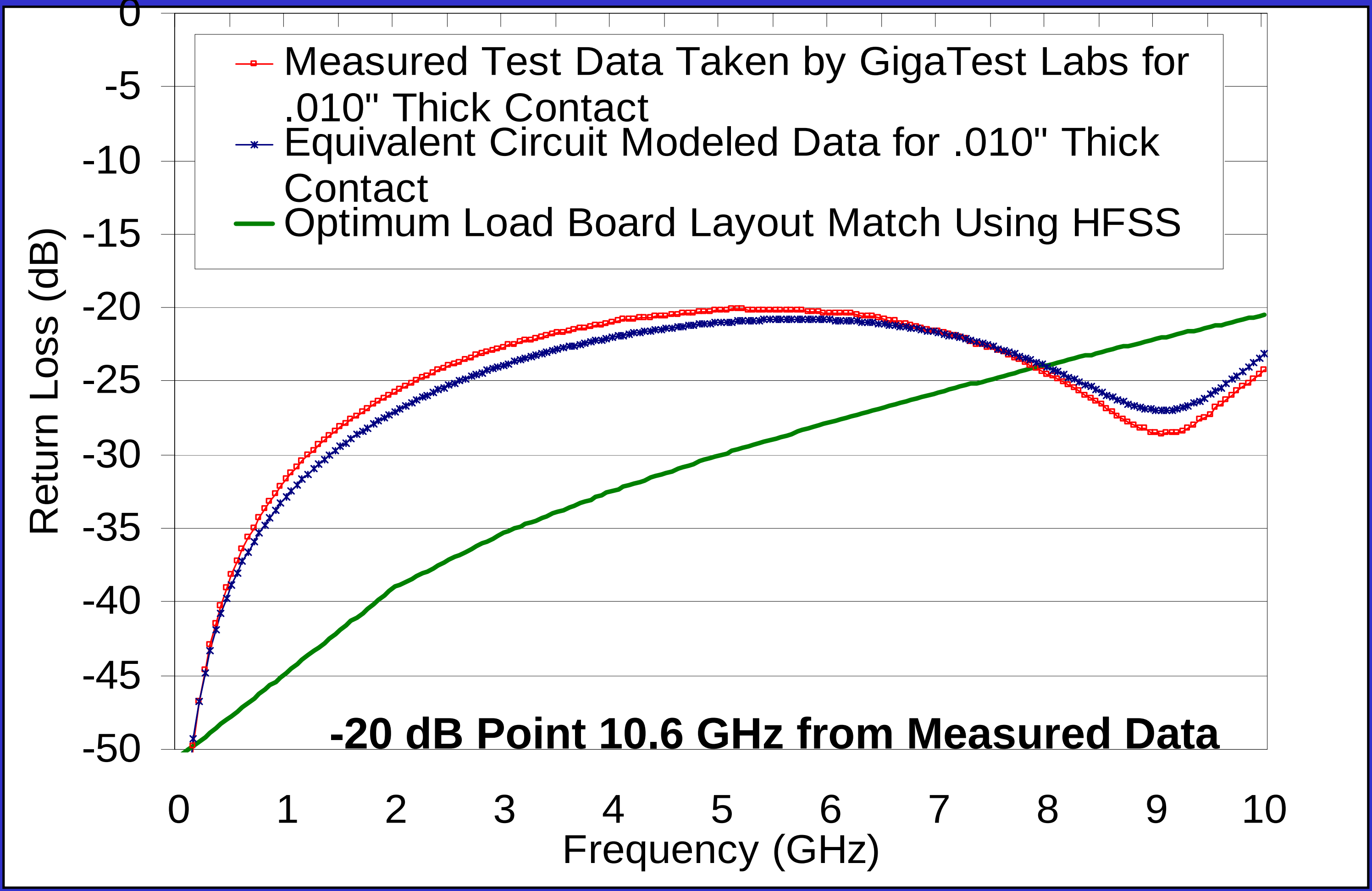
Model Validation & Performance Examples

Leaded Series Return Loss (S_{11}) Data



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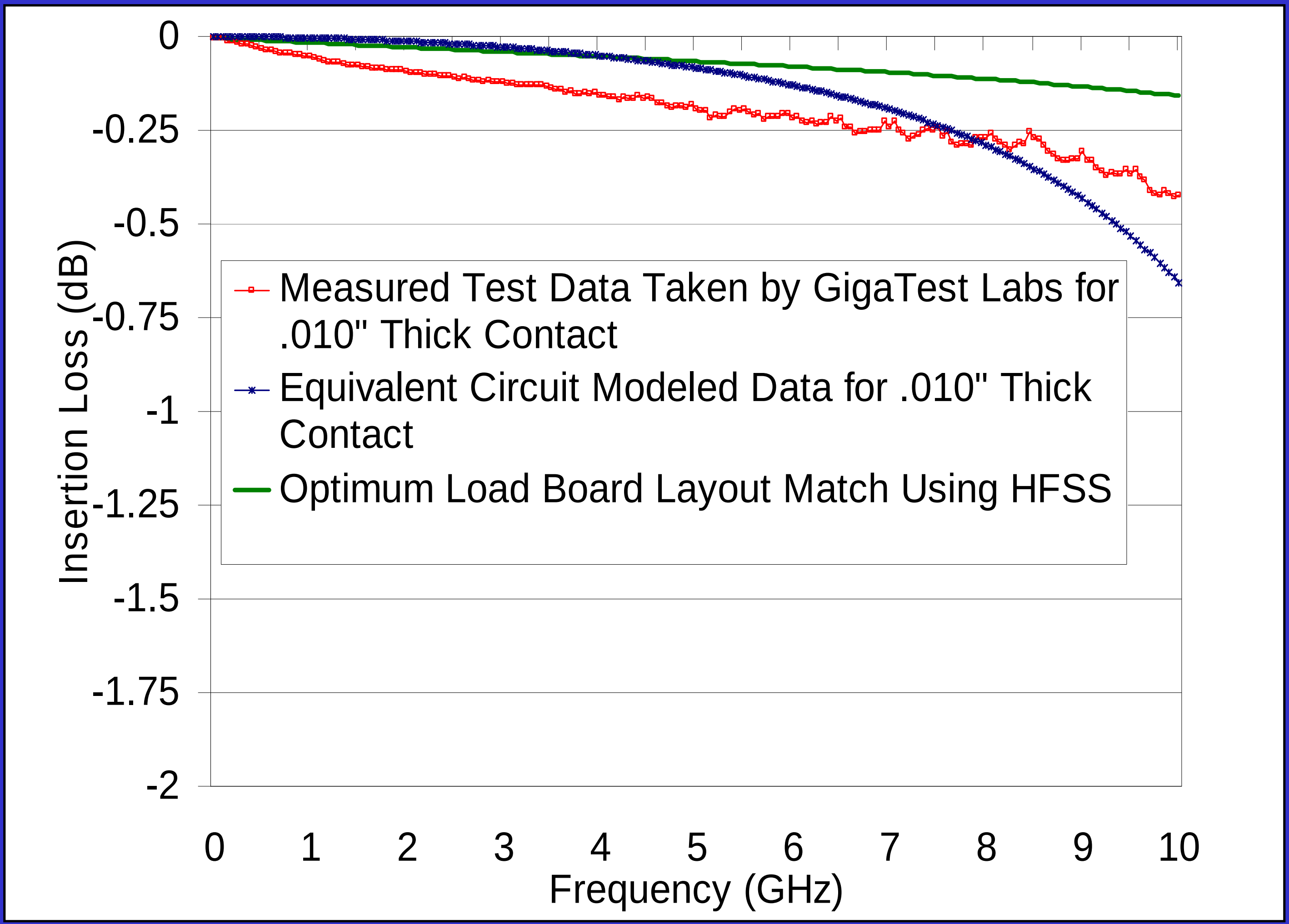
Model Validation & Performance Examples

Leaded Series Insertion Loss (S_{21}) Data



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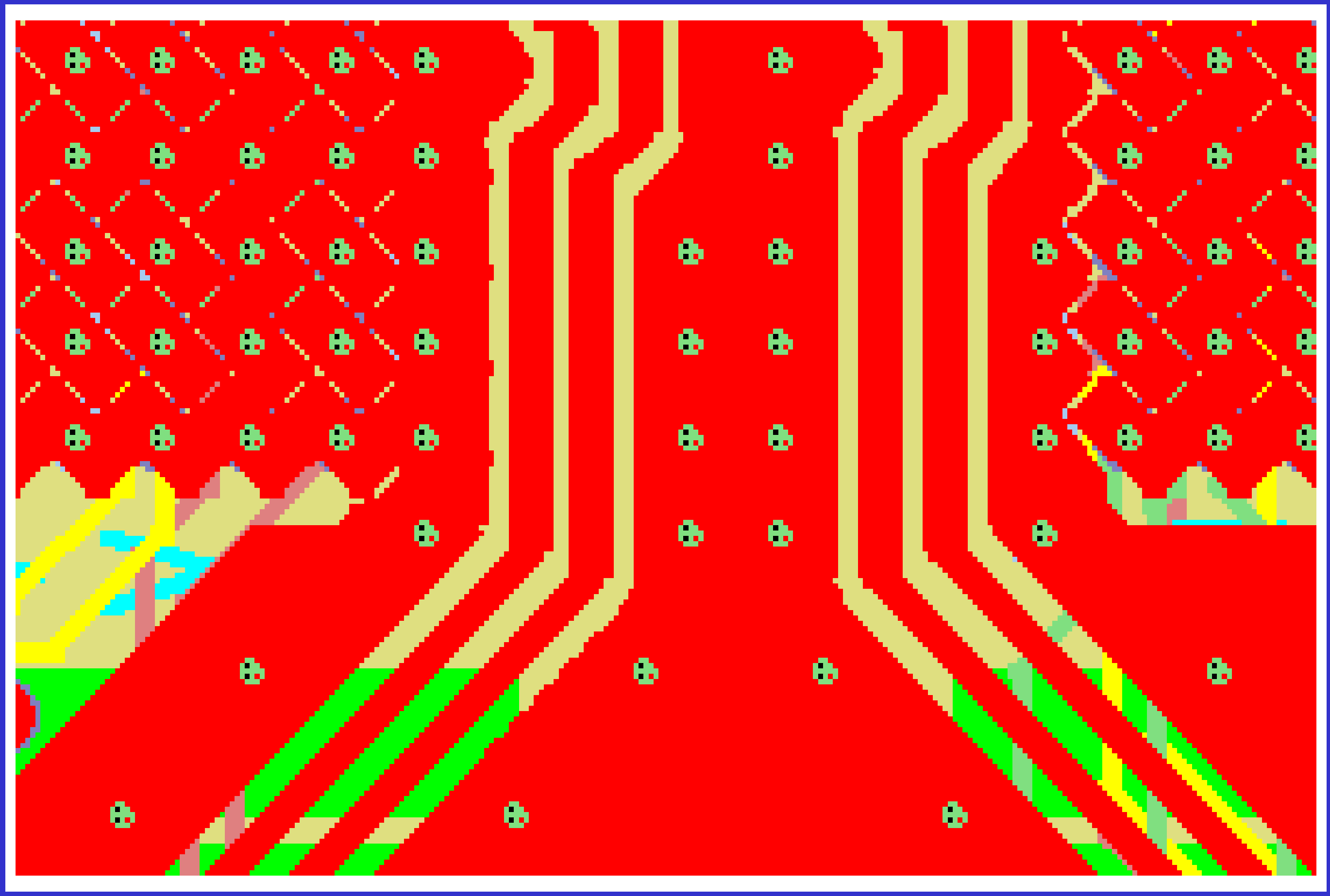
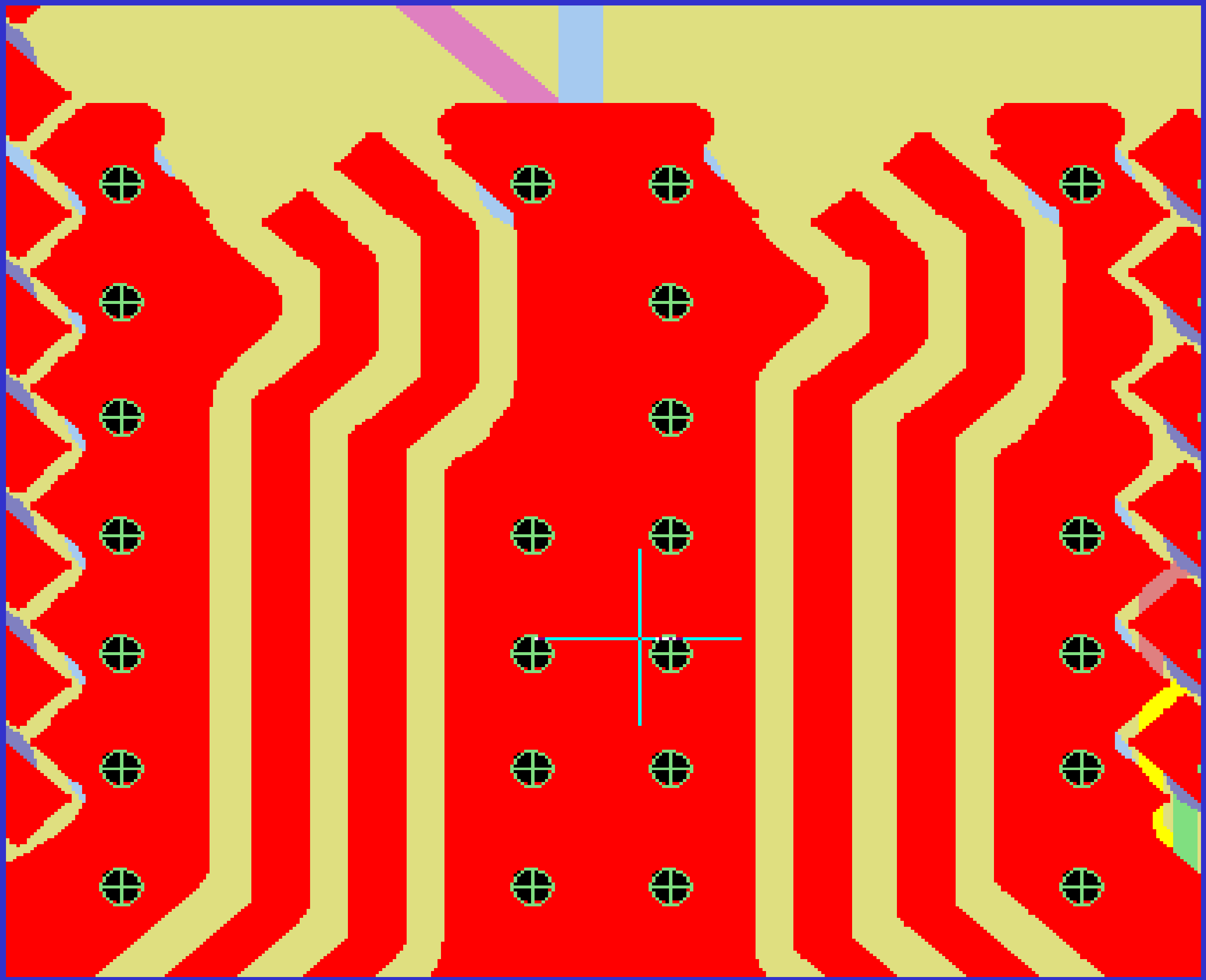
Model Validation & Performance Examples

10GBit/s BGA Non-Optimized Load Board Layout



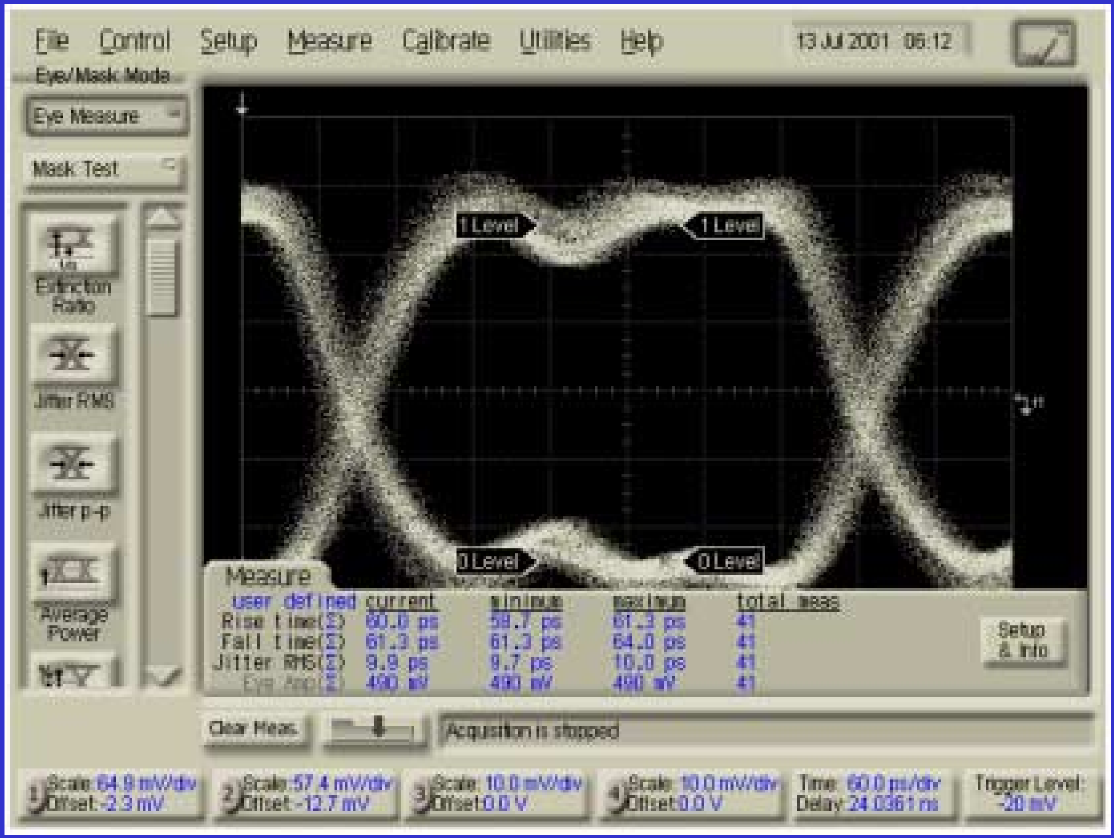
Model Validation & Performance Examples

10GBit/s BGA Optimized Load Board Layout



Model Validation & Performance Examples

10GBit/s BGA With Non-Optimized Load Board Layout



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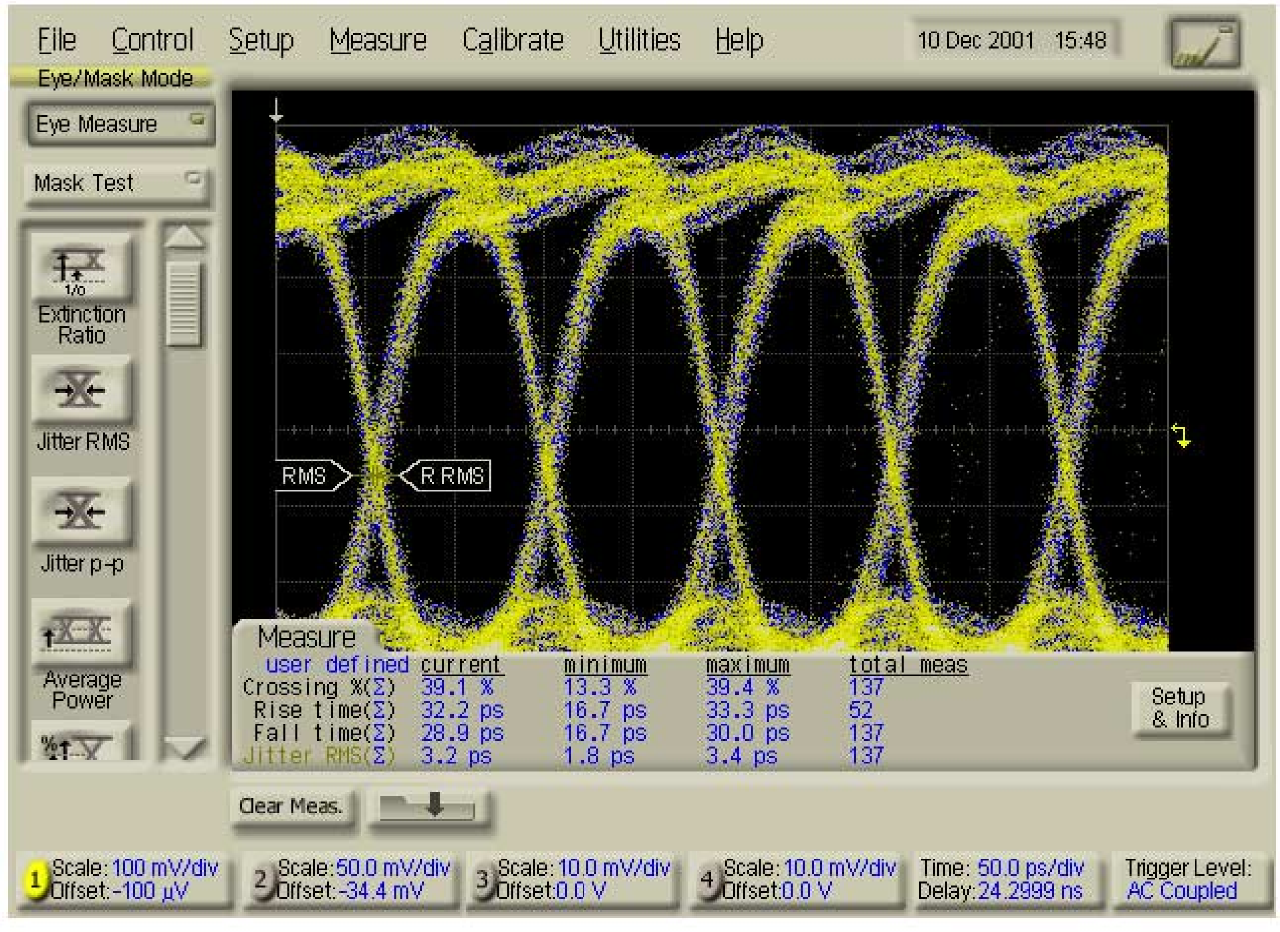
Model Validation & Performance Examples

10GBit/s BGA With Optimized Load Board Layout



Quake Technologies Inc.

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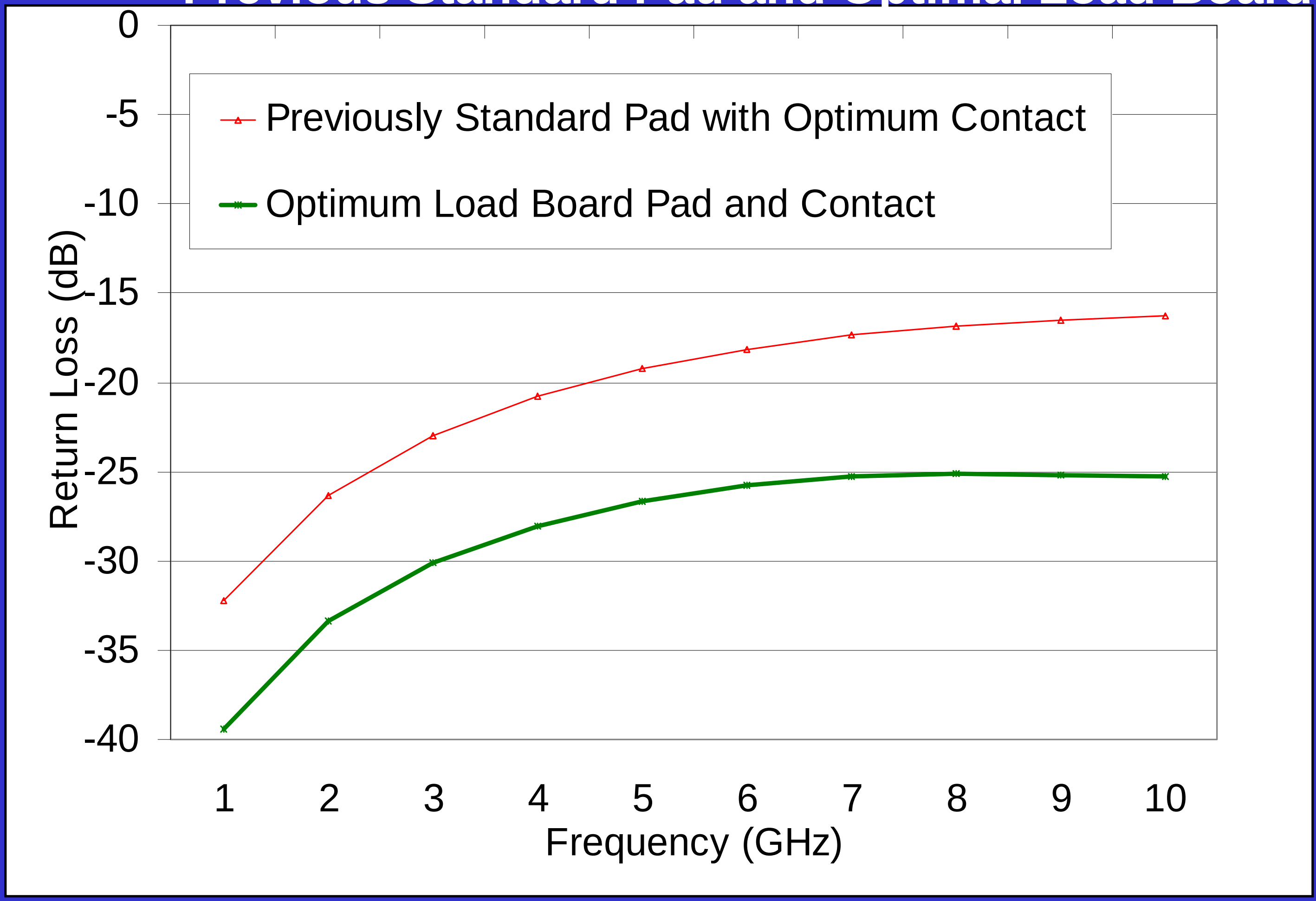
Model Validation & Performance Examples

Return Loss (S_{11}) of Enhanced Pad Series Contact with Previous Standard Pad and Optimal Load Board Pad



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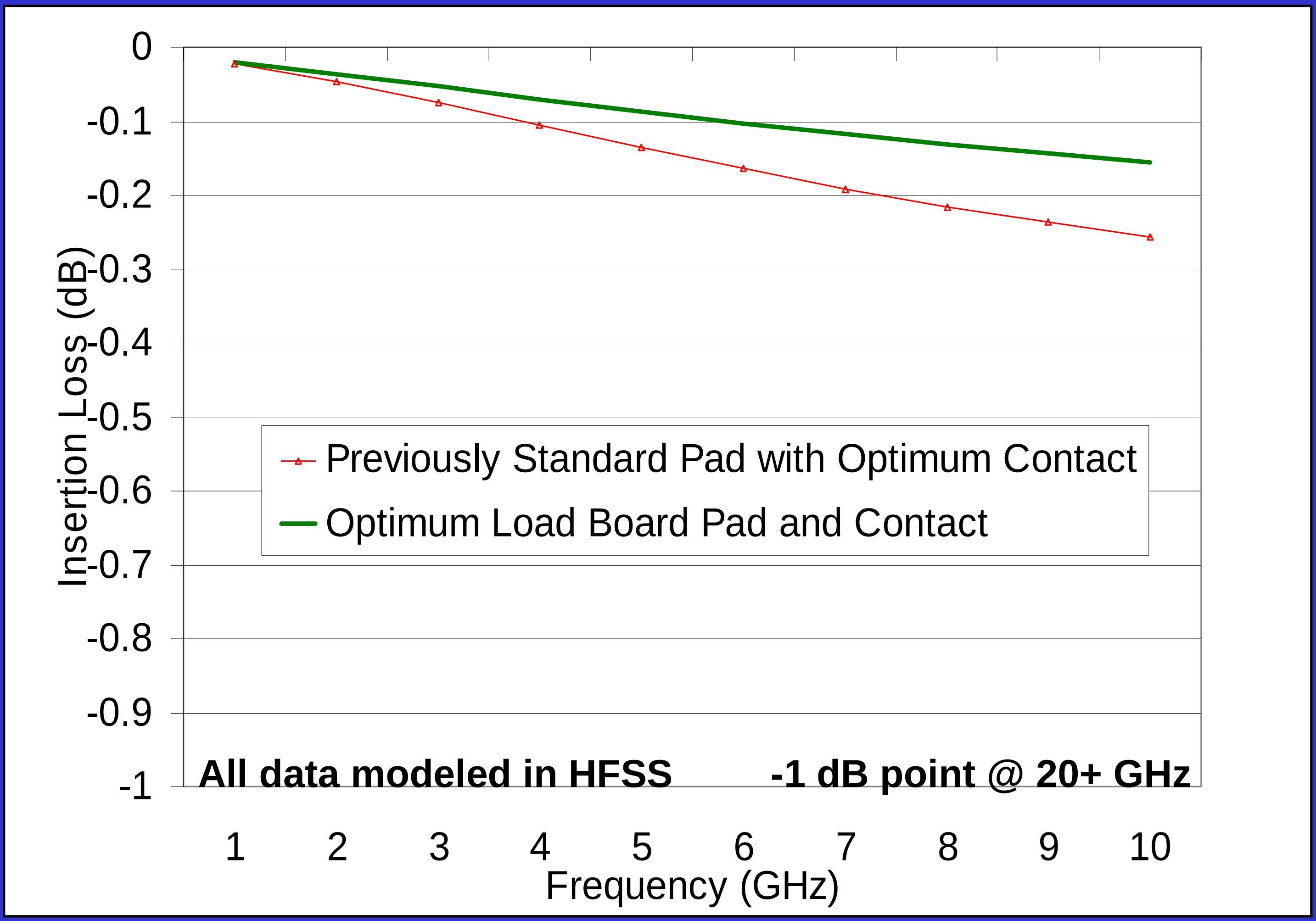
Model Validation & Performance Examples

Insertion Loss (S_{21}) of Enhanced Pad Series Contact With Previous Standard Pad and Optimum Load Board Pad



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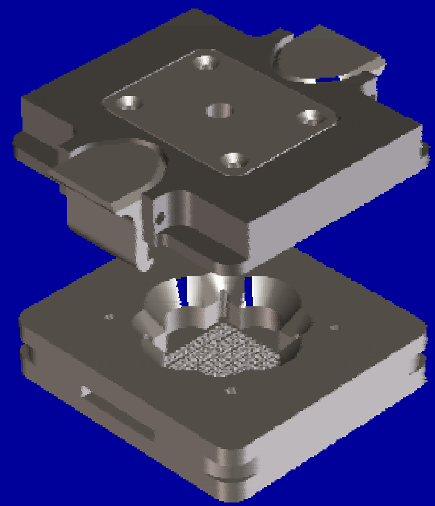
Conclusion

- Modeling trends can determine how to improve load board layout
- Load board layout can greatly affect test data
- Good microwave design principles apply to load board design
- Modeling and test data have shown that significant improvement can be attained by better matching load board and contactor impedance to the Device Under Test (DUT)
- Ball Series contributions from Quake Technologies indicated with the Quake logo

Johnstech

The New YieldPro Array Series Contactor

Patent USP# 6,299,459



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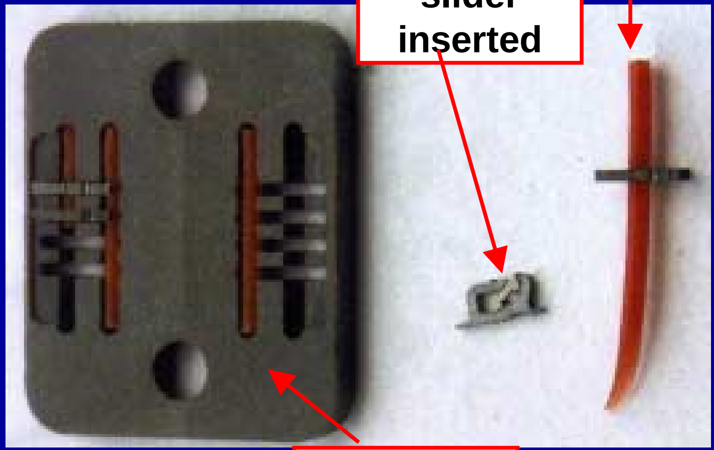
Julius Botka, Master Scientist
julius_botka@agilent.com

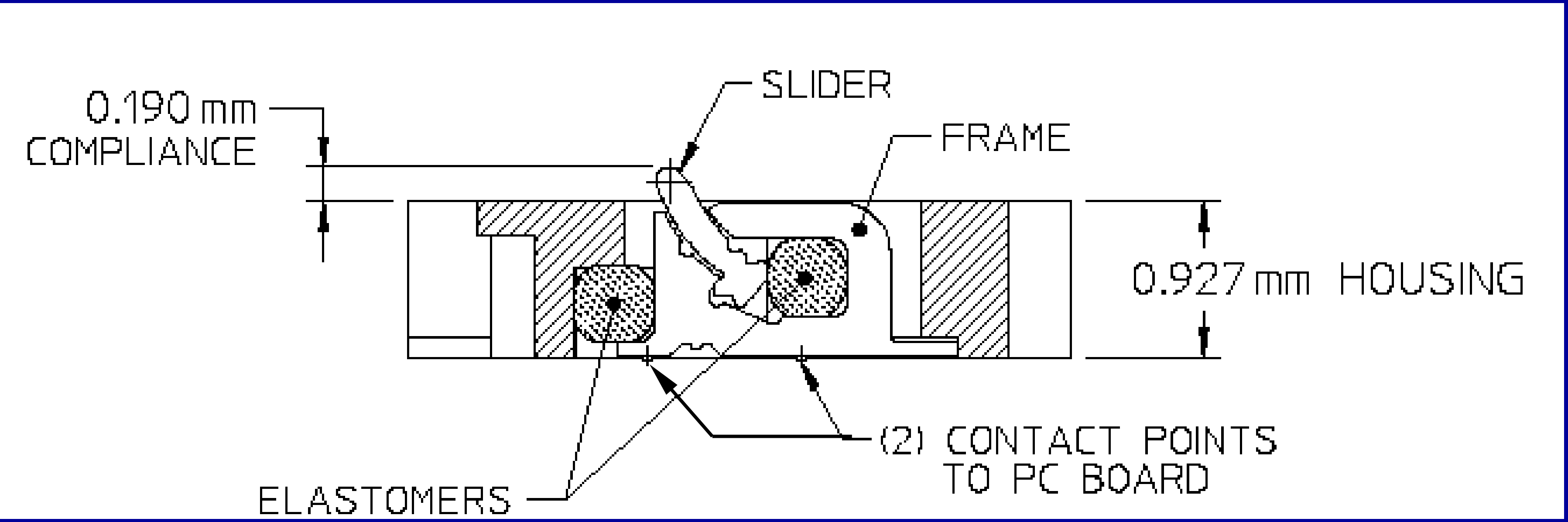
Agilent Technologies

Brief History

- Semiconductor manufacturers and test houses are required to test devices with multiple functions
- Packages vary in type, size and pitch
- Contactors provide the final crucial link to testers
- First YieldPro contactor patented in 1997
  - Lowest parasitics with independently compliant wiping contacts
  - Path length is 0.037", performance up to 18GHz



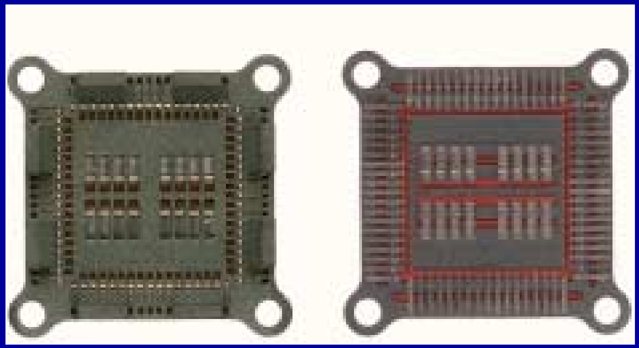
Original YieldPro Contactor for Leaded Components



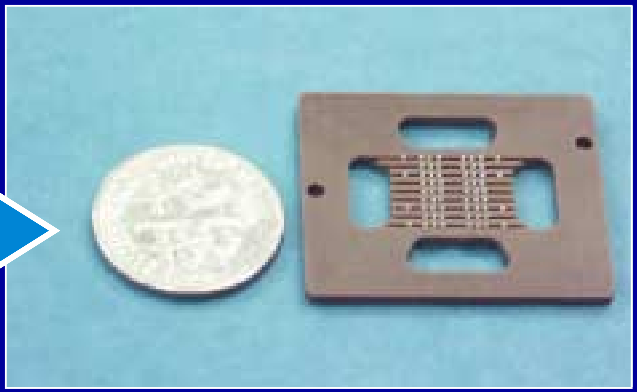
Patent USP# 5,609,489

Today's evolution of the business:

- Size and pitch keep getting smaller, number of contacts increasing
- Move from leaded to leadless BGA/LCC packages (Ball Grid Array and Leadless Chip Carrier)



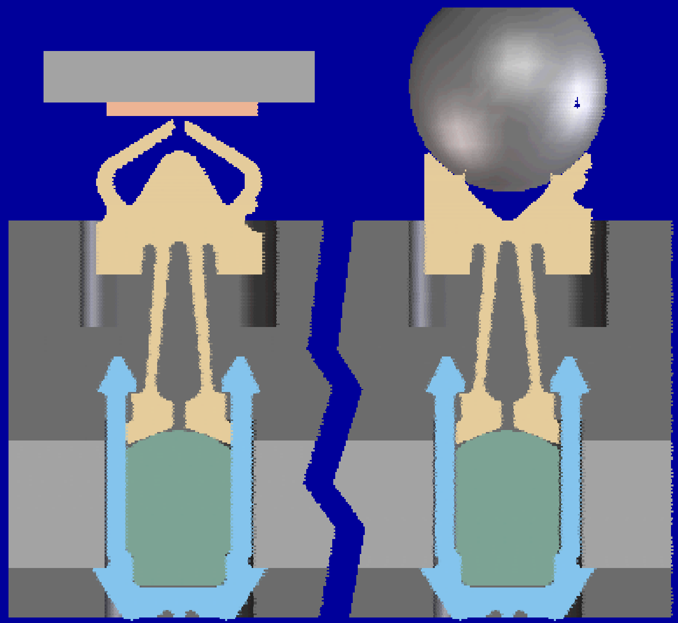
Leaded YieldPro Contactor



YieldPro Array Contactor
USP#6,299,459

The New YieldPro Array Contactor

- A new solution is needed for contacting new chip scale packages, such as BGA and LCC
- Agilent's new YieldPro Array design addresses technologies, Bluetooth®, Wireless LAN and high speed digital components
- All are heading toward higher frequencies and require good performance in high speed digital, and at the 3rd harmonic of the RF fundamental



Patent USP# 6,299,459

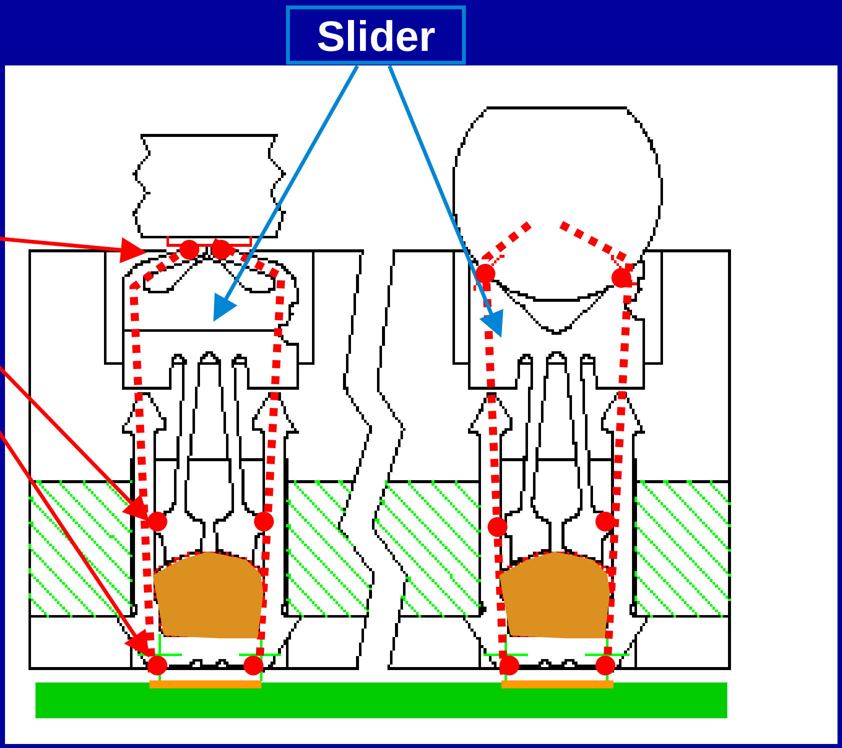
Design Considerations

Problem:

Lack of reliable/repeatable contact between tester and component to be tested

Solution:

- **Two parallel contact paths from solder ball/contact pad to DUT board**
- **Contacts do not wear the DUT board**

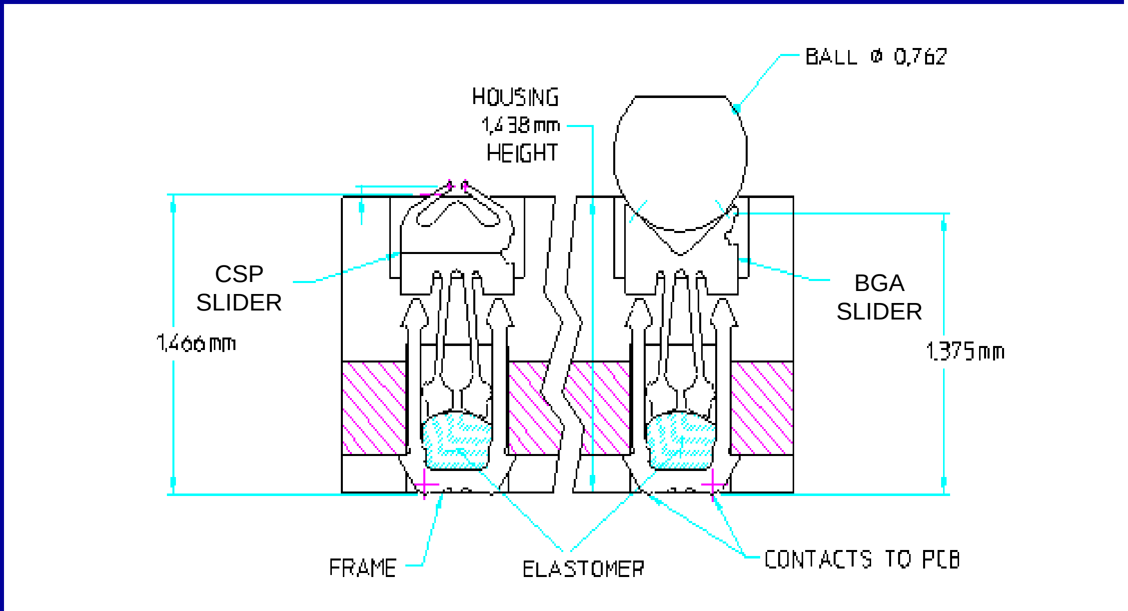


Problem:

Unwanted and unmanageable inductive or capacitance parasitics

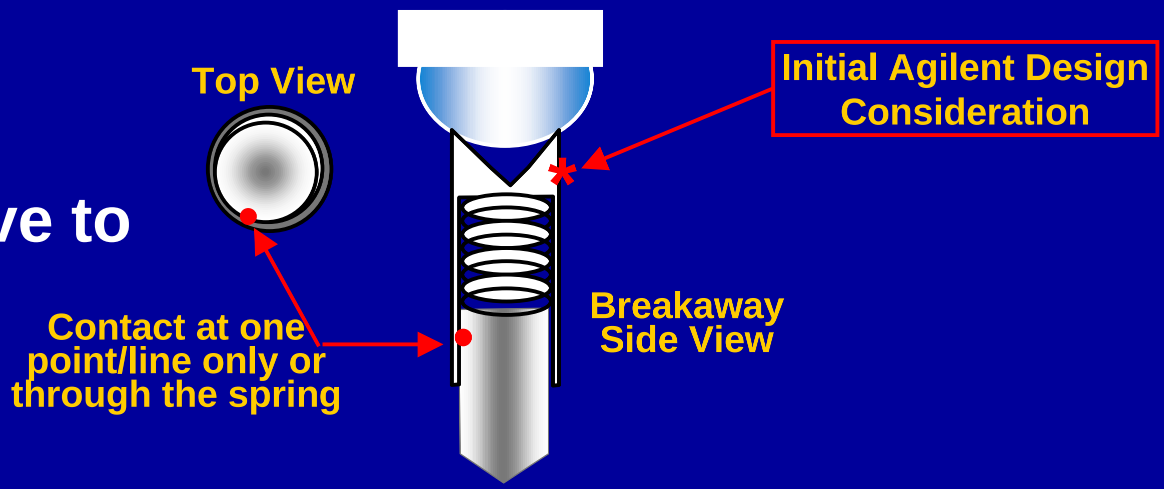
Solution:

- **Parasitic inductance and capacitance are reduced by controlling impedance to be closer to 50Ω**
- **Parasitics are further reduced by minimizing height of the contactor**
- **If increased impedance is required, adjacent ground contacts can be removed**



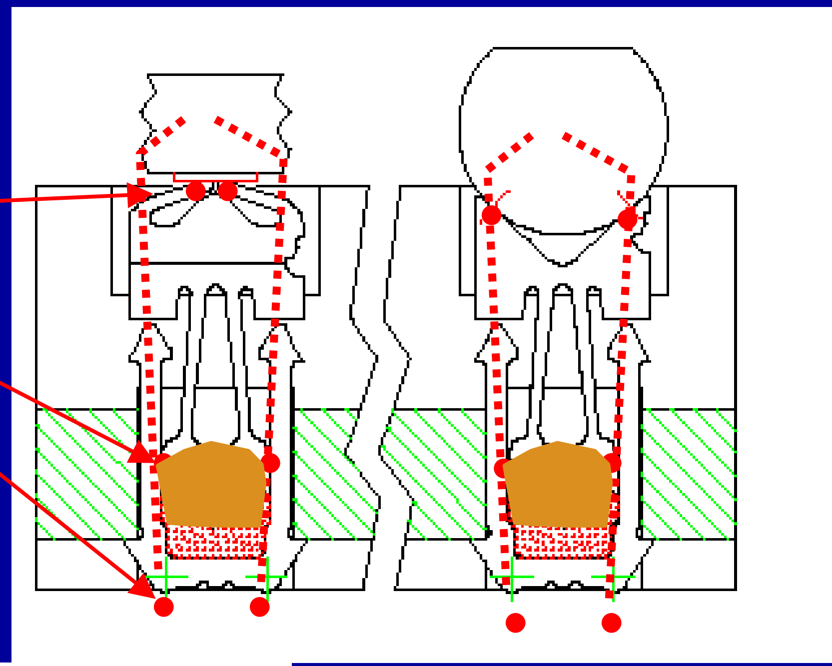
Problem:

Excessive and undefined contact resistance sensitive to contaminants



Solution:

- **Resistance is lowered by having two parallel contact paths**
- **The slider can follow the ball, always maintaining two contacts to pad or the sides of the ball**



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Problem:

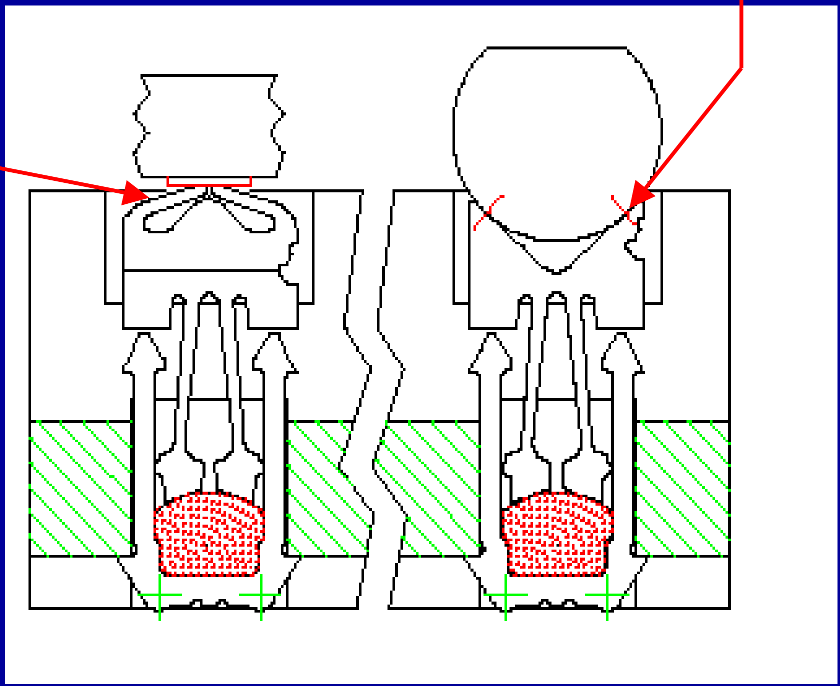
No wiping contact to ball/pad

Flexible heads provide wiping action

Slider wipes the sides of the ball, barbs pierce the oxide layer

Solution:

- Slider wipes the sides of the ball, while barbs pierce through the oxide layer without gouging either the ball or the pad
- CSP Head contacts flex and wipe contact pad toward each other

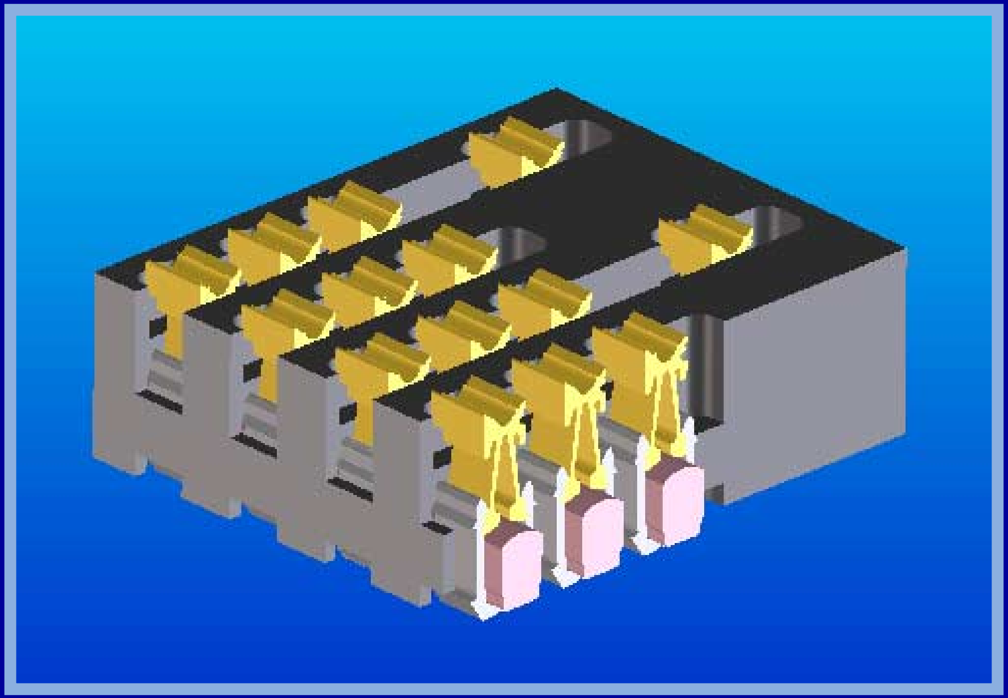


Problem:

Damage to the bottom of the solder ball/pad due to direct hit and excessive pressure from contact

Solution:

- **No sharp points associated with the top of the contact. Therefore, no gouging or re-shaping can occur. The ball/pad is not damaged by the YieldPro Array contactor.**

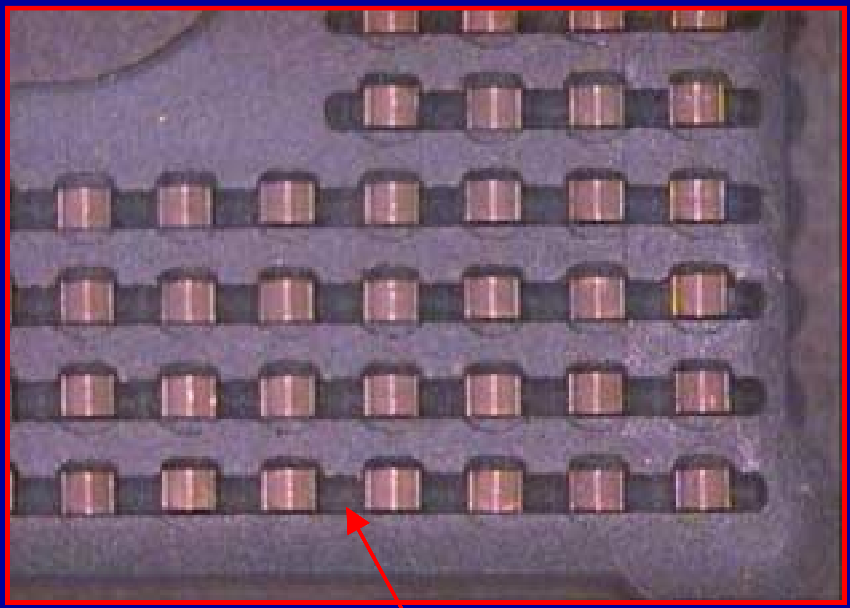


Problem:

Given there is always contamination in a test operation, it becomes very difficult to clean the contactor due to narrow open spaces on the top surface where contamination can lodge

Solution:

- **Housing designed for easy removal of contaminates using low pressure compressed air**
- **Complete contactor can be thoroughly cleaned ultrasonically**



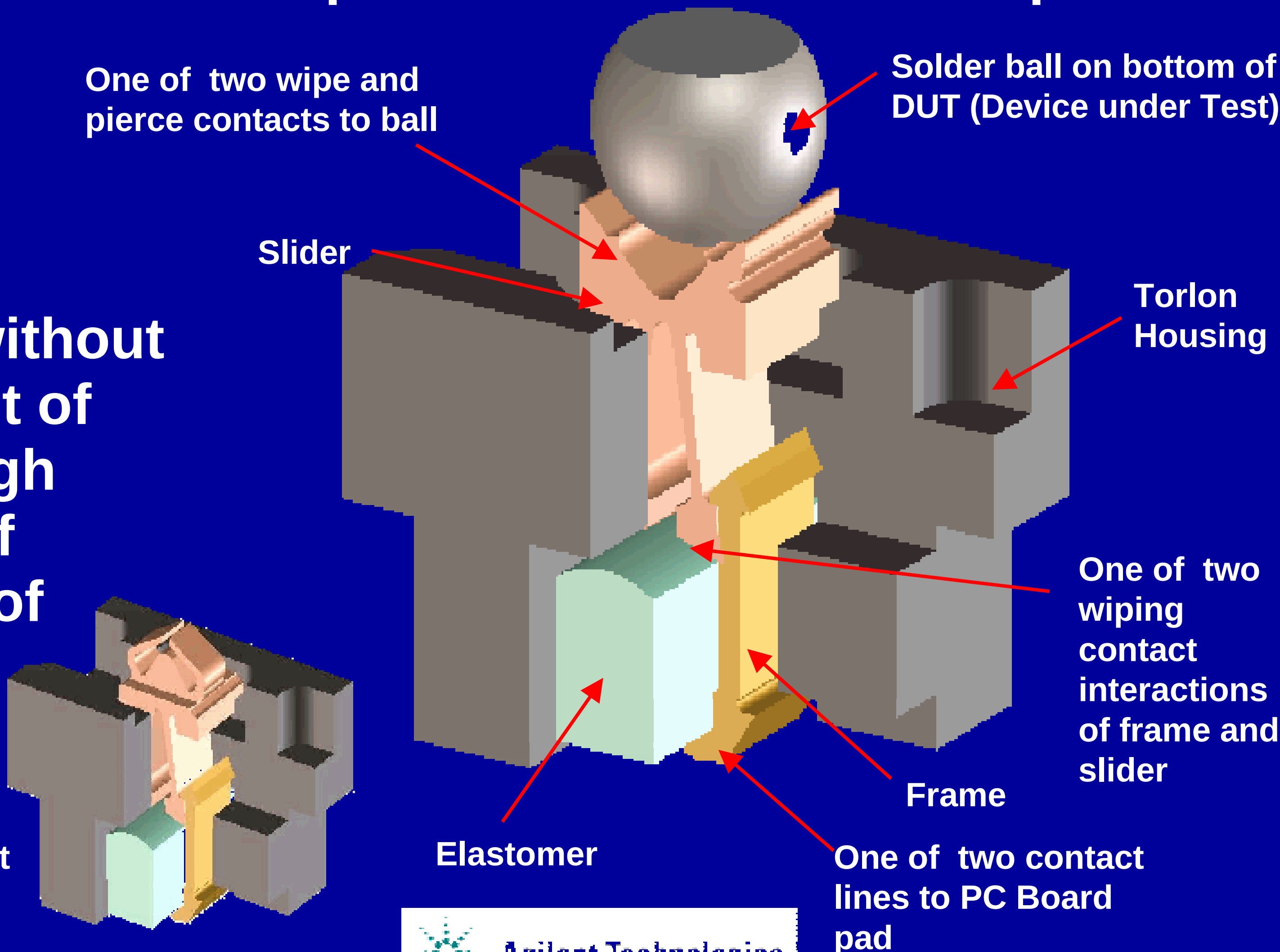
Large gaps in between contacts

Problem:

After 100,000 plunges, excessive wear requires costly and frustrating contactor component maintenance or replacement

Solution:

- **New design supports operation without replacement of parts through hundreds of thousands of cycles**



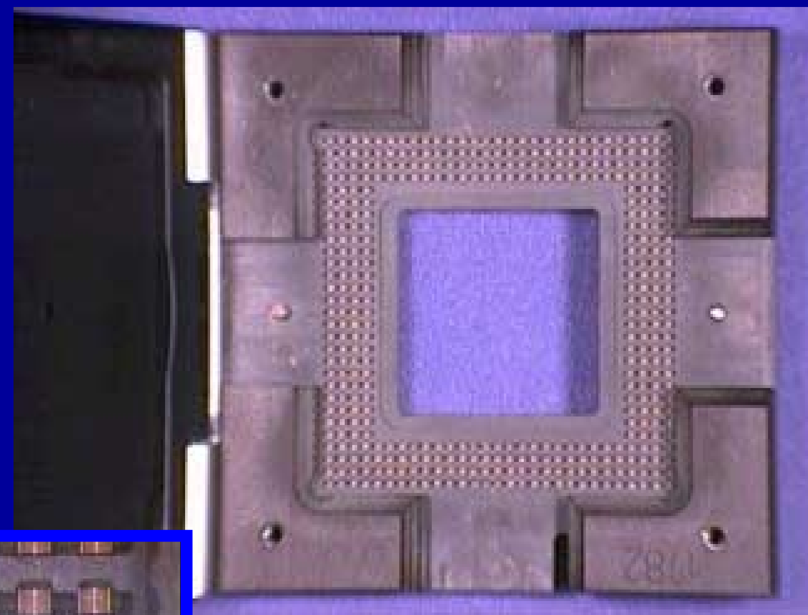
Agilent Technologies

Problem:

Life of some contactors is limited to a few tens of thousands plunges, offsetting the initial lower price

Solution:

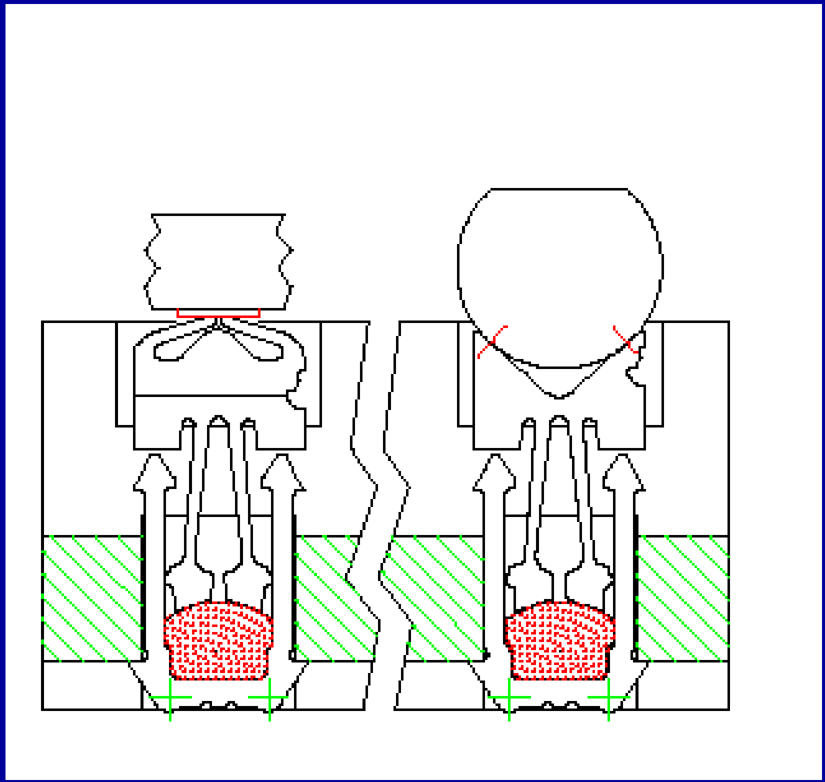
- **Typical life of a new YieldPro Array contactor is well over a million cycles**
- **Contacts can be easily replaced on site**



Problem:
Plating will wear away, oxidation may occur

Solution:

- **Metal contact components of the YieldPro Array contactors are made of solid precious and semi-precious metals**
- **No increase in contact resistance with wear**

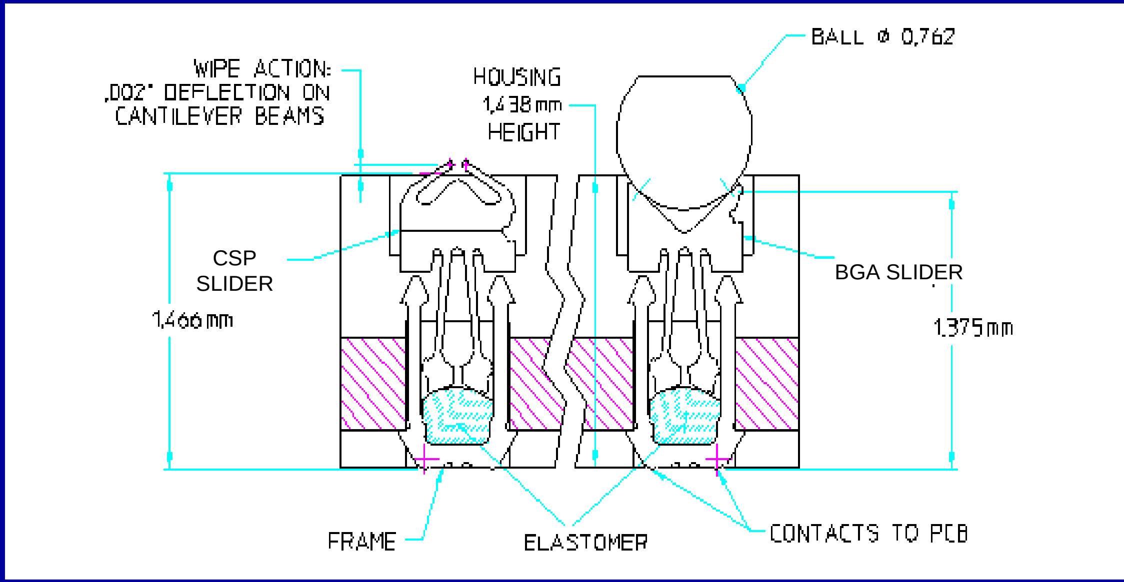


Problem:

Part handler alignment is difficult.

Solution:

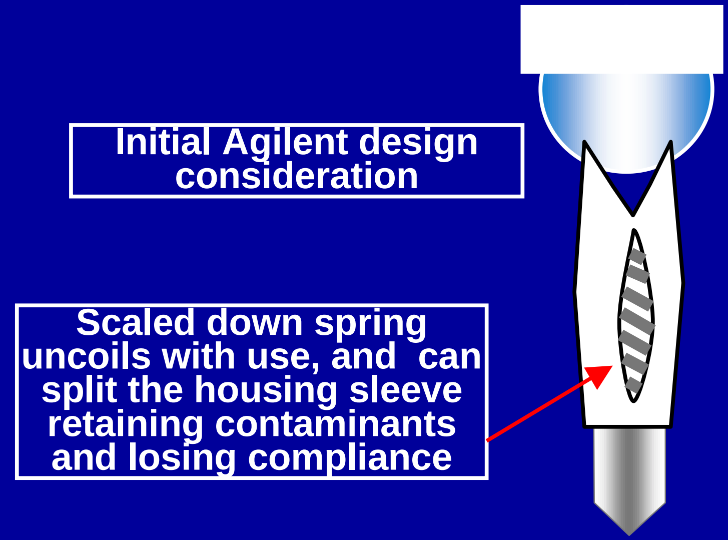
- **Generous individual independent contact compliance, up to 0.011"**
- **With the contactor attached to the DUT board, there is no force between the bottom of the housing and the DUT board. This eliminates housing distortion over time**



- **Sliders shown in fully compressed position**

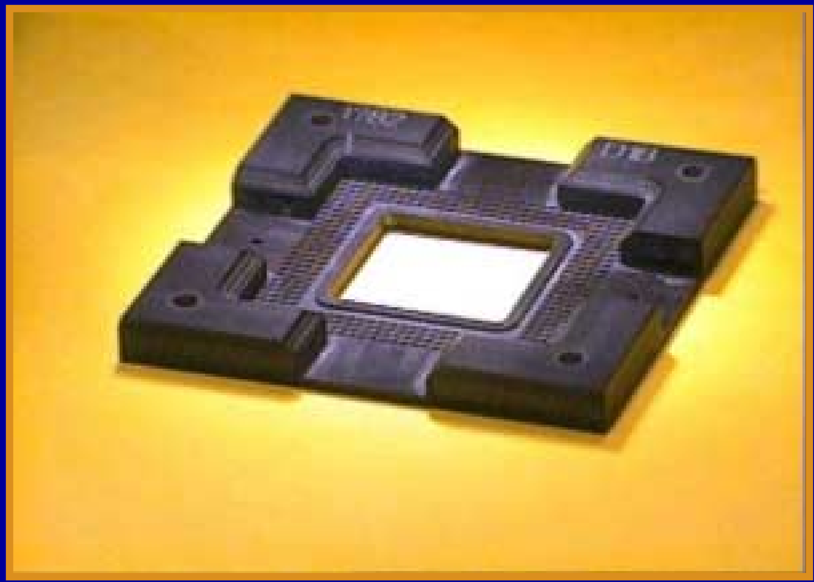
Problem:

Usability issues revolving around scaled down versions of large designs, first developed for lower frequency applications

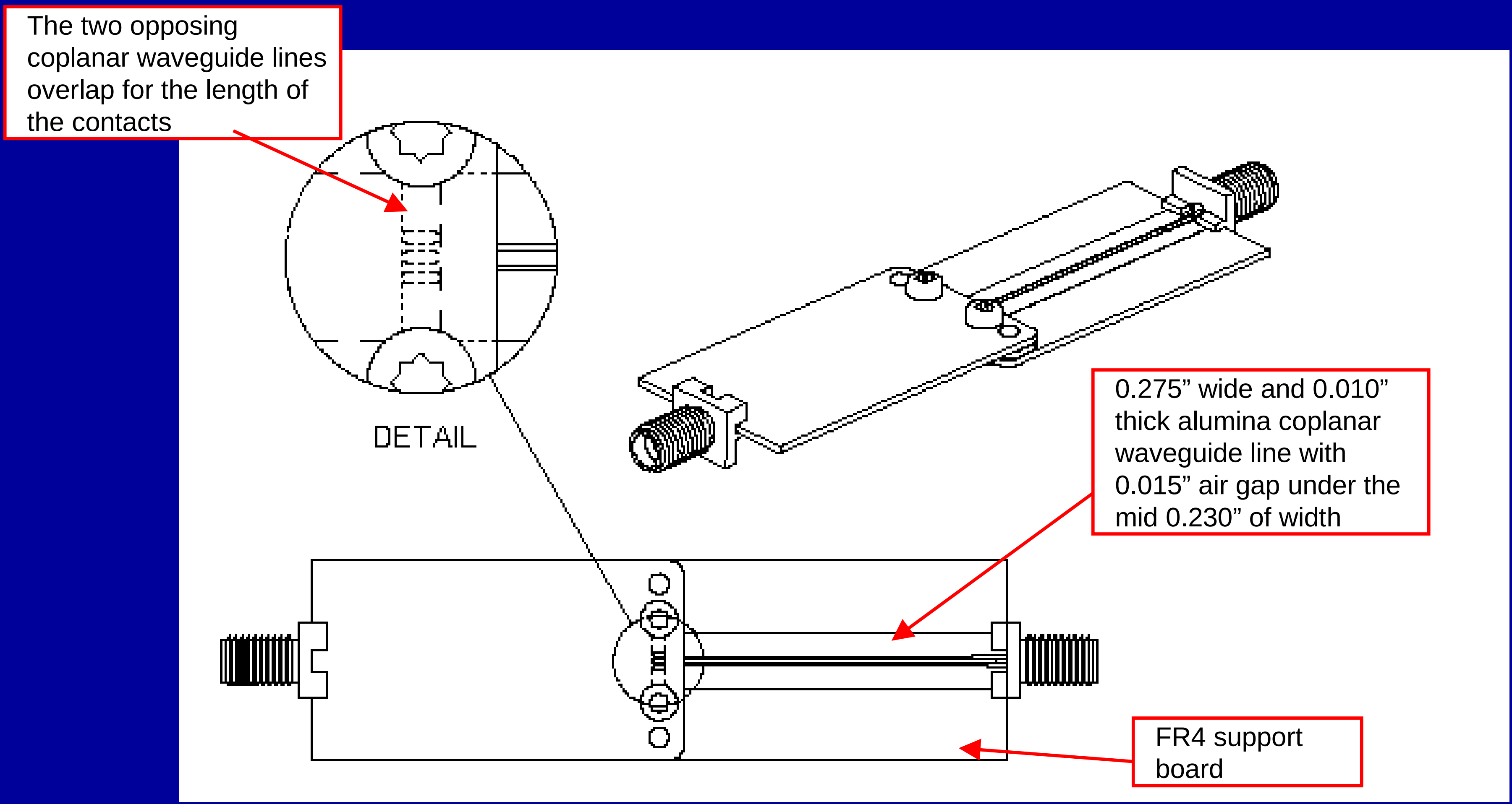


Solution:

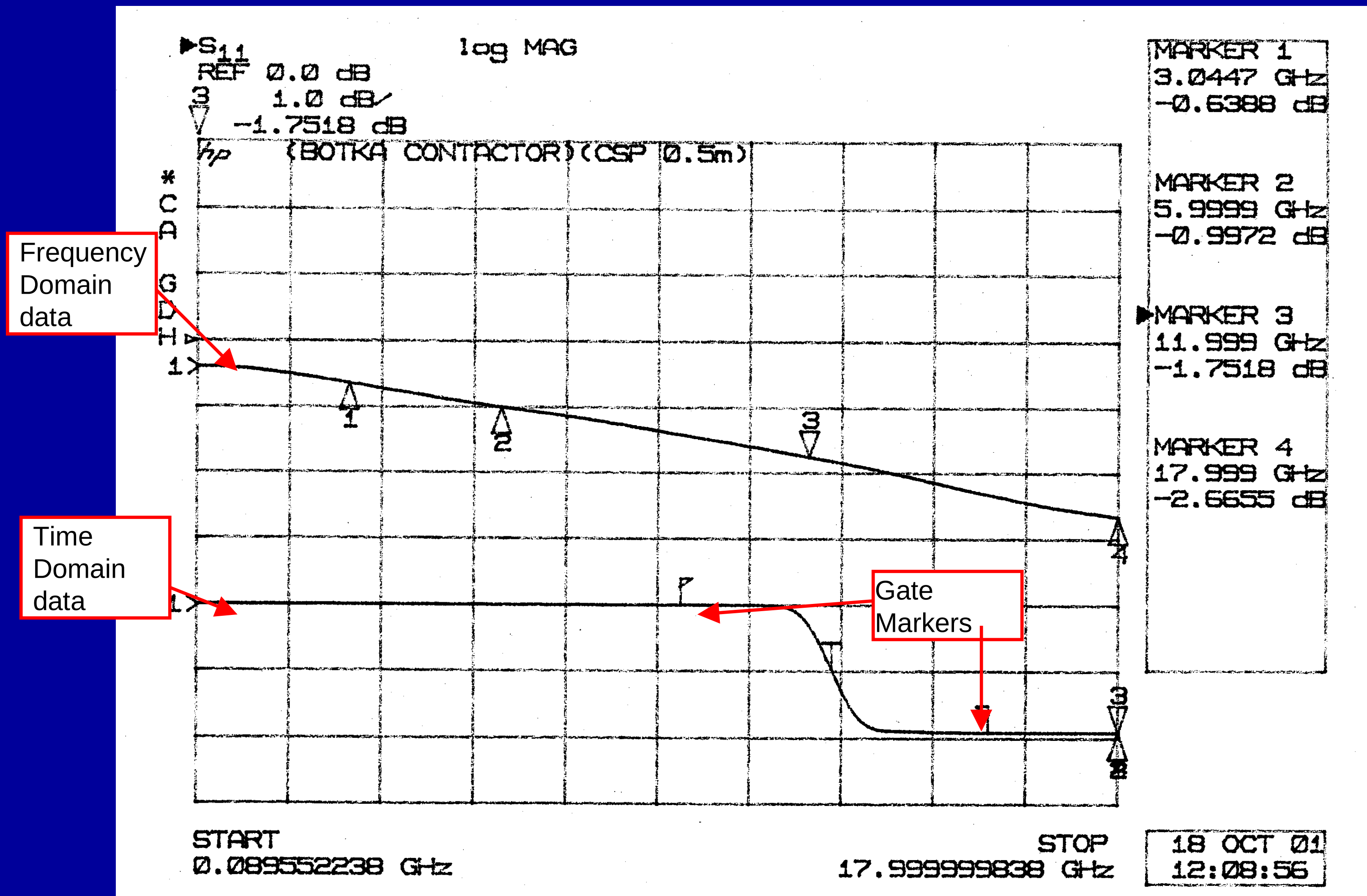
- **The YieldPro Array design concept is not subject to problems associated with scaled down designs**
- **Performs at high RF and microwave frequencies in demanding applications**



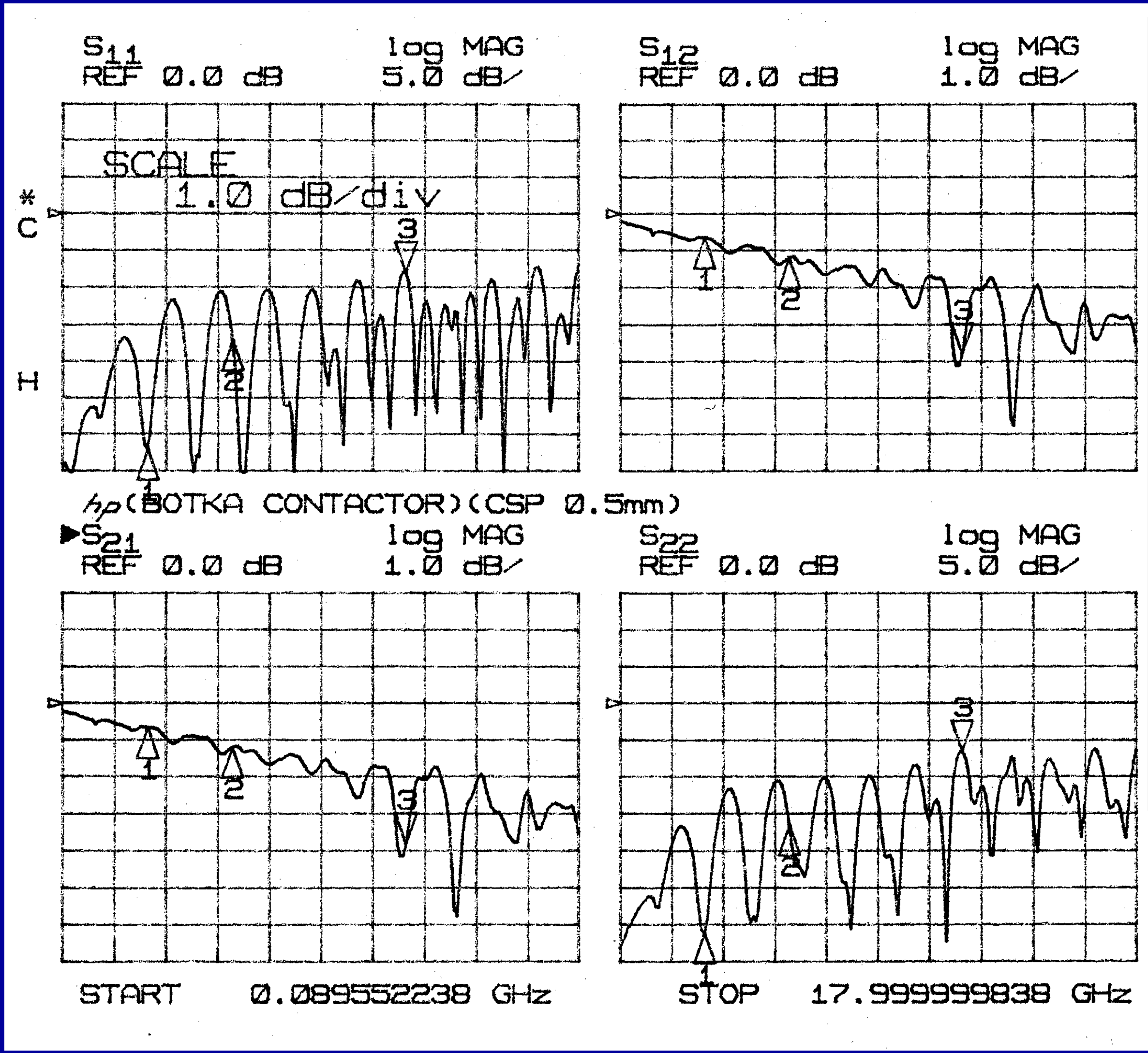
Fixture for Contactor Evaluation



Coplanar waveguide substrate with gated short at contactor plane. Measurement yields 2 x loss and dispersion. (Shift phase 180° before saving)



Fixture S-parameters measured

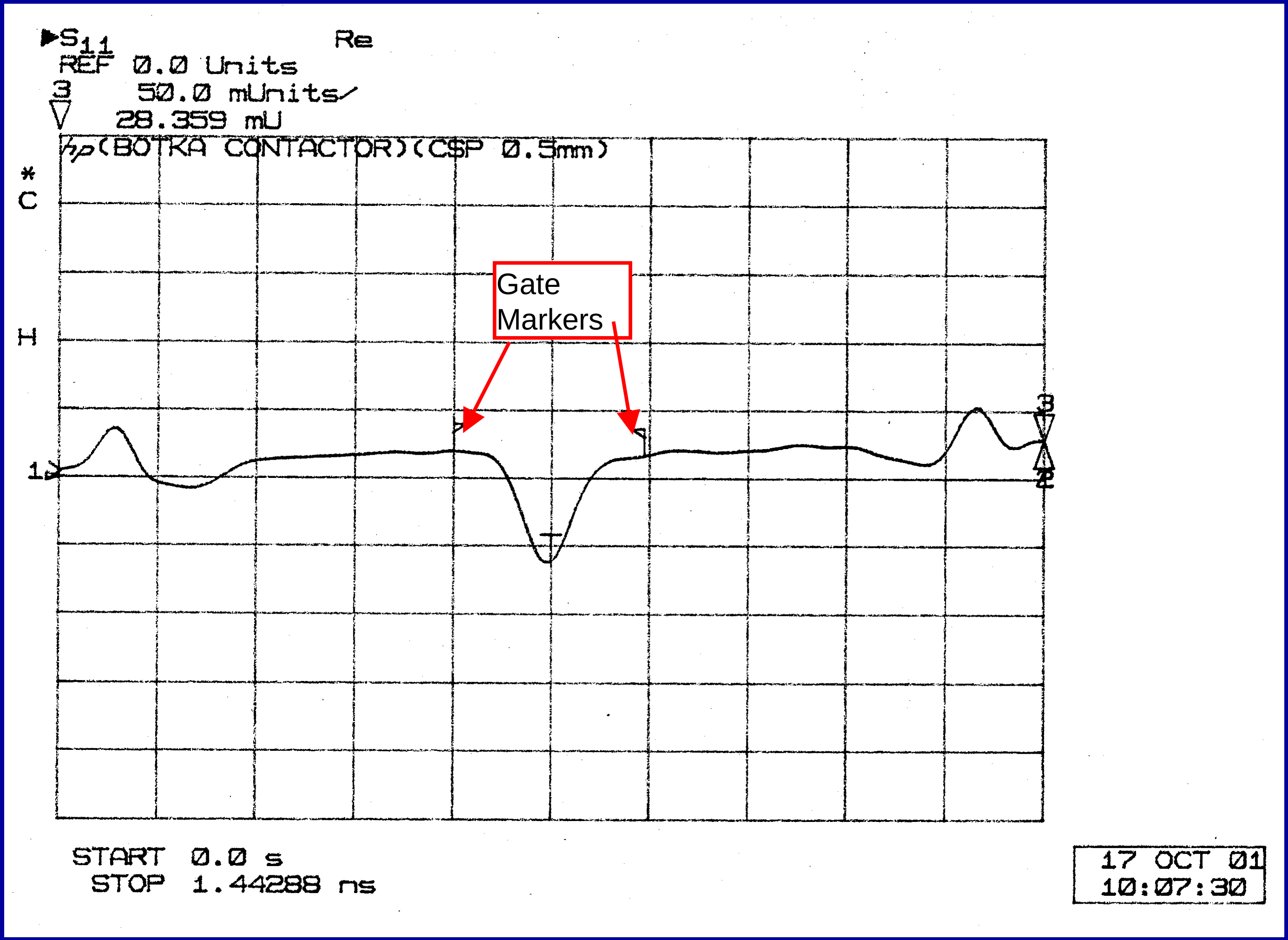


MARKER 1
3 GHz

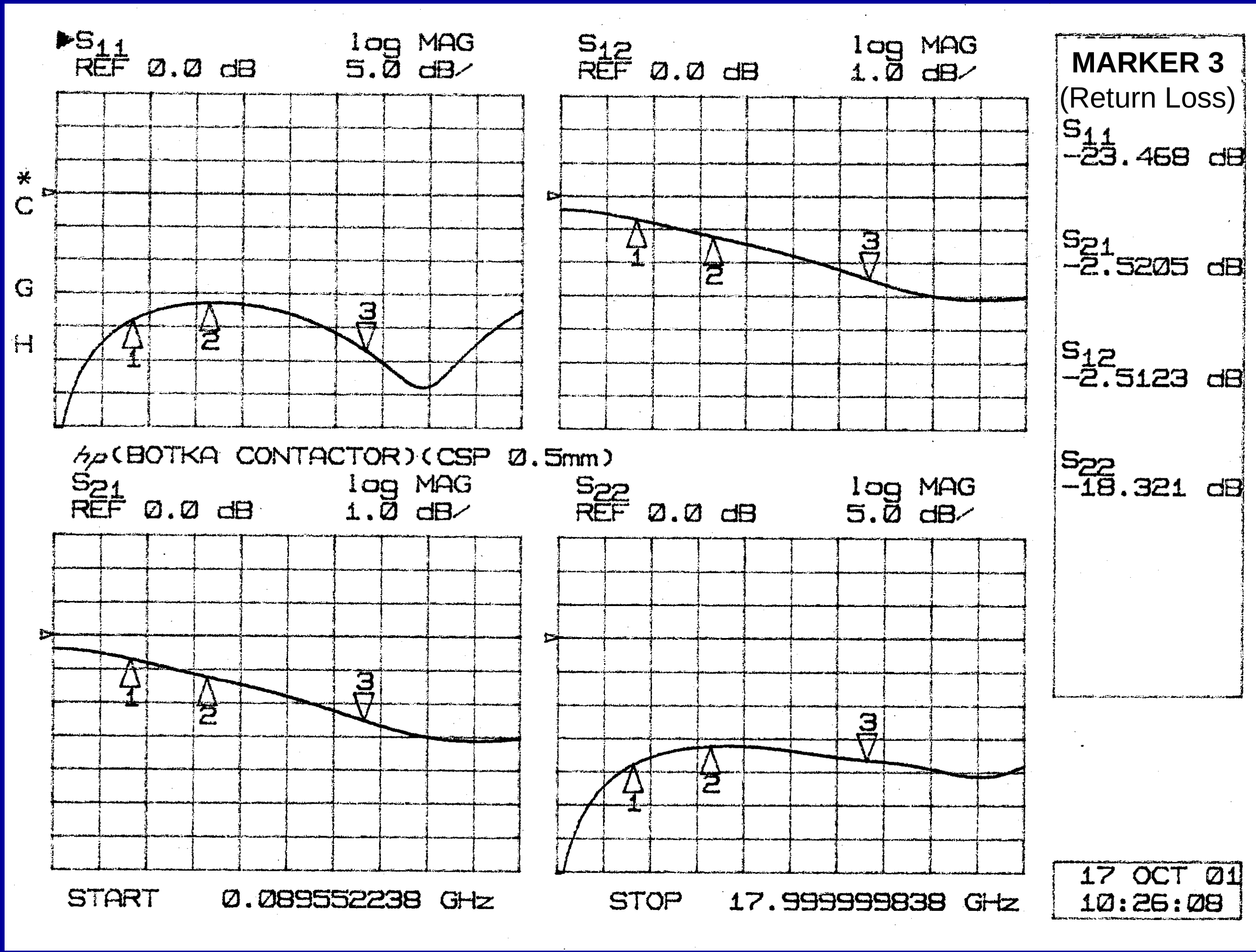
MARKER 2
6 GHz

MARKER 3
12 GHz

Fixture time domain is computed from S-Parameters Housing and contacts gated



S-Parameter of fixture with gates “on”



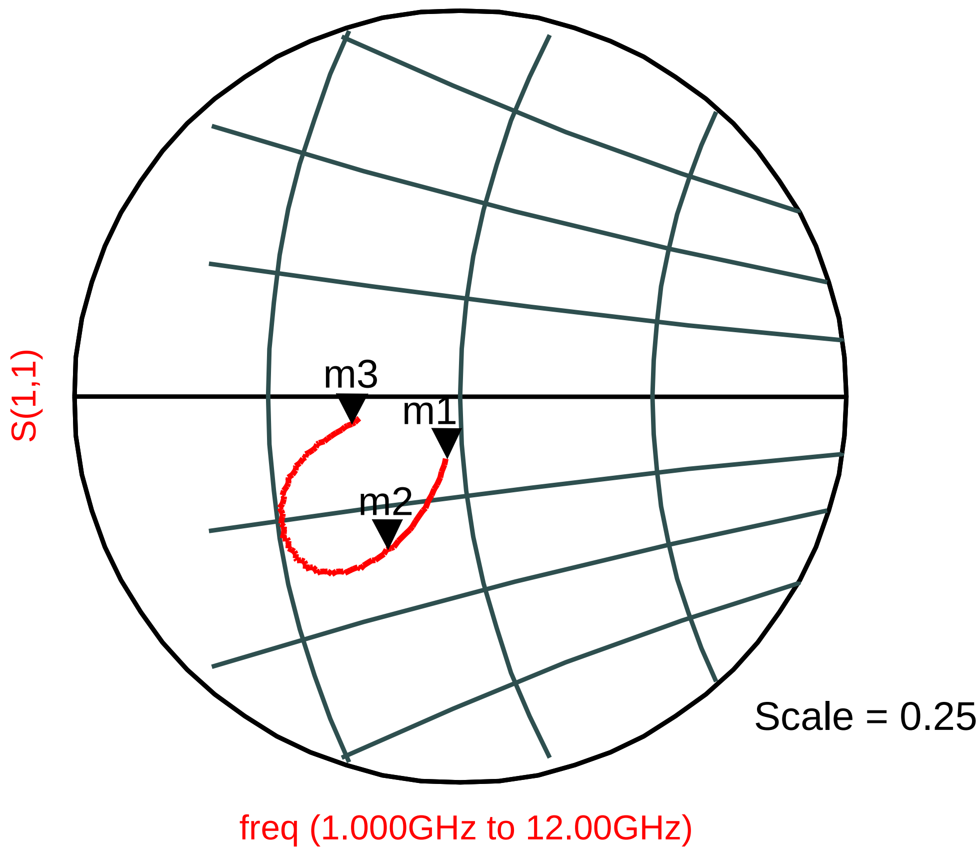
MARKER 1
3 GHz

MARKER 2
6 GHz

MARKER 3
12 GHz

S_{11} Gated, coplanar substrate electrical length is removed with port extension, no loss or dispersion correction

Port Extension = 348 ps, 104.33 mm, 125.196 degrees

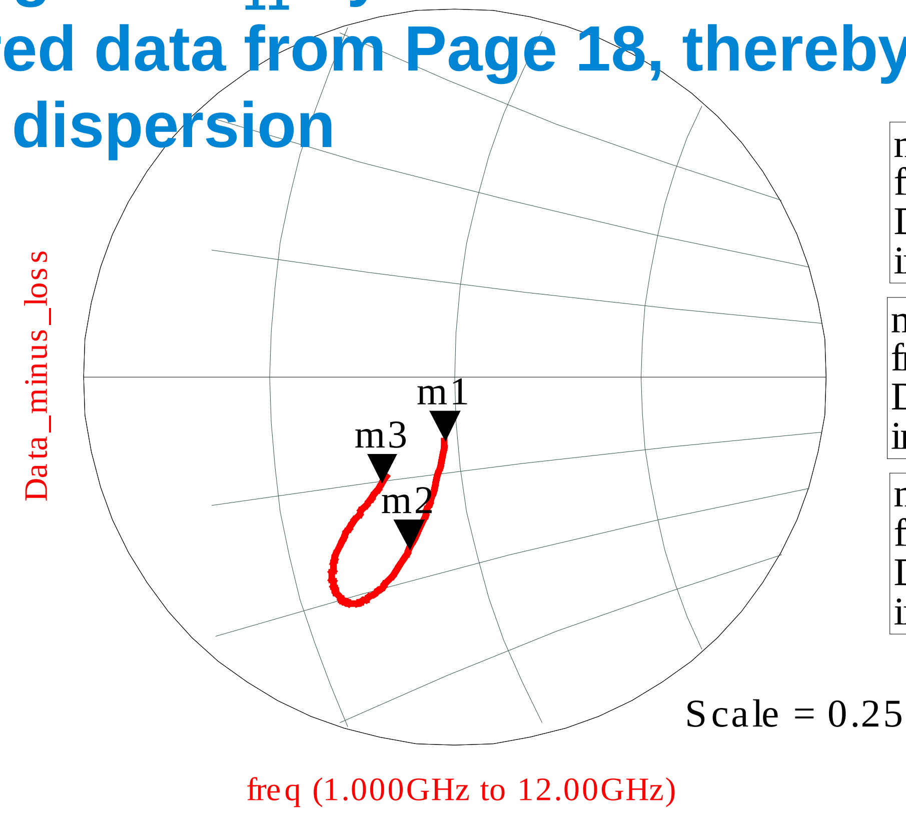


m1
freq=1.000GHz
S(1,1)=0.041 / -102.526
impedance = Z0 * (0.979 - j0.079)

m2
freq=3.090GHz
S(1,1)=0.110 / -115.386
impedance = Z0 * (0.893 - j0.180)

m3
freq=11.67GHz
S(1,1)=0.073 / -166.014
impedance = Z0 * (0.868 - j0.031)

S_{11} gated of contacts and housing with 2x loss and dispersion removed by vectorially dividing measured and gated S_{11} by stored data from Page 18, thereby correcting for loss and dispersion



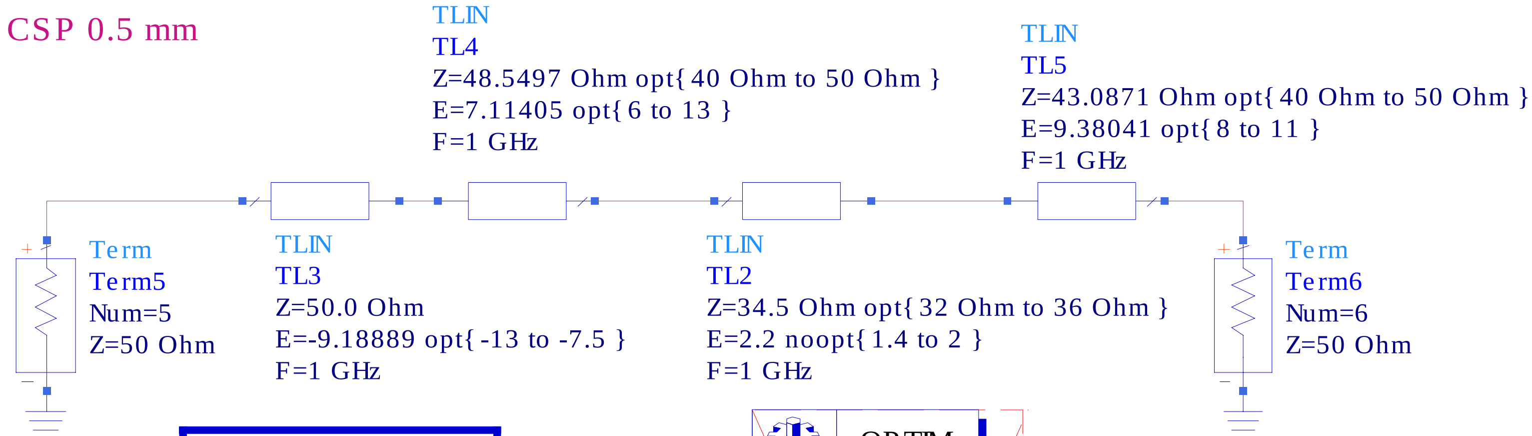
m1
freq=1.000GHz
Data_minus_loss=0.044 / -98.862
impedance = Z0 * (0.983 - j0.085)

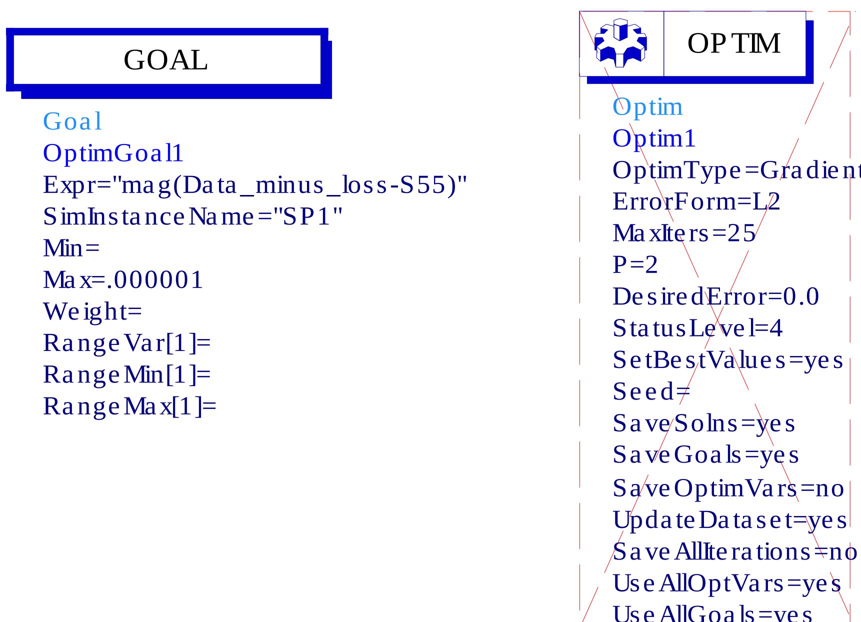
m2
freq=3.090GHz
Data_minus_loss=0.121 / -104.742
impedance = Z0 * (0.916 - j0.217)

m3
freq=11.78GHz
Data_minus_loss=0.087 / -124.213
impedance = Z0 * (0.898 - j0.130)

Use this data to generate model

Model of Contacts with Effects of Housing Overlay



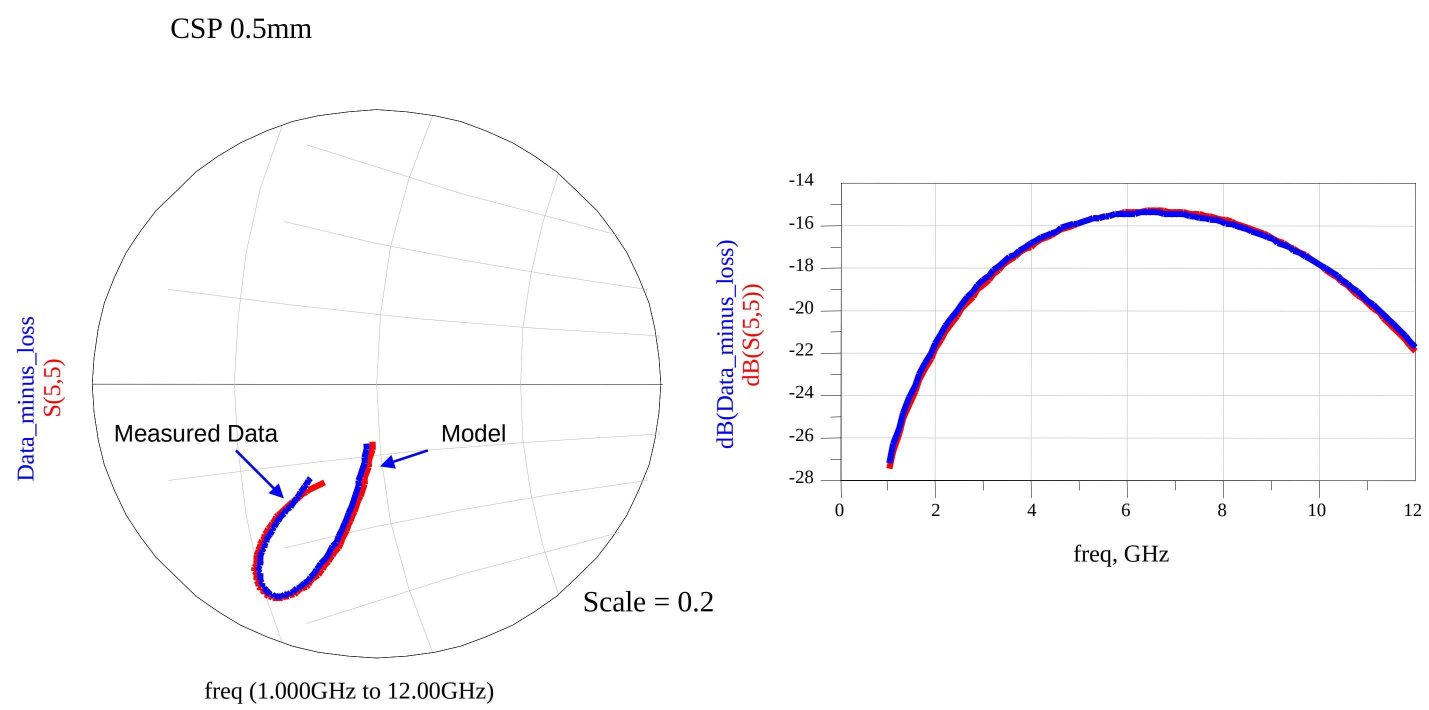


TL3: Its negative electrical length resets the phase to zero from the contacts to the edge of housing.

TL4 and TL5: Represent lower impedance of coplanar waveguide lines under housing to contacts.

TL2: Is the transmission line representing the contacts, one signal and two grounds on either side

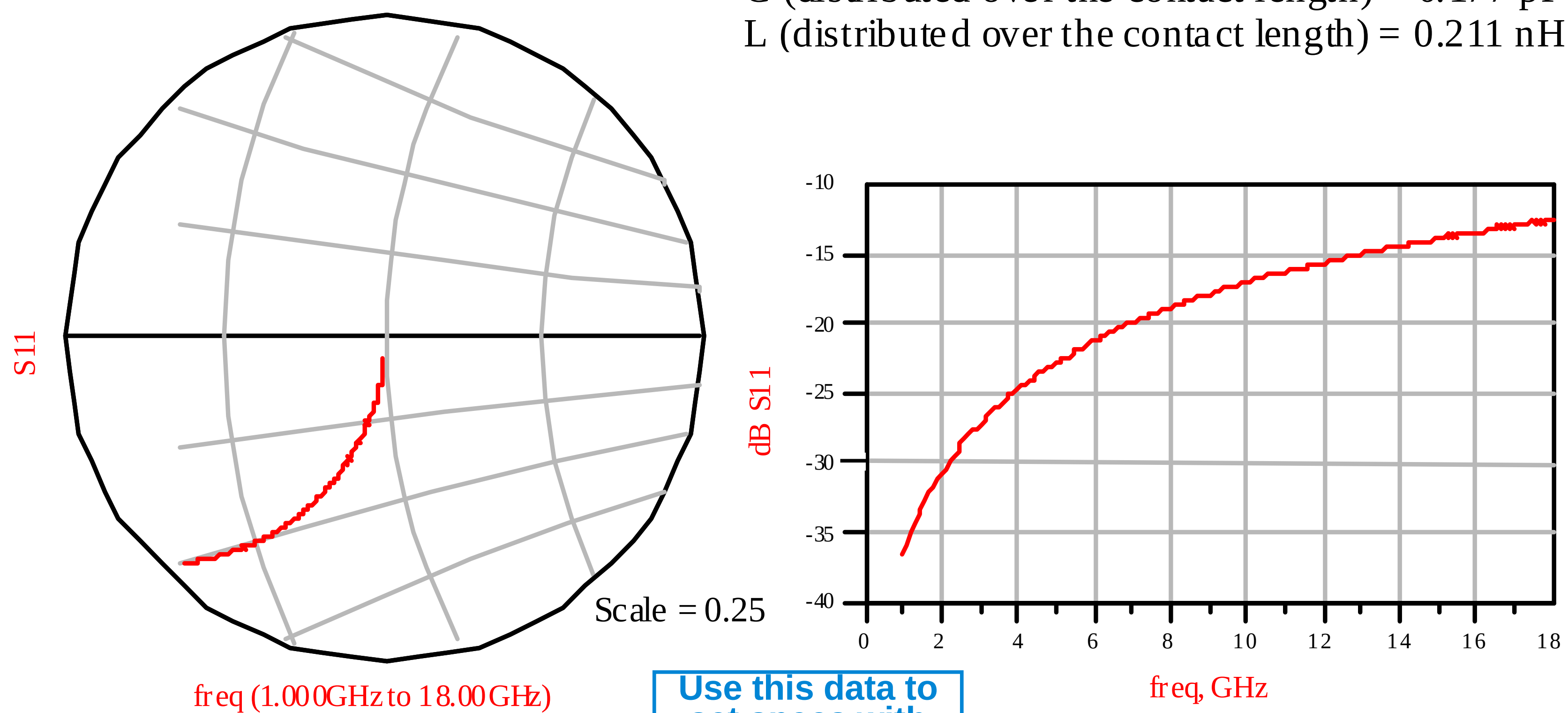
Measured S_{11} of gated housing and contacts and computed S_{11} (S_{55}) from model is shown.



S_{11} of contact region from model

CSP 0.5 mm Contactor

Z1 = 34.5 Ohms
Electrical Length @ 10 GHz = 22 degrees
C (distributed over the contact length) = 0.177 pF
L (distributed over the contact length) = 0.211 nH

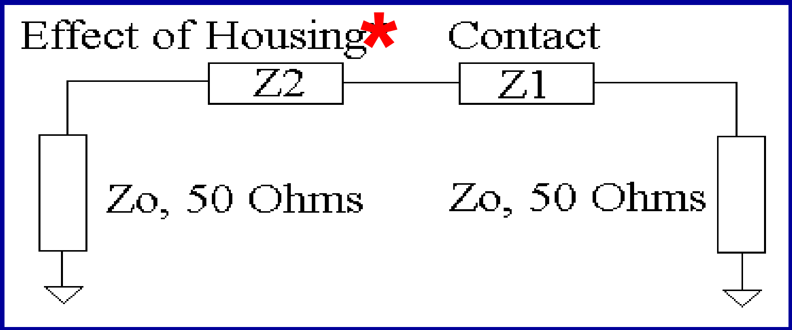


Use this data to set specs with guardband

Best DUT Board Practices at High Frequencies

- Coplanar waveguide to contactor is best transmission type, use on top surface of the board above 6 GHz
- In microstrip, minimize lengths of vias to pads under contactor
- Use blind vias, not to have the signal via extend down to or through the ground plane
- Control impedance between pads under contactor
- Compensate signal path extending below contactor housing, to achieve desired impedance/compensation for best contactor match

Accounting for housing effects



- *This transmission line represents a reduced impedance segment of the Zo transmission line due to the overlay of the housing from the edge to the contacts
- A reduction from 50 Ohms to ~ 40 Ohms was seen due to the overlay of the housing on a coplanar waveguide transmission line on the top layer of the DUT board; Less reduction is expected for microstrip lines
- The effect of the housing overlay can be mitigated by accounting for the higher effective overall permitivity under the housing material
- Adjusting the dimensions of the transmission line accordingly can maintain Zo to the contacts
- This same region’s impedance Z2 can be adjusted to values other than Zo to transform/improve the contact’s specified impedance over the desired frequency range

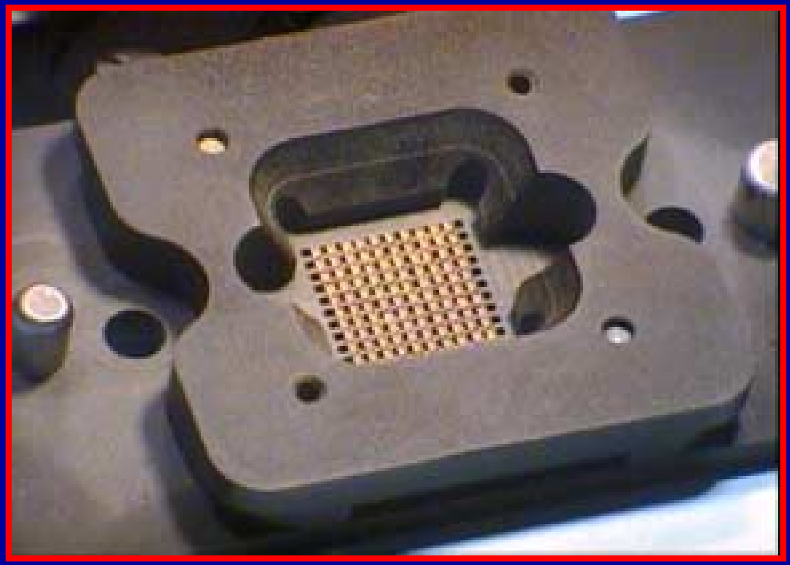
Values in this table pertain to center contact with ground contacts on two sides

Contactor Type & Pitch	Contact Pressure	Contact Width	Recommended Ball Sizes	Recommended Size Pad Min.	Contact Compliance	DC Resistance	Leakage	Return Loss 3 GHz	Return Loss 10 GHz	Return Loss 18GHz	Impedance Zo Along the Length of Contacts	Electrical Length @ 10 GHz in Degrees	Max. Current Carrying Capacity	Capacitance	Inductance	Physical Length	Effective Dielectric Constant, ε_{eef} Center Contact to Ground
For leaded packages/LCC						Note 1	Note 2	Note 3					Note 4	Note 5		Note 6	
YieldPro 1.25 mm	40 gr	0.020"			0.007"	<40m Ohm	<I nA	>21 dB	>12 dB	>8 dB	26.3 Ohm	18	3 A	0.190 pF	0.131 nH	0.927 mm / 0.0365"	2.65
Note 7	70 gr max																
YieldPro 0.8 mm	25 gr,	0.015"			0.007"	<40m Ohm	<I nA	>18.5 dB	>9.5 dB	>5.9 dB	22 Ohm	18	2 A	0.227 pF	0.11 nH	0.927 mm / 0.0365"	2.65
Note 7	40 gr max																
YieldPro 0.5mm	20 gr,	0.010"			0.007"	<40m Ohm	<I nA	>16.25 dB	>7.25 dB	>4.5 dB	17.6 Ohm	18	1 A	0.284 pF	0.088 nH	0.927 mm / 0.0365"	2.65
Note7	28 gr max																
YieldPro 0.4mm	15 gr,	0.007"			0.007"	<40m Ohm	<I nA	>18.45 dB	>9.45 dB	>6.15 dB	21 Ohm	18	0.75 A	0.238 pF	0.105 nH	0.927 mm / 0.0365"	2.65
	20 gr max																
For CSP: BGA/LGA Packages																	
YieldPro Ultra	30 gr,		0.6-0.762	0.5 x 0.5	0.011"	<40m Ohm	<I nA	>27.5 dB	>17.8 dB	>14 dB	38.5 Ohm	22	2 A	0.159 pF	0.235 nH	1.438 mm / 0.0566"	1.65
BGA/LGA 1.0mm	50 gr max		mm	mm													
YieldPro Ultra	25 gr,		0.48-0.54	0.35x0.35	0.011"	<40m Ohm	<I nA	>20.75 dB	>11.5 dB	>8 dB	28.6 Ohm	22	2 A	0.213 pF	0.175 nH	1.438 mm / 0.0566"	1.65
BGA/LGA 0.8mm	40 gr max		mm	mm													
YieldPro Ultra	20 gr,		0.3-0.42	0.2 x 0.2	0.007"	<40m Ohm	<I nA	> 24.5 dB	>15 dB	>11.2 dB	34.5 Ohm	22	1 A	0.177 pF	0.211 nH	1.438 mm / 0.0566"	1.65
BGA/LGA 0.5mm	28 gr max		mm	mm													

Note 1: Resistance measured on a clean contactor.
Note 2: Leakage current measured w ith 10V applied to signal contact.
Note 3: Assumes 50 Ohm environment.
Note 4: Apply current only after making contact.
Note 5: Capacitance and Inductance are distributed over the contact length.
Note 6: Physical length is show n fully compressed.
Note 7: Agilent YieldPro contactors for leaded/LCC packages support: SOT, SOIC, SSOP, TSSOP, MSOP, QFN, TQFP, MLF, and MLP device package requirements.

Economic Benefits:

- Increase the yield by not rejecting good parts. Smaller guard bands can be used because of less uncertainty in the measurement
- Contacts are made of precious metal and will not oxidize. Good performance is maintained due to lack of corrosion
- The longer life of the contactor reduces cost per parts tested



Agilent Technologies

Electrical and Mechanical Performance Characterization of High Frequency Test Sockets

Authors: Dr. Hanyi Ding
and Lisa Steckley,
IBM Microelectronics
Presented by: Lisa Steckley

BURN-IN & TEST SOCKET WORKSHOP

Introduction

This presentation summarizes the ongoing work at IBM to understand the factors affecting both the electrical performance and mechanical durability of several commercial RF test sockets.

Objective

- Purchase from a single source to reduce COST
- Choose best socket for specific application; PERFORMANCE
- Deliver ROBUST manufacturing solution

Socket Requirements for Testing RF Modules

- High frequency – to 12 GHz
- Low inductance
- Repeatability
- High manufacturing precision – fine pitch
- High volume test – ease of maintenance
- Heat dissipation

Socket Qualification Process

1. Determine package
2. Collect multiple socket contactor technologies
3. Test sockets mechanically
4. Test electrical continuity
5. Perform RF analyses
6. Compare with electrical simulations

Qualification Process:
Determine package

- Leadless Plastic Chip Carrier (LPCC) 20 lead-tin leads, 4x4mm, 0.5mm pitch, exposed paddle ground

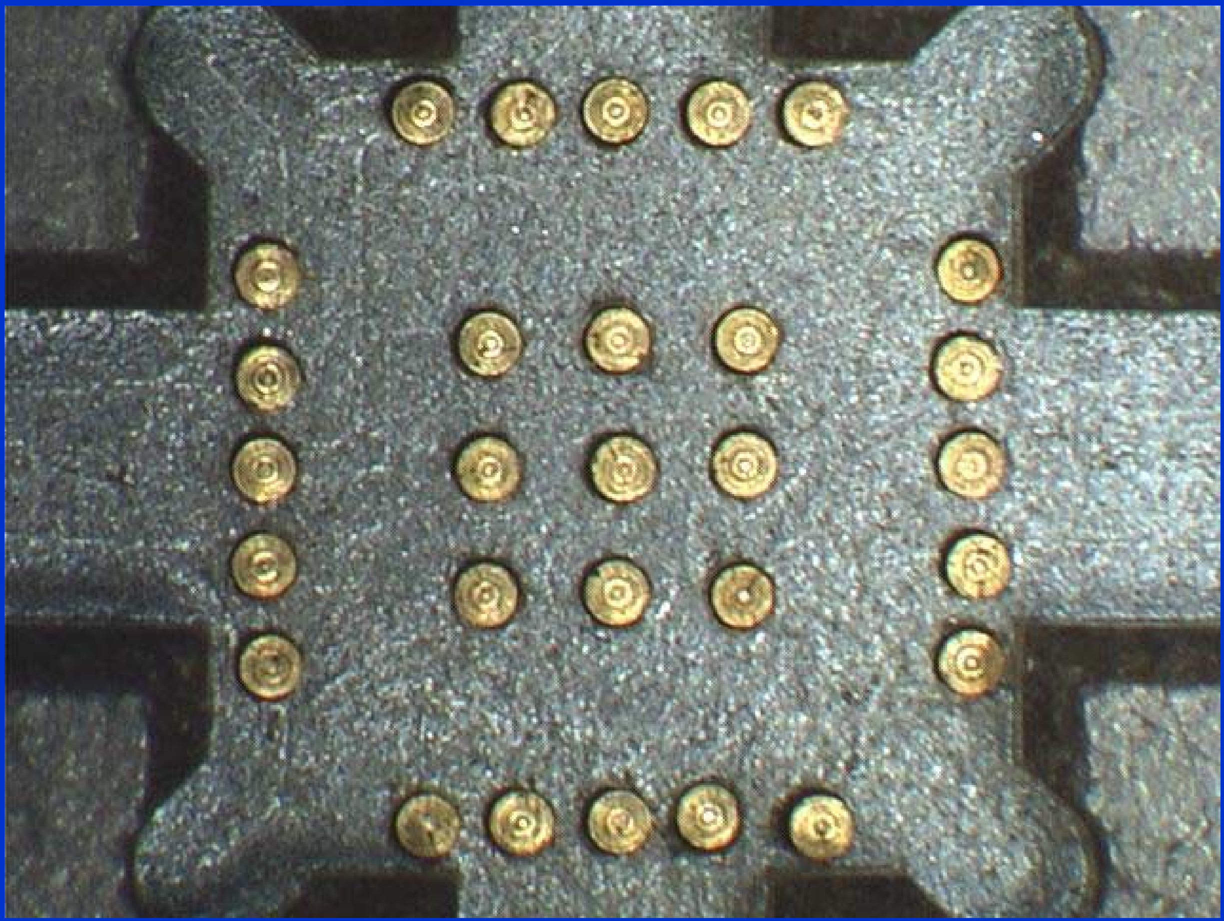
Qualification Process:
Contactor technologies studied

- Pogo-style
  - Spring loaded, gold plated, BeCu pogo, torlon housing
- S-geometry
  - Gold plated, BeCu contact, torlon and elastomer housing
- Low-profile interconnect
  - Conductive interconnect simulating plunge-to-board, torlon housing
- Conductive elastomer
  - Gold plated contact set plus conductive elastomer, torlon housing

Qualification Process:
Test Sockets Mechanically

- Build packages with shorted die
- Build board for continuity test
- Inspect packages, contacts, and board
- Cycle packages through handler, testing for DC contact
- Re-inspect for contact and board wear

Mechanical Analysis:
Pogo-style socket before test

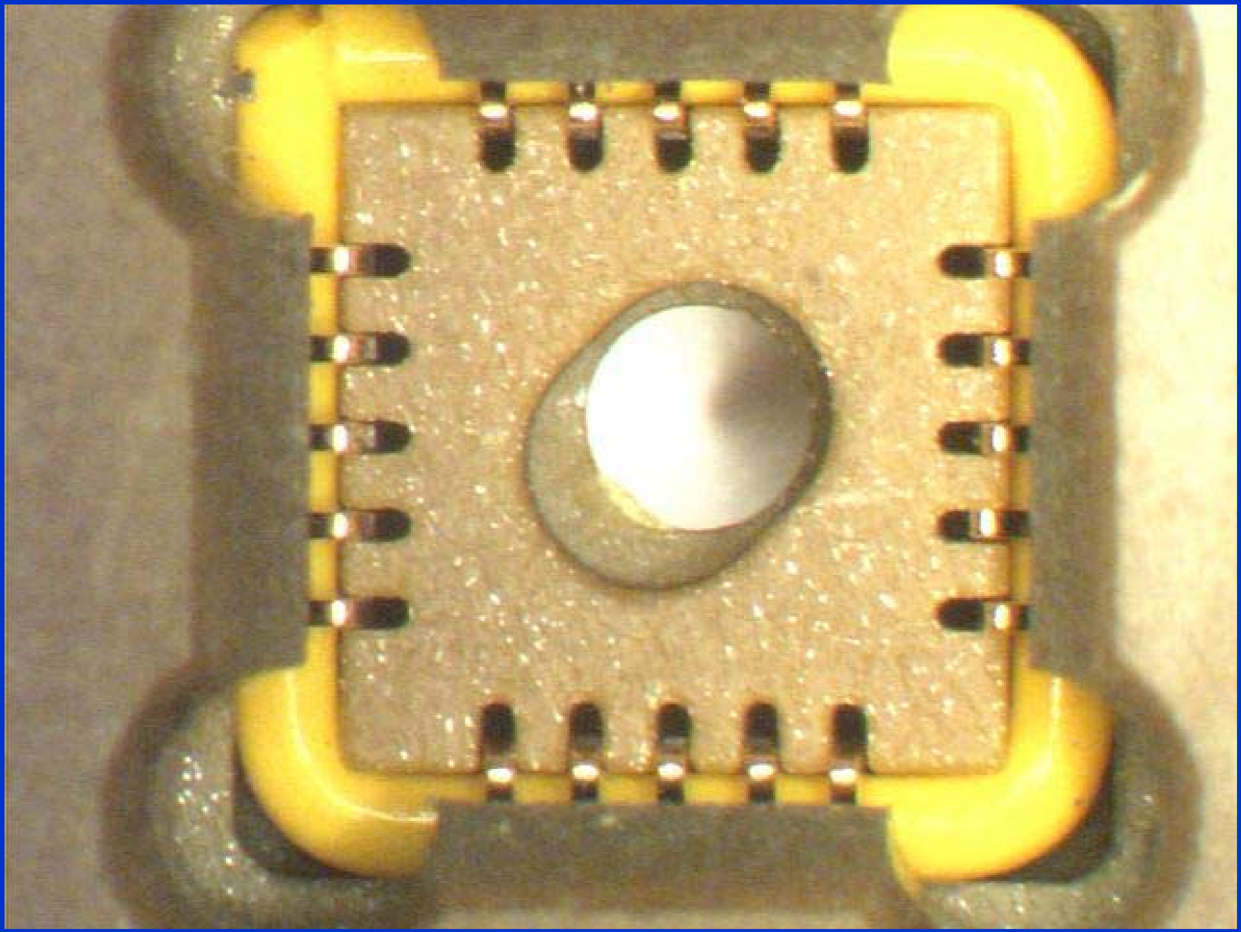


Mechanical Analysis:
Pogo-style socket after test

(picture after 5000, 10000 parts cycled)

- Lead-tin from package collects on gold pogo
- Inexpensive maintenance
- Further testing required to determine cleaning frequency

Mechanical Analysis:
S-contact socket before test

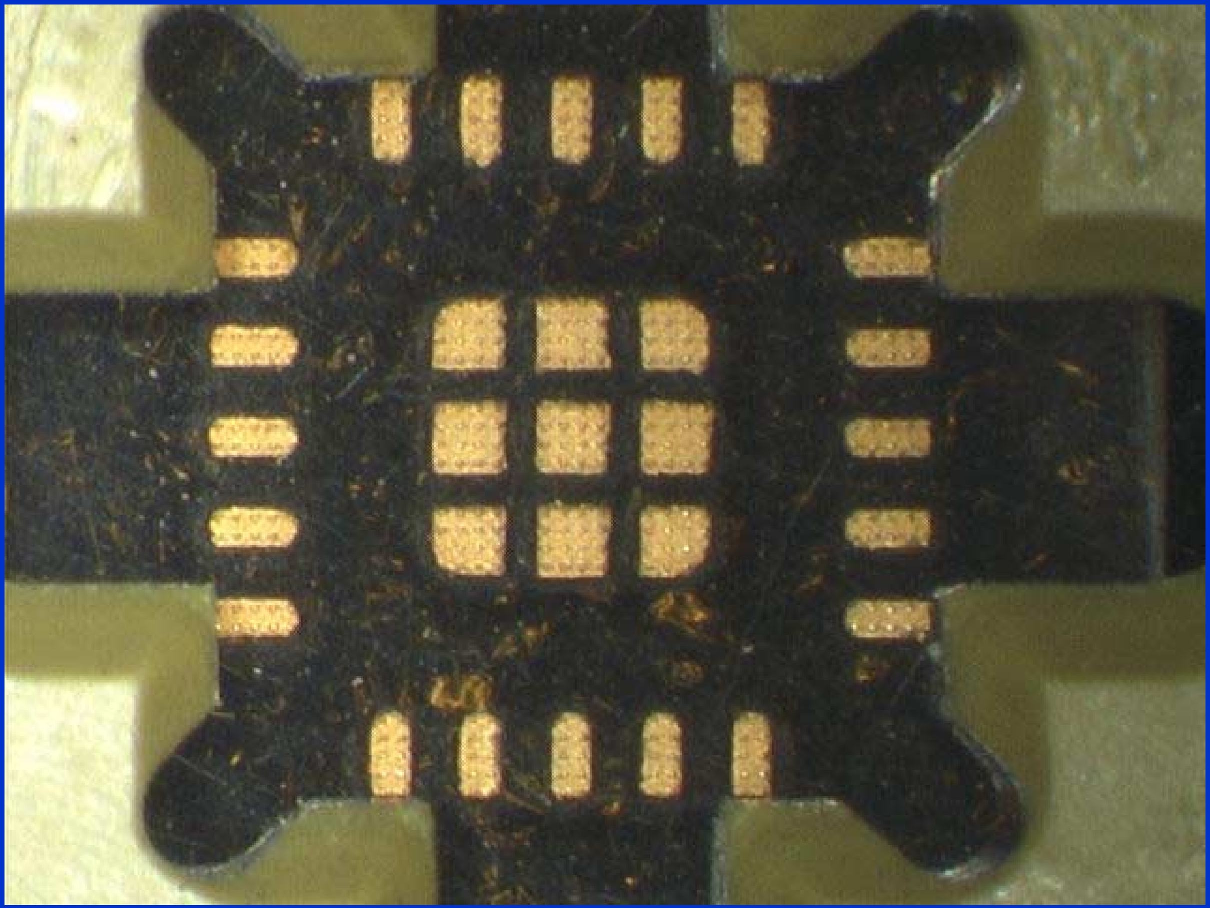


Mechanical Analysis:
S-contact socket after test

(picture after 5000, 10000 parts cycled)

- Lead-tin debris on elastomer; potential for shorting
- Little to no damage on contacts
- Inexpensive maintenance
- Further testing required to determine cleaning frequency

Mechanical Analysis:
Low-profile interconnect socket before test

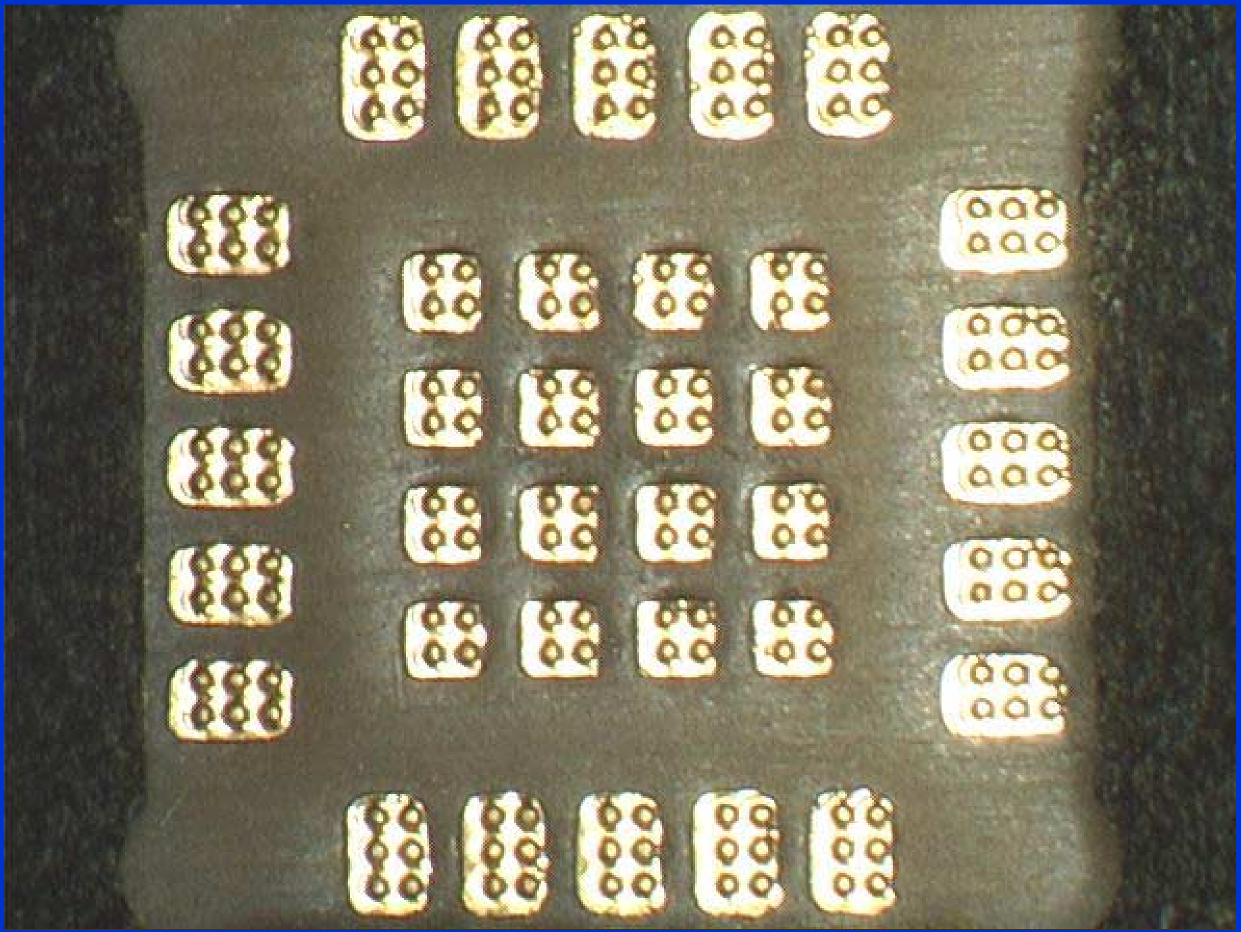


Mechanical Analysis:
Low-profile interconnect socket after test

(picture after 5000, 10000 parts cycled)

- Lead-tin debris visible
- Contact scrubbing points show little wear
- Expensive maintenance; further testing to determine mechanical life
- Further testing required to determine cleaning frequency

Mechanical Analysis:
Conductive elastomer socket before test



Mechanical Analysis:
Conductive elastomer socket after test

(picture after 5000, 10000 parts cycled)

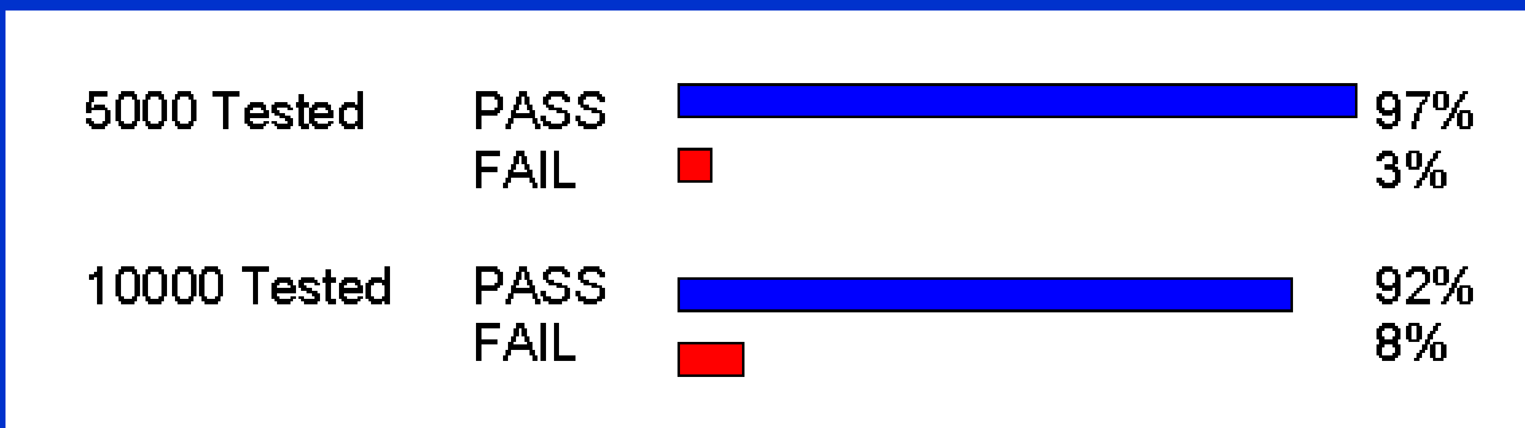
- Lead-tin collects on gold contact set
- Expensive maintenance; further testing to determine mechanical life
- Further testing required to determine cleaning frequency

Mechanical Analysis:
Board wear after test

- Pogo-style socket
  - ➢ Little wear on board; consistent witness marks
- S-contact socket
  - ➢ Evident wear from wiping action
- Low-profile interconnect socket
  - ➢ Visible wear on board; can be improved by using elastomer added for compliance
- Conductive elastomer socket
  - ➢ Little wear on board

Qualification Process:
Test socket continuity

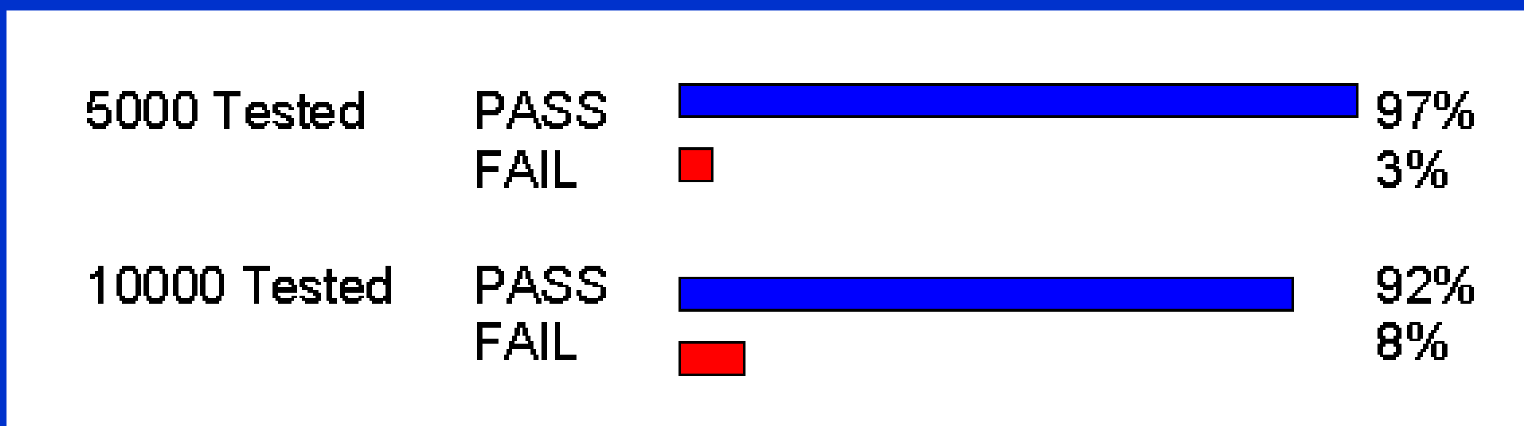
Yield using pogo socket:



Qualification Process:

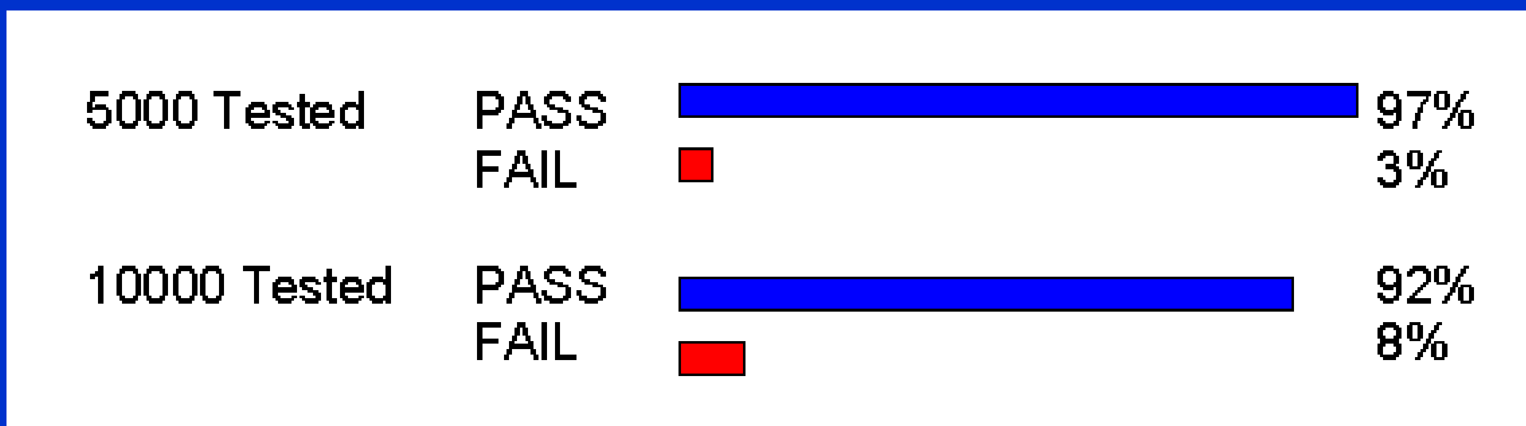
Test socket continuity

Yield using s-contact socket:



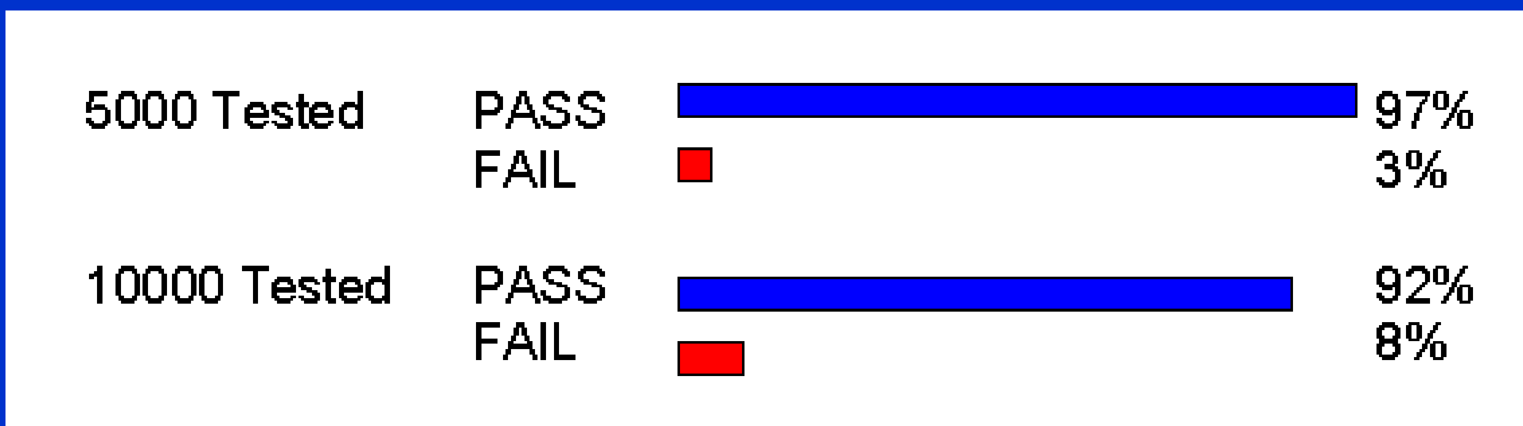
Qualification Process:
Test socket continuity

Yield using low-profile interconnect socket:



Qualification Process:
Test socket continuity

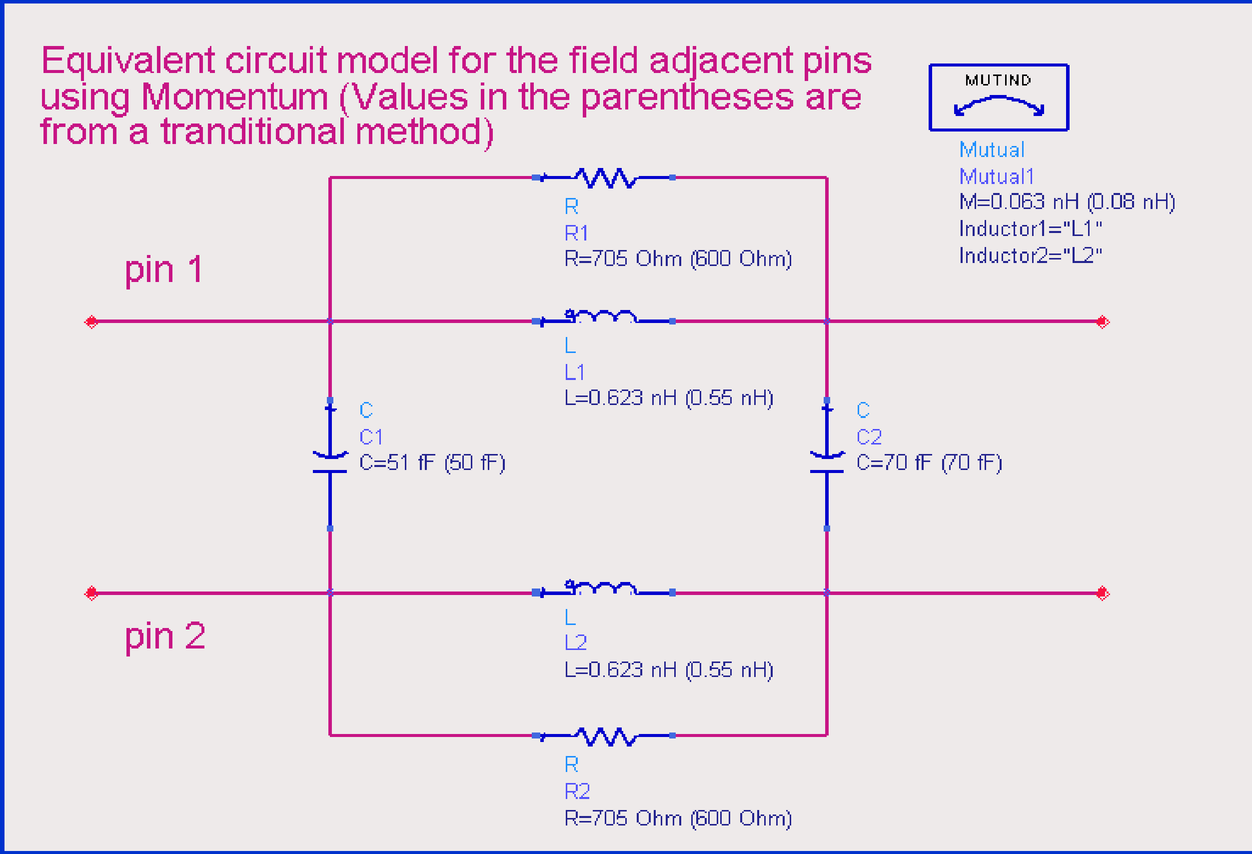
Yield using conductive elastomer socket:



Electrical Performance Simulations

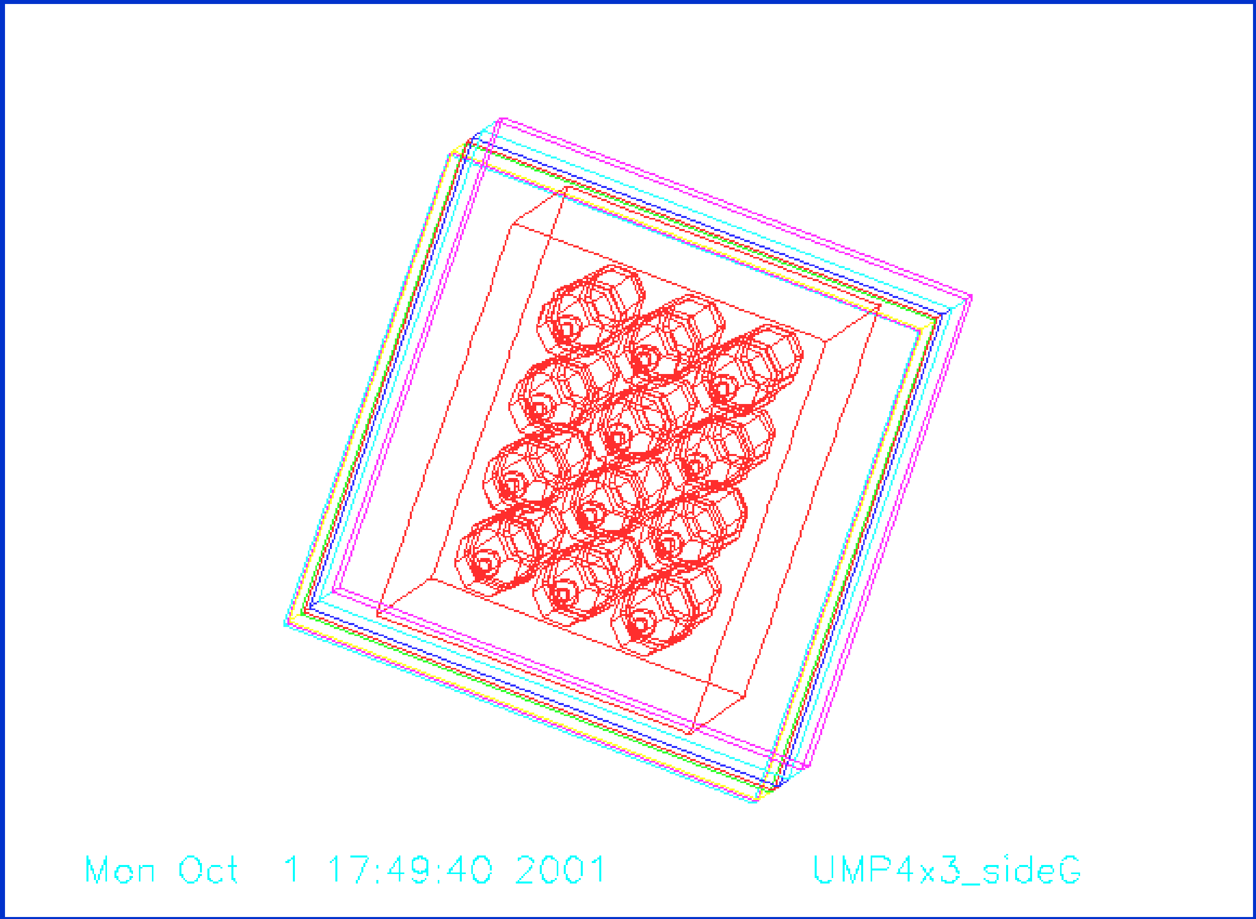
- Socket companies typically provide characterization reports based on a very simple equivalent circuit.
- Our goal is to verify the performance parameters they claim using:
  - Momentum, a 2.5D electromagnetic simulator
  - Ansoft HFSS, a 3D modeler and simulator

Electrical Performance Simulations



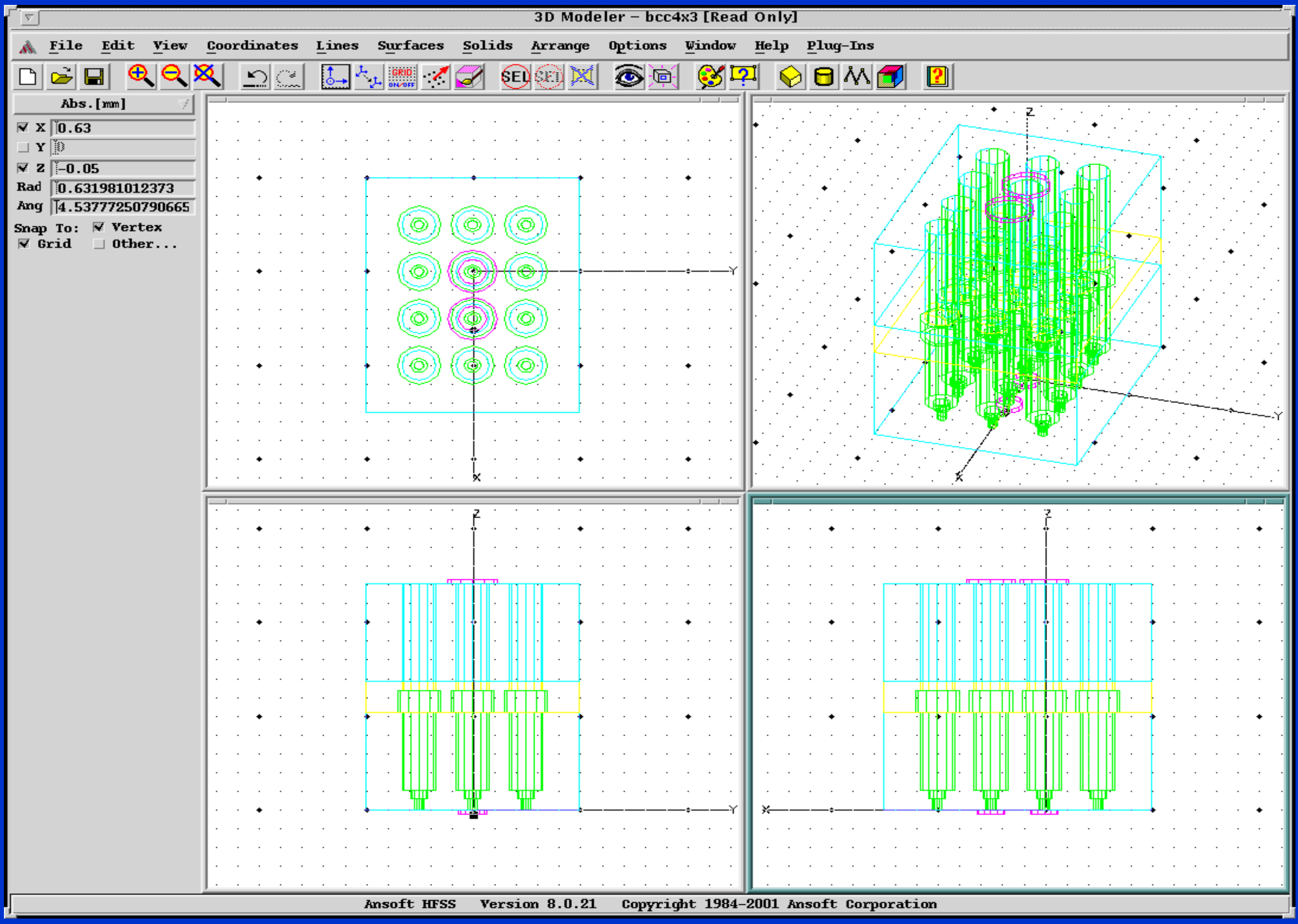
Equivalent circuit for socket pins

Electrical Performance Simulations



Structure setup for pogo pin type socket modeling using Momentum

Electrical Performance Simulations



Structure setup for pogo pin type socket modeling using HFSS

Recognition of Support

- John Blondin – IBM, Front-End-Hardware
- Ronald Clarke – IBM, Test Applications Eng.
- Dr. Hanyi Ding – IBM, RF Board Design
- John Ferrario – IBM, Manager RF Test Development
- Gene Patrick – IBM, Front-End Hardware
- Kevin Potasiewicz – IBM, RF Test Engineer
- Randy Wolf – IBM, RF Board Design