
# Burn-in & Test Socket Workshop

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**Hilton Mesa Pavilion Hotel**
**Mesa, Arizona**

**IEEE**

IEEE COMPUTER SOCIETY

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**Test Technology Technical Council**

# Technical Program

**Session 8**
**Wednesday 3/07/01 10:30AM**

## Test And Burn-in At The Wafer Level

**"Wafer Level Burn-in And Test"**
**Teresa McKenzie** - Motorola
**Walid Ballouli** - Motorola
**John Stroupe** - Stroupe Consulting

**"Some Scenarios On Wafer-Level Test & Burn-in"**
**Robert Y. Million** – Yamaichi Electronics USA, Inc.

MOTOROLA

*Semiconductor Products Sector*

# Wafer Level Burn-In and Test

## 2001 Burn-in and Test Socket Workshop

**Teresa McKenzie**, Motorola (ra5800@email.sps.mot.com)
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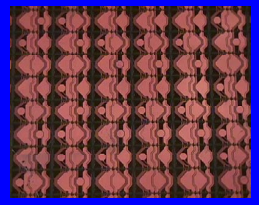
Digital DNA™ from Motorola

# Agenda / Outline

- Purpose for Developing Wafer Level Burn-in
- Overview of Wafer Level Burn-in Methodology
- Design Considerations
- Accomplishments
- Process Improvement Work
- Summary

# KGD Sacrificial Metal WLBI

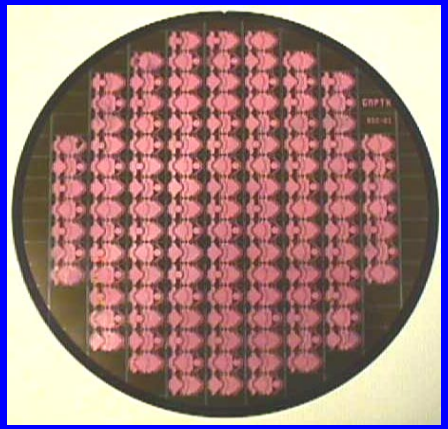
- Definition of Known Good Die (KGD)
  - Die having the same quality and reliability level as that of an equivalent packaged part.



- Definition of Sacrificial Metal (SM)
  - Metal which is temporarily deposited on a wafer to provide electrical signal paths to a die and surrounding die during wafer level burn-in and test. The sacrificial metal is etched away after burn-in and test is complete.

# KGD Sacrificial Metal WLBI

- Definition of Wafer Level Burn-In (WLBI)
  - Simultaneous burn-in of all die on a wafer to screen out marginal devices for infant mortality by dynamically stressing the integrated circuit at elevated temperature and voltage.



# Purpose For Developing Wafer Level Burn-In

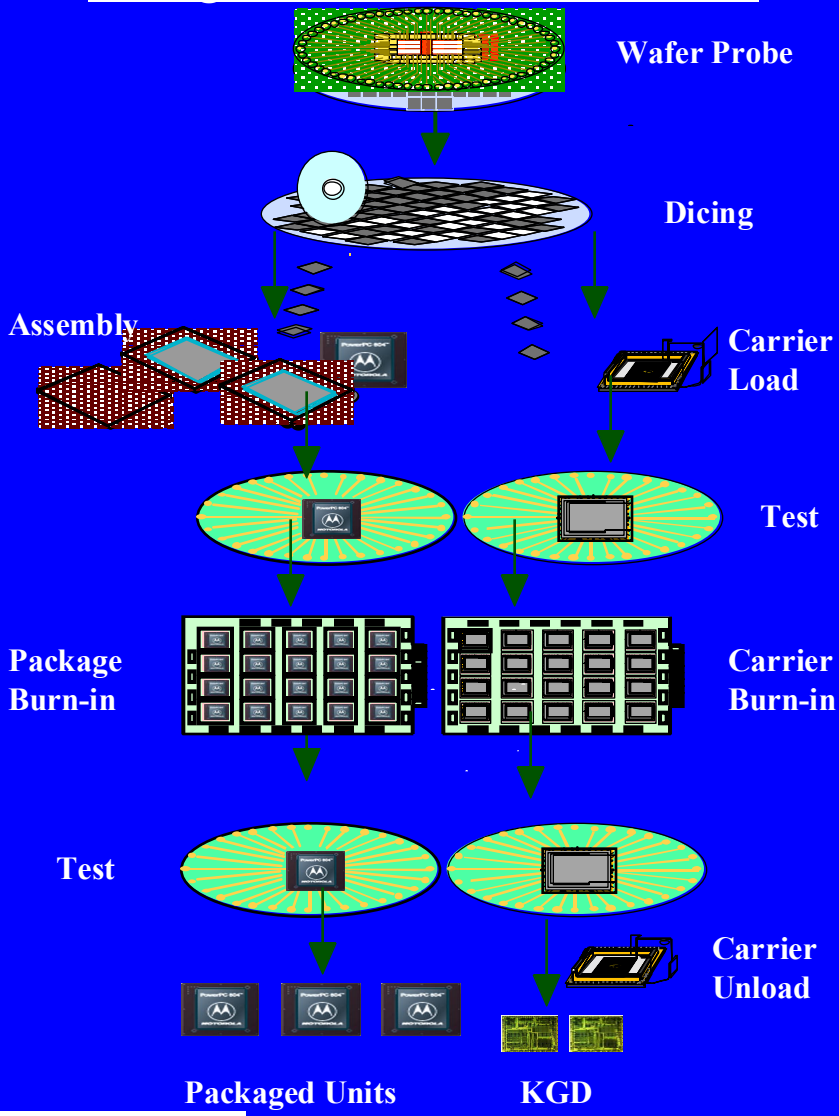
- Industry Requirements
  - Packaging miniaturization technology driving need for Known Good Die (KGD).
  - Use of flip chips in multi-chip modules (MCM), direct chip attach (DCA), and chip-on-board (COB).

# Purpose For Developing Wafer Level Burn-In

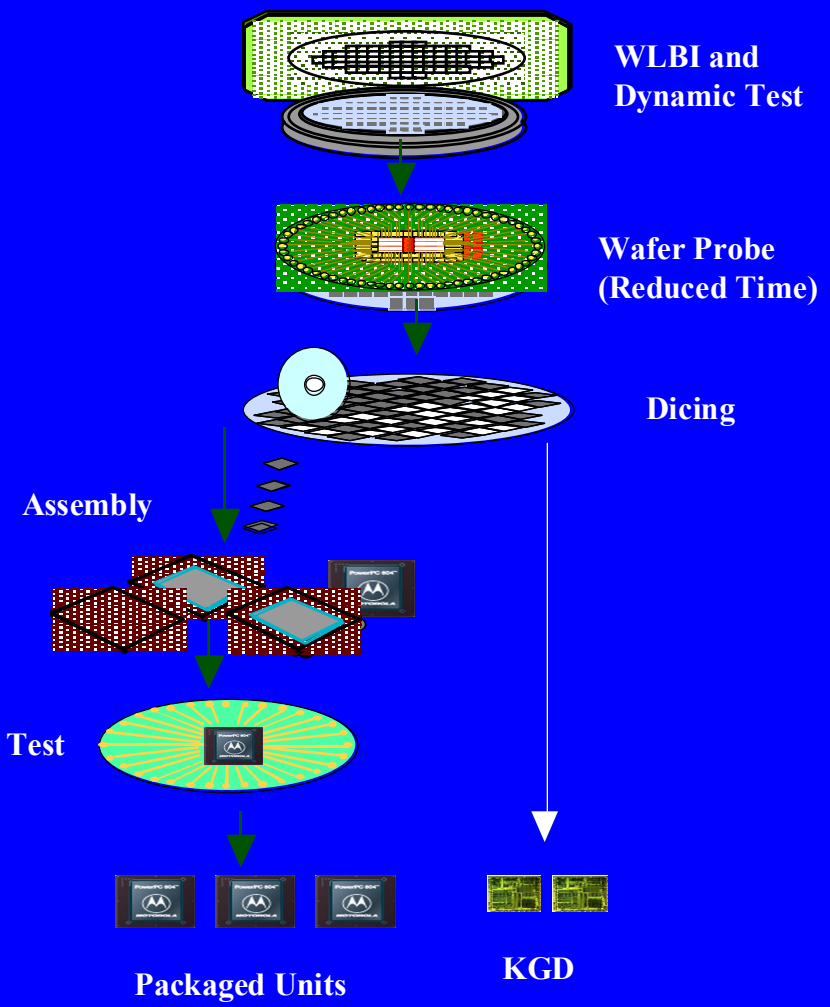
- WLBI Known Good Die (KGD) Benefits
  - Lower cost method than die level burn-in.
  - Use of KGD flip chips in multi-chip modules (MCM), direct chip attach (DCA), and chip-on-board (COB).
  - Reduction in process steps when compared to packaged-level and die-level burn-in.
  - Reduction of wafer test insertion and probe time.
  - Faster test result feedback to the fab.

# Wafer Level Burn-in Methodology

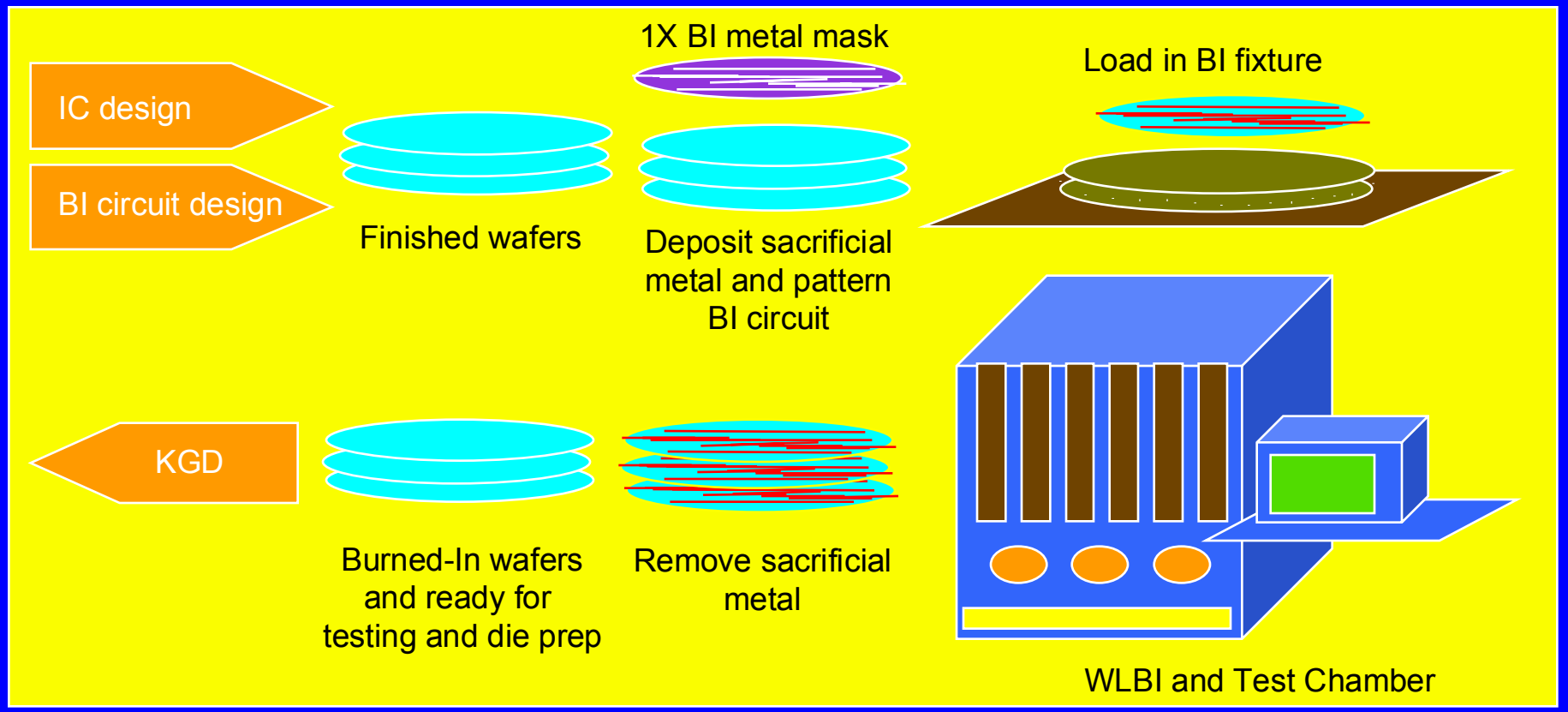
## Package Burn-in / Die-Level Burn-in




## Sacrificial Metal Wafer Level Burn-in



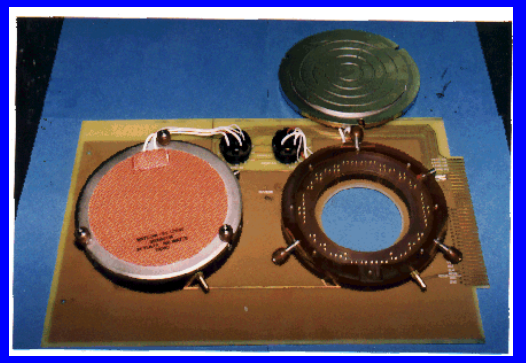
# Wafer Level Burn-in Methodology



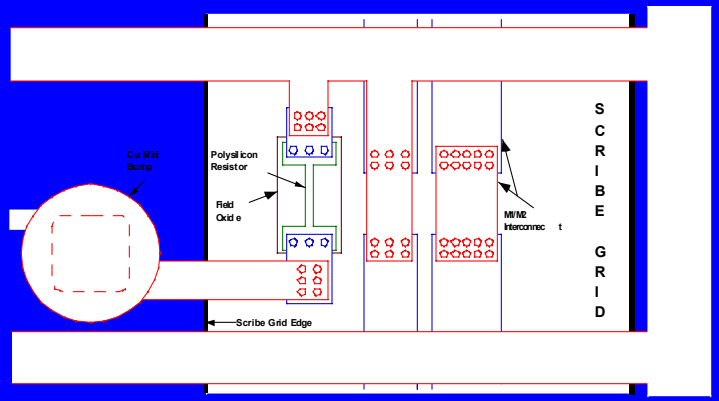
# 5 inch Wafer Level Burn-In Methodology

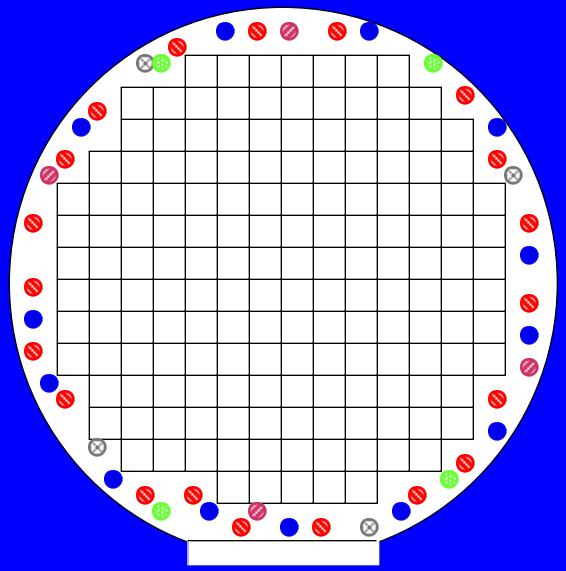
Post wafer fab process (with polyimide)

- Deposit, pattern and etch sacrificial metal
  - Parallel electrical bussing of all die per quadrant
  - Photo define burn in contact pads
  - Contact current limiting resistors
  - Contact scribe grid cross-unders
- Burn-In and Data Retention Bake (DRB) test
- Remove sacrificial metal
- Die sales, bump or package



# 5 inch Wafer Level Burn-In Methodology



VSS

VDD

RECEIVE

RESET

CLOCK

Digital DNA™ from Motorola

# 5 inch Wafer Level Burn-In Systems

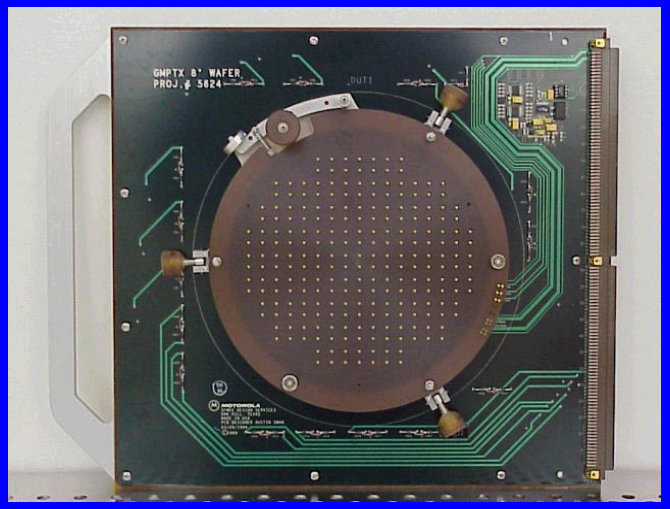
First Prototype

Current Production

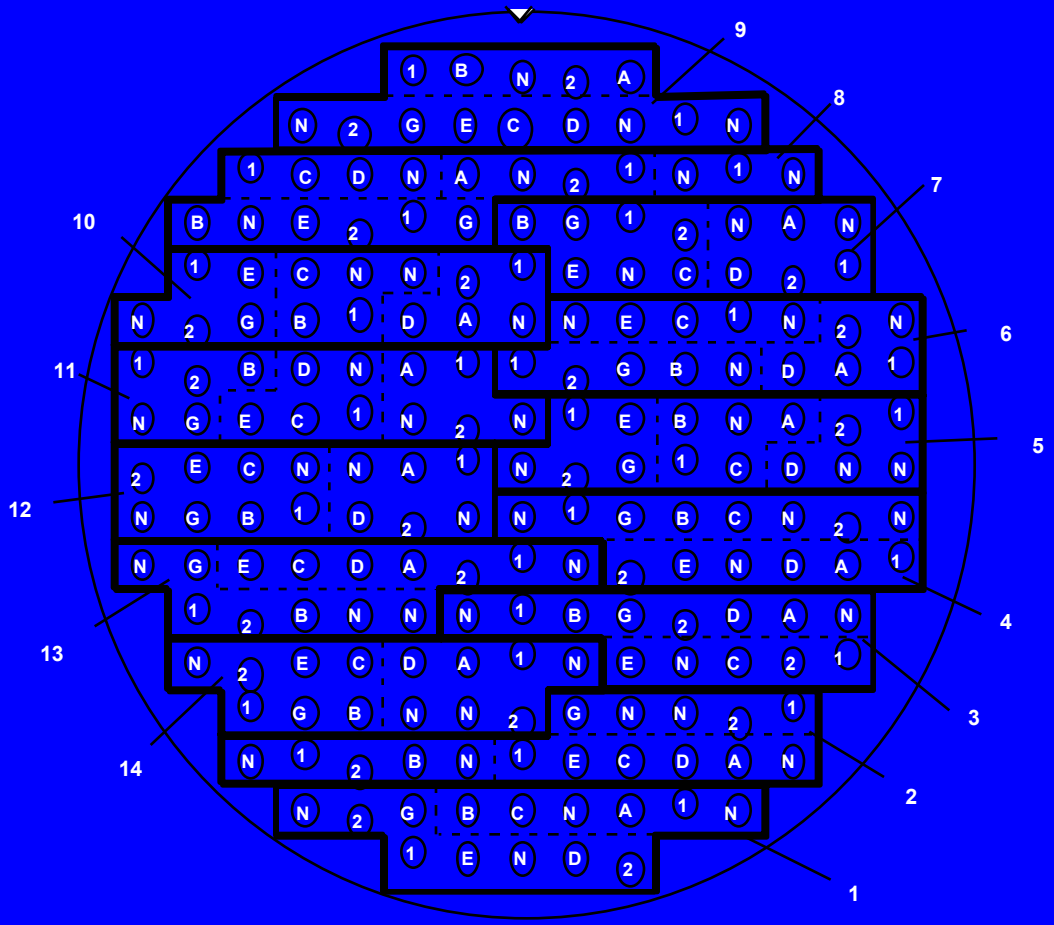
# 8 inch WLBI Methodology

Post wafer fab process (with polyimide)

- Deposit, pattern and etch sacrificial metal
  - Parallel electrical bussing of all die in a cluster
- Wafer level burn in (24 hours @ 125 °C)
- Data Retention Bake (24 hours @ 270 °C)
- Remove sacrificial metal
- Bump (flip chip only)
- Wafer probe
- Visual, dice and T&R
- Ship to customer



# 8” WLBI Methodology

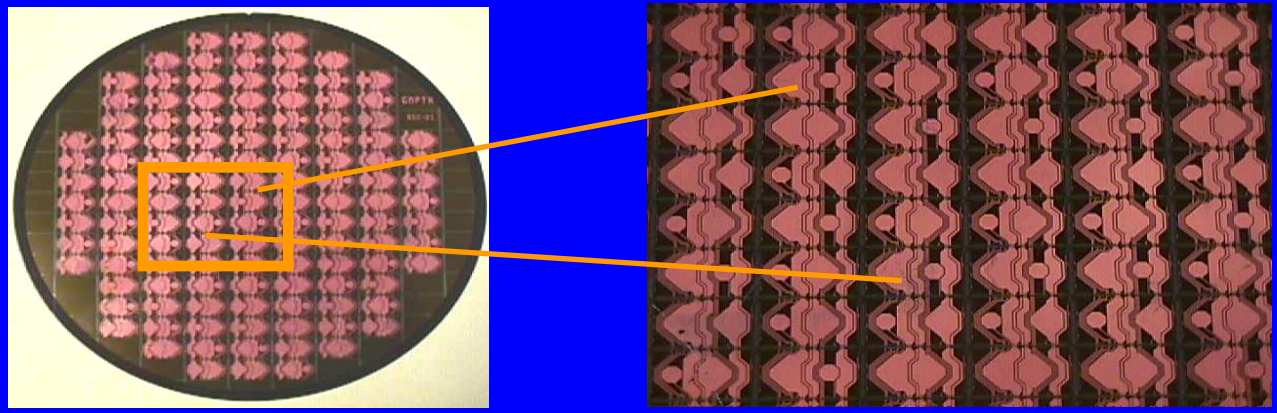



Cluster Arrangement - Viewed Looking at the Wafer Face

# 8 inch Wafer Level Burn-In System


Current Production System

# WLBI Design Considerations



- Additional scribe area to support burn-in circuit interconnect and current limiting resistors
- Proper burn-in metal width and space to support photo and etch process
- Proper pogo pin pad size for gross wafer alignment

# WLBI Design Considerations

- Minimum die per cluster defined by the number of required signals, power lines, and grounds.
- Metal bus width is designed to support current density requirement
- Proper adhesion between burn-in circuit metal and polyimide at elevated temperature (Burn-In 125 °C/Data Retention Bake 270°C)
- Polyimide to support burn-in contact over active circuit
- Maintain aluminum pad integrity after burn-in metal removal

# Verification of Aluminum Pad Integrity

| Mechanical Test | Engineering Wafer | Control Wafer |
|---|---|---|
| **Ball Shear (gmf)** | | |
| Average | 43.8 | 43.2 |
| High | 54.3 | 51.3 |
| Low | 31.2 | 36.7 |
| Std Dev | 5.1 | 3.7 |
| **Tensile Pull (gmf)** | | |
| Average | 9.6 | 8.7 |
| High | 11.0 | 10.2 |
| Low | 7.6 | 7.3 |
| Std Dev | 0.8 | 0.8 |

# System Design Considerations

- Maximum wafer power dissipation under natural and forced convection
- Effect of heatsink thickness and shape
- Thermal transfer between wafer and heatsink
- Inlet air temperature
- Airflow speed and circulation pattern
- Temperature uniformity across the wafer

# Accomplishments

- 5 inch Wafer Program

✔Development began in 1992

✔Eighteen wafer capacity system built in 1994

✔Production started in 1995

✔Full lot capacity production system built in 1997

✔Over 2 million KGD delivered since 1995 with no documented non-volatile memory (NVM) field failures

# Accomplishments

- 8 inch Wafer Program

✔Single engineering wafer system built in 1997

✔Successful 8 inch Wafer Level Burn-In in 1997

✔Prototype Production system built in 1998

✔Production system built in 1999

# Accomplishments

- Reliability Studies on WLBI die
- ✔ Life stress tests (op life, data retention bake (DRB), temperature cycle, etc …)
- ✔ Bump shear tests
- ✔ Under-fill adhesion tests

# Accomplishments

- Reliability Studies on WLBI fixture
- ✔ Uniform temperature control
- ✔ Power and signal integrity
- ✔ Pogo pin characterization

# Process Improvement Work

- Coefficient of Thermal Expansion Matching
- Uniform Thermal Control
- Cluster Yield Improvement
- Wafer Cold Test

# Summary

**Sacrificial Metal Wafer Level Burn-in**

- **Sacrificial metal wafer level burn-in is a low cost test solution to achieving known good die.**
- **Motorola has been in production utilizing this technology since 1995.**

# Acknowledgments

**The authors would like to acknowledge the teamwork from various Motorola SPS groups and Delta V Instruments that contributed to the development and continuous improvement of this sacrificial metal wafer level burn-in program (AVSD, SMD, FMTC, MOS12, and MOS5).**

# Reference Articles


• W. Ballouli, T. McKenzie, and N. Alizy, "Known Good Die Achieved Through Wafer-Level Burn-In and Test", 26th IEEE/CPMT IEMT Symposium, October 2000, pp. 153-159.

• W. Ballouli, C. Beddingfield, F. Carney, and R. Nair, "Wafer-Level KGD Technology for DCA Applications", *Advanced Packaging*, September 1999, pp. 26-30.

• T. McKenzie, "Wafer Level Burn-in (WLBI) Workshop", Motorola Internal Publication, November 5, 1997.

• W. Ballouli, J. Stroupe, "TSM Approach to Wafer Level Burn-in", Motorola Internal Publication, Motorola AMT Symposium, January 25, 1995.


*For Bits 2001 Workshop on Test & Burn-In*

# SOME SCENARIOS ON WAFER-LEVEL TEST & BURN-IN

***Robert Y. Million***
***Marketing Manager***
***Yamaichi Electronics U.S.A., Inc.***


## Chip Scale Packages (CSP)

Chip Scale Packages (CSP) have been the design darlings of advanced packaging, but starting last year 1999, the trend is on wafer-level packaging. The following five areas have seen significant breakthroughs which collectively provide a unique technical foundation for a new type of electronics package:

- Copper metallurgy and low dielectric materials for IC development
- Wafer-level test & burn-in (WLBI)
- The use of integrated passives (IPDs)
- Design automation tools
- Wafer bumping services

This presentation will define and describe some of the current technologies which address the issues involving **Wafer-level test & burn-in**, a key element for the entire back-end assembly/test function in IC production.

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## Wafer-Level Test & Burn-In

Wafer-level test & burn-in = the 'ultimate interconnect'? Why? Some significant obstacles to overcome in realizing a truly viable Wafer-level test & burn-in system:

- A lot of Z-axis bumps and high-density interconnects
- CTE matching of contactor to silicon under high temperature for long duration
- Heavy loads or high-forces to make electrical connection
- Uniform forces to all of the bumps or coplanarity issues
- A low cost contactor system

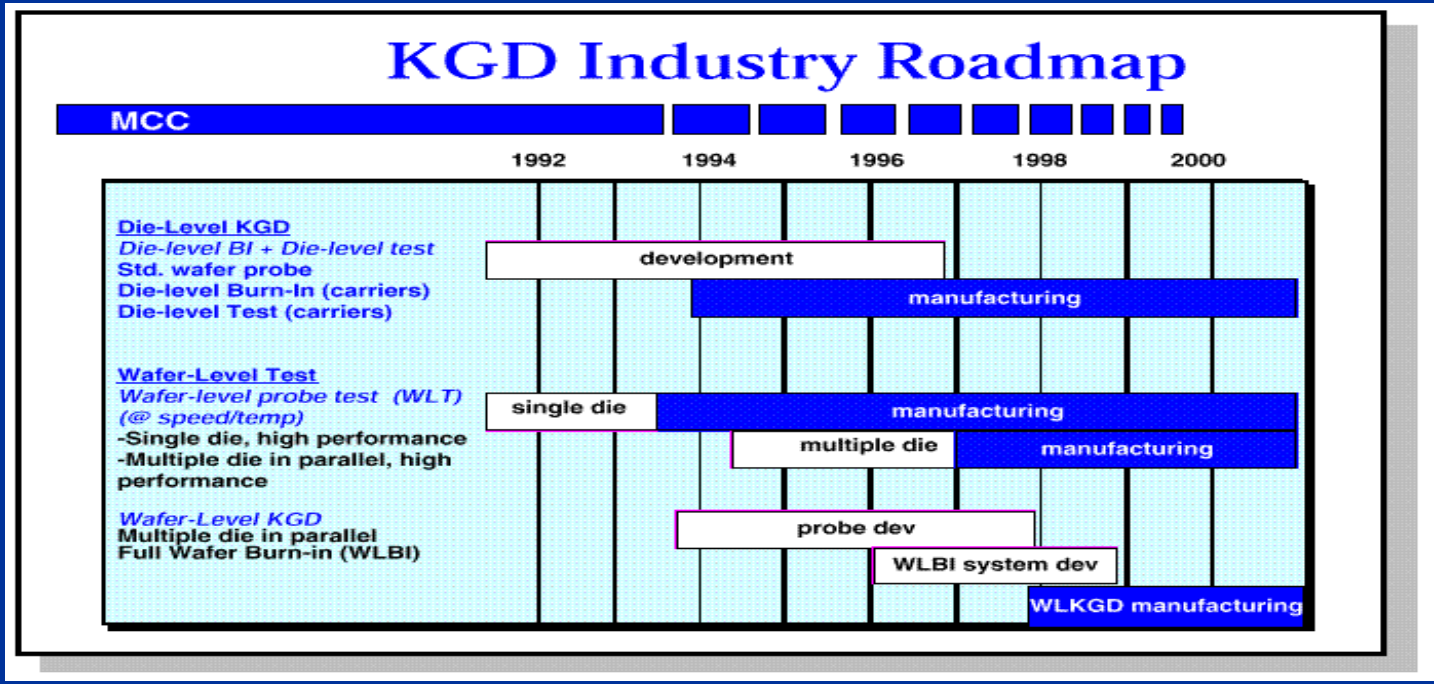
These obstacles only relevant to probe or contactor portion - just first step towards practical WLBI system. Subsequently, we have other issues:


- Automation issues in handling wafers
- How to get 10,000 ~ 20,000 contact pads on the wafer into ATE
- Cost / Performance ratios - the ultimate arbiter in success of WLBI system

On cost/performance, we must compare historically on what has gone before


# KGD (Known Good Die)

- MCC's interest in KGD began in late 1980s
- DARPA funding led to joint-effort with Sematech and MCC Consortia




Became nucleus for such KGD socket/carrier technologies as:

T.I./M.M.S.'s DieMate® - Aehr Test's DiePak®
Yamaichi's KGD/Gold Dot® Program - Bear Technology/
Micron Technology - EPI Technologies EPIK® System
Chip Supply's TAB system - etc.

! Goal of these technologies was to get KGD (test & burn-in) down to less than $0.01/pin = about parity with that of typical TSOP memory package.

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Never reached that goal for numerous reasons:

! 'Handling' (loading/unloading) of singulated bare die in carriers proved too cumbersome and unwieldy


High volume throughput, or an automated KGD system, to achieve KGD at a price of below $25 per site on a Burn-In Board (BIB) could never be realized - actual cost was more like $40 ~ $125 / site with lots of tooling for substrates, carriers and sometimes sockets - vendors tried to standardize on the sockets.

Curtailed the growth of MCMs (Multi-Chip Modules) as a major market

May have actually led to present day onslaught of CSPs (Chip Scale Packages)

- CSPs growing at 108% from 1997 ~ 2002
- More rugged and easier to handle than KGD - eliminates yield losses
- Burn-in sockets cost $25 ~ $45 per site on BIB for lower I/O count memory
- High-speed test contactors, if required, cost $1,500 ~ $5,000 each


- Over 65 different CSP packages from over 40 different companies - really hard to standardize on test & burn-in sockets

MCC's commercial project in 1995 to evaluate feasibility of wafer-level burn-in for reliability screening of KGD - several of the WLBI systems to be shown next were germinated from DARPA/MCC/Sematech consortia effort.

**Wafer-Level Burn-In at Motorola - A Joint Development Project between Motorola, Tokyo Electron Ltd.(TEL), and W.L. Gore & Associates**

- Motorola - process development, integration and qualification
- W.L. Gore - supplying wafer contactor materials in the form of GoreMateII™ Contactor and Inferno™ IC Board
- Tokyo Electron Ltd. - supplying burn-in equipment and automation
- Project located at BAT-1 (Bump, Assembly, and Test) - Motorola's integrated back-end factory in Austin, TX - all operations from unit probe through final test are under one roof.

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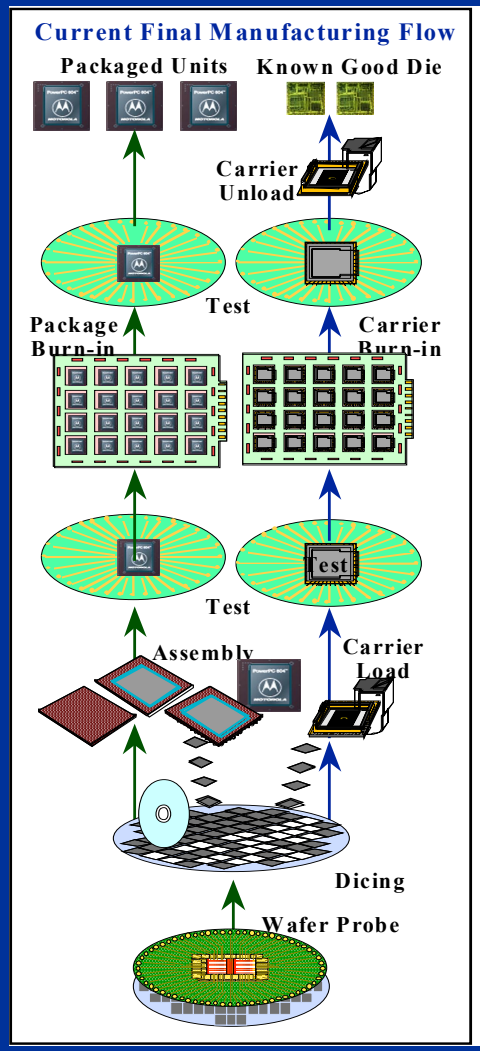
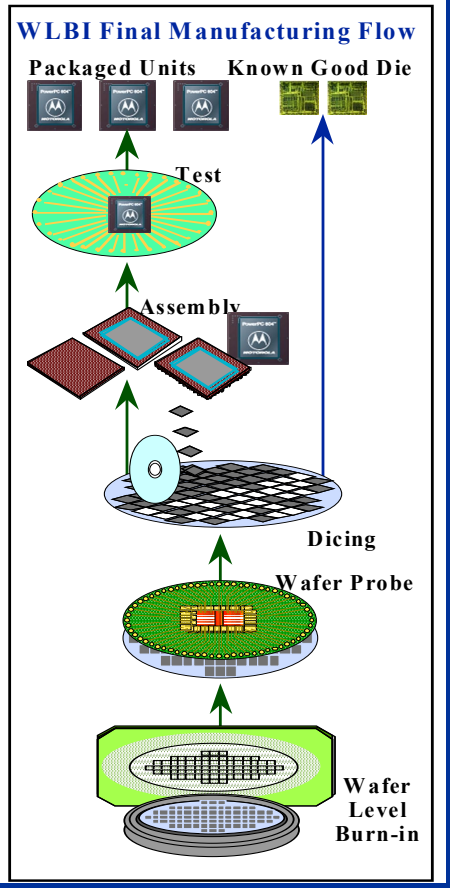
# *Current Final Manufacturing Flow; WLBI Advantages; and WLBI Final Manufacturing Flow*




- **WLBI Advantages**
  - Product Cost Reduction
  - Cycle Time Reduction
  - Capital Cost Reduction



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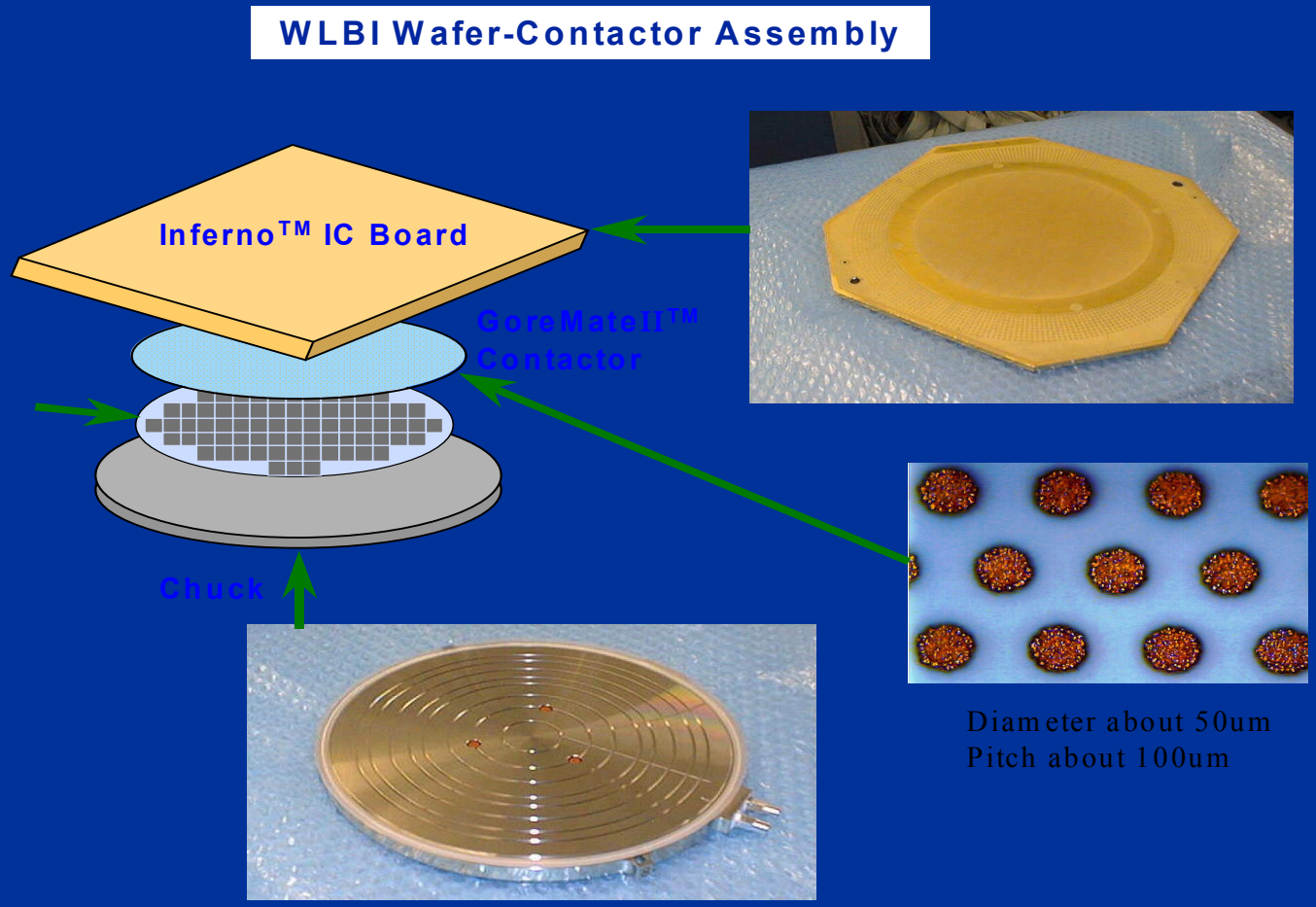
# *WLBI Wafer-Contactor Assembly*



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# *WLBI Beta Development System*

## WLBI Beta Development System

- Beta Development system is a 7-wafer system including
  - 7-chamber burn-in rack
  - Aligner for wafer-contactor assembly
  - WLBI Electronics
  - System Control Module

System Control Module

WLBI Electronics

Burn-In Rack & Lifter

Align and Assemble Module

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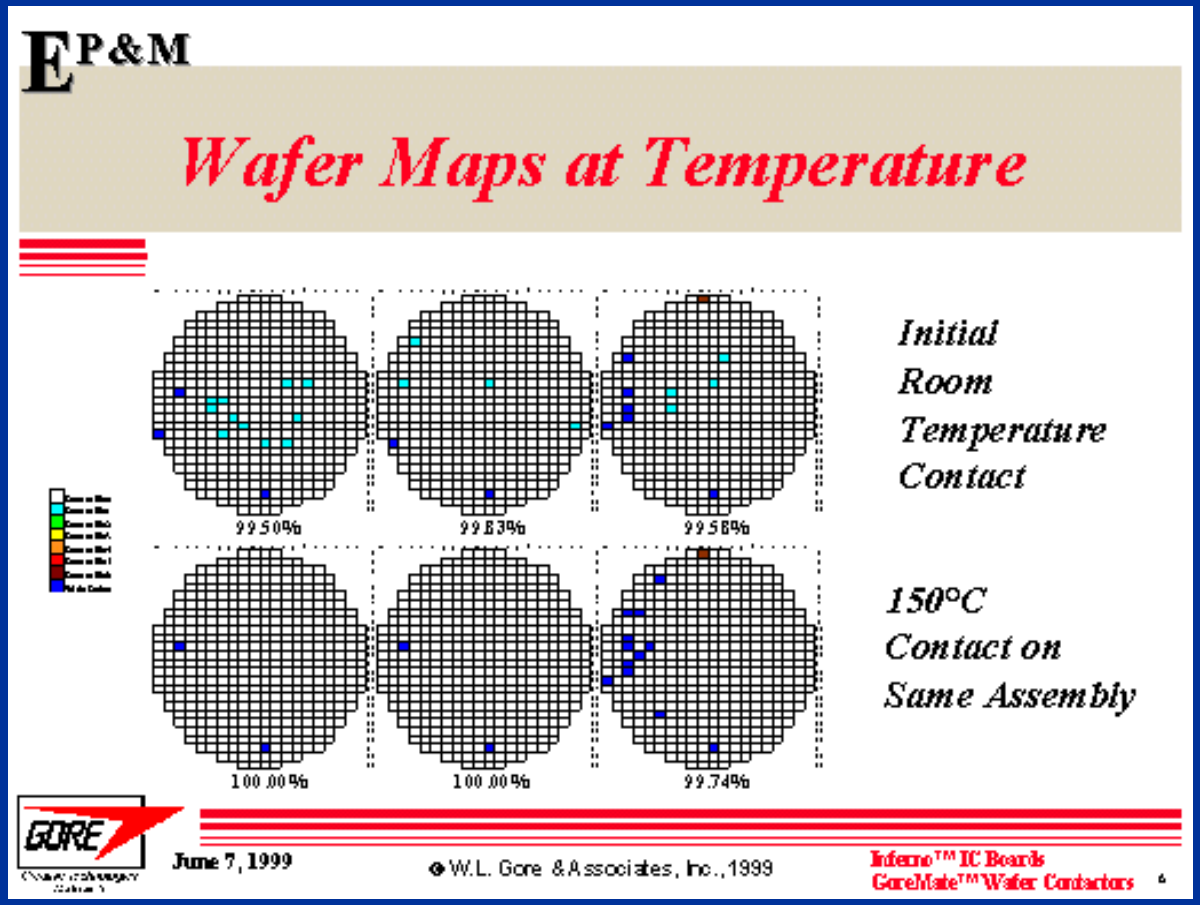
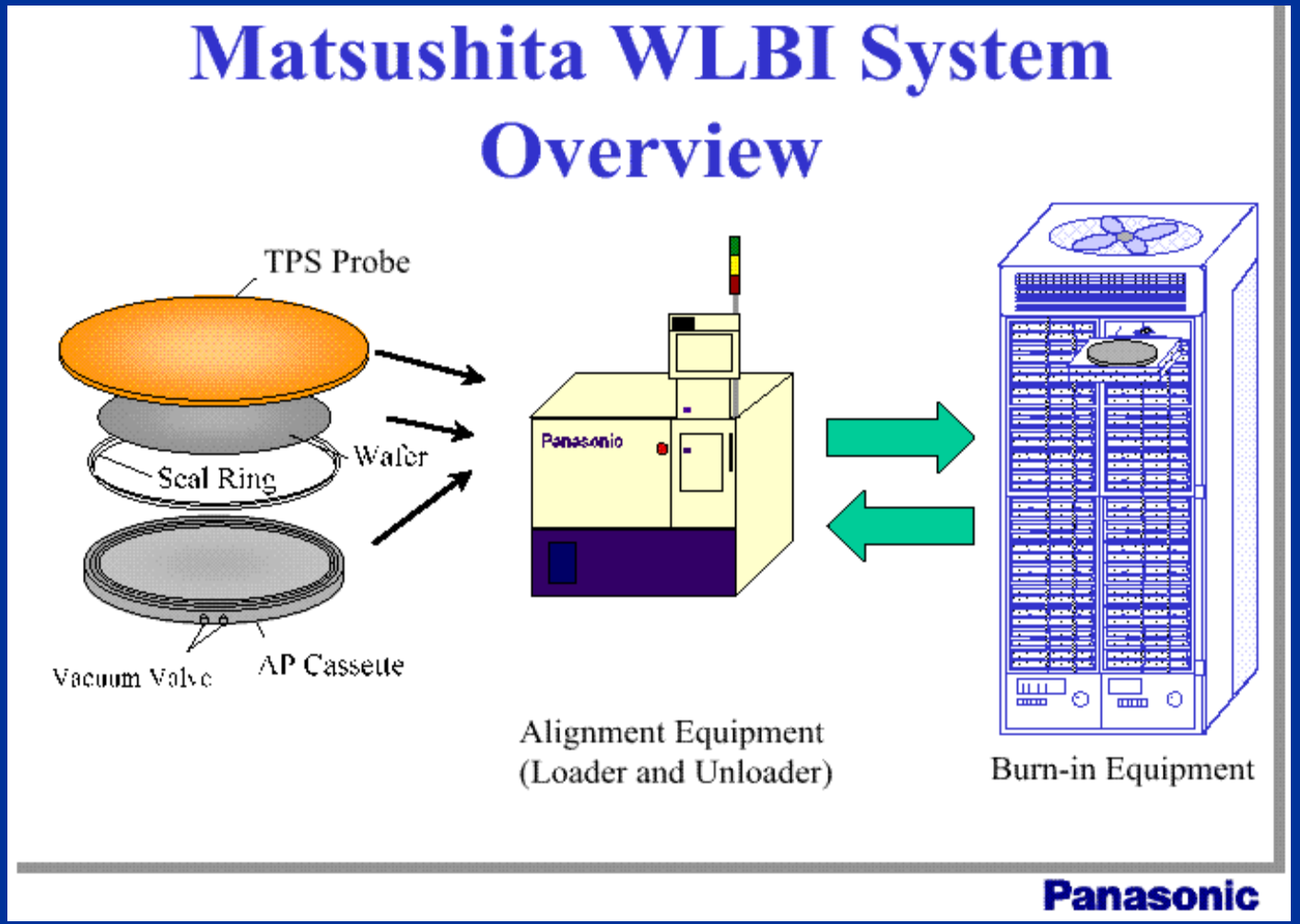
## Wafer Maps at Temperature



## *Matsushita WLBI System Overview*



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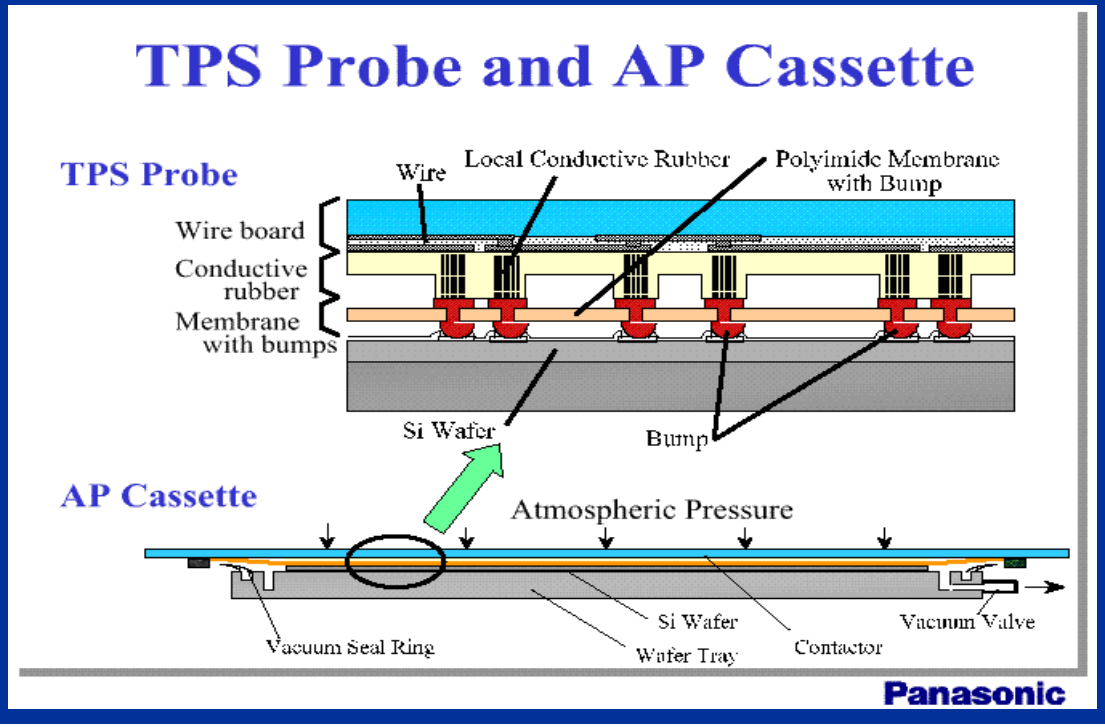
Three Part Structure Probe (TPS):

- Contactor which provides compliance by utilizing multi-layered interconnecting wire board, conductive rubber, and a membrane with Z-axis bumps
- Control CTE of bumped membrane



In conclusion, a first step towards practical WLBI technology has been realized:

- CTE matching of contactor to silicon
- The absorption of bump height differences
- Uniform pressure with the atmospheric cassette
- Firm contacts have been achieved on 2,756 bumps which have remained stable up to 125☜C
- Goal on membrane/substrate life is 1,000 cycles, but they are not there yet.

**FormFactor Inc. - Using Microspring™ Contacts for Wafer-Level Packaging & Test**

FormFactor has invented a new contact technology called a MicroSpring™ suited for electronic applications of a low force, low profile, z-axis, wiping, gold on gold contact.

- These are true springs requiring around one gram of compression force for every one mil of displacement and exhibit low contact resistance, typically below 30 milliohm♦ per contact pair.
- They can be used as a fine pitch contact down to pitches of 225 microns, ie., as in current production of contacting C4 (Flip chip) arrays of 1000's of contacts.
- They have been profiled as being ideally used in LGA production sockets and have been used in FormFactor's own Probe Cards to test DRAMs or CPUs at the wafer level.


## FormFactor

**The ultimate extension of their MicroSpring technology comes in the form of their WOW™ technology or Wafer On Wafer**. WOW is the IC industry's first back-end process that provides full wafer level package, burn-in, test and module assembly - all steps to be performed on a whole wafer thereby reducing costs.

*The key element in FormFactor's success is the MicroSpring™ contact which is formed by placing a specifically designed and shaped wire bond at the desired pad or contact location, and then plating up with a proprietary process the wirebond, transforming it into a spring.*

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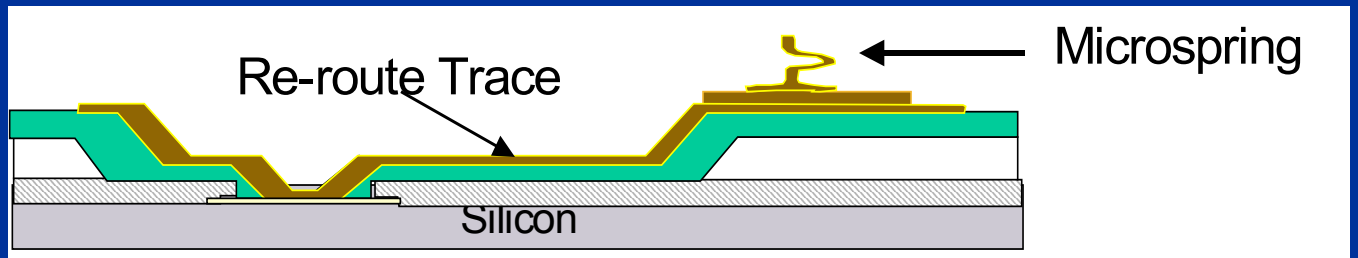
## *Microspring Contacts on Silicon*




- Microsprings provide:
  - ① Temporary (pressure) connection during test and Burn-in
  - ② Permanent Interconnect in the final product

- Microsprings can be located anywhere on the die surface including directly on the bond pads

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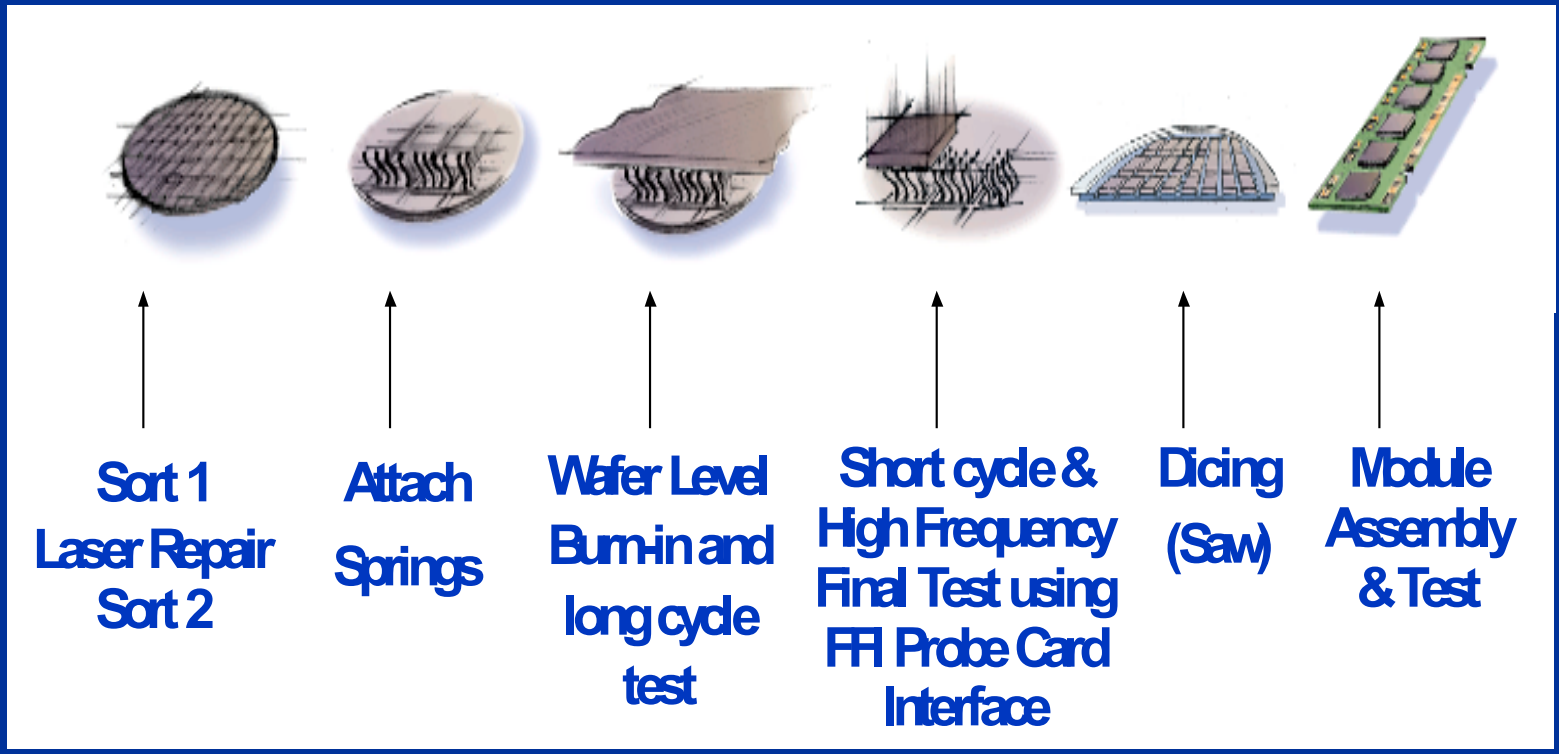
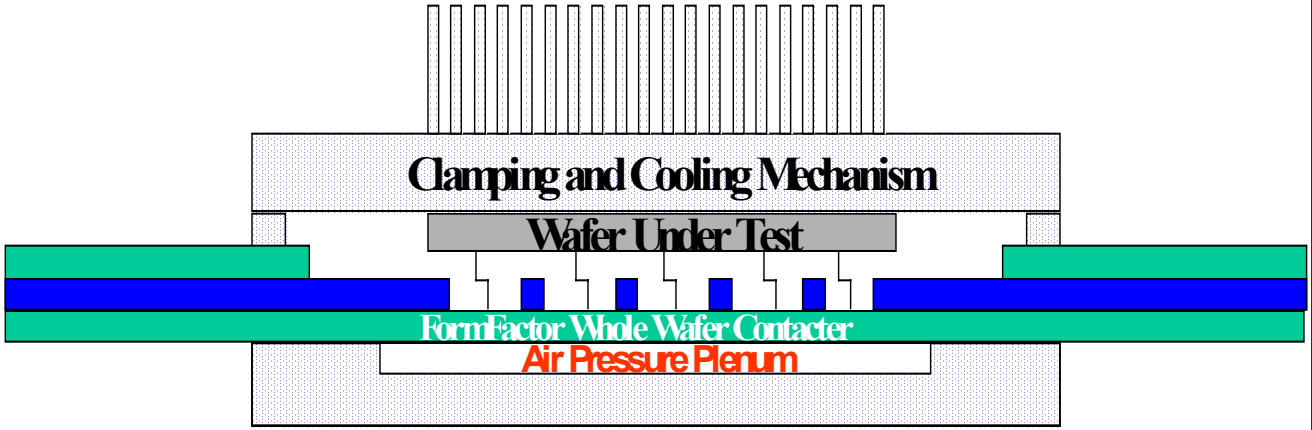
## *The WOW Process: A Wafer Level Flow for Low Cost KGD*



## *FormFactor's WLBI Solution*

- Design Approach: "Don't fight the mechanics"
  - ➔ Compliant Contacter: Conform to the wafer
  - ➔ Use positive pressure to drive contacter




  - ➔ Use Compression stop to nullify variations

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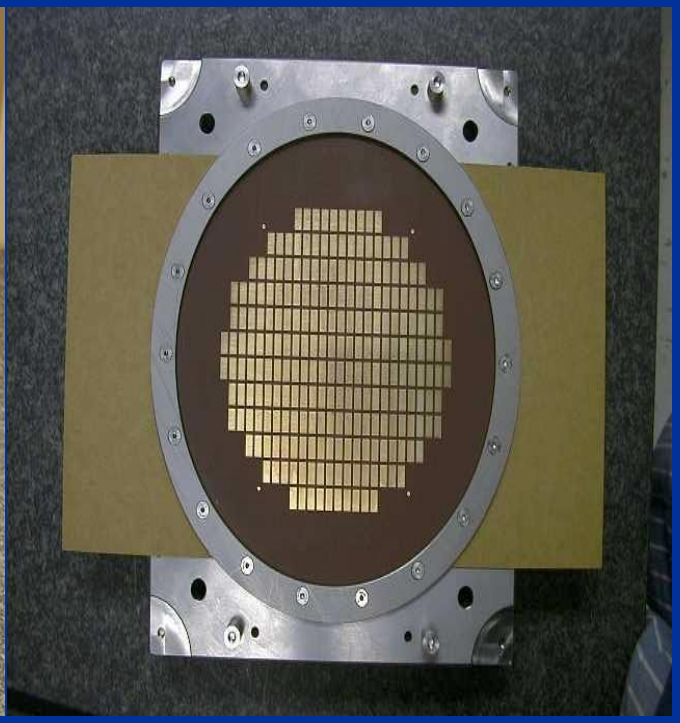
## *WLBI Clamping and Cooling System*






Current Projects with Three Alternative Test Flows:

! WLBI and Wafer-Level at speed test - demonstrated with Teradyne Aires tester and Infineon's Rambus die tested at 800MHz (12x faster than any other wafer-level test reported)

! Dicing after CSP packaging at wafer-level and using existing CSP handlers and test boards with $10~20 Yamaichi sockets (x-y registration frame and lid - the microspring contact is on the die) instead of high-cost, and high-speed test contactors ($1500~4000).

! Package, dice, then assemble into modules - do all burn-in and test at the module level. No underfill required which makes repair simple. Since the microsprings are self-socketing, one can utilize a use a pressure mounted connection and elimininate solder or conductive epoxies altogether.

**Gryphics®, Inc.**
**In Development: A Controlled Compliance Probe with Generic Applications as a Wafer Probe**

Another Company with quite innovative technology is Gryphics, Inc., located in Plymouth, MN. Gryphics is developing a patented group of products which incorporate low cost and high performance into what are referred to as **Removeable Chip Modules (RCM™)**. These high-density modules can accept a wide variety of devices in many applications with each device being interconnected by a very low inductance Multi-mode Compliance contact system, which is solderless and dematerable.

The RCM can be used as a prototyping, test & burn-in, and production IC socket as well as products integrating removeable ICs into high volume connector applications.

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## Gryphics

The suggested interface below consists of a controlled compliance Module having a suspended contact set to interface with a bumped device by means of several contact members. The module is to act as the interface to the device, which can be demated from the substrate without solder reflow and subsequently moved to another location such as a tester or additional circuit board:

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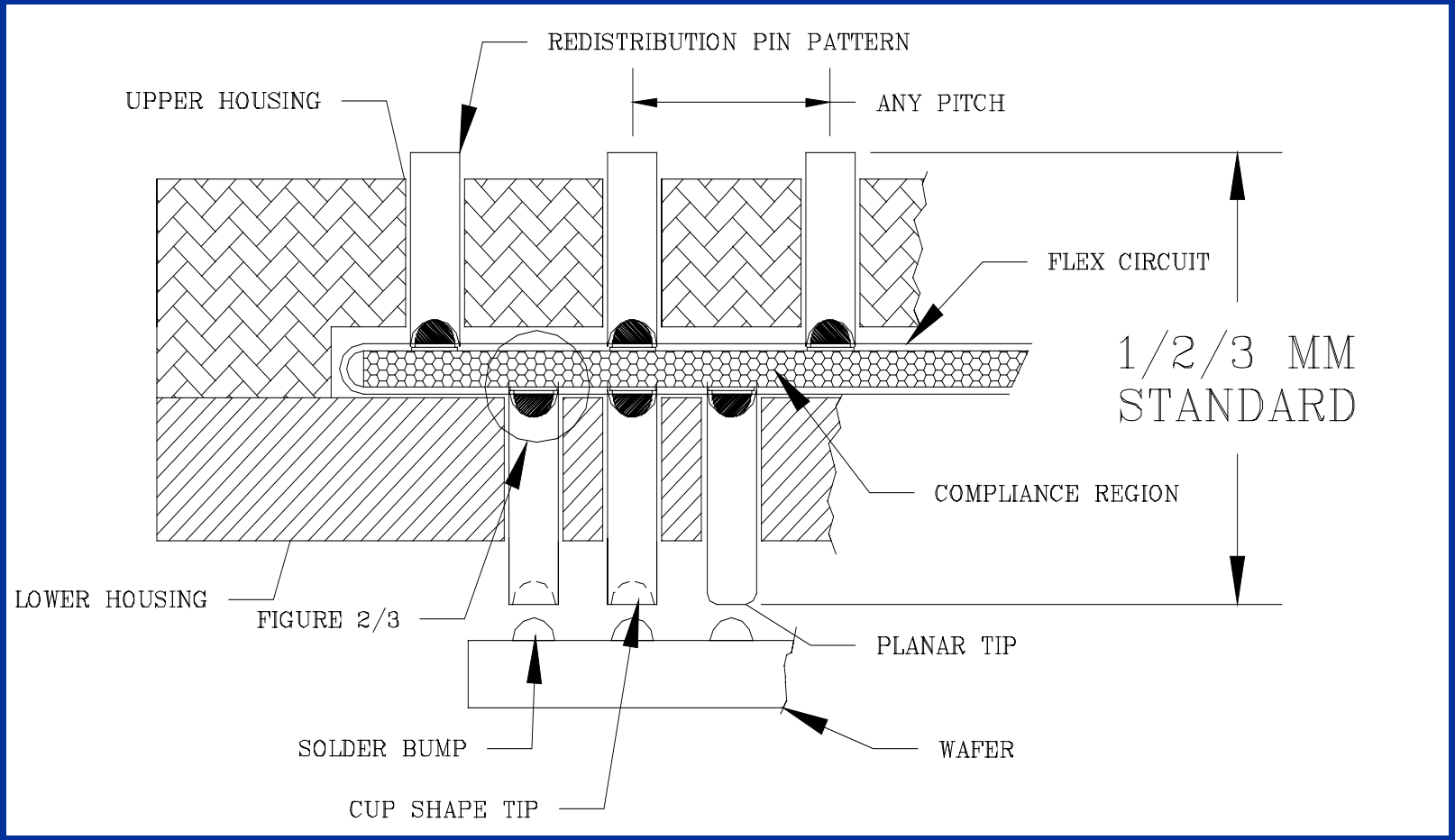
REDISTRIBUTION PIN PATTERN
UPPER HOUSING
ANY PITCH
FLEX CIRCUIT
1/2/3 MM
STANDARD
COMPLIANCE REGION
LOWER HOUSING
FIGURE 2/3
PLANAR TIP
SOLDER BUMP
WAFER
CUP SHAPE TIP

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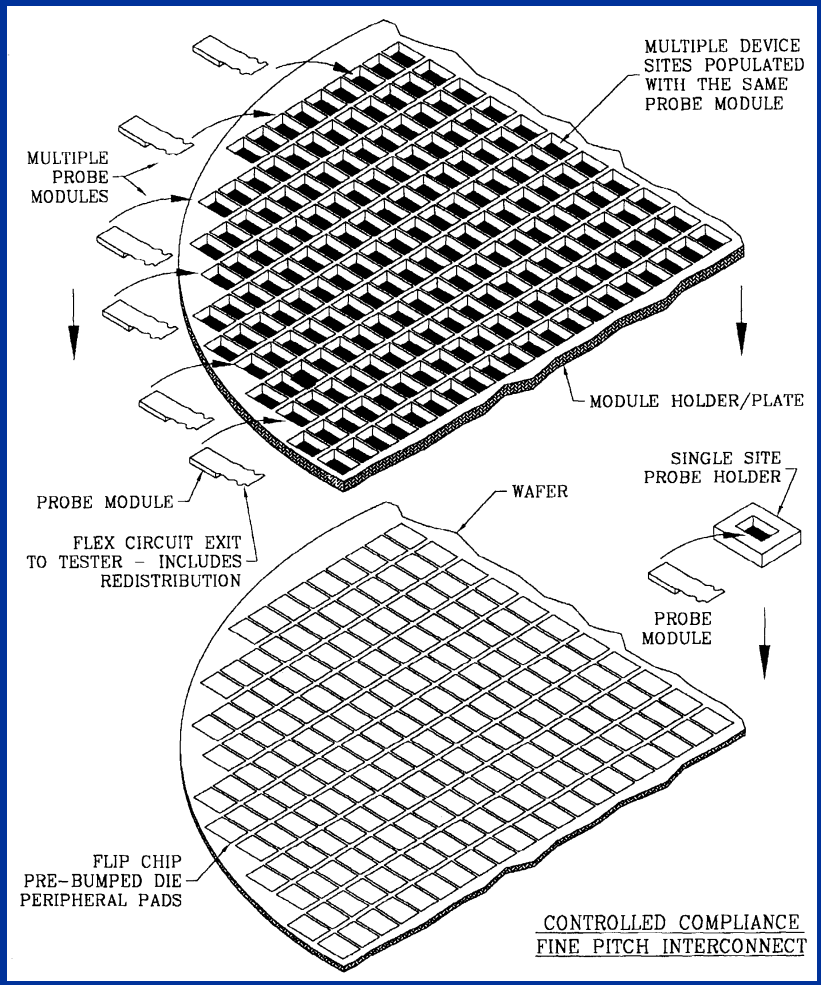
The following is an example of such controlled compliance fine pitch interconnect utilized in the same probe module for testing and burning-in multiple device sites:



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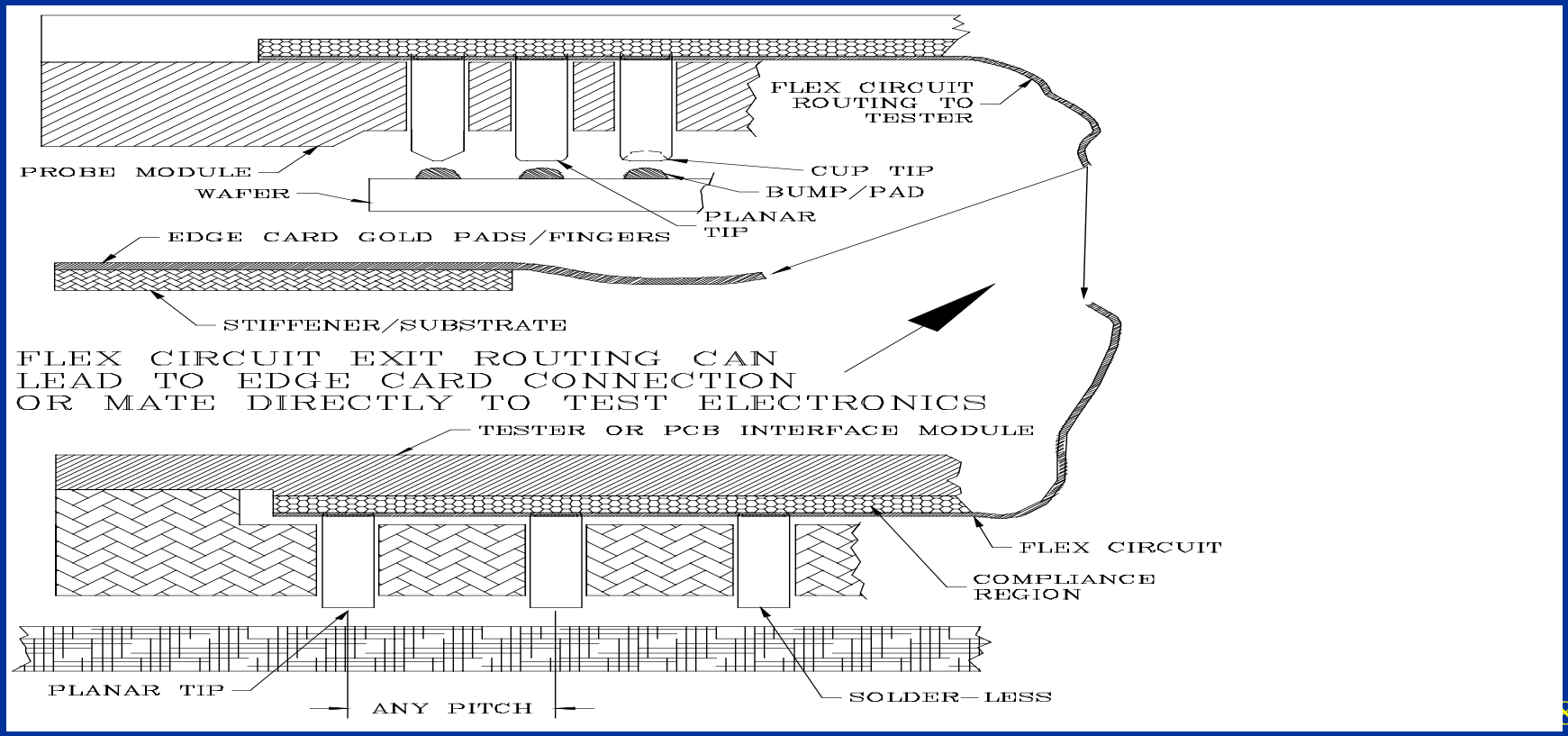
## Gryphics

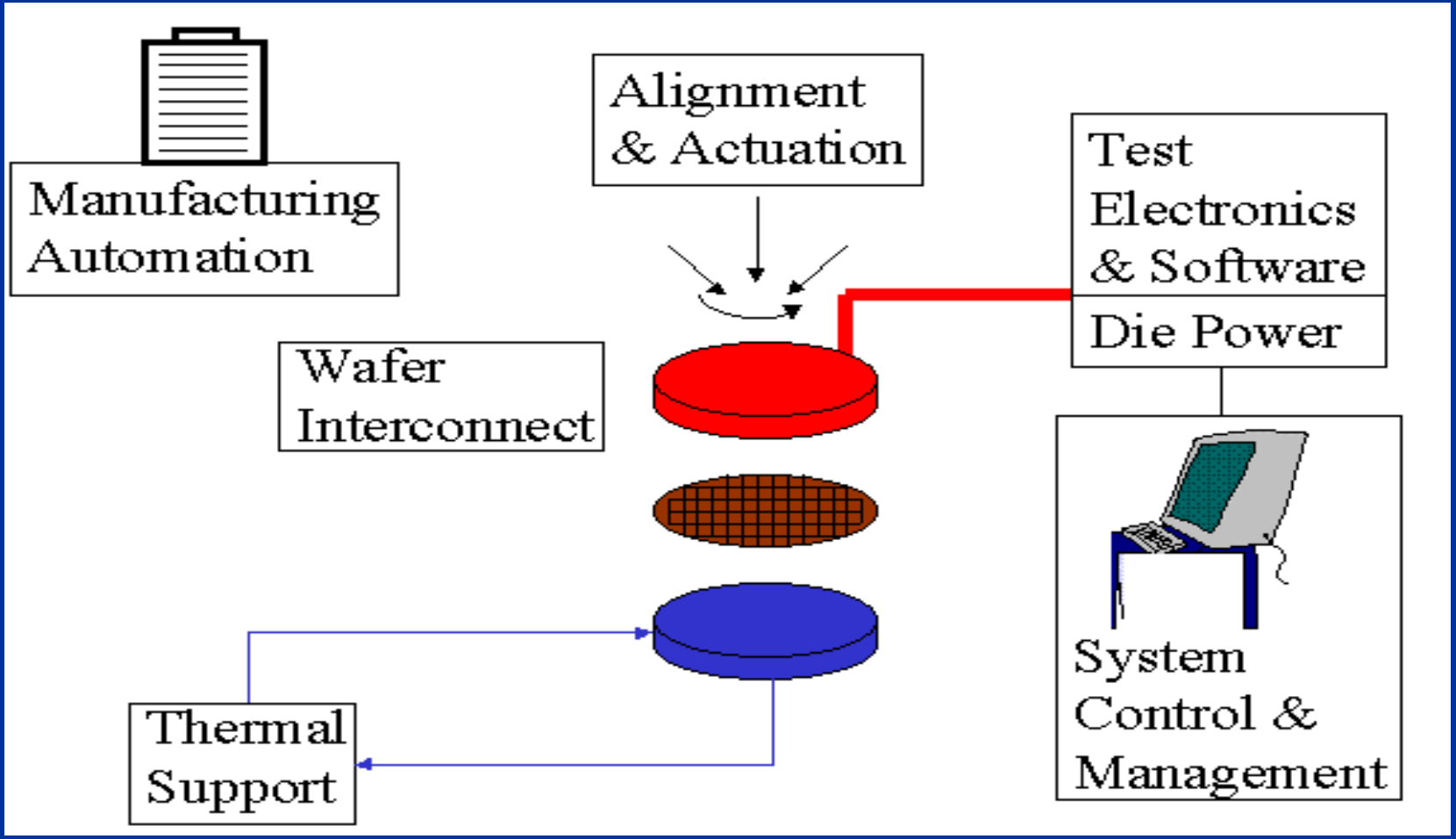
Using this approach, a flex circuit exit routing coming off the probe module can lead to edge card connection or mate directly to test electronics:



## Aehr Test Systems - Wafer Level Burn-In and Test System

Recently Aehr Test Systems announced development agreements with NHK Spring Co., Ltd. of Yokohama, Japan for Full-Wafer probe contactors for WLBI and Electroglas, Inc. for a complete Wafer-Level Burn-in and Test solution. Aehr Test has been working in this area for several years with cofunding from DARPA. This section will describe the requirements for a comprehensive WLBT system and the solutions Aehr Test Systems has developed.

## *WLBT System Requirements*



The economics and time requirements of the alignment and burn-in processes dictate the WLBT System Architecture:

- Wafer alignment is short duration but uses expensive hardware
- Burn-In process is time extensive
- Cartridge based system separates the two processes for best cost effectiveness

Test Electronics and Software are critical to ensure that effective contact is being made to the devices:

- Must test to ensure electrical connection
- Additional time for test is insignificant compared to burn-in time
- Functional test can be cost effective at this step of the process


Aehr Test System' s WLBT system is able to support different contactors into its cartridge system - experimenting with NHK Spring probes (12K ~13K), Goremate, and Nano Plexus's fab'd 'Electronic Membrane'.

Manufacturing Integration and Automation Support is necessary to integrate the WLBT system into the product flow of the manufacturing line:

- Cassette-to-cassette wafer handling required
- Cartridge handling in fab requires precision fixtures and is best not handled manually
- Aehr WLBT system offers semi-automatic handling at first but automation decisions are on a per-installation basis




## Sacrificial Metal Wafer Level Burn-in KGD

Motorola has been developing and evaluating WLBI technologies since the early '90s as seen in the earlier presentation on the Motorola/TEL/Gore alliance. This particular development and implementation of 127mm and 200mm Sacrificial Metal Wafer Level Burn-In KGD at Motorola is a strategic enabling technology that allows Motorola to maintain a competitive edge in the electronic personal communications, computer and automotive marketplace.

This has been a joint effort between teams at:

- Motorola Austin - TSG (Transportation Systems Group)
- Motorola Chandler - SMD (Strategic Manufacturing Deployment)
- Motorola Chandler - MOS 12 Group

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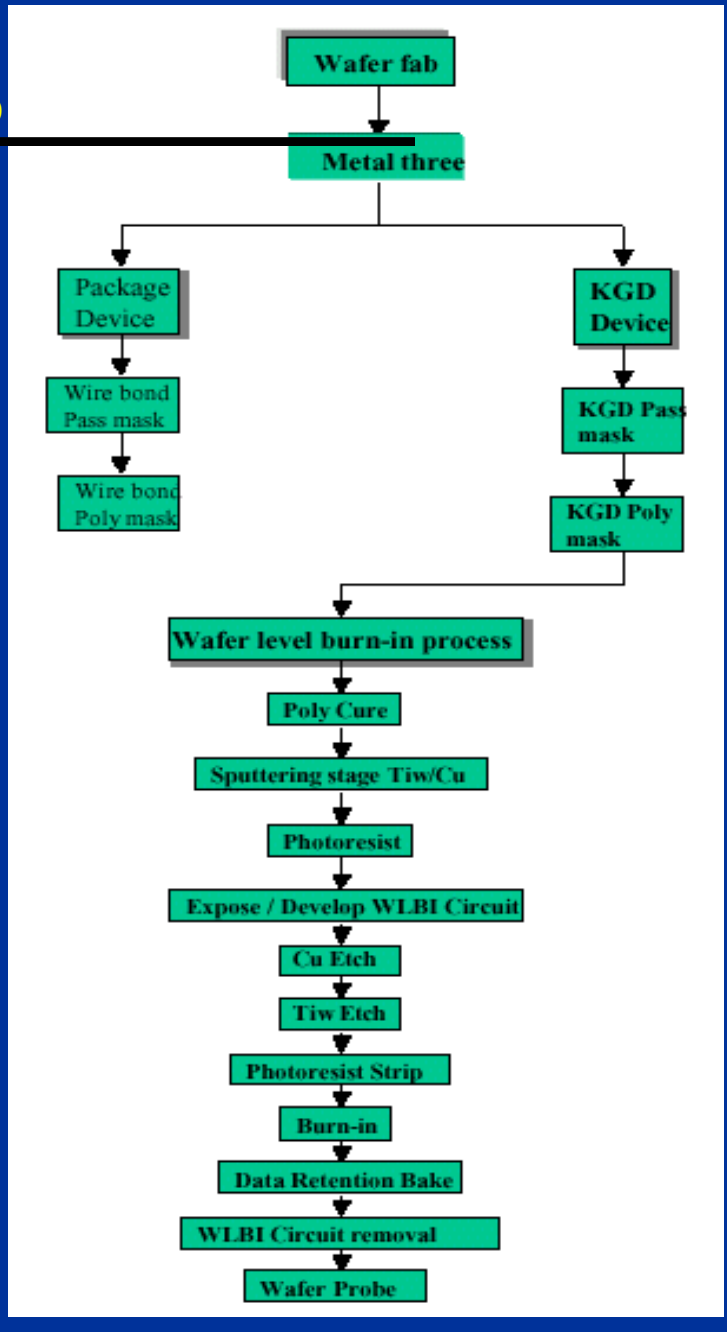
The WLBI process flow at the wafer-level:

- WLBI process flow is identical to package level devices all the way to Metal-3 at the MOS
- The special passivation mask enable contact along the scribe grid whose contacts accommodate excercising of the device during burn-in
- A final polyimide over-layer acts as a stress buffer in aggressive environments (ie., automotive) - need to be free of unstable components to prevent outgassing
- Wafer-level burn-in circuit removal comprised of wet etch processes with chemistries identical to that used in defining the WLBI circuit - TiW and/or Cu must be completely removed



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Test System Design:

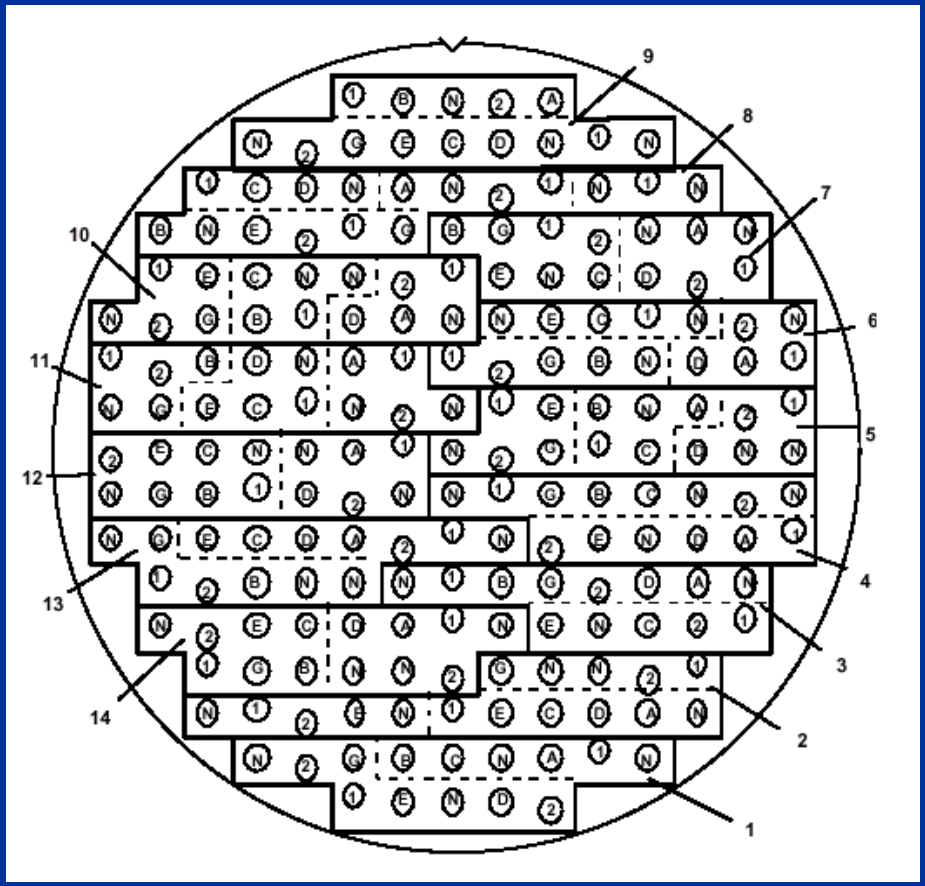
## Motorola Inc. / SPS Group

The test system consists of:

- Two separate chambers containing 14 individual slots for accepting DUT boards
- HDI connector provides signal path between the DUT board and its respective driver board located internal to the test platform
- All necessary power and drive signals are made available to the wafer via this interface

## Fixture Design and Contact Technology:

The wafer, with the WLBI circuitry (sacrificial metal layer) applies, sits in a fixture which supplies proper alignment, thermal stress and creates the electrical test path.




! Die on the wafer are electrically grouped into clusters and share power and drive signals in common


- Electrical contact is made with the wafer through the use of pogo pins interfacing with test pads provided through the WLBI circuitry applied earlier

- Pogo pins specially designed to provide robust electrical and mechanical contact - pins are replaceable in the event performance becomes degraded

Motorola has used this system for several years to provide KGD for use as Flip Chip or wire-bonded die in the automotive industry and for providing non-volatile memory chips.




**Die Products Consortium (DPC) - KGD Test and Reliability Screens Methods Demonstration Project**

The Die Products Consortium (DPC) is a cooperative effort among several leading microelectronics companies to advance the development of a support infrastructure that will accelerate the adoption of die products by electronic system manufacturers worldwide. **Currently, there are seven members involved with the Test Methods Demonstration Project - these include Chip Supply, IBM, Lucent, Intel, T.I., National Semiconductor, and Cypress Semiconductor. The Consortium is being managed by MCC, recognized as a global leader in KGD technology.**


*The goal of the Test Methods Demonstration Project is to demonstrate that wafer level test and stress screening methods are effective for the acceleration and detection of various types of defects*.

This project will provide a baseline for members to compare defectivity of their fabs with other members' experience on a strict confidential basis.

*The Project will develop the tools and provide understanding of the industry's "best practice", enabling members to determine the most cost effective means to achieve their particular reliability goals.*


## Contributors

1. Flynn, Greg W., “Wafer Level Burn-In (WLBI) at Motorola - Outline” for Fleck Research Chip Scale International 1999.

2. Mosko, John, “Full Wafer Burn-In and Test” from Sixth Annual KGD Workshop, W.L.Gore & Associates, Inc.

3. Nakata, Yoshiro and Kawai,Makoto, “A Wafer-Level Burn-in Technology” from ULSI Process Technology Development Center, Matsushita Electronics Corporation.

4. Whitten, Ralph, “Using Microspring™ Contacts for Wafer Level Packaging and Test” from FormFactor, Inc.

5. Rathburn, James, “In Development: Controlled Compliance Probe with Generic Applications for Wafer Probe” from Gryphics, Inc.

6. Carbone, Mark C., “Wafer Level Burn-In and Test System (WLBT)” presented at Semicon West, 1999 by Aehr Test Systems.


## Contributors

7. Godavarti, Prasad and Ivy Jr., Wilburn, “Sacrificial Metal Wafer Layer Burn-In KGD” presented at ECTC, 2000 from Motorola Incorporated

8. Gilg, Larry, “ Die Products Consortium - KGD Test and Reliability Screens Methods Demonstration Project” for 6th Annual KGD Workshop, co-sponsored by MCC.