Burn-in & Test Socket Workshop

March 4 - 7, 2001
Hilton Mesa Pavilion Hotel
Mesa, Arizona

IEEE

IEEE COMPUTER SOCIETY

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Technical Program

Session 7
Wednesday 3/07/01 8:00AM

<u>Advancements In Socket Products</u>

"PASS Chip"
Min Cho – Inabata America Corporation

"Evaluating Elastomer For High Density BGA Socket"
Ila Pal - Ironwood Electronics, Inc.

"Low Cost Thermal Management Using Compliant Thermal Interface Materials"
Nancy Dean – Honeywell Electronic Materials (Presenter)
Kenichiro Fukuyama - Honeywell Electronic Materials

2001 Burn-in and Test Socket Workshop

PASS CHIP

March 4 - 7, 2001

Presented By : Min Cho

Manufactured by

PASS *Corporation*

Distributed by

Inabata America *Corporation*

Mission

•Based on years of experience and survey, we have successfully invented the most effective, simple, and least costly tools for electrical contact cleaning: PASS CHIP products.

•To be a unique provider of the best solution for the contact problems which inevitably arise with all kinds of electronic devices to be seen everywhere today.

•To contribute toward more productivity yielded by more effective and less costly production in the electronics industries worldwide, resulting in higher quality goods and higher cost-performance that can more comfortably surround and further enrich the daily lives of people.

Market Outlook -1

The following facts will dramatically expand the market of contact cleaners.

Semiconductors are in huge demand

The IT revolution is creating a large variety of applications of powerful semiconductor products.

PCs, Mobile Phones, Video Cameras, DVD players, Communication Devices, Home Appliances, etc...

•Estimation of monthly worldwide production of semiconductors

Year	**2000**	**2003**	**2005**
Number of Unit (in Millions)	30,000	60,000	100,000

This creates a need for more frequent contact cleaning!

Market Outlook -2

Lighter, more compact packages of semiconductors will inevitably follow.

It is a fact: Electronic commodity goods are produced lighter, more compact, more ergonomic with each new generation. Newer types of semiconductors, such as FBGA & CSP will become more prevalent.

This creates the need for more advanced contact cleaning <u>methods</u>.

Market Outlook -3

•More productivity and more effectiveness in every process of production are needed

As the usage of mass-production increases, our testing process must become more effective.
An efficient contact cleaning operation should be easily done without a burden of cost.

This creates the need for an easier & cheaper method for contact cleaning

Before PASS CHIP -1

The semiconductor industry has been looking for a better solution of contact cleaning for years.
The following methods of contact cleaning are currently widely used:

•Ultrasonic-Wave cleaning

The outside cleaning company usually needs 4-5 days for cleaning time, and this requires substitutes of burn-in or final testing board

Costly, time consuming, troublesome in-out handling

Professional services are needed

Costly

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Before PASS CHIP -2

- **Brush cleaning**

  Manual brushing takes a lot of time

  Time consuming, less productive

- **Air blow cleaning**

  Solder residues cannot always be completely removed

  Less effective

Before PASS CHIP -3

•Replacement of contact pins instead of cleaning

Re-manufacturing the contact pins is costly

Expensive

Replacing the pins requires a professional service

Costly, time consuming

With PASS CHIP -1

" PASS CHIP " has created a perfect solution for contact cleaning to eliminate all sort of headaches that keep annoying production managers.

•Proven effectiveness in cleaning

Major manufacturers in the semiconductor industry have thoroughly evaluated "PASS CHIP" models and been well satisfied with its effectiveness in cleaning.

With PASS CHIP -2

Evaluation Test of Cleaning operation

•Package Used	:	TSOP2
•Burn-in Boards	:	48 sockets x 66 boards
•Evaluation method	:	Compared occurrence of defective devices before and after PASS Chip application

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With PASS CHIP -3

Evaluation Test Results (66 Boards)

	Before Cleaning			After Cleaning		
Board	Good	Defective	Ratio	Good	Defective	Ratio
1	42	6	12.5%	48	0	0.0%
2	42	6	12.5%	48	0	0.0%
3	45	3	6.3%	48	0	0.0%
4	46	2	4.2%	47	1	2.1%
5	43	5	10.4%	47	1	2.1%
6	44	4	8.3%	48	0	0.0%
7	40	8	16.7%	47	1	2.1%
64	37	11	22.9%	45	3	6.3%
65	39	9	18.8%	46	2	4.2%
66	43	5	10.4%	48	0	0.0%
Total	2667	503	15.9%	3109	59	1.8%

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With PASS CHIP -4

•**Ease of usage**

"PASS CHIP" can be easily placed on the contact pins manually or by a vacuum pad, and requires NO professional services for effective cleaning.

•**Low cost**

Cleaning your contactors with a disposable "PASS CHIP" requires no additional costs.

With PASS CHIP -5

•**Short cleaning time**

One or two wipes with "PASS CHIP" can instantly remove the solder residues or dirt from the contact pins, which results in shorter down time and a more productive testing process.

PASS CHIP Products-1

•Products for IC Socket contact cleaning

1. Flat sheet model for TSOP / QFP type of socket
   (Single coated or Double coated)
2. Cubic sheet model for TSOP / QFP type of socket
3. Pad model for CSP / BGA type of socket

•Useful both in a burn-in and a final test process as well as in a writing process of SRAM or Flash Me

•Available to any type of socket, i.e. OPENTOP, LID or LIDLESS.

•Available to any customer specifications.

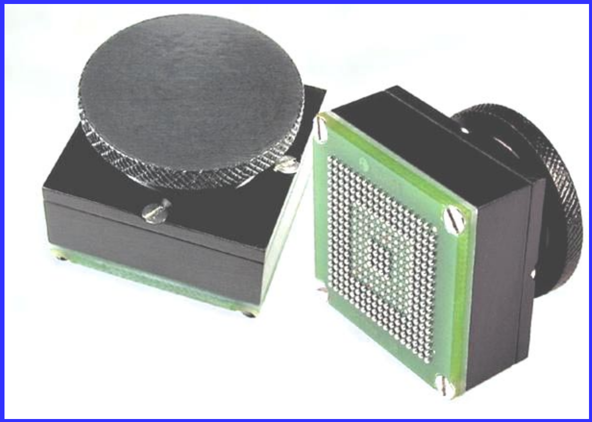
PASS CHIP Products-2

•**Product for Probe Card contact cleaning**

Available to any customer specifications

•**Product for DIMM contact cleaning**

Available to any customer specifications



Ironwood Electronics, Inc.

Evaluating Elastomer for High Density BGA Socket

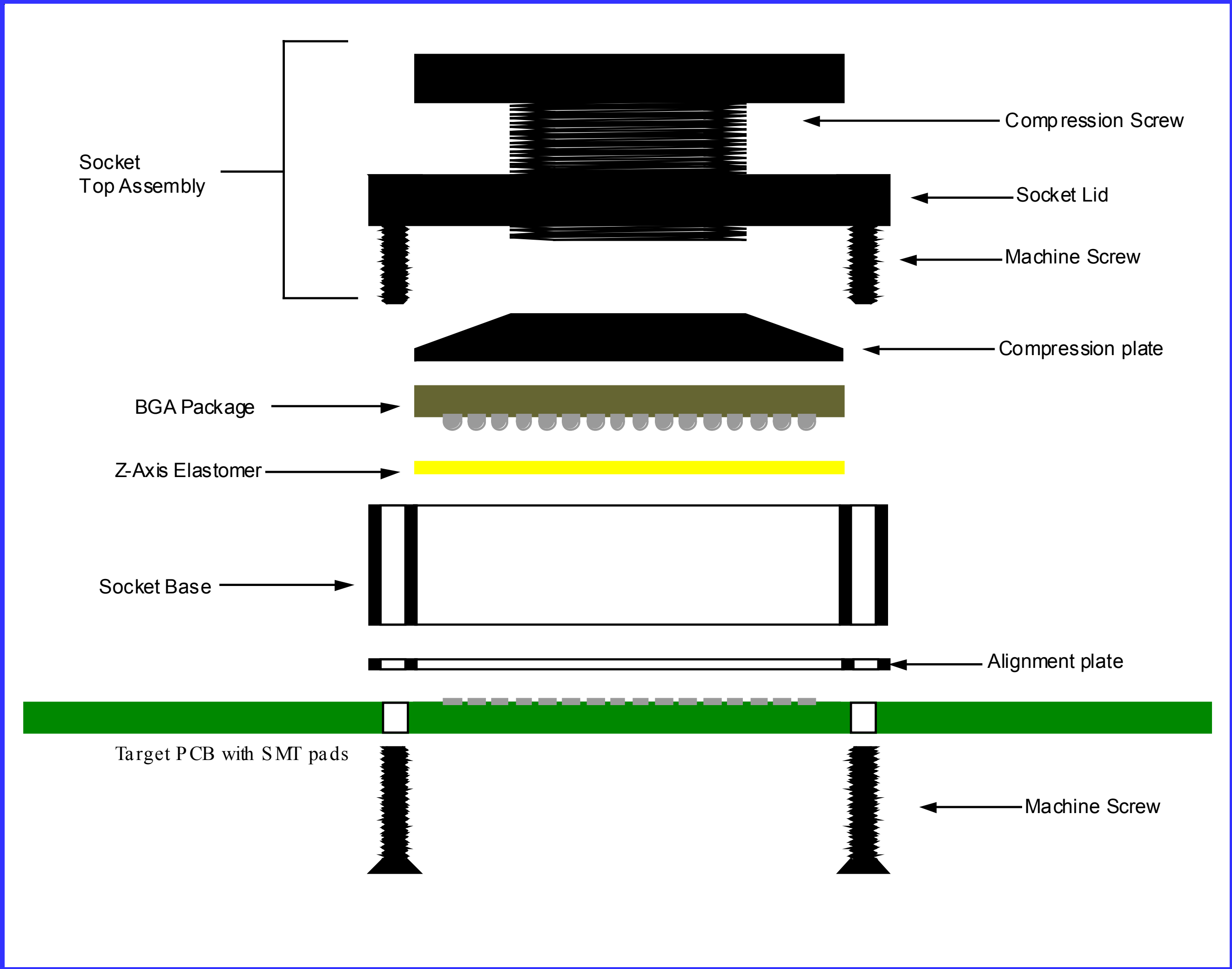
Ila Pal

Ironwood Electronics, Inc.

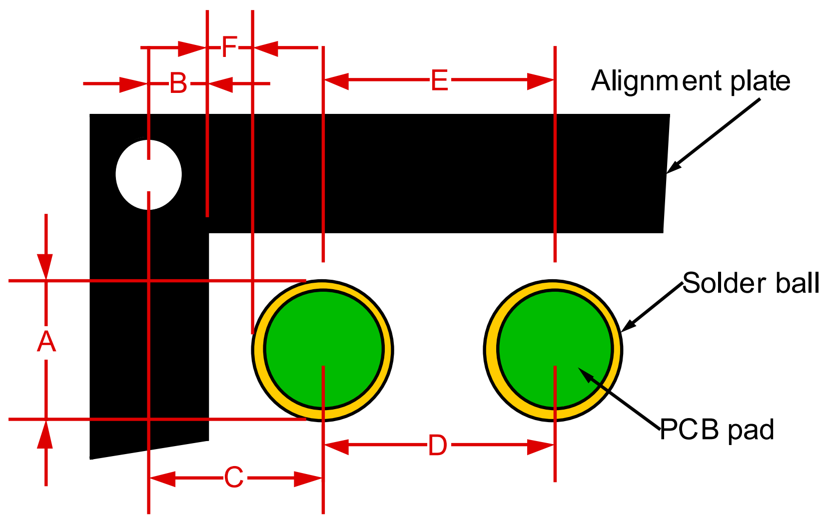
Agenda

- Socket design
- Tolerance analysis
- Elastomer properties
- Electrical characteristics
- Mechanical characteristics
- Transmission line theory
- Conclusions

Socket Design



Alignment Plate Design



A = Ball diameter
B = Hole to edge of alignment plate
C = Hole to PCB pad
D = PCB pad to PCB pad
E = Ball to ball
F = Edge of ball to edge of alignment plate

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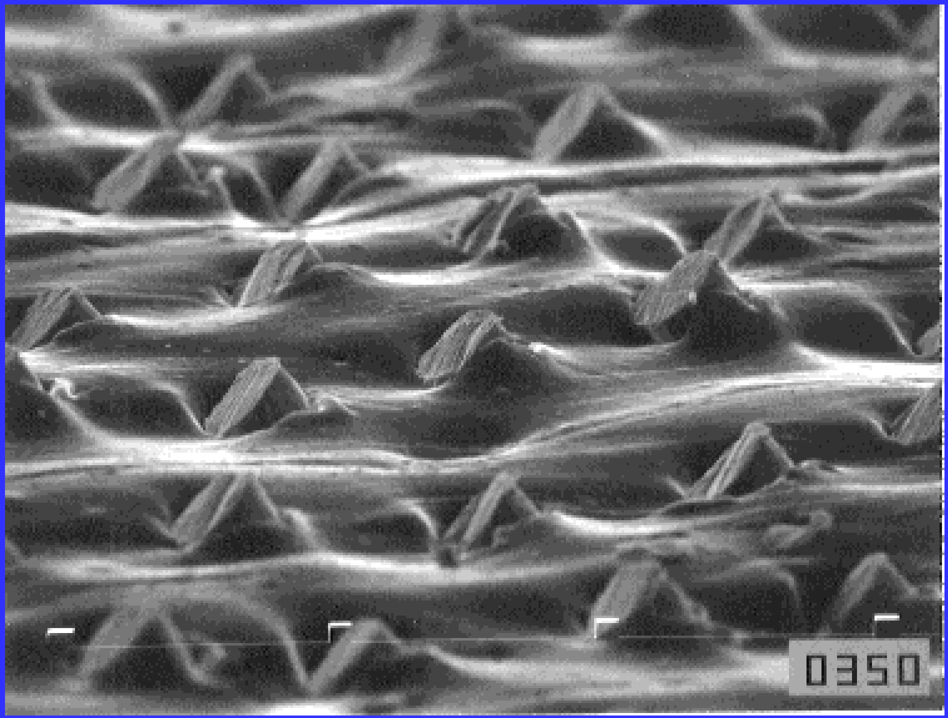
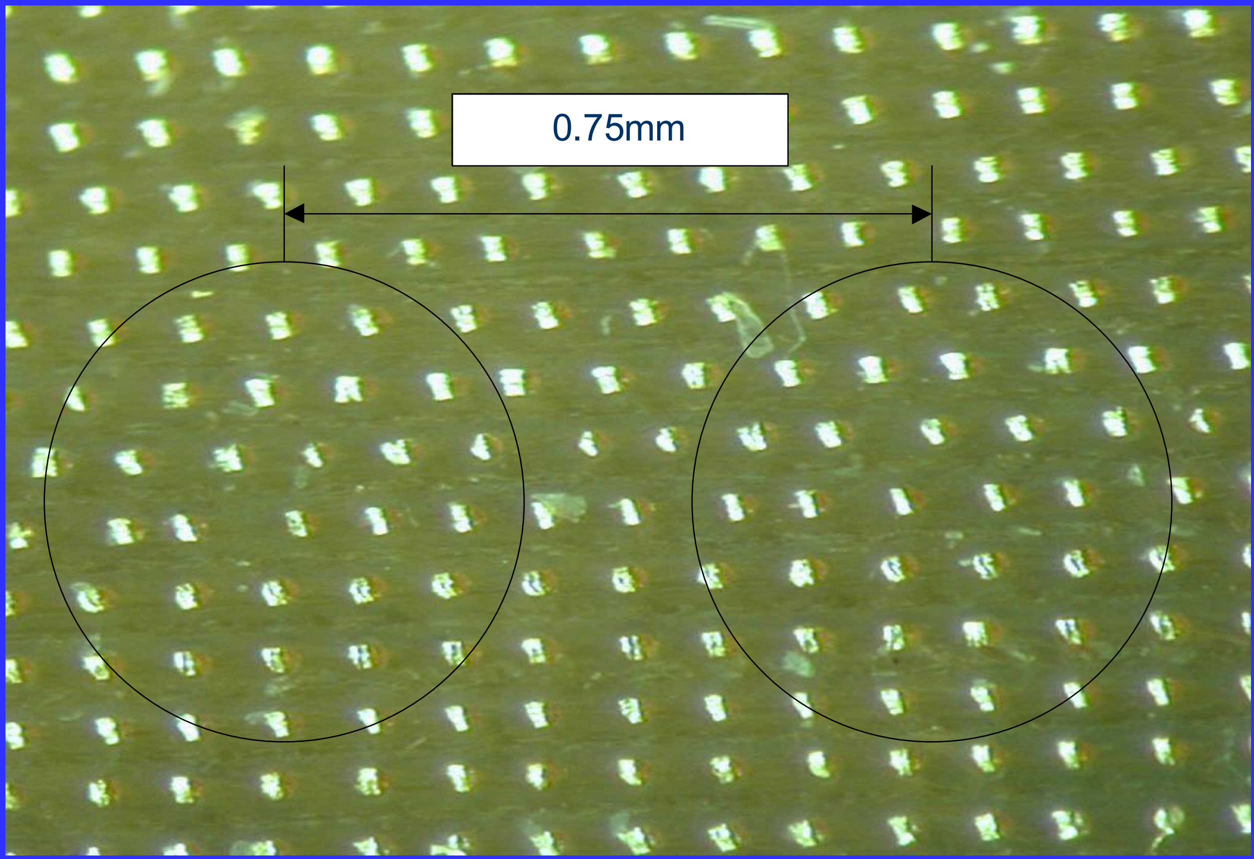
Z-Axis Conductive Wire on Elastomer

- Low-resistance (<0.01Ω) connector
- 30 Micron diameter gold plated brass wires
- Wire density - 0.1mm or less
- 63° angled wire embedded in silicone
- Insulation resistance: 1000 MΩ @500V DC
- 50mA per filament
- Operating temperature: -35° to 100° C

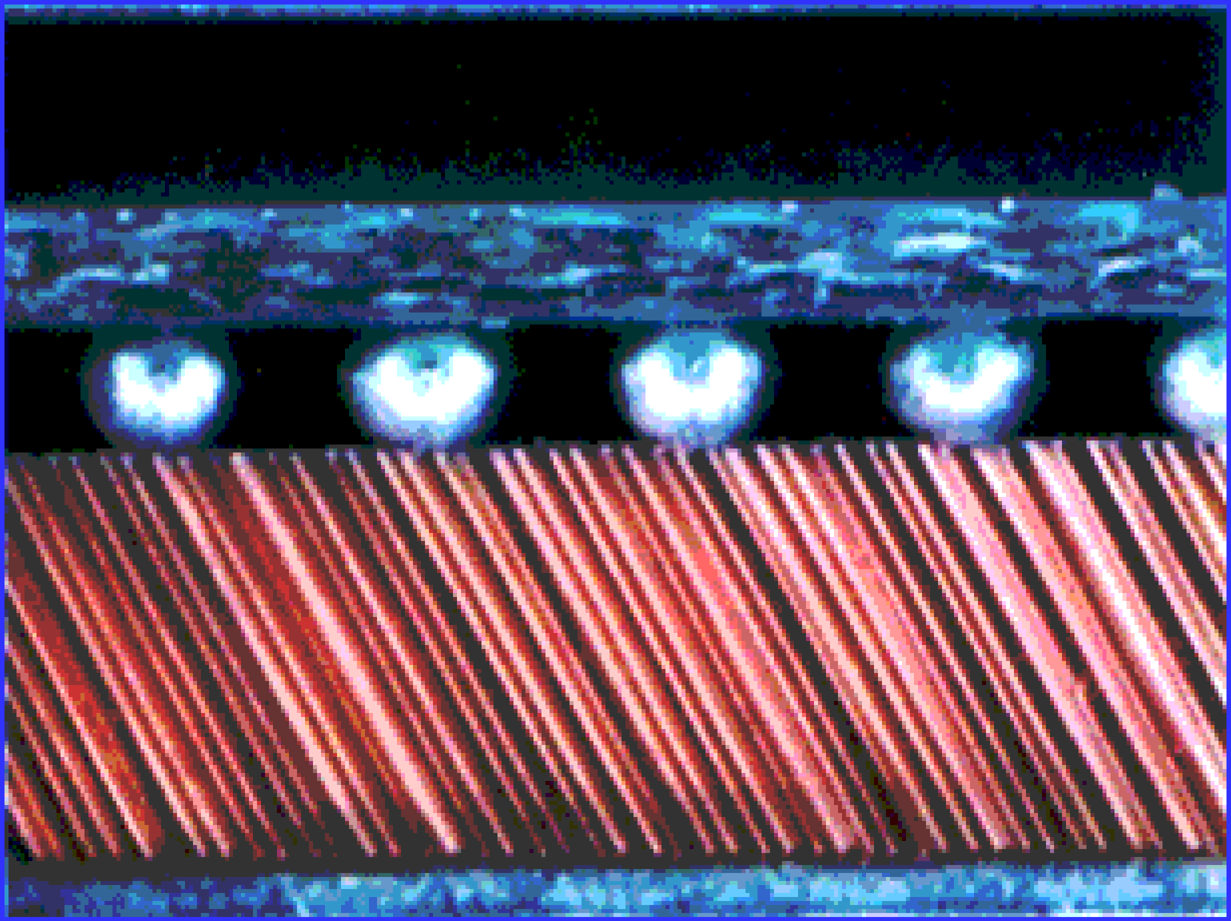
SEM Picture of Elastomer



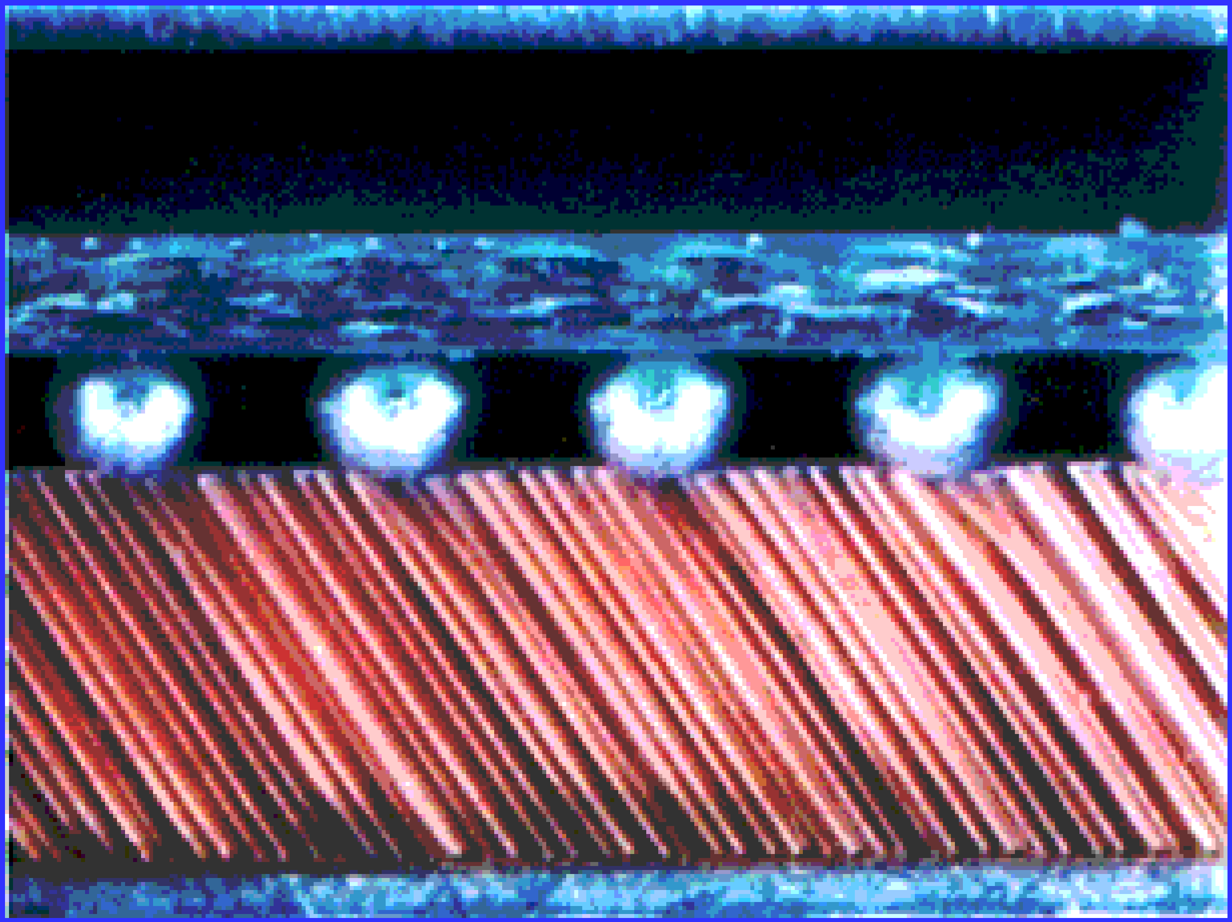
Solder Ball on Elastomer



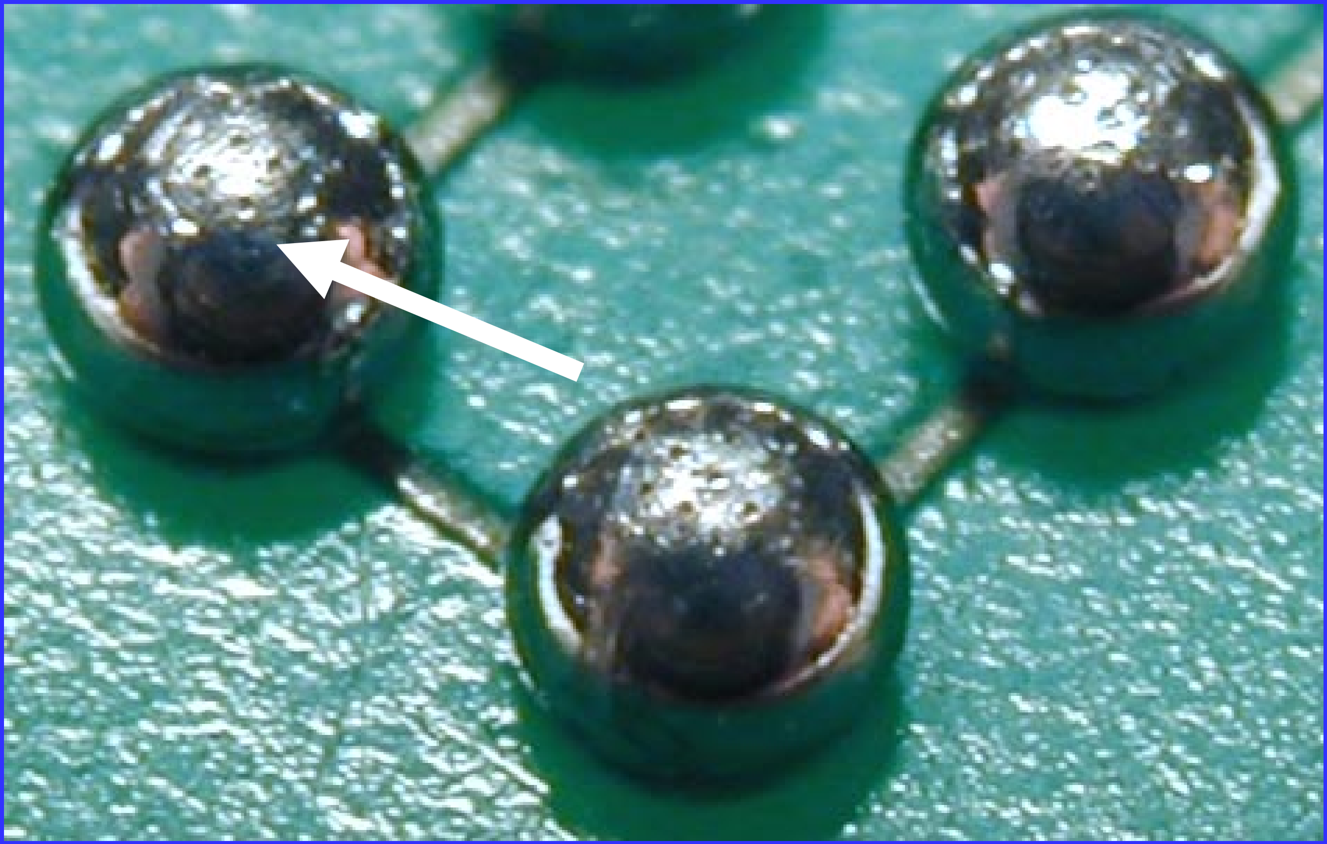
Elastomer before Compression



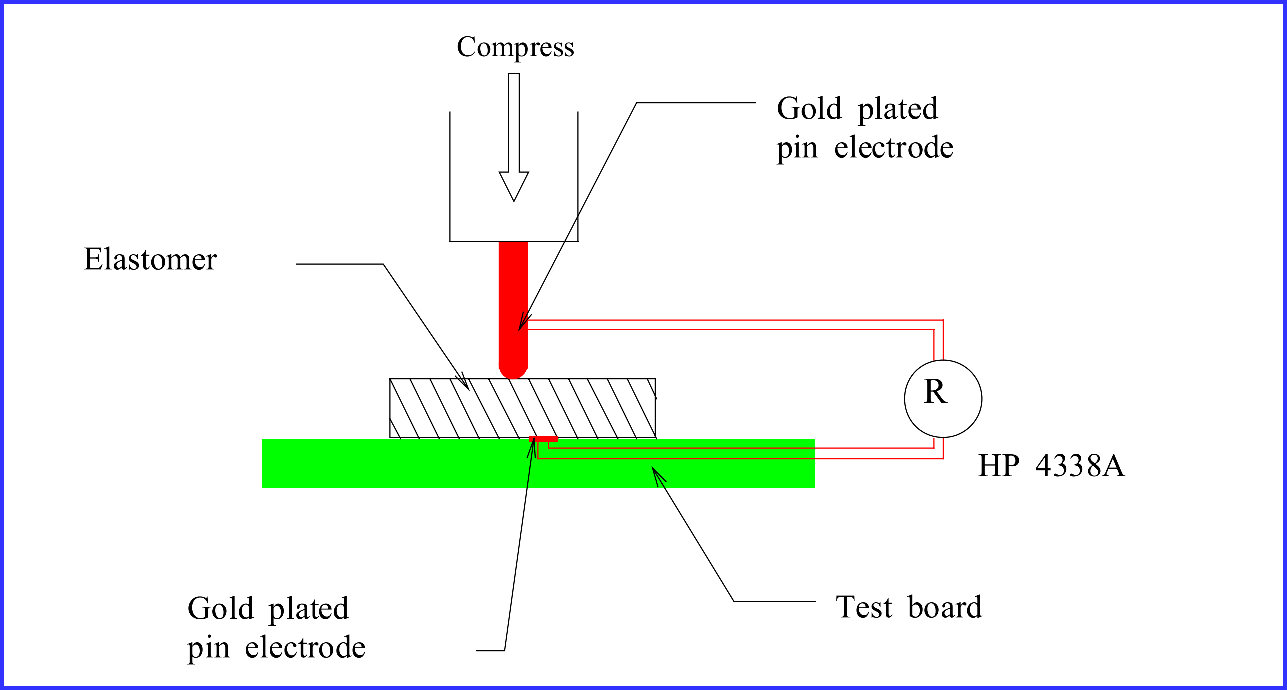
Elastomer after Compression



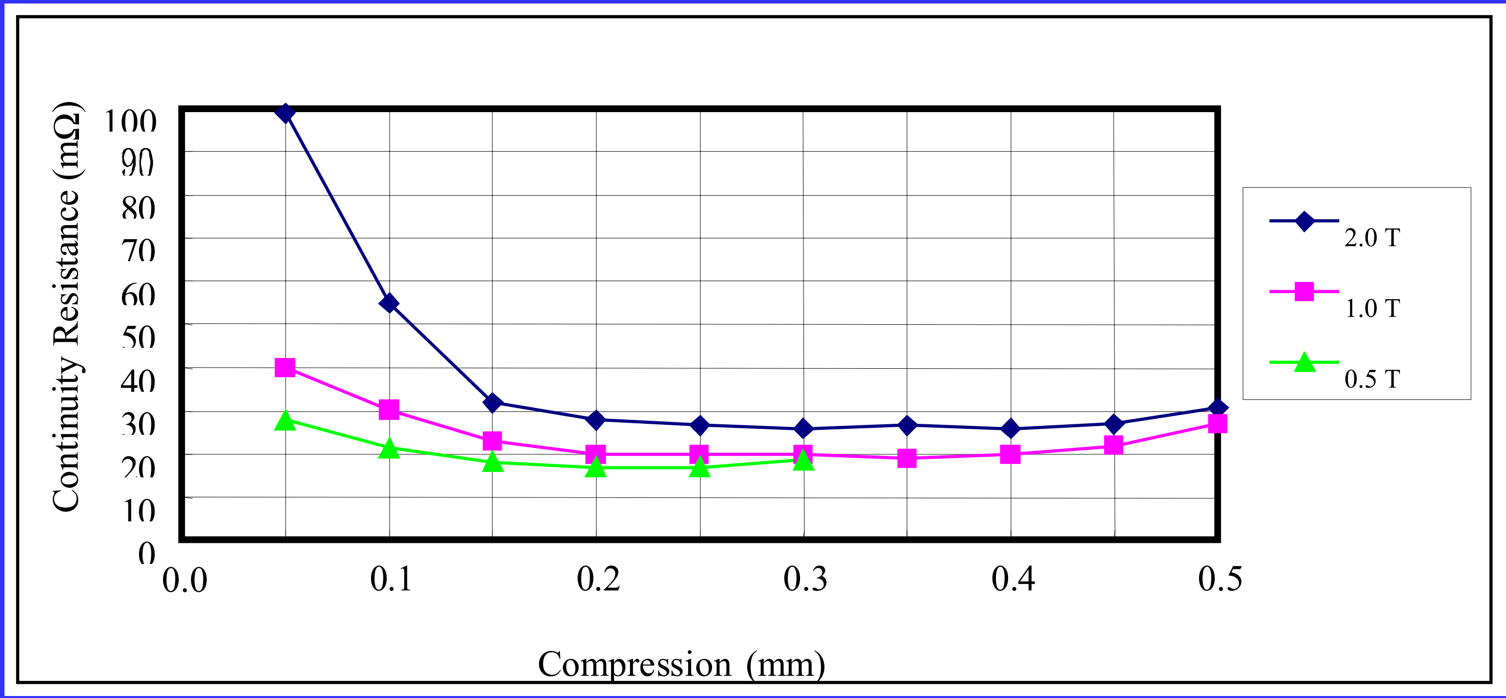
Surface Effect on Solder Ball



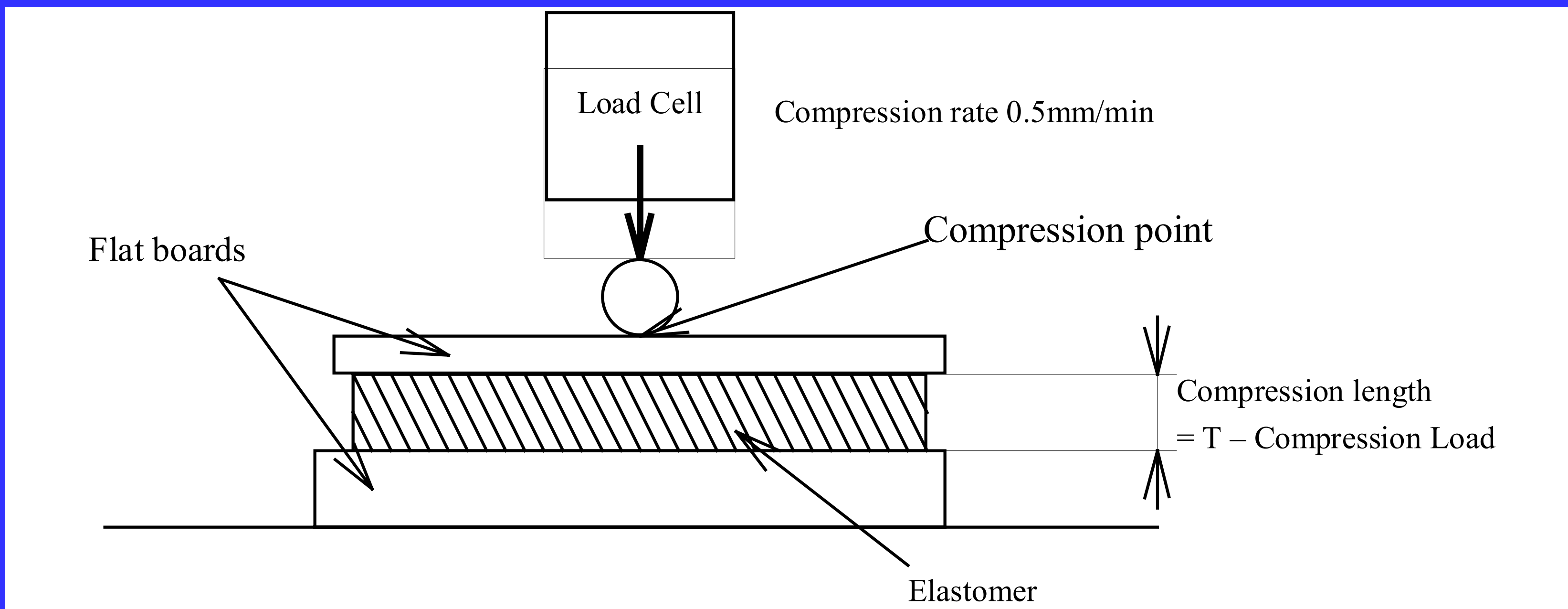
Resistance Test Setup



Compression Vs Resistance



Compression Load Test Setup



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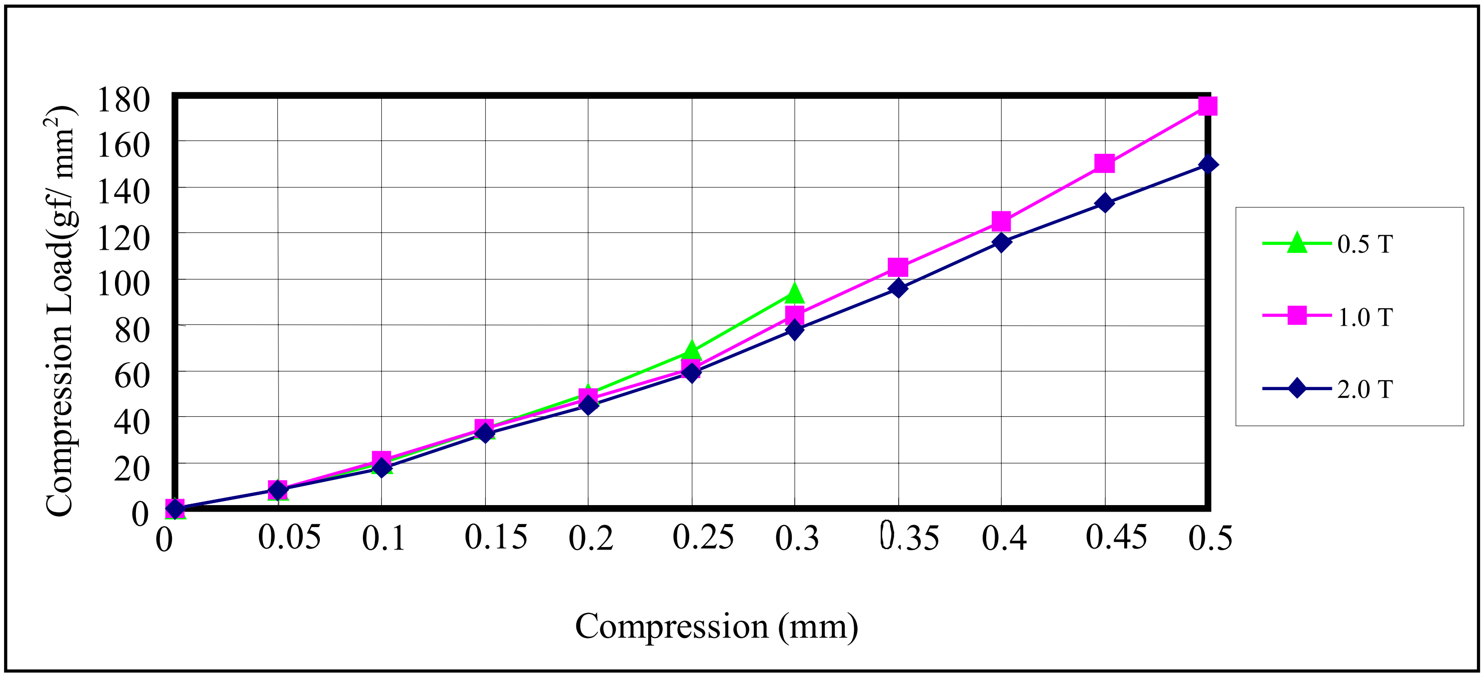
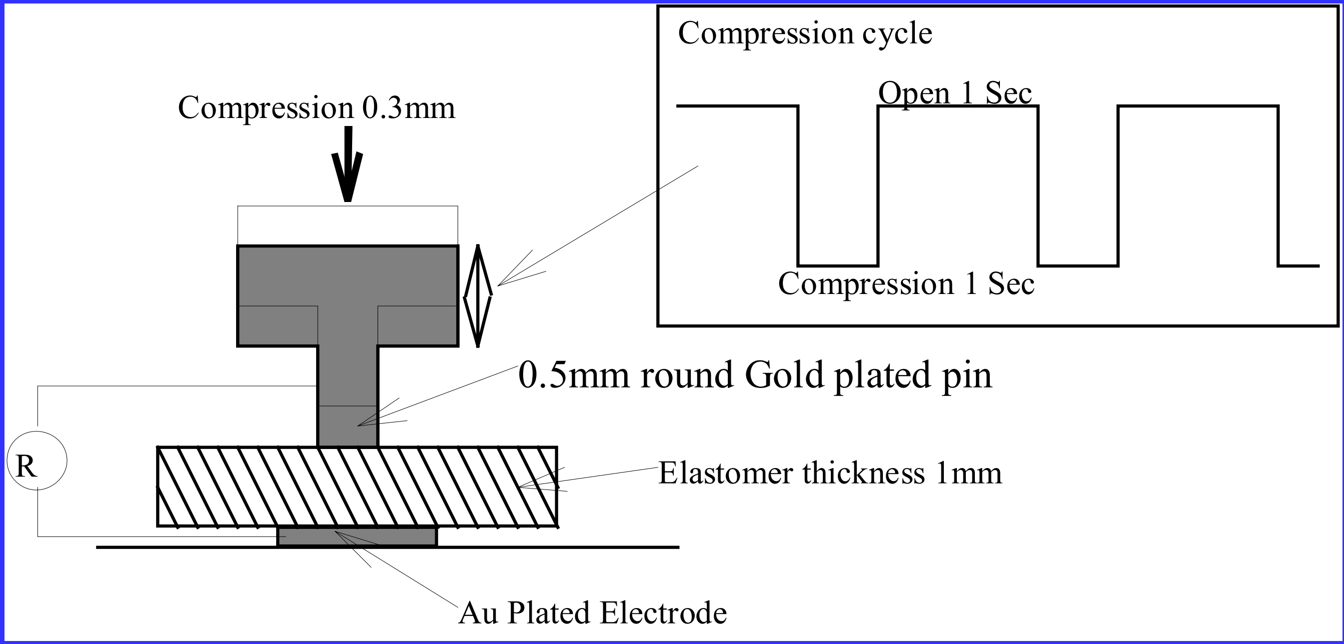
Compression Vs Load



Reliability Test Setup



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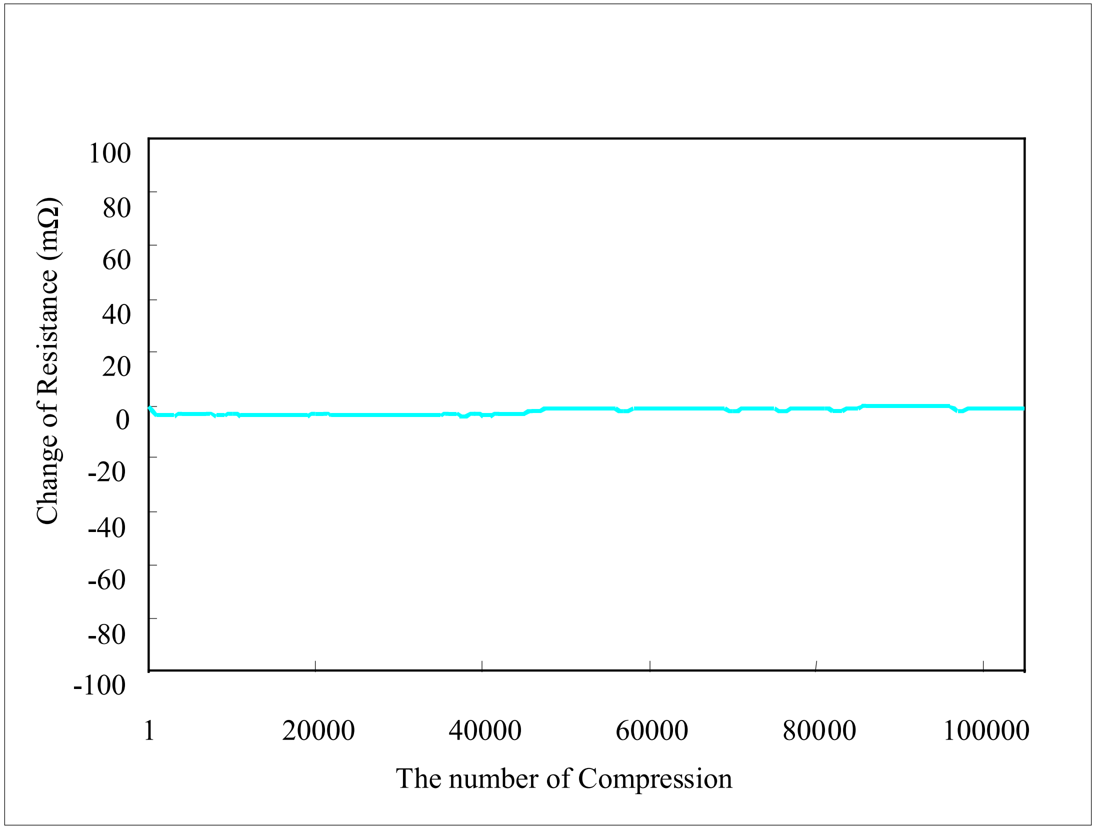
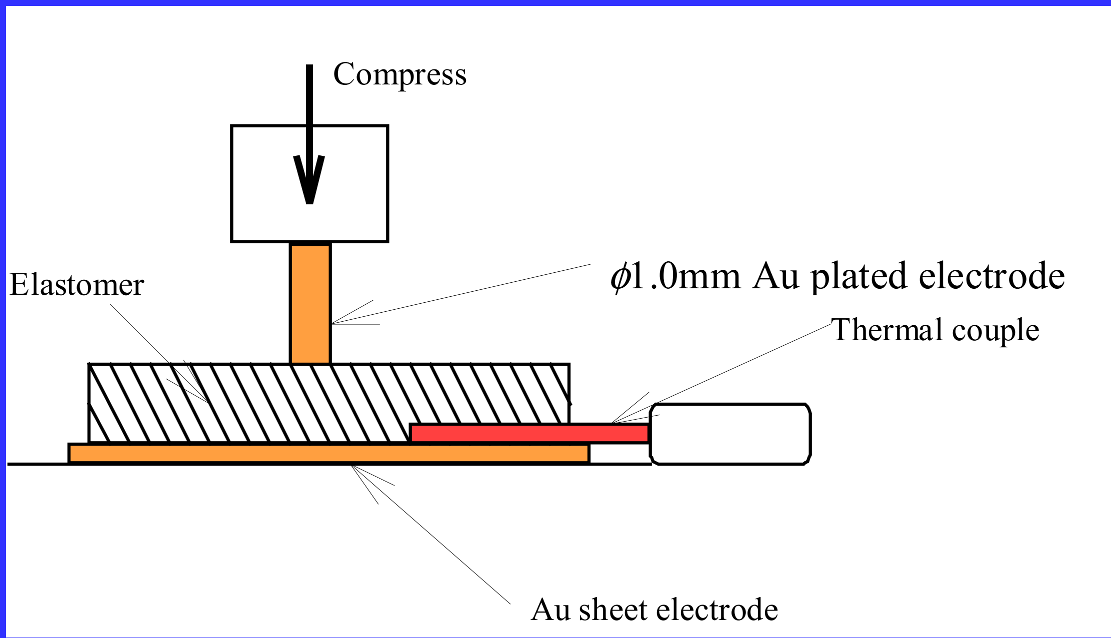
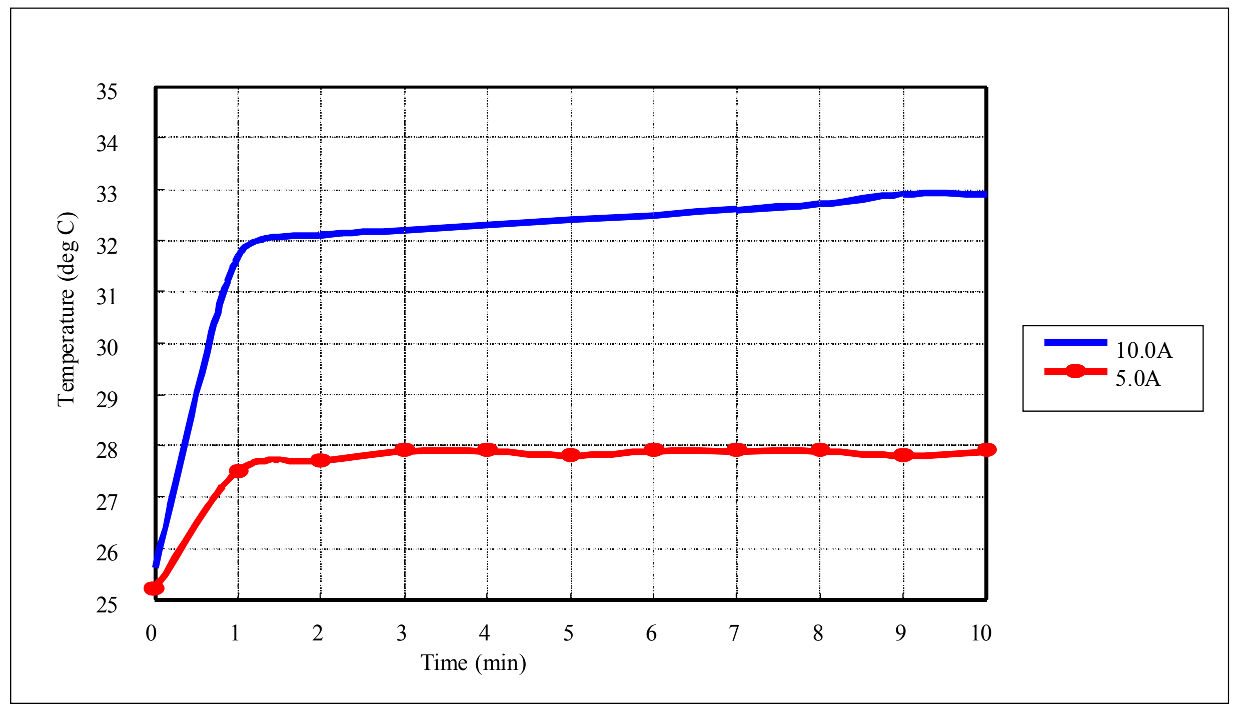
Endurance Characteristics



Test Setup for Measuring Current



Current Carrying Capacity



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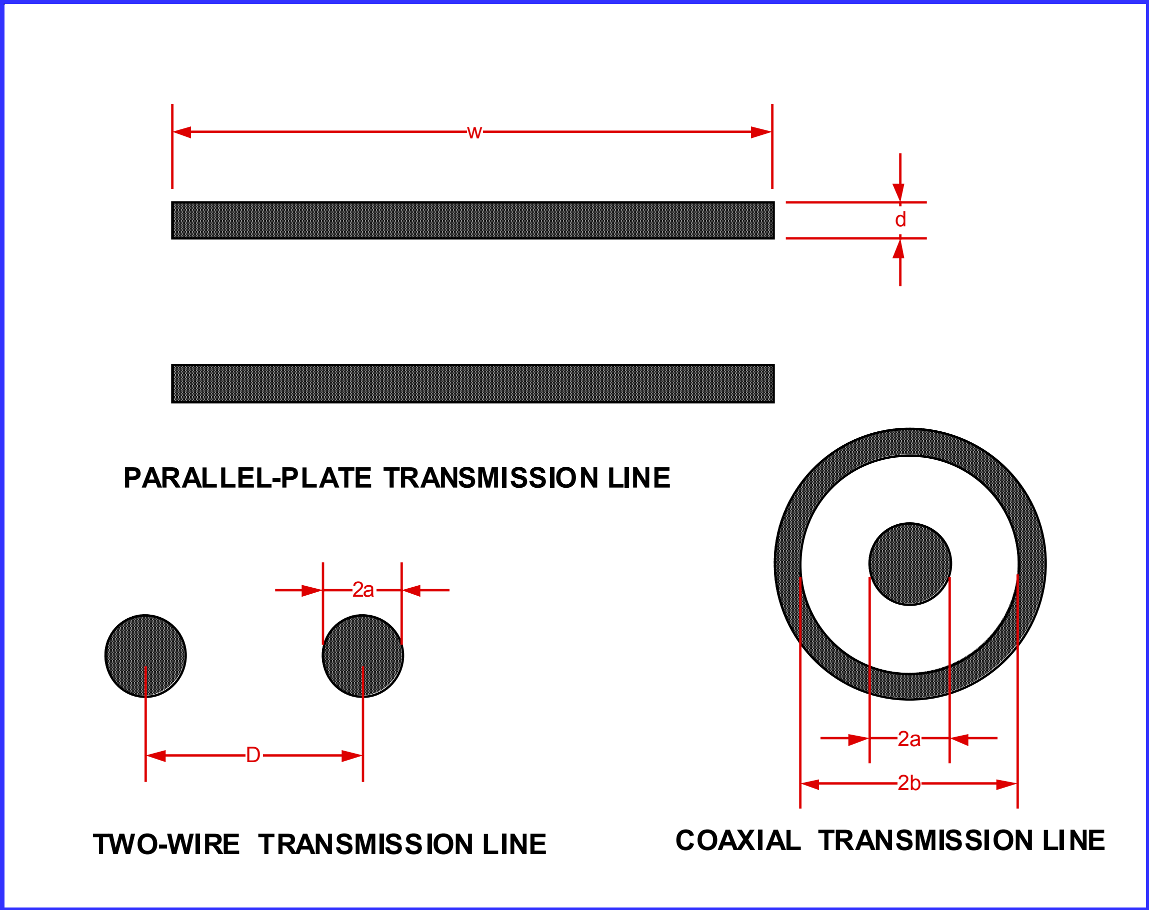
Transmission Line Types



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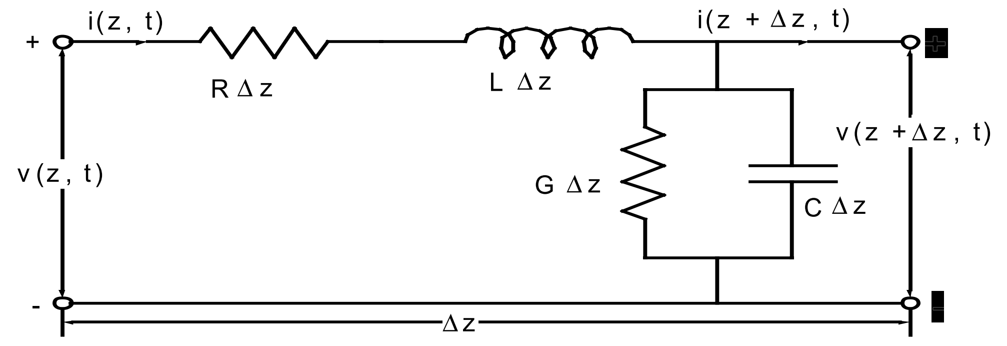
Equivalent Circuit of Transmission Line



Parameter	Parallel-Plate Line	Two-Wire Line	Coaxial Line	Unit
R	$\frac{2}{w} R_s$	$\frac{R_s}{a\pi}$	$\frac{R_s}{2\pi}\left(\frac{1}{a}+\frac{1}{b}\right)$	Ω/m
L	$\frac{d}{w}\mu$	$\left(\frac{\mu}{\pi}\right)\cosh^{-1}\left(\frac{D}{2a}\right)$	$\left(\frac{\mu}{2\pi}\right)\ln\left(\frac{b}{a}\right)$	H/m
G	$\frac{w}{d}\sigma$	$\frac{\pi\sigma}{\cosh^{-1}\left(\frac{D}{2a}\right)}$	$\frac{2\pi\sigma}{\ln\left(\frac{b}{a}\right)}$	S/m
C	$\frac{w}{d}\in$	$\frac{\pi\in}{\cosh^{-1}\left(\frac{D}{2a}\right)}$	$\frac{2\pi\in}{\ln\left(\frac{b}{a}\right)}$	F/m

Source: Fundamentals of Engineering Electromagnetics - David K. Cheng

Results

For 0.3mm thick elastomer:

- Capacitance = 0.006 pF
- Inductance = 0.06 nH
- Resistance < 0.010 Ω

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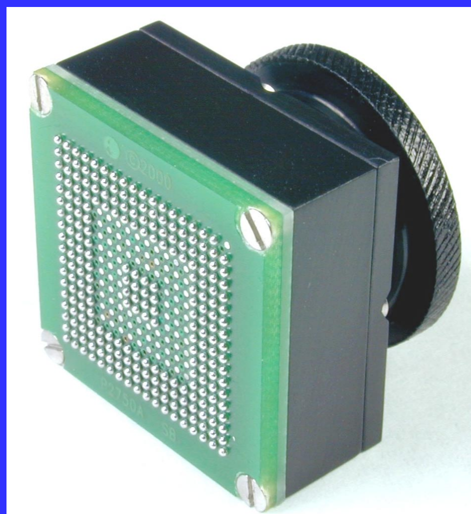
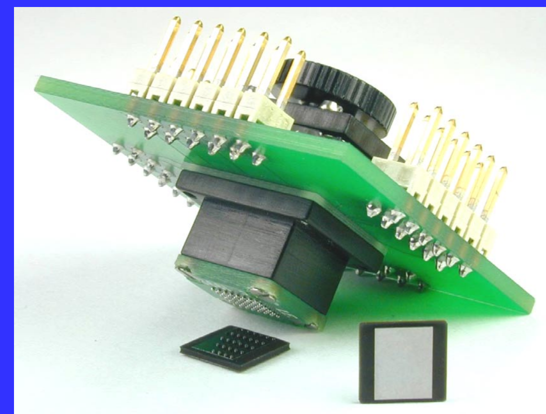
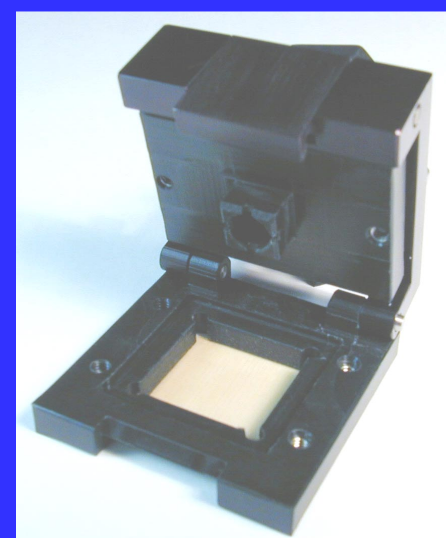
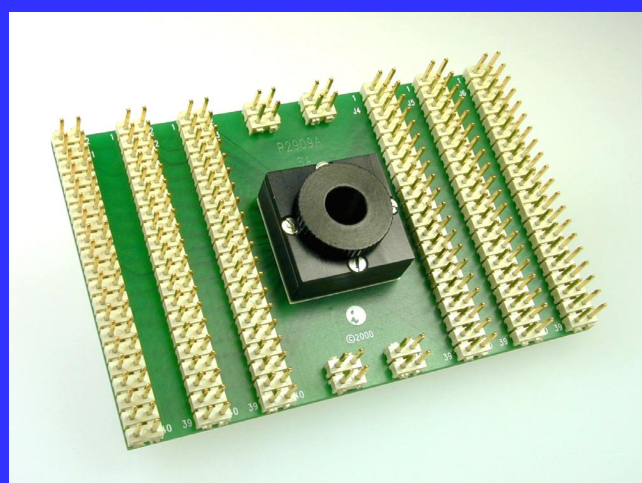
Surface Mount Socket





Solderless Socket





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Conclusions

- Simple design of socket
- Easy manufacturability of components
- Better electrical and mechanical characteristics
- Low compression force per solder ball
- Damage free solder balls
- Fast, dense and durable
- High frequency IC prototyping applications
- Field upgradeable systems applications

Low Cost Thermal Management using Compliant Thermal Interface Materials

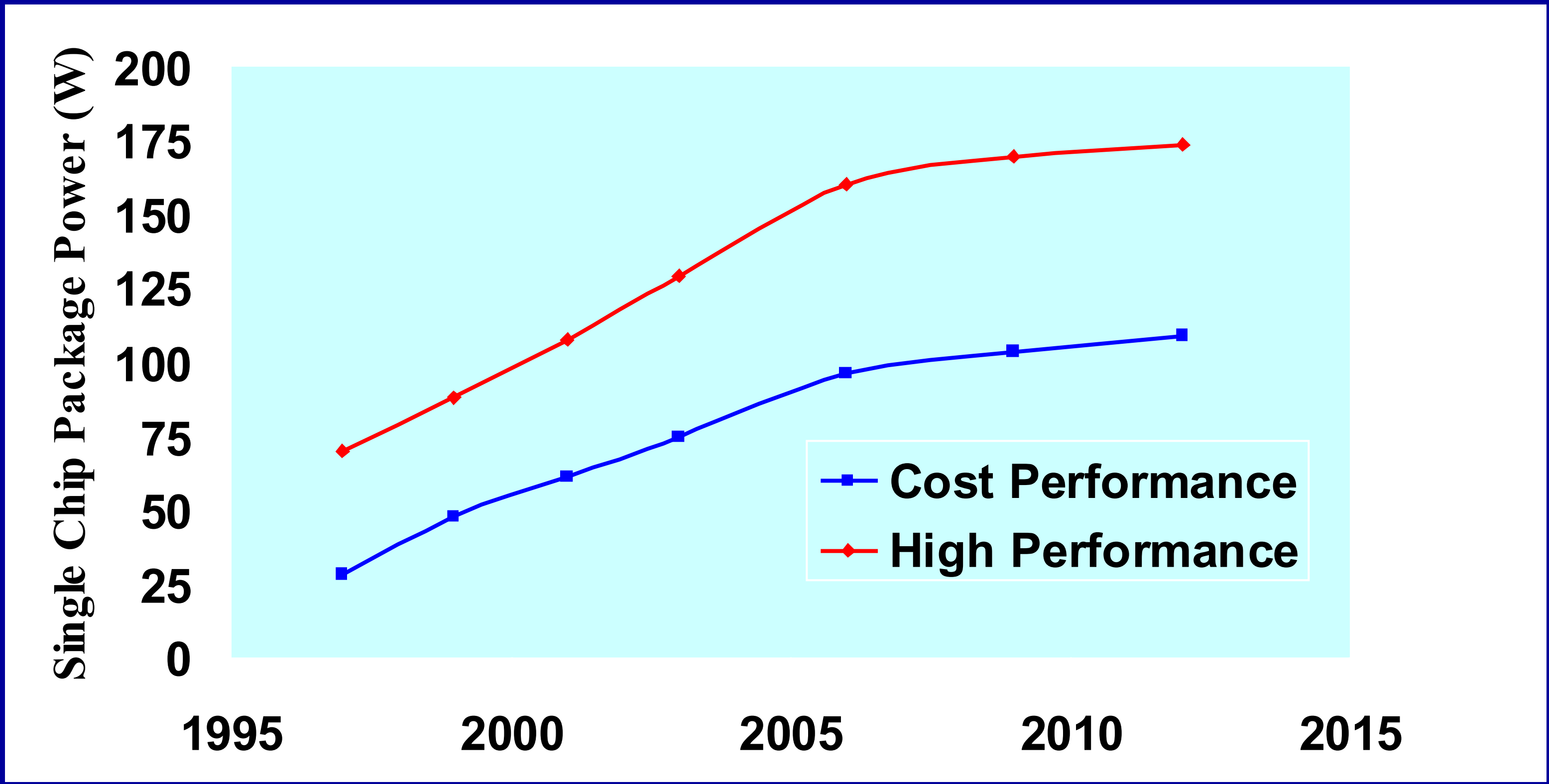
Nancy Dean

Kenichiro Fukuyama
Honeywell Electronic Materials

Honeywell

ELECTRONIC MATERIALS Interconnect Solutions

SIA Roadmap - Projected Power Dissipation



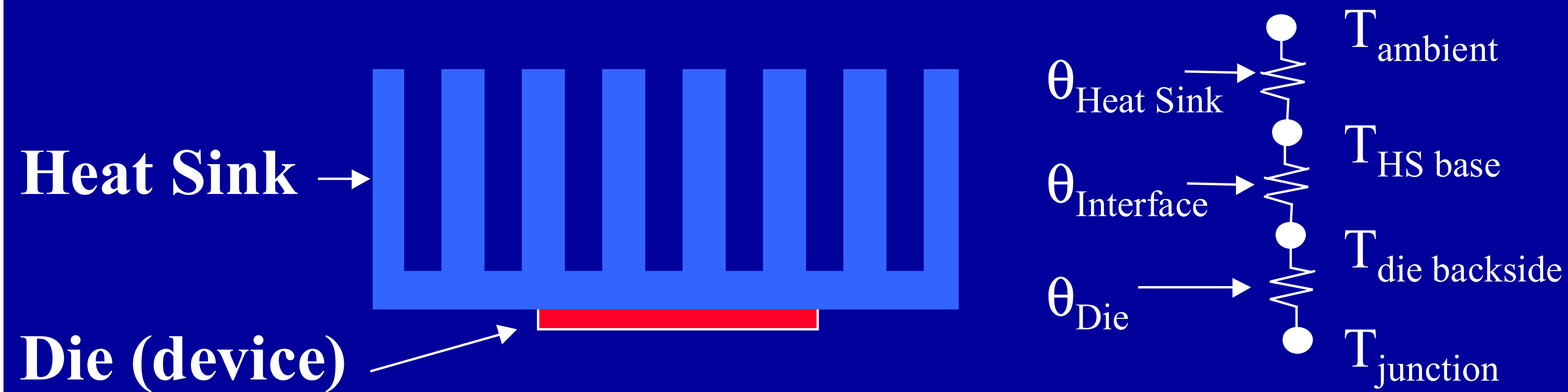
Power Dissipation at Burn-in and Test increases

- Thermal Management becomes more of an issue.

Thermal Resistance Calculations

Total Thermal Resistance =($T_{junction}$ - $T_{ambient}$)/Power

High interface thermal resistance means Heat Sink thermal resistance must be lower (i.e., heat sink larger or more expensive)

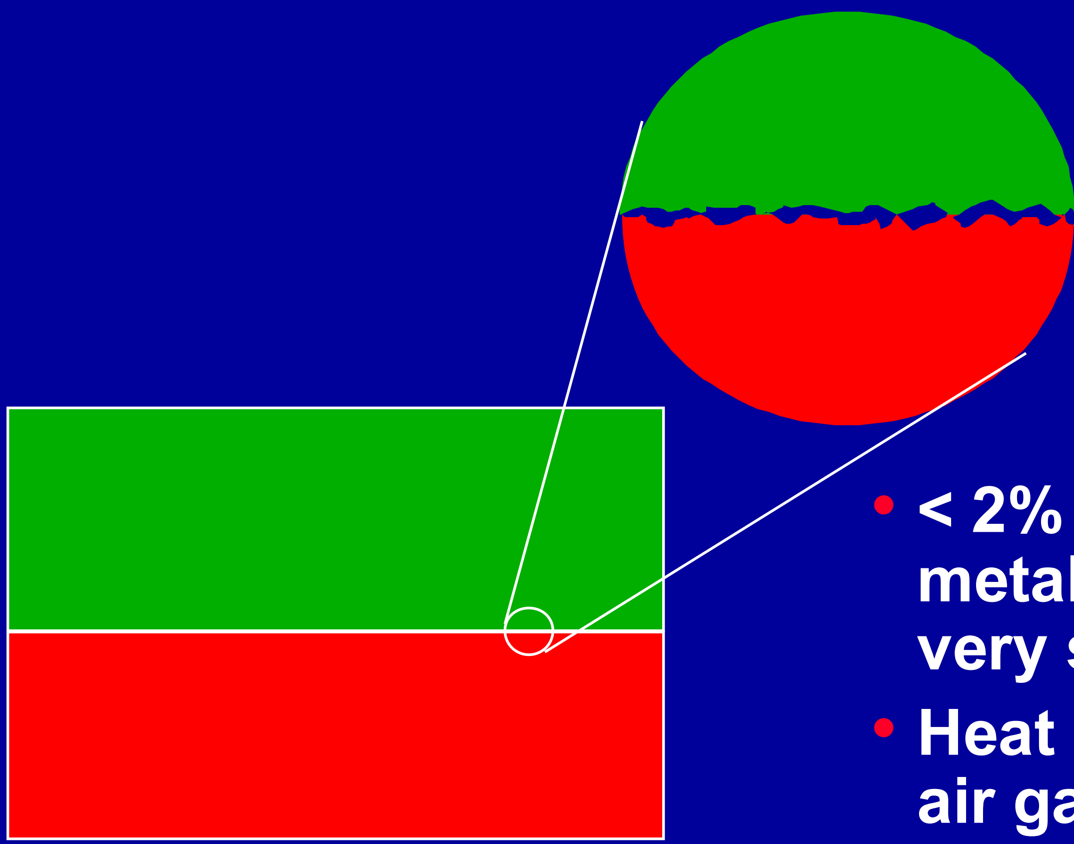


Heat Sink Thermal Resistance

- As a general rule, heat transfer from a heat sink scales with fin area.
- Heat spreading on heat sink base becomes important for large heat sinks.
- High density fins (large number of tall fins per unit length) can be expensive to manufacture.
- Want to minimize heat sink size to allow greater packing of sockets.
- Lowering thermal resistance in the rest of the system allows a less expensive heat sink to be used.

Why is an Interface Material Needed?

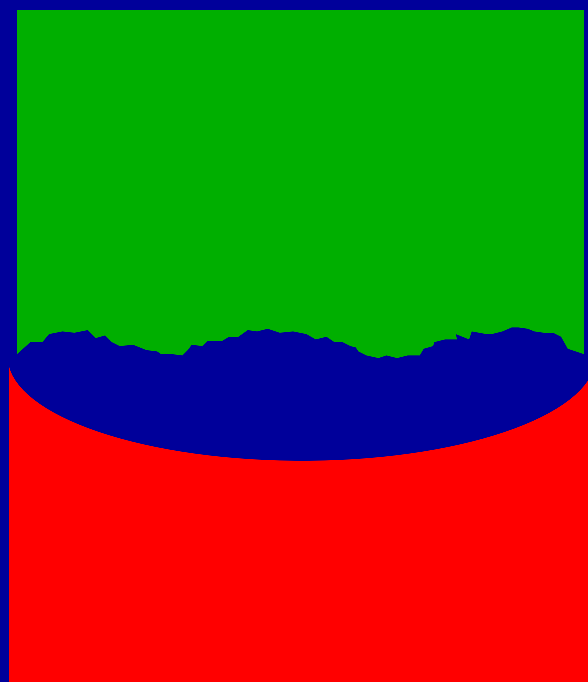
Real Surfaces are not smooth



- < 2% of area is in metal to metal contact, even for very smooth surfaces.
- Heat conduction across air gap is poor.

Why is an Interface Material Needed?

Surfaces are not Planar



- Gaps in interface due to non-planarity.
- Gaps can be quite large.
- Conduction across gap is poor.

Thermal resistance of Interface Material is

$$\theta = (T_{sink} - T_{die})/Q$$

Use of a Thermal Interface Material During Burn-in

- Ideally, you would use no interface material
  - No need to clean
  - No need to replace material after each cycle.
- But, Then
  - Don't have cushioning for die.
  - Usually must polish heat sink base.
  - More of the thermal budget will be occupied by interface thermal resistance $\rightarrow$ larger heat sink.
- Compromise by using an interface material that lasts many cycles, performs well under burn-in conditions but does not leave a residue.

Characterizing interface materials for Burn-in Use

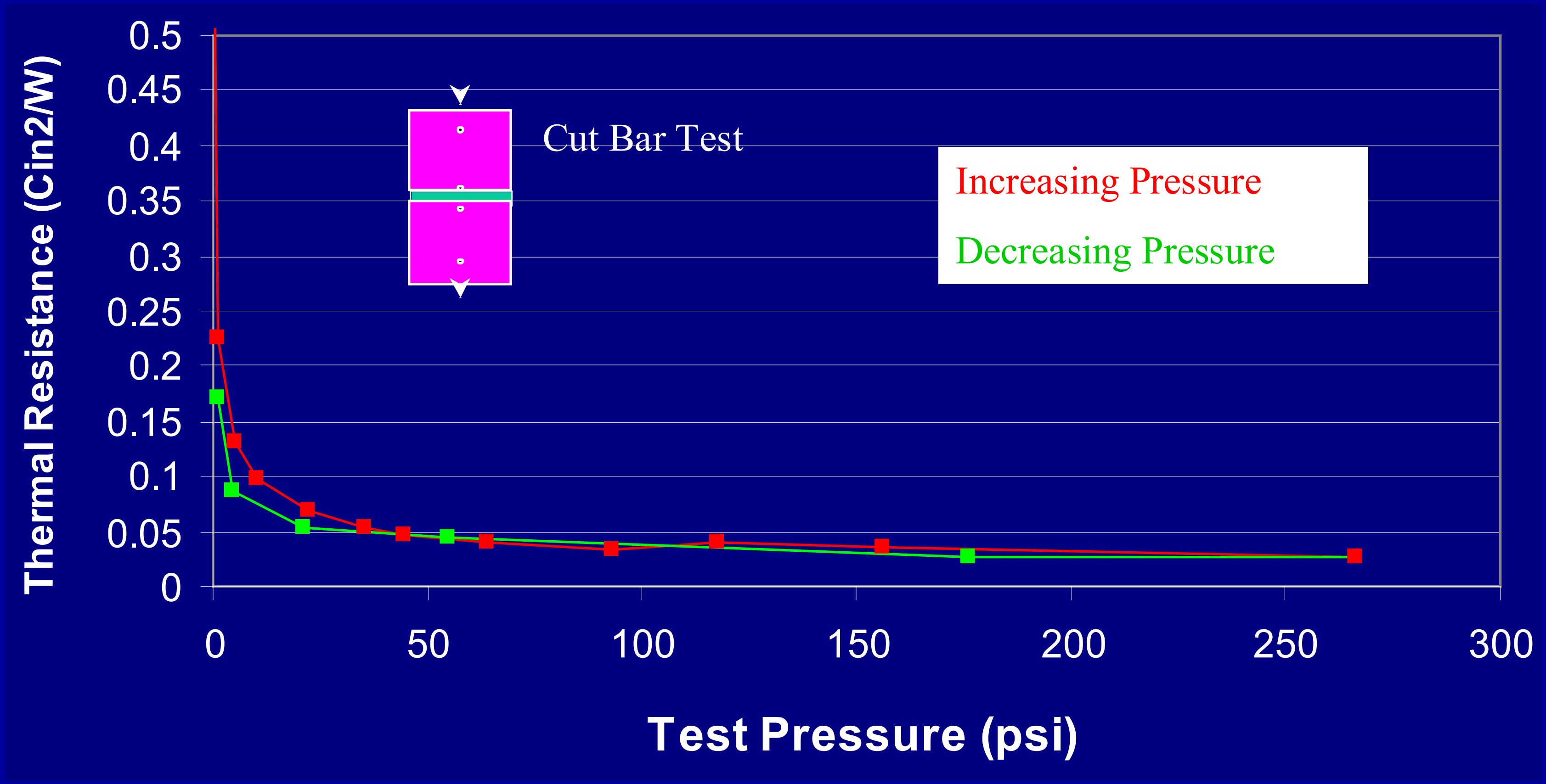
Desired Properties	Typical available Information
Low Thermal resistance	Thermal resistance at one pressure
High Mechanical Compliance	(sometimes) mechanical compliance data.
Robust enough to last several hundred + cycles	No cycling info
Leaves no residue on die that must be cleaned.	No residue info
Easy to use and apply	Some use info
Withstands high temperature burn-in environment with no degradation in properties from lower temperature	No measurement of high temperature properties.

Materials Used in Characterization Tests

Material	Description
A	Silicone Gel material with conductive filler, 0.010” thick
B	Elastomeric Pad with thermally conductive filler, 0.020” thick
C	Graphite foil, 0.020” thick
D	Composite of aligned carbon fibers in polymeric matrix [2], 0.020” thick
D1	Improved version of material D, 0.020” thick

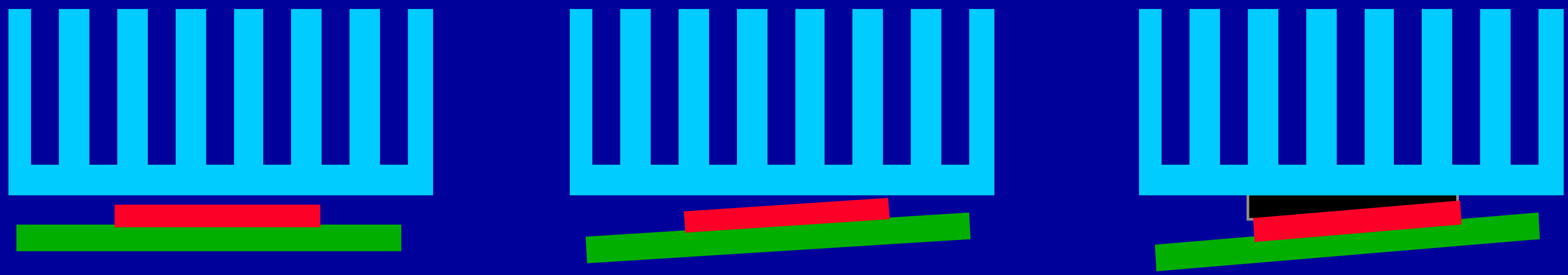
Pressure Sensitivity of Thermal Perf.

Ensure Material Performs Well at pressure in burn-in



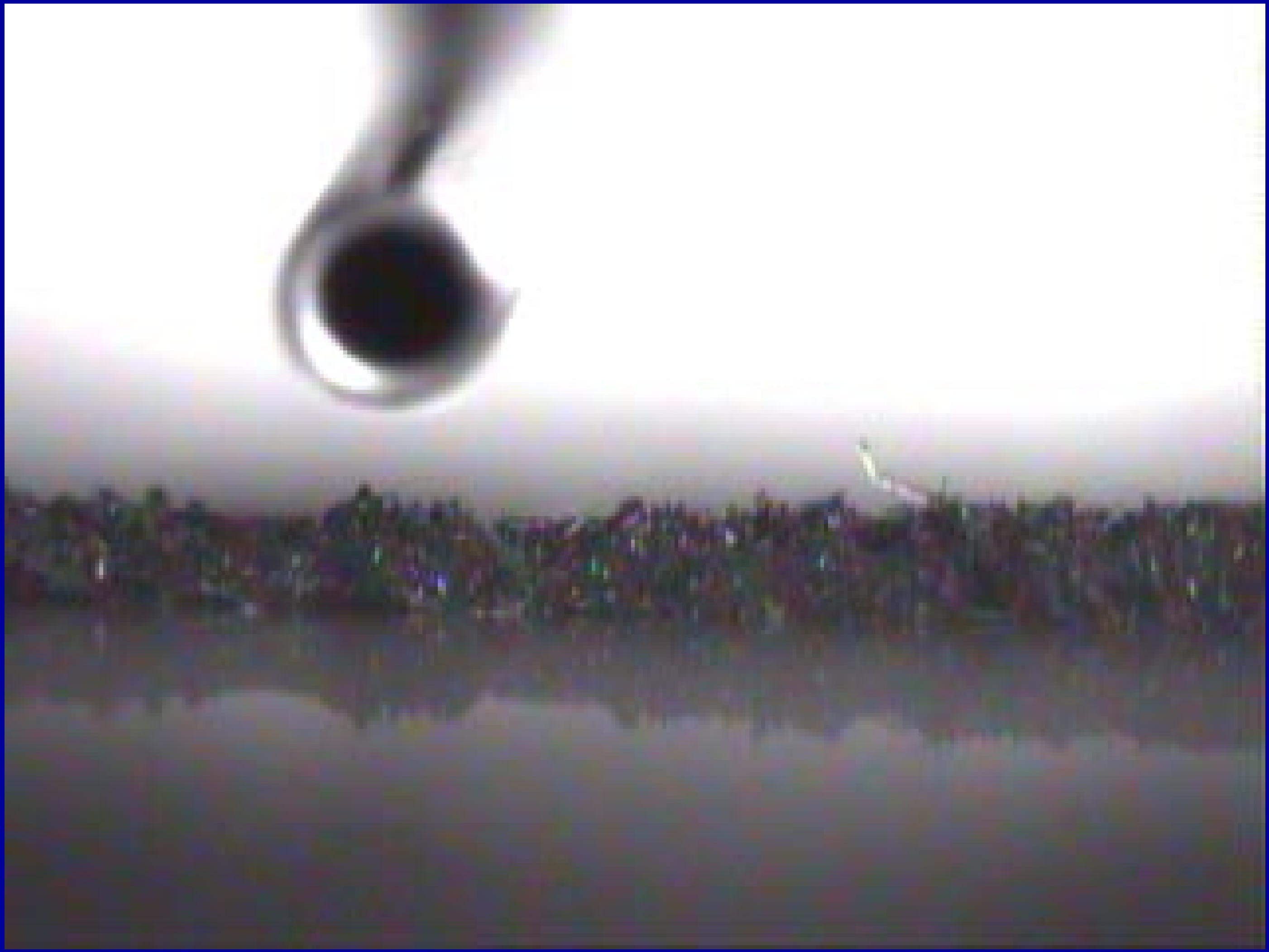
Benefits of Having a Compliant Interface

- Force across die surface and thermal contact can be more uniform.



- Die surface is cushioned
  - will not scratch

- Can absorb tolerances if die height from device to device is different



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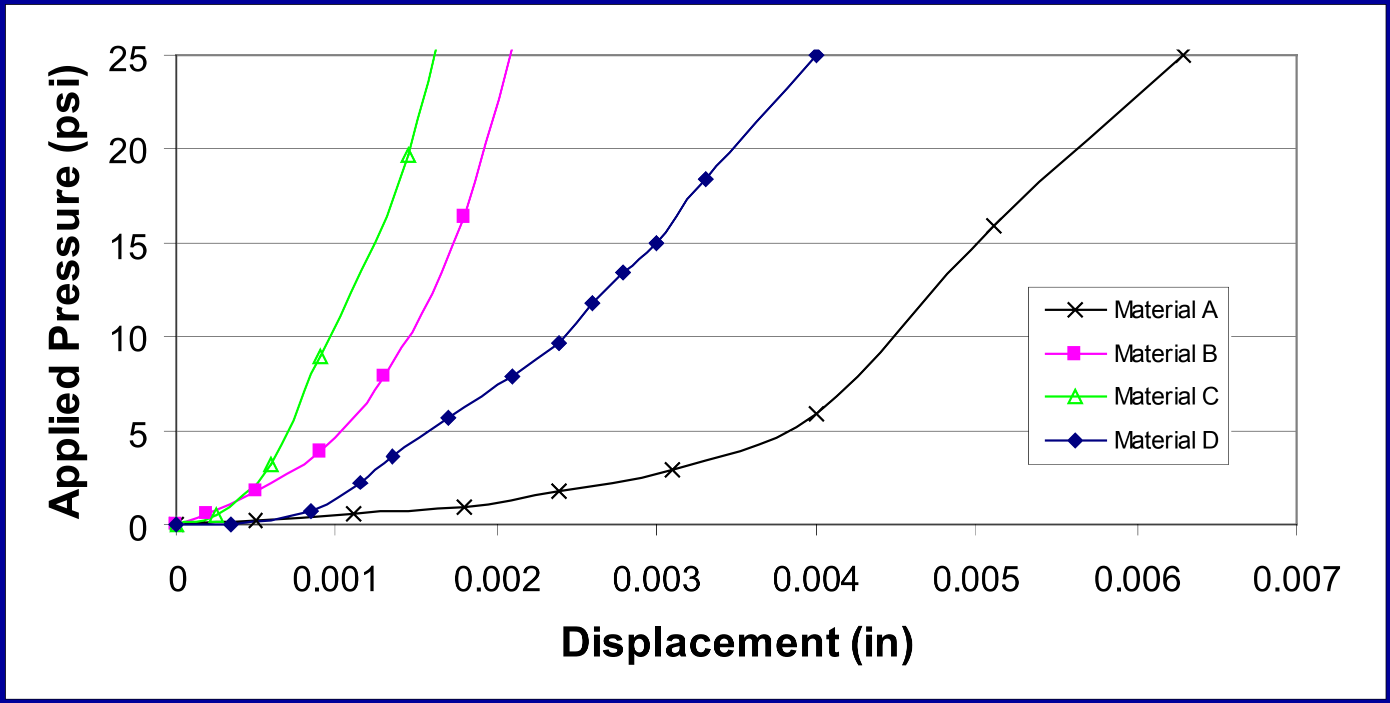
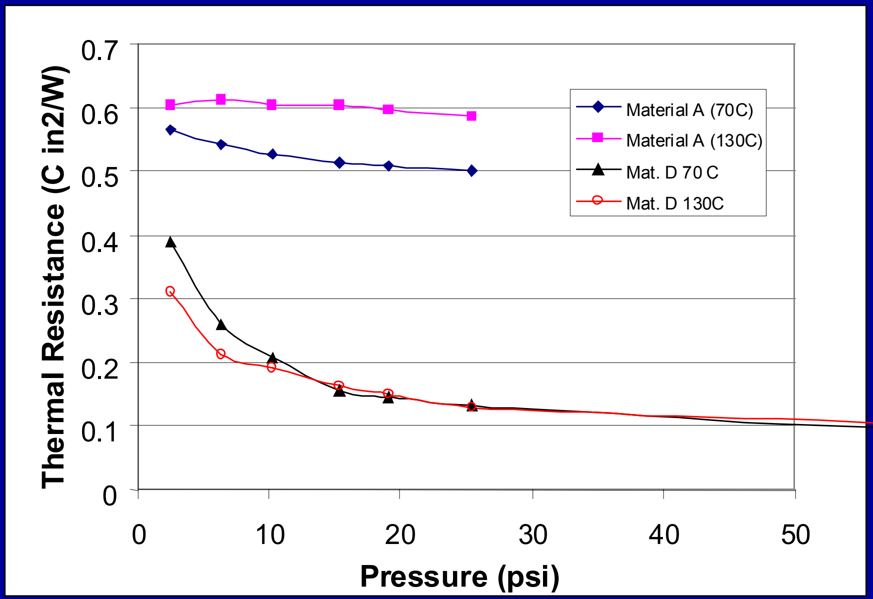
Mechanical Compliance

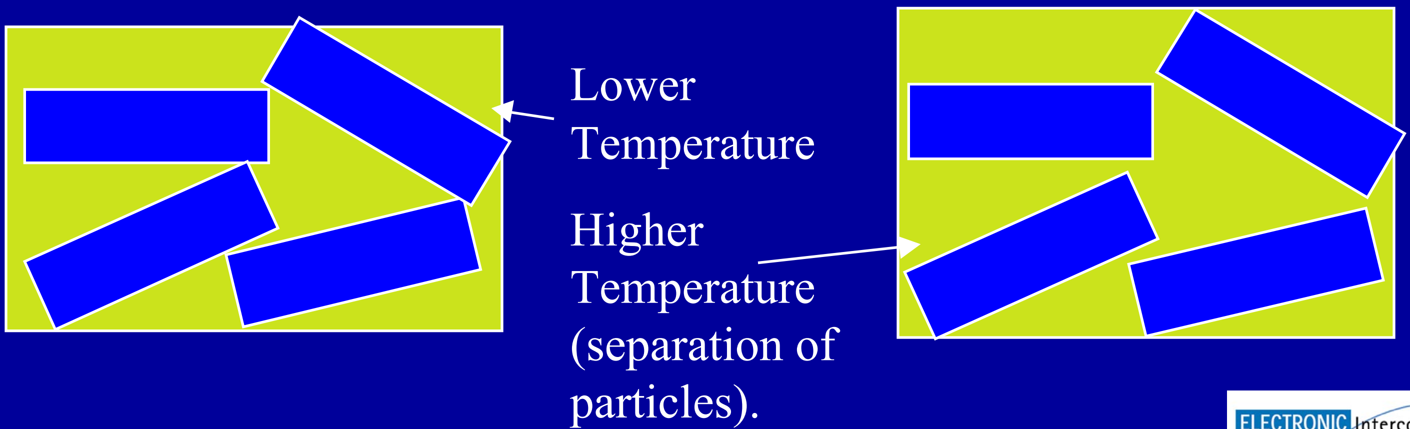


- Many material suppliers report some mechanical compliance.
- Need enough compliance at socket pressure to overcome mechanical tolerance stackups.

Thermal Performance At Elevated Temperature

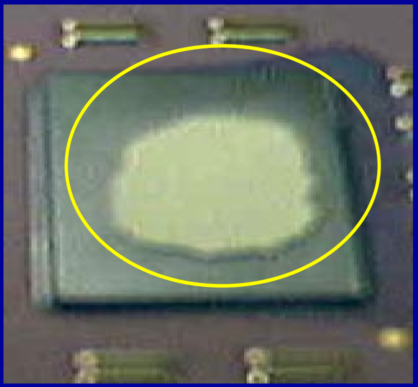


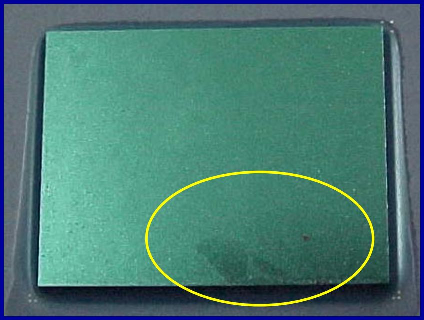
- In general, you want thermal performance reported as a function of pressure.
- Some materials may perform differently at elevated temperatures, so characterization should be done at use temperature.

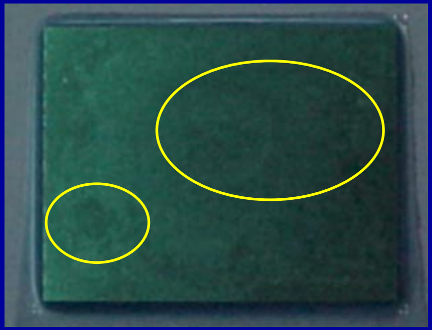


Filmy Residue left on Die

- **Residue Left on die can cause problems with downstream processes**
  - marking
  - bonding
  - thermal interface application
- **Residue must be cleaned, if present.**
- **Metric for characterizing residue is a visual since amount of residue is usually too little to detect otherwise.**
- **Some materials leave an oily film.**

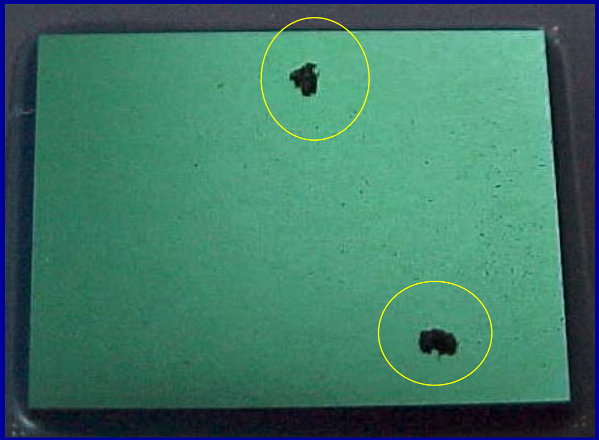


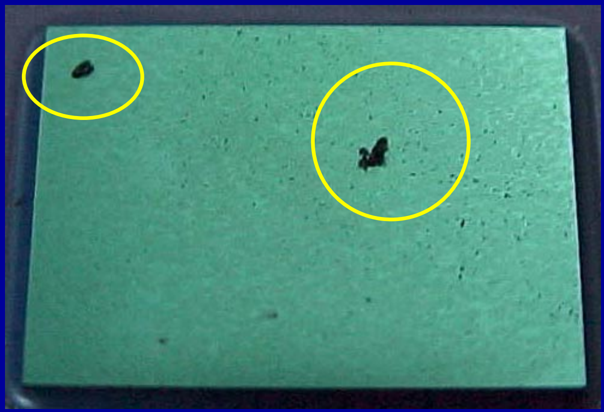




Flake type Residue Left on DIe

- Some interface materials lost chunks of material on the die
  - Chunks could migrate off die and cause problems elsewhere.
  - Interface material performance will degrade as the material falls apart.

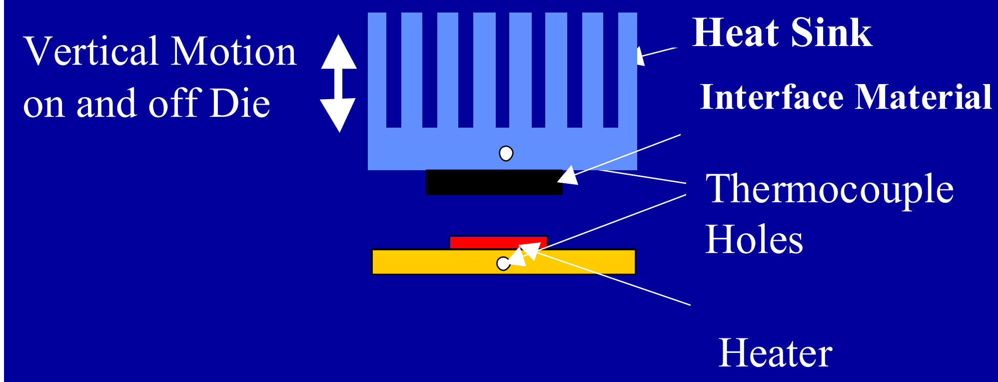


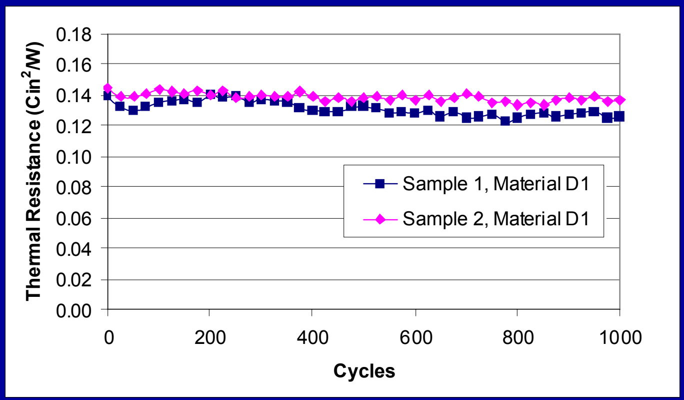


Residue Left on Die

Interface Material	300 pressure cycles at room temperature	20 temp cycles, 25C-150C	Bake 48 hours at 150°C
Material A	Residue	Residue	Residue, sticks to die.
Material B	Residue	Residue	Residue
Material C	No Residue	Flaking	Residue, Flaking
Material D	No Residue	No Residue	Residue Poor adhesion
Material D1	No Residue	No Residue	No Residue Good adhesion

Material Robustness

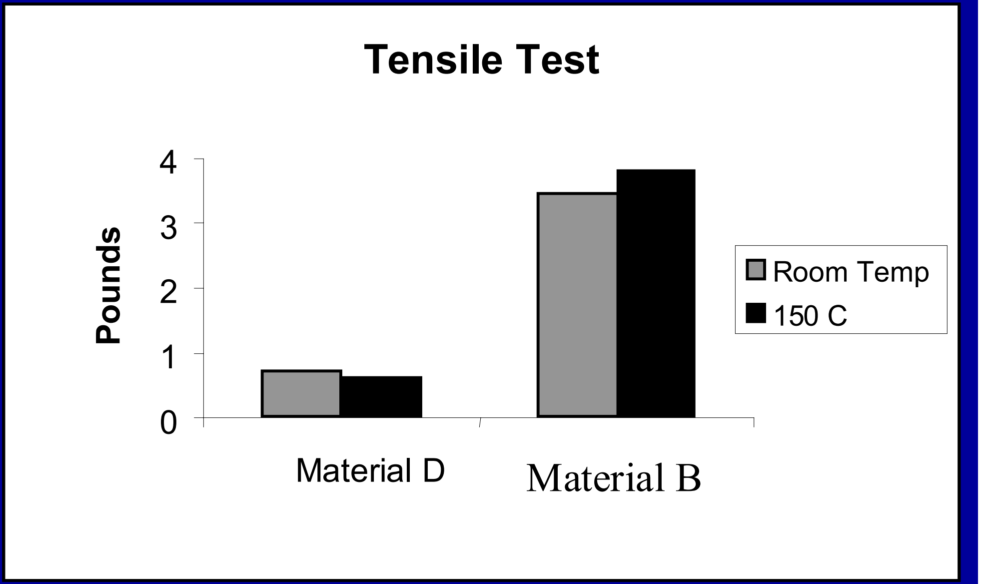




- Want interface material to last many cycles without a degradation in performance.
  - Cycle several hundred to several thousand on-off pressure cycles.
  - Use application temperature
  - Use application pressure
- Cycling tests can be difficult or time consuming to make
  - try to correlate other tests methods or materials properties.

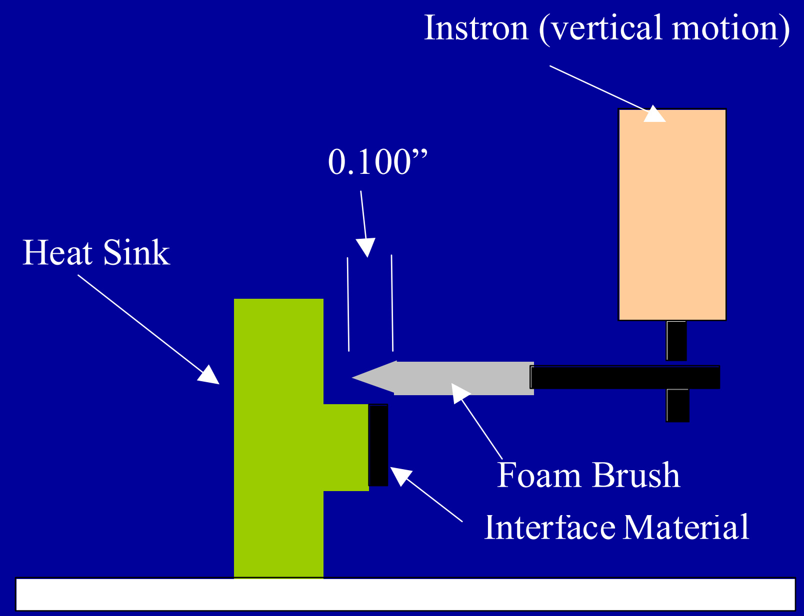
Robustness - Material Strength

- Do a tensile test on material
  - pull a 0.5” wide strip to breaking.
  - Record load at failure
- Tests had similar results at room temperature and elevated temperature
- Results did not correlate with robustness behavior.



Robustness - Abrasion Resistance

- Cycling, particularly with a clamshell socket, is more represented by abrasion.
- Standard abrasion tests are too severe.
- Tried to automate an abrasion tests using a soft, foam brush.
  - Materials that tended to flake or tear in cycling failed here



Cost Advantages in Using an compliant interface

- Use lower thermal resistance heat sink
  - Smaller heat - can put more sockets per board
  - Reduce fin height - reduce distance between boards/racks
  - Reduce heat sink aspect ratio (fin packing) leads to a less expensive heat sink
- Yield improvements
  - mechanical cushioning of die will reduce breakage or damage.

Summary

- Using an interface material for a burn-in thermal solution may enable lower cost heat sinks to be used.
- Burn-in is a severe environment for an interface material.
- Conventional interface tests do not tell everything that is needed to predict success in a high temperature, repetitive assembly environment.
- Conventional tests that are of interest are
  - Thermal resistance as a function of pressure
  - Mechanical compliance
  - Bake tests

Summary

- New characterization methods that did correlate with burn-in suitability
  - High temperature bake in contact with silicon die
  - abrasion test
  - high temperature thermal resistance
- Characterization methods were used to optimize a material (D) for burn-in use
  - Maximize mechanical cycling
  - minimize residue
  - maintain good thermal performance at elevated temperatures

[redacted]