



Burn-in & Test Socket Workshop

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Mesa, Arizona

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Technical Program

Session 6

Tuesday 3/06/01 10:30AM

Thermal Management Approaches

“Dynamic Junction Temperature Control For Lidded C4 Packages”

Joe Hovendon - Schlumberger

“Approaches To Thermal Management Of High Power Devices”

Paul Nesrsta - Reliability Incorporated

“Dixie Chips - 'Too Hot To Handle'”

Jim Ostendorf - Dynavision

Dynamic Junction Temperature Control for Lidded C4 Packages

2001 Burn-in and Test Socket Workshop



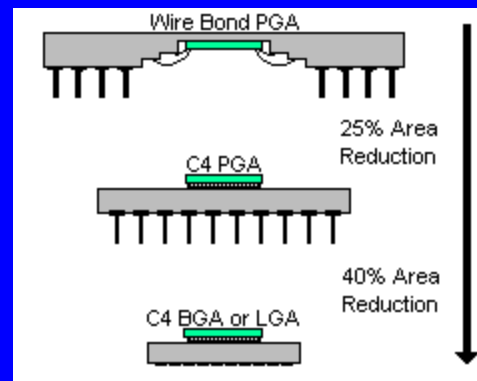
Joe Hovendon
Product Manager, Schlumberger

Agenda

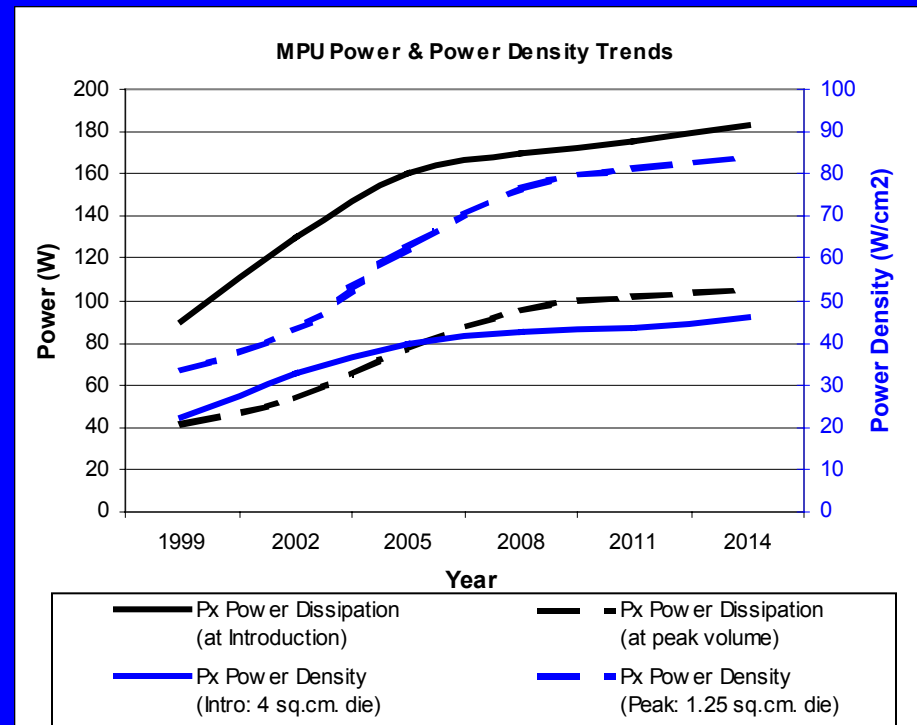
- **Package Shift to C4**
- **MPU Power Roadmap**
- **Lidded C4 Package Detail**
- **C4 Package Thermal Circuits**
- **Lidded vs. Non-Lidded T_j error (passive control)**
- **Active Conduction Thermal Control Solution**

Packaging Shift for MPUs

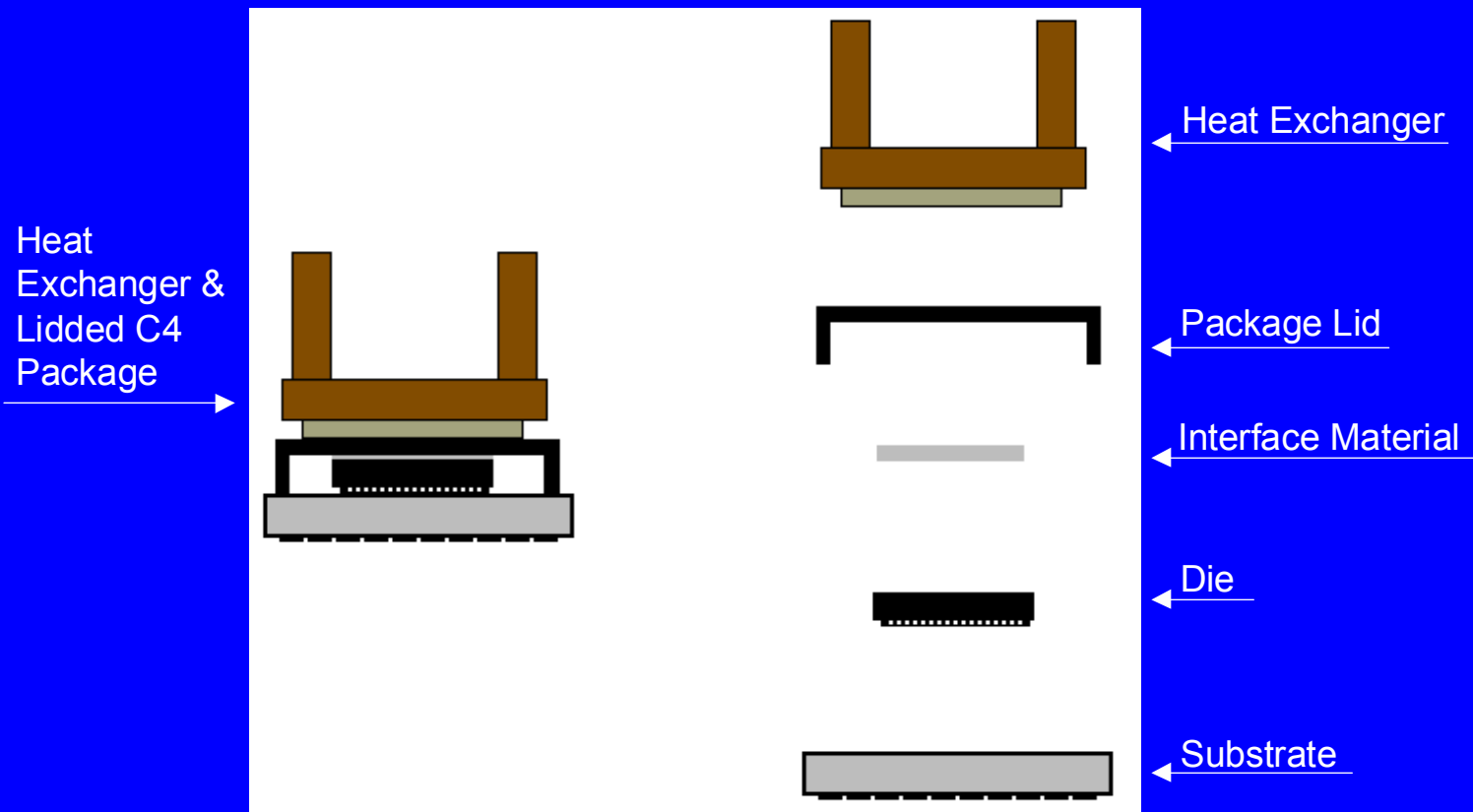
- MPUs are shifting to C4 packaging for improved electrical and thermal performance



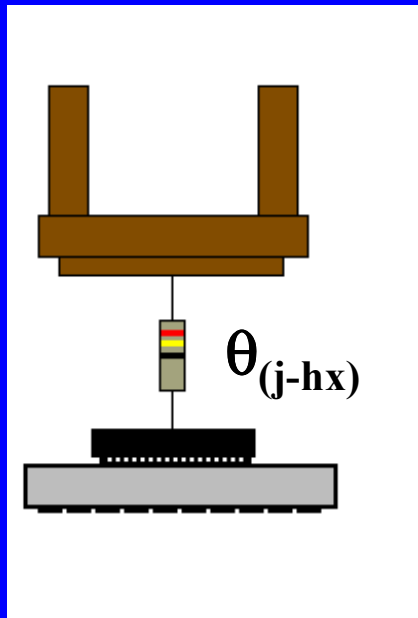
Power Density Roadmap



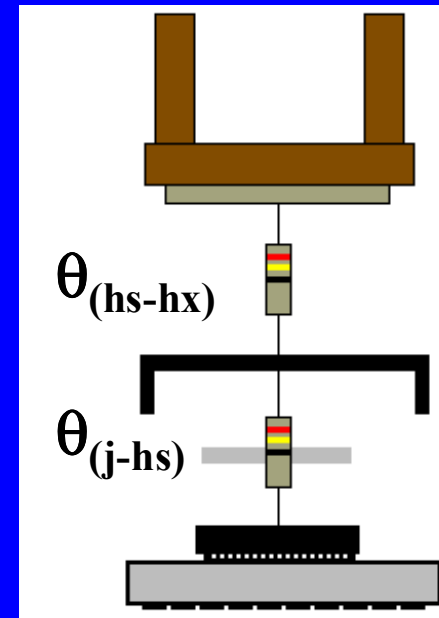
Lidded C4 Package Details



Lidded vs. Non-Lidded C4 Package Thermal Circuits

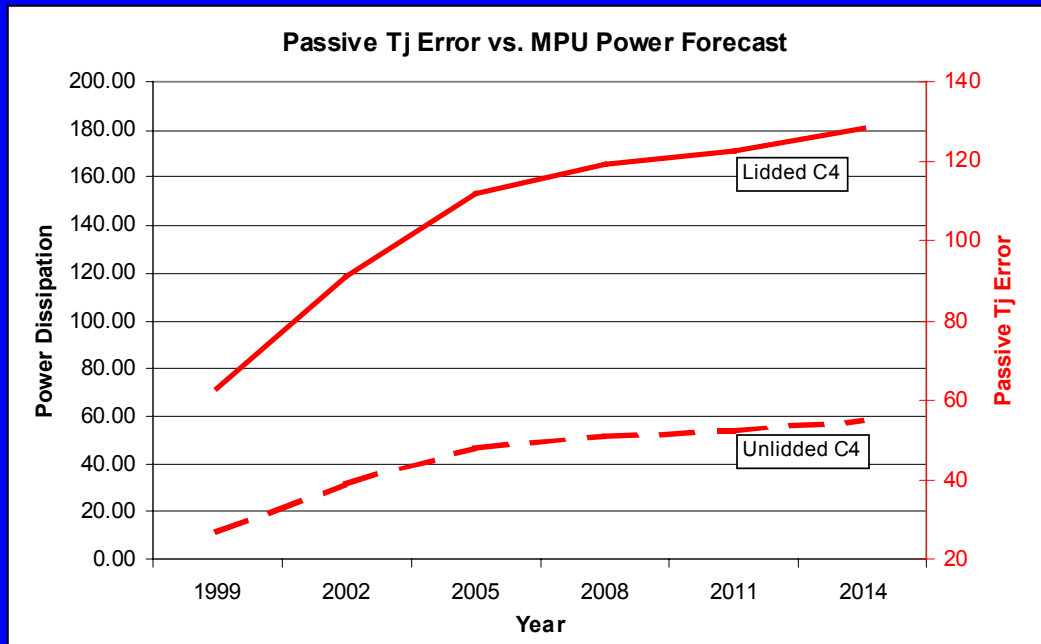


$$T_j(\text{error}) = \theta_{(j-hx)} * \text{Power}$$



$$T_j(\text{error}) = (\theta_{(j-hs)} + \theta_{(hs-hx)}) * \text{Power}$$

Lidded vs. Non-lidded T_j Error (Passive Conduction Thermal Control)

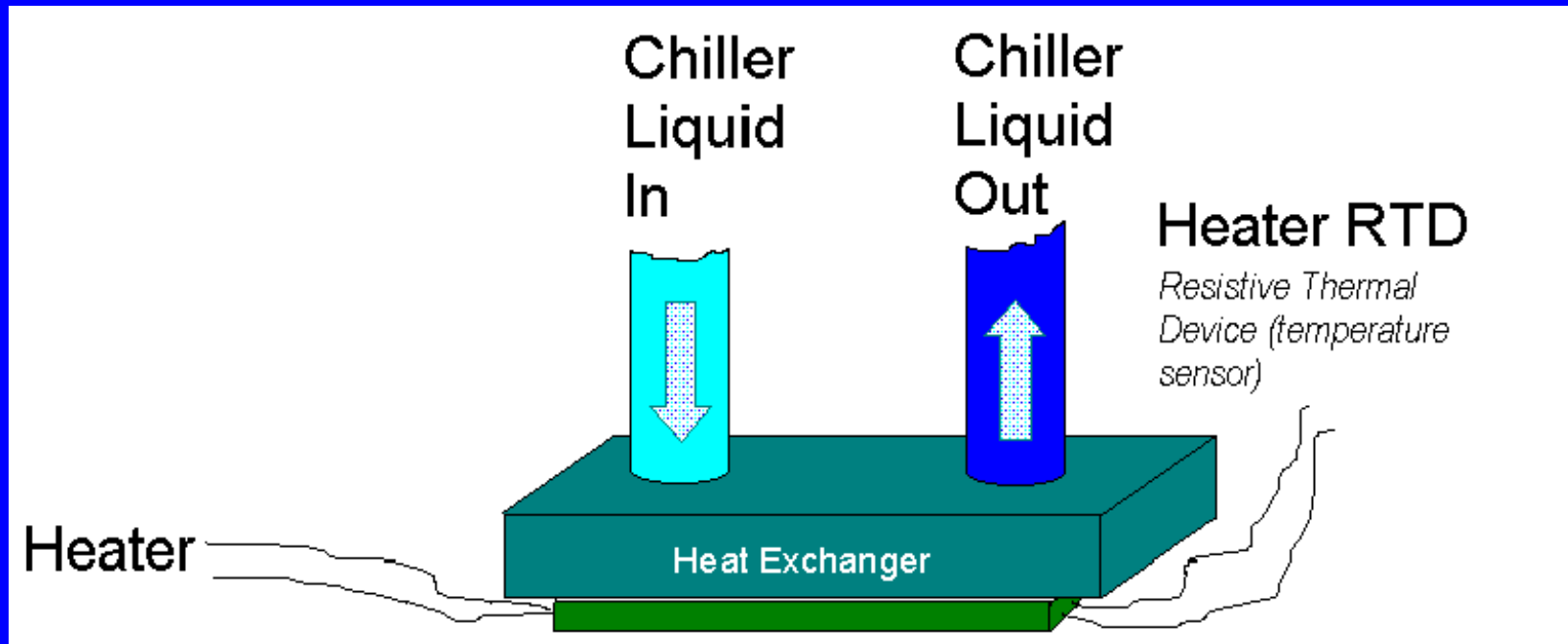


$$\text{Lidded } T_j(\text{error}) = (0.3 + 0.4) * \text{Power}$$

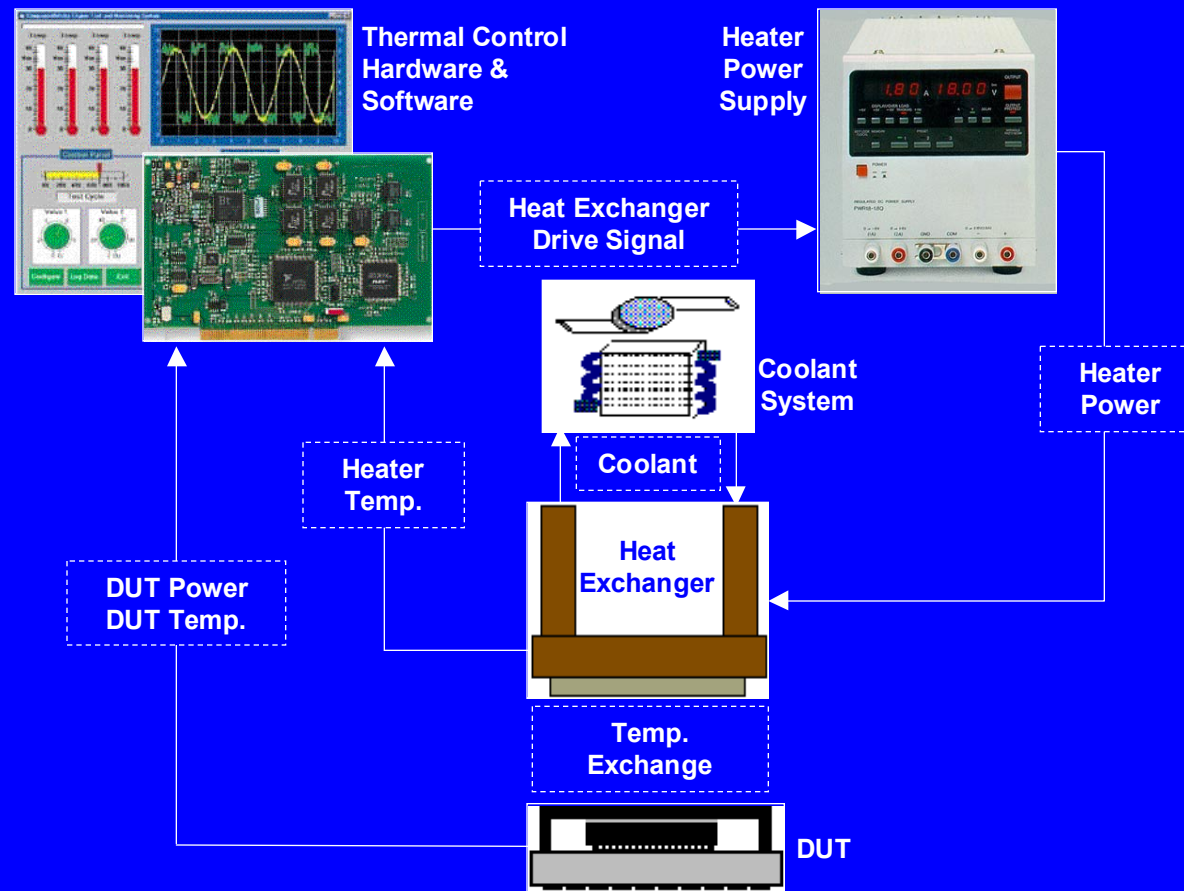
$$\text{UnLidded } T_j(\text{error}) = 0.3 * \text{Power}$$

Active Conduction Thermal Control

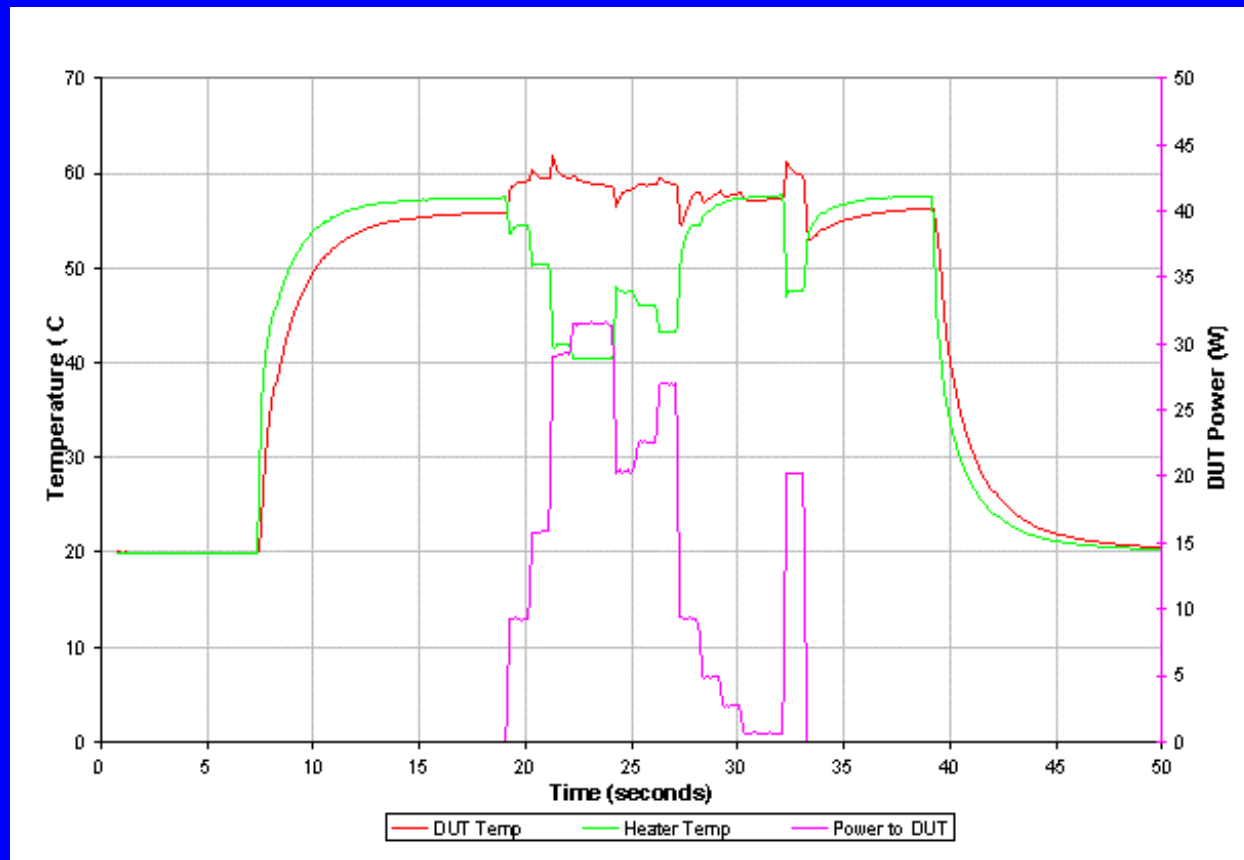
Heat Exchanger



Active Conduction Thermal Control System Architecture



Active Conduction Thermal Control Data





Approaches to Thermal Management of High Power Devices

Paul Nesrsta
Reliability Incorporated

Scope of Presentation

- This presentation deals with methods for control dut junction temperatures in a parallel test or burn-in environment.
 - What is the maximum dut power that can reasonably be accommodated using circulating air as the heat transfer medium?

Presentation Road Map



- Process Cost reduction is the Goal
- System Capacity vs Throughput
- Dut Stress Uniformity vs throughput
- System capacity determinants
- Max dut power vs system capacity
- Max reasonable dut power in air

The Real Goal: Reduced processing cost for higher power devices

- Cost determinants;
 - tooling cost
 - operating cost
 - **System throughput**
 - **Yield**



Two keys to Throughput



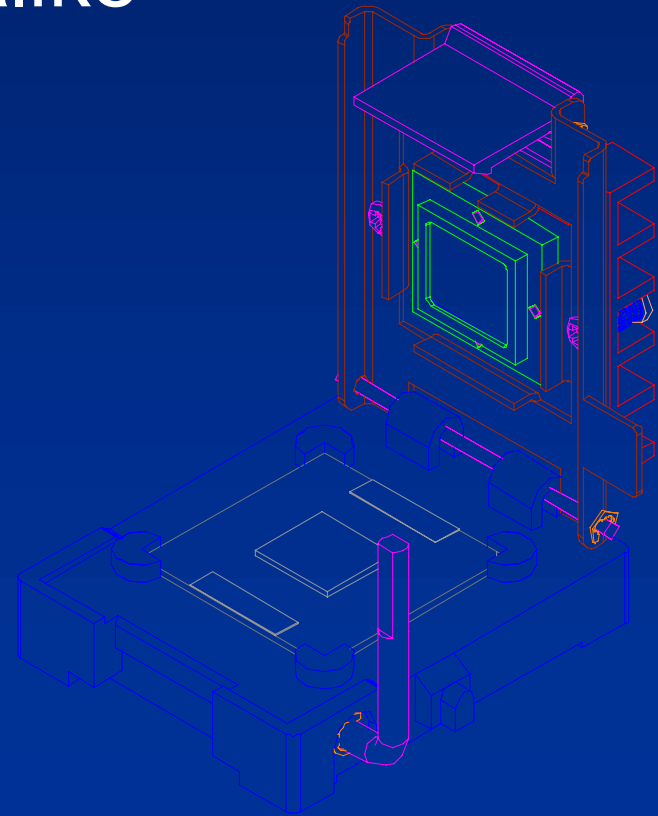
- System Capacity
 - Shouldn't be compromised if possible
- Stress Condition Uniformity

Uniformity affects Throughput

- All duts subjected to exactly identical test/stress conditions
- Why?
 - Closer tolerances allow higher stress temps without compromising yield
 - Higher stress temps allow shorter BI duration
 - Shorter BI duration allow higher throughput
 - Higher throughput = lower cost

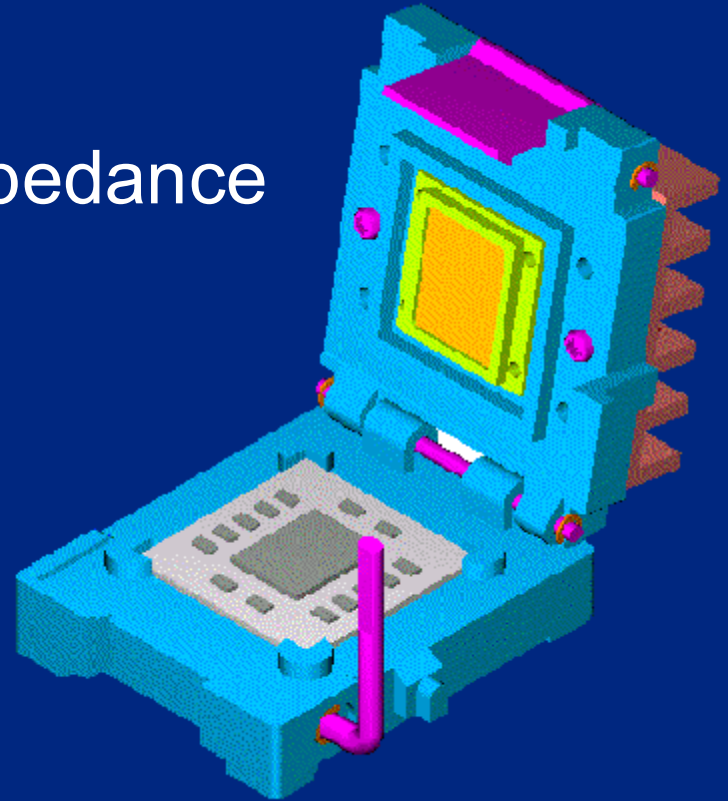
Uniformity determinants

- All test fixturing is not alike
 - Socketing variations
 - chamber variations
 - Ambient Temperature
 - Air flow velocity
- All duts are not alike
 - Mechanical
 - Electrical performance



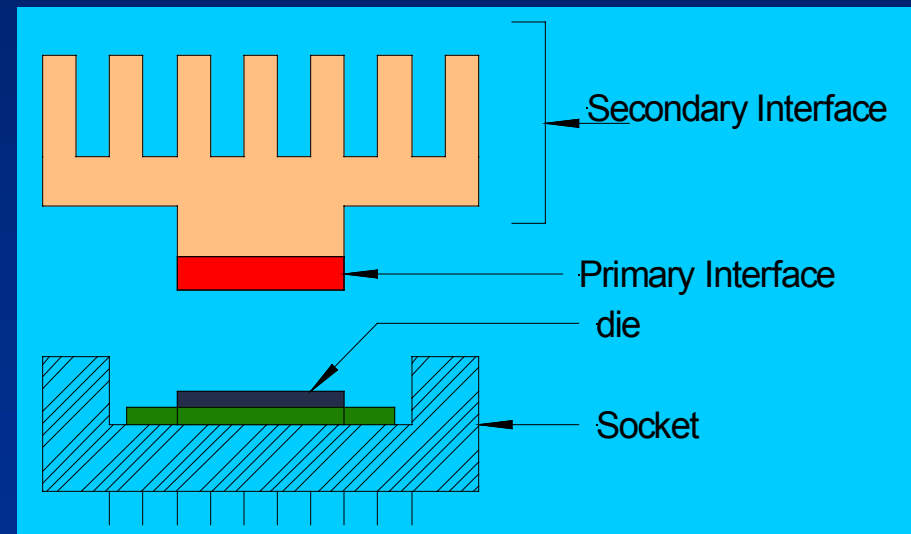
To achieve uniform die temps

- The thermal management system must compensate for variations in:
 - Dut to dut packaging
 - Socket to socket thermal impedance
 - Ambient temperature
 - Dut to dut power dissipation



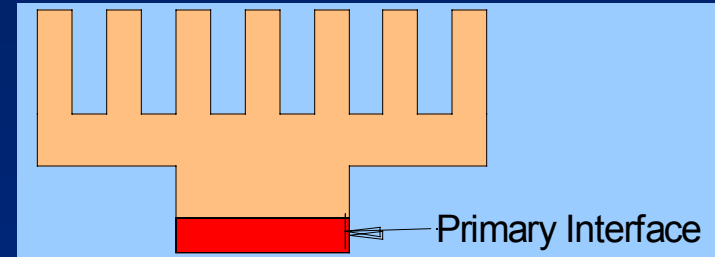
Dut to Ambient Interface

- Dut to Ambient interface comprises 3 elements:
 - Dut to heat sink interface (Primary)
 - Heat sink to ambient (Secondary)
 - Dut to socket heat leakage (small)



Dut to Heat Sink interface

- Ideal interface would:
 - Provide low thermal impedance
 - Uniform from dut to dut
 - Provide even coverage across die surface
 - Leave no residue
 - Robust
 - Low cost



Two choices for low primary thermal impedance

- Near perfect flatness and coplanarity
or
- Conforming thermal interface

“Any air space between two heat conducting surfaces greater than 50×10^{-6} ” adversely affects heat conduction”

Primary interface comparison

- Hard copper surface
 - θ j-hs: 3-5 °C/W/cm²
 - Variations due to lack of conformability
 - die coverage variations
 - Requires high contact pressure
 - Die cracking
 - solder ball
- Conformable elastomer pad on Copper
 - θ j-hs: 1-2 °C/W/cm²
 - >15psi contact pressure
 - May leave residue
 - maintenance issue

Primary interface comparison

- Hard copper surface
 - θ j-hs: 3-5 °C/W/cm²
 - Variations due to lack of conformability
 - die coverage variations
 - Requires high contact pressure
 - Die cracking
 - solder ball damage
- RI's conform-able interface on copper
 - θ j-hs:
 - ~0.5°C/W/cm²
 - +/- 5%
 - ~15 psi contact pressure

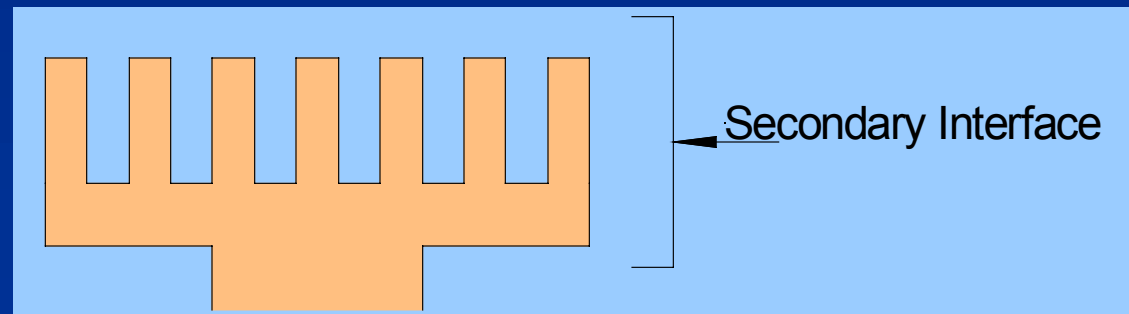
Yield vs Throughput



- Pressing hard enough on a hard interface to insure even, consistent contact may lead to mechanical damage.
- Not pressing hard may lead to inconsistent thermal management
- Allowing for inconsistent thermal management compromises throughput

Heat sink to Ambient interface

- Ideal (Secondary interface)
 - low thermal impedance to ambient
 - uniform from dut to dut
 - cheap
- Our answer: Finned copper in high velocity air

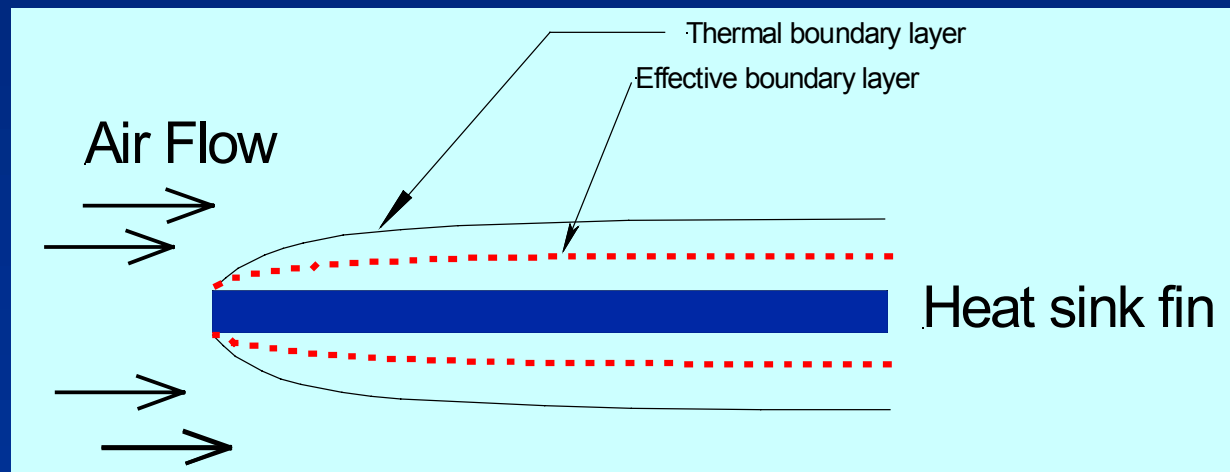


Coolant uniformity

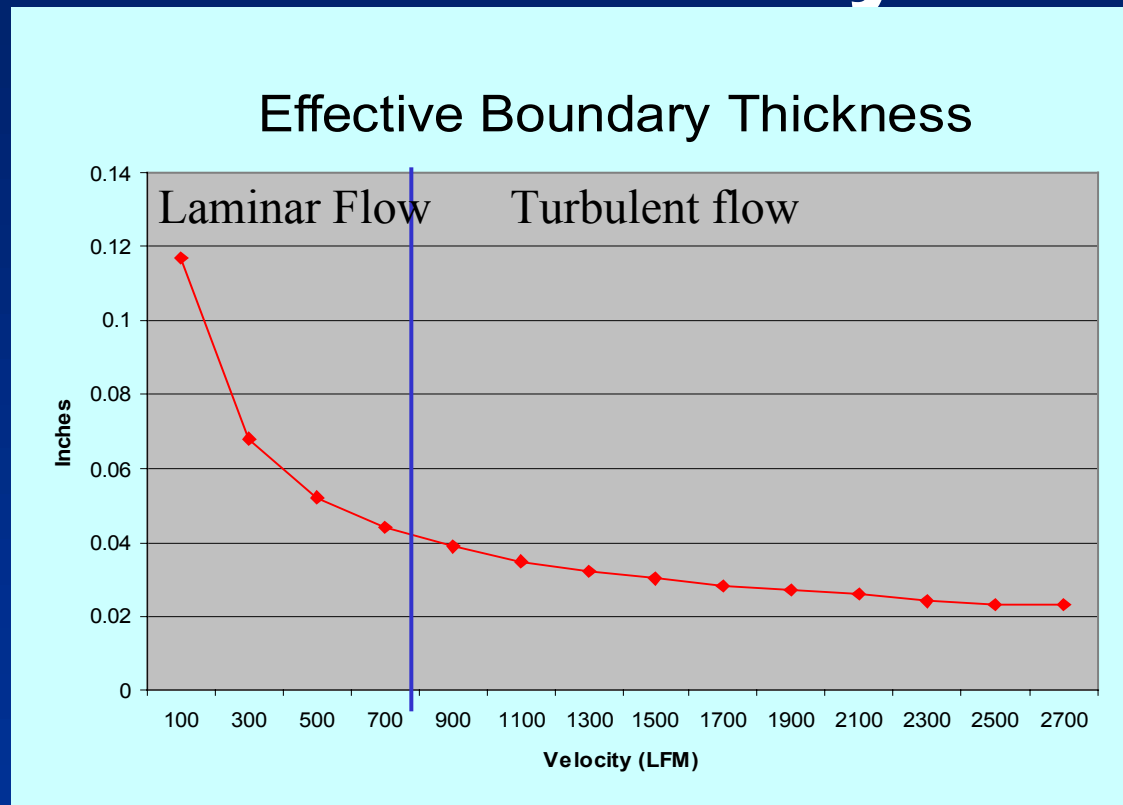
- Ambient temperature must be the same for all duts
- Secondary thermal interface is a function of heat sink to coolant contact
- HS to coolant contact is a function of heat sink design & coolant velocity

Coolant velocity

- Thermal boundary layer gets thinner as velocity increases



Heatsink effectiveness vs air flow velocity



- Boundary layer changes less above 1000 lfm

RI Criteria System Air flow

Calculated:

Velocity Min/Max = 1800/2533 lfm

Measurement Results

Top Backplane

Min = 2105 lfm

Max = 3680 lfm

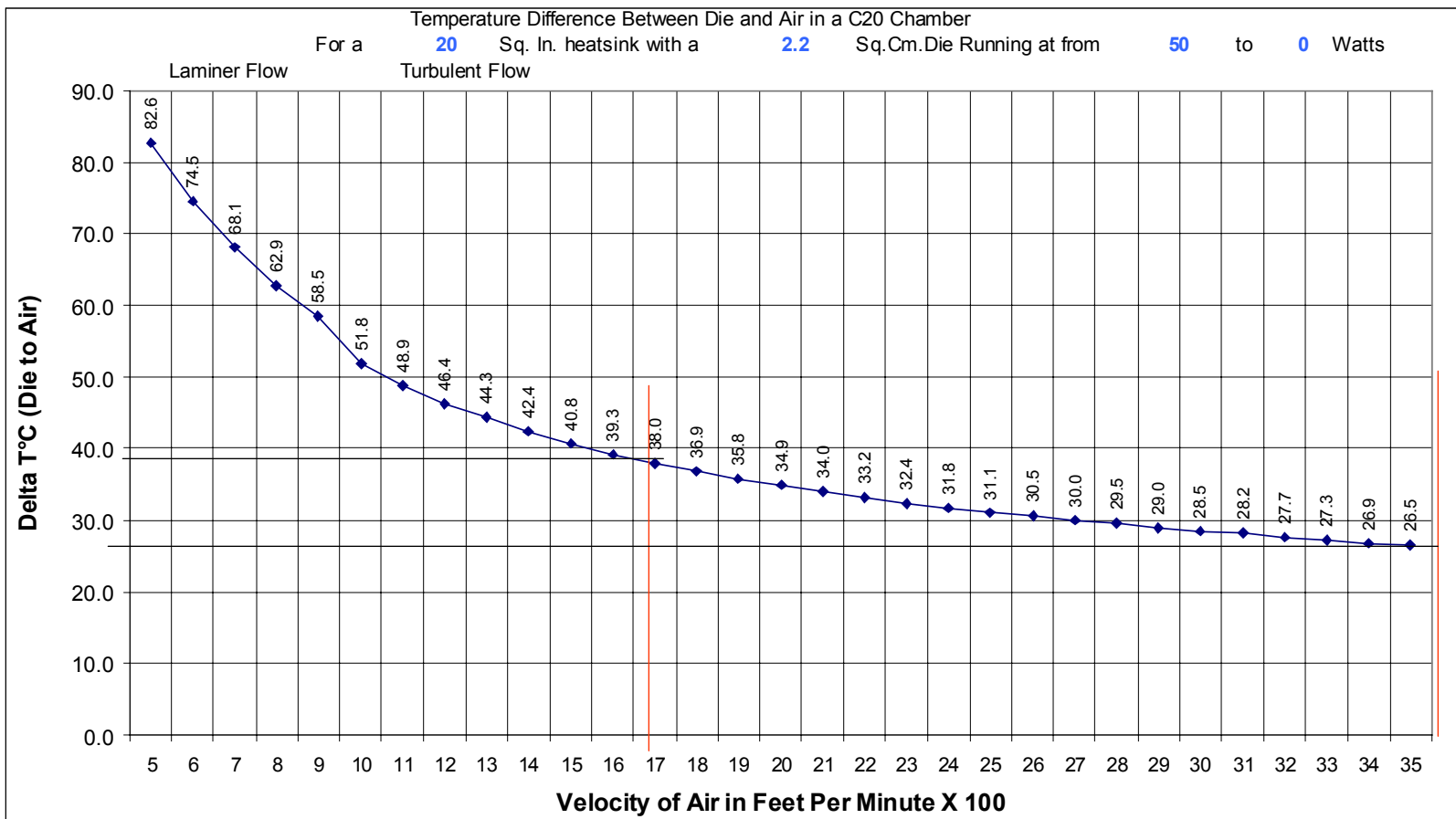
Bottom Backplane

Min = 1715 lfm

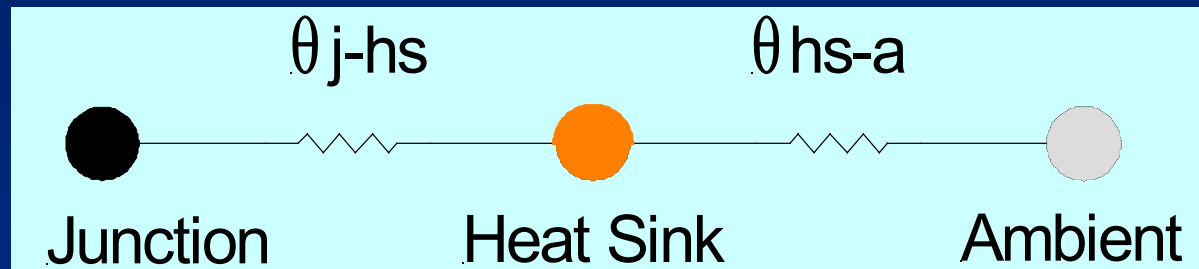
Max = 2905 lfm

Total ΔT Vs Air velocity

DUT Power (Watts)	50	DUT to Heatsink Interface	
		Die size (mm) X (mm)	14.7 14.7
Heatsink Area (Sq.In.)	20.0	Thermal Resistance in °C per Watt per Sq. CM	
			0.52



Thermal impedance stack-up



- $\theta_{j-hs} \sim 0.5 \text{ C/W/cm}^2$
 $\sim 2 \text{ cm}^2 = 0.25 \text{ C/W/cm}^2 \text{ +/-} 5\%$
Calibrated per device
- $\theta_{hs-a} = 0.42 \text{ C/W +/-} 15\%$
- Total $\theta_{j-a} = 0.67 \text{ C/W +/-} 20\%$

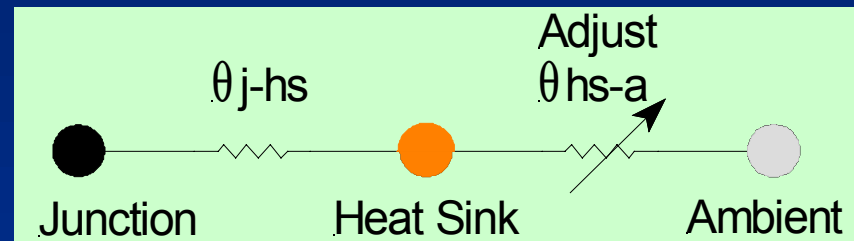
Temperature uniformity compensation

- Contributors:
- Dut to Dut power variation
- θ_{hs-a} variation
- θ_{j-hs} variation

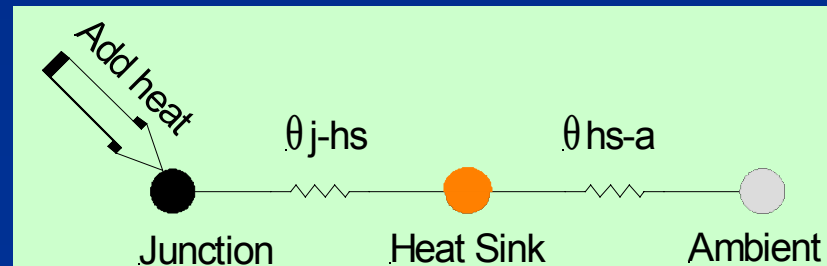
- Can compensate for dut power, θ_{j-hs} & θ_{hs-a}

Per DUT Compensation methods:

- Control thermal impedance path

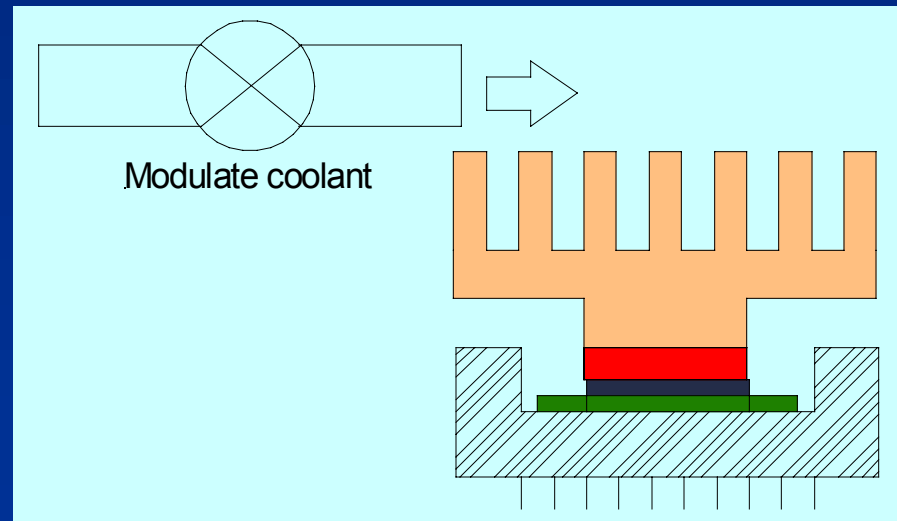


- Add heat with fixed thermal impedance path



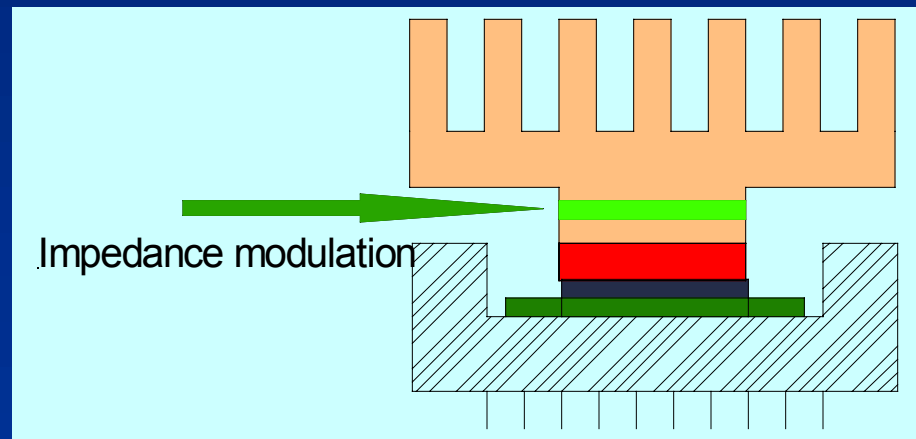
Individually Controlled impedance path per dut

- modulated coolant
 - complex electromechanical mechanism
 - thermally efficient
 - not robust
 - expensive



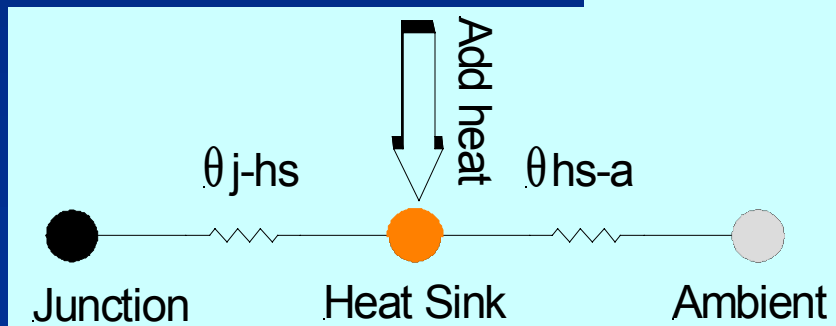
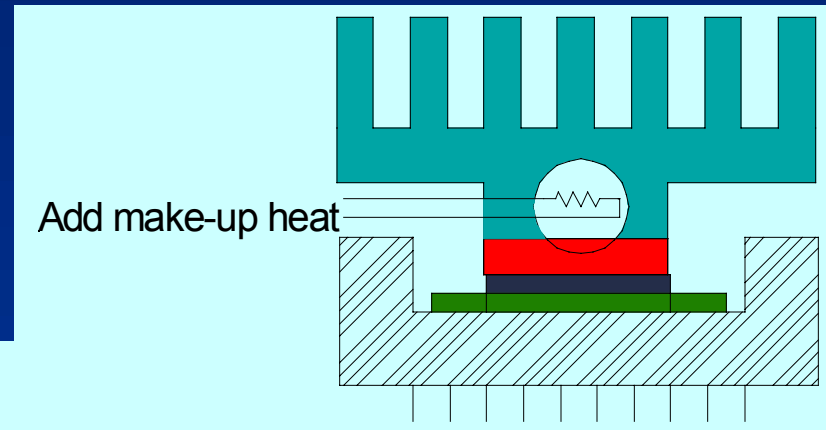
Method 2

- Thermo-electric cooler impedance modulation
 - allows higher chamber ambient temperature
 - robust
 - low efficiency
 - expensive



Added heat compensation

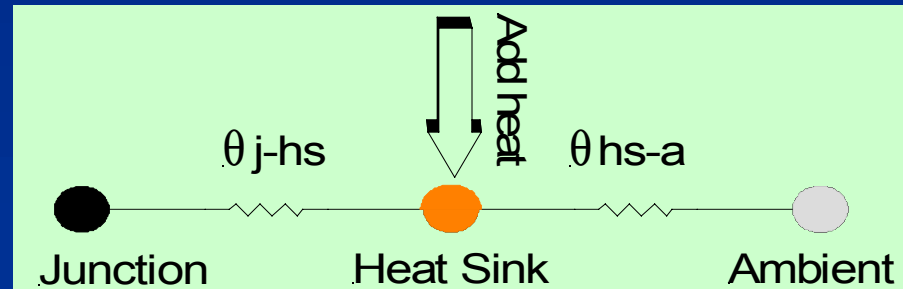
- Resistive element heater
 - robust
 - cheap
 - not efficient



Net effect is reduction of ΔT_{j-hs}

Heater sizing

- Assume 100% variation in dut power
- θ_{j-a} varies from 0.54C/W to .80C/W
- Therefore $50W * .80C/W = 40C$
- Smallest θ_{hs-a} is 0.36C/W
- Therefore we must add $\sim 112W$ to make up 40C

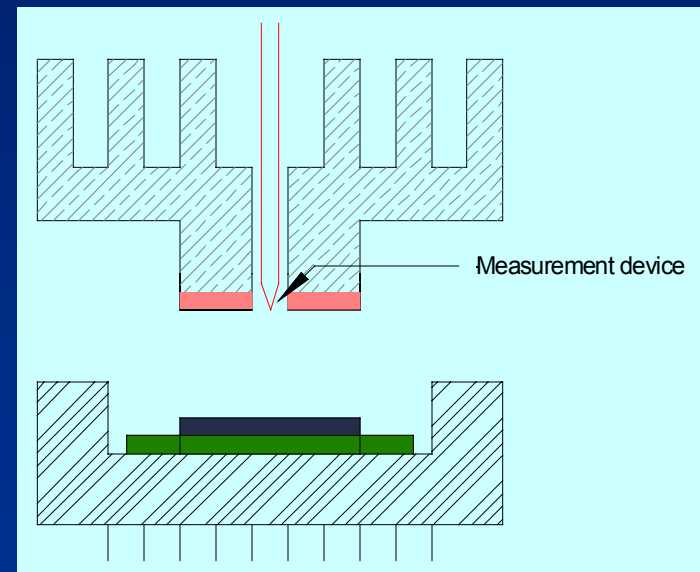


Dut Temperature Measurement

- To compensate for variations we must know:
 - Dut power
 - Ambient temp
 - Die Temp
- **Plea to Device Designers:**
Please put accessible, accurate, temp measurement devices on the die!

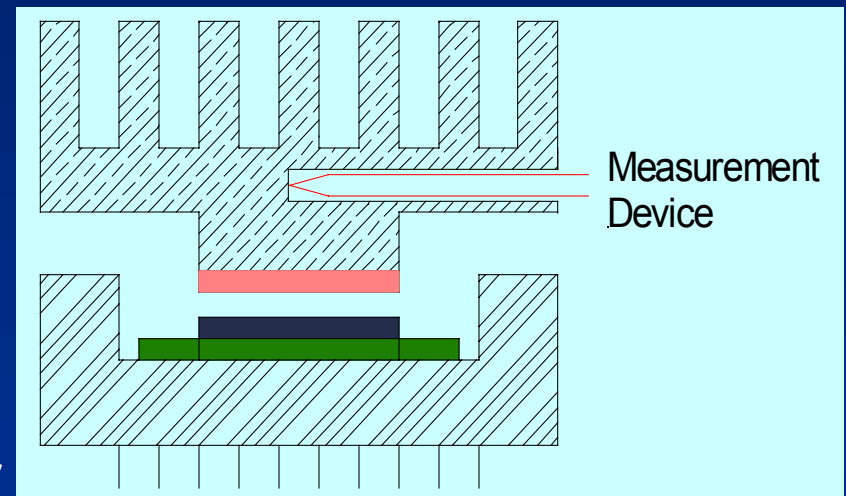
Measurement Method 1

- Die measurement outside the thermal path
 - disturbs heat removal uniformity
 - susceptible to local variations in die temp



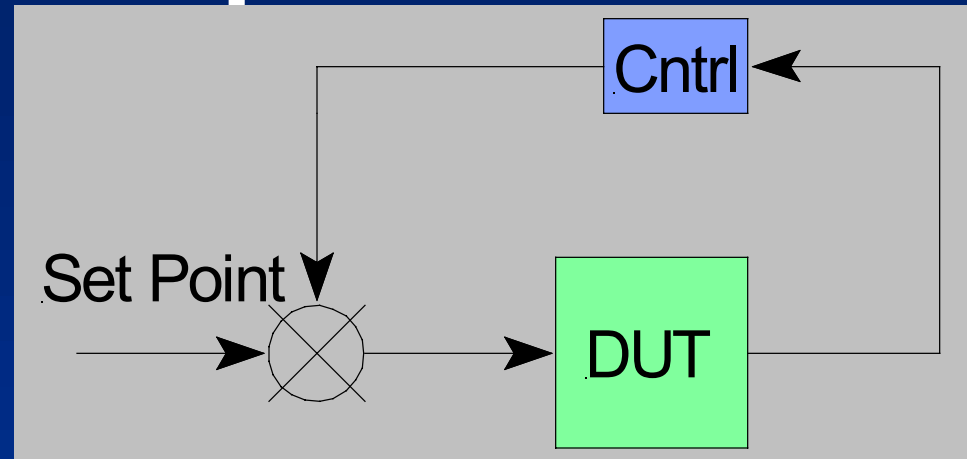
Temperature Measurement Method 2

- Measure heat sink temp
 - maintains uniform die coverage
 - provides die temp averaging
 - allows compensation for h_{s-a}
 - must compensate for d_{ut} to h_s thermal interface

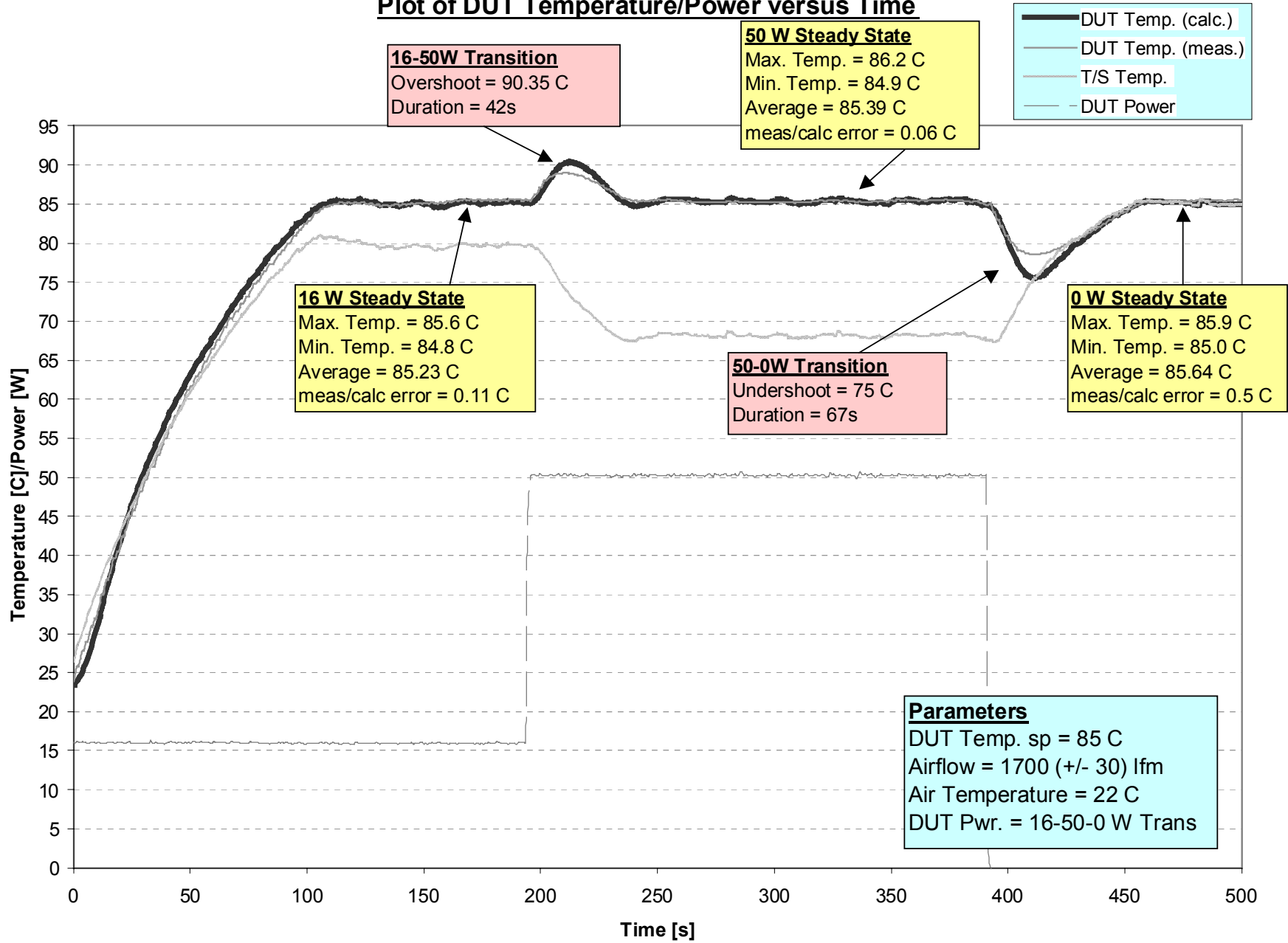


Dut temp prediction/compensation

- If we know:
 - dut power
 - ambient temp
 - thermal impedance from dut to ambient
- Then we can calculate dut temp and correct



Plot of DUT Temperature/Power versus Time



So far we have provided:

- a consistent low thermal impedance from the die to ambient
- Worst case = $0.8 \text{ }^\circ\text{C/W}$
- $0.80 \text{ }^\circ\text{C/W} * 50\text{W} = 40 \text{ }^\circ\text{C}$ rise from die to ambient
- IF target T_j is $125 \text{ }^\circ\text{C}$ then Ambient must be $125 - 40 = 85 \text{ }^\circ\text{C}$

System Power Sizing

- Assume normal distribution of 0 to 50W/duts
- Therefore avg Power = 25W
- Therefore must make up 25W/dut
- If 115W make up for 0W then avg make-up heat = $(25/50) * 112W = 56W$
- $56W + 25W = 81W/dut$

System Capacity

- Standard C18 dissipates 5500W @ 85 °C
- $5500W / 81W/dut = 67$ duts/system
- C20 dissipates 24,000W @ 50 °C
- $24000 / 81 \Rightarrow 296$ duts/system
or >12 duts/burn-in board

The total system must:

- Combine:
 - Low thermal impedance path to coolant
 - dut power variation compensation
 - High power handling at low ambient set points



Conclusions



- “Conventional” circulating air Test &BI is viable for dut power dissipation $<50W$
- This is desirable because it:
 - High throughput
 - Robust
 - Maintains current process paradigm
 - Saves money!

Dixie Chips

“Too Hot to Handle”

by

Jim Ostendorf

DYNAVISION

Bibs

- Electrical
- Mechanical
- Thermal
- Cost

Electrical

- Noise; Cross Talk
- Rise/Fall Times
- Functional Test
- Bist

Mechanical

- Loader/Unloader
- Rigidity
- Bowing
- Accuracy
- Plating

Thermal

- Objectives:
 - Temperature
 - Voltage
 - Fail Safe Protection
 - Cost

Thermal

- Design Goal:
 - Tight Die Temperature Control for Differing DUT Power Dissipation

Thermal

- Smart Heat Sink
- Thermocouple
- Heat Pump
- Control Module

Thermal

- Voltage:
 - Low Voltage 1.8 V
- Current:
 - High Current Up to 30.0 A
- Power Characteristics of Target DUTS:
 - Wide Range of Power Dissipation

Thermal

- **System Description:**

- An intelligent heat sink is assigned to each DUT allowing bi-directional transfer of heat between DUT and heat sink surfaces.

- The intelligent heat sink pulls heat out of hot devices and pushes heat into cold devices maintaining the desired uniform temperature on each DUT.

- The intelligent heat sink consists of a bi-directional heat pump sandwiched between two parts of a passive metal heat sink.

Thermal

- **Temperature Control:**
 - A temperature sensor and one side of the modified heat sink get into direct contact with the surface of the DUT.
 - The other portion of the modified heat sink has the fins that interface with the oven air flow.
 - The temperature of the oven is set at an appropriate level that would allow the thermal control system to work.

Thermal

- **Temperature Control cont.:**
 - Imbedded between the two portions of the metal heat sink is the heat pump. the heat pump is electric current controlled.
 - The direction of the heat flow is determined by the direction of the current through the heat pump.
 - The direction of the current depends on whether the DUT temperature that is sensed is higher or lower than the target temperature.

Thermal (Voltage)

- Voltage:
 - DC to DC Converter
 - Sense at DUT

Thermal (Voltage)

- **Design Goal:**
 - Tight Voltage Control Throughout the Full Target Current Range

Thermal (Voltage)

- **System Description:**
 - One dc to dc converter is dedicated to each DUT cell, allowing very tight voltage regulation and control over each cell.
 - Voltage sensing for regulation is picked up right at the DUT load thereby reducing drastically the voltage variations caused by the large current draws.

Thermal (Protection)

- **Design Goal:**
 - Provide Fail Safe Control to Protect Devices Under Test
- Shut Down Mode

Thermal (Protection)

- **Fail Safe Features:**

- Power is turned off to a DUT on thermal runaway, over voltage and over current conditions.
- No power is applied to a cell on "DUT absent" condition.
- No power is delivered to the bib while the the heat sink and power control assembly is "in transit".
- Burn-in board can not be withdrawn unless the control assembly is in the retracted position.

Thermal (Protection)

- **System Description:**
 - Some standard, widely-used burn-in systems have user-designed back planes and driver boards for exercising and stressing microprocessor and asic products.
 - New burn-in board design plugs into these existing systems but with provisions for individually controlling the power to each DUT cell and individually controlling the temperature of the device in each cell.

Thermal (Protection)

- **System Description cont.:**
 - These power and thermal control functions may be housed in a separate assembly plugged into the slot next to the burn-in board it is intended to control.
 - This second approach allows for use of these control overhead over several application devices provided that a standard density and geometry of the burn-in board is implemented. choice of socket is very important in order to allow efficiency in thermal interface and transfer.

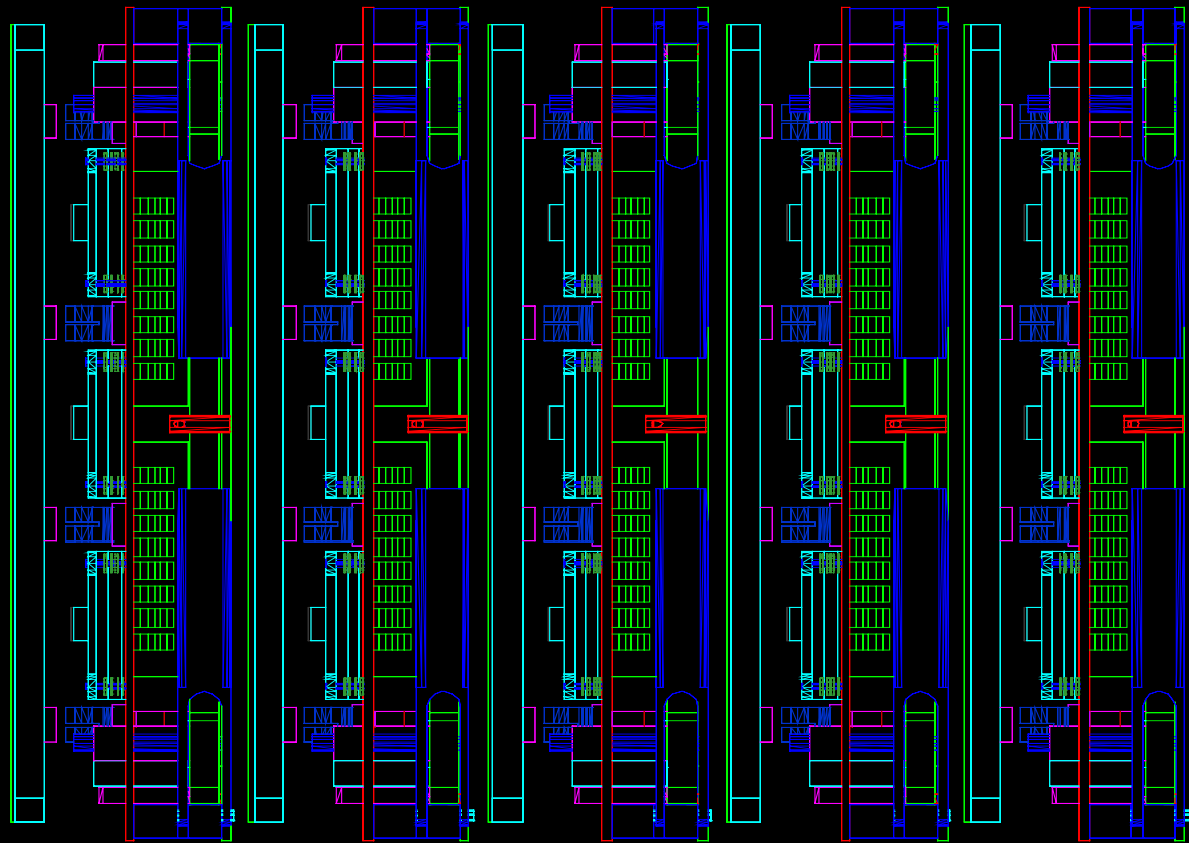
Thermal (Cost)

- **Design Goal:**
 - Design into a wide-based, standard, and familiar burn-in system
- Air Heat Exchange
- Existing Hardware
- Total Solution

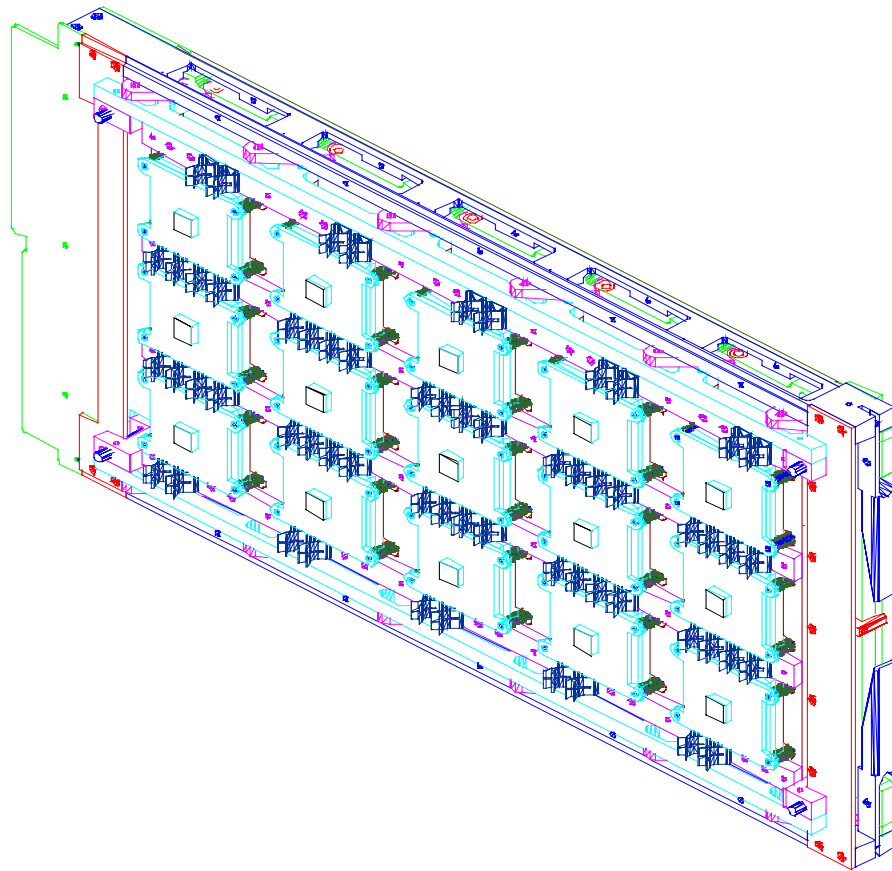
Thermal (Mechanical)

- **System Description:**
 - The mechanical design of the voltage and control assembly and the kinematics of mechanical motion required to move the heat sink and power tabs against the required surface contact pressure between the DUT surface and the heat sink is the most challenging part of this project.

Front



Left



Right

