Burn-in & Test Socket Workshop

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Mesa, Arizona

IEEE

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Technical Program

Session 5
Tuesday 3/06/01 8:00AM

Methods In Burn-in And Test

“Active Thermal Control During Burn-in”
Ken Heiman - Micro Control Company

“Embedded Test Solution For Burn-in”
Charles McDonald - LogicVision, Inc.
Presented By**: Steve Pateras** - LogicVision, Inc.

“Next Generation Burn-in & Test System For Athlon Microprocessors: 'Hybrid Burn-in'”
Mark Miller - Advanced Micro Devices

ACTIVE THERMAL CONTROL DURING BURN-IN

Ken Heiman

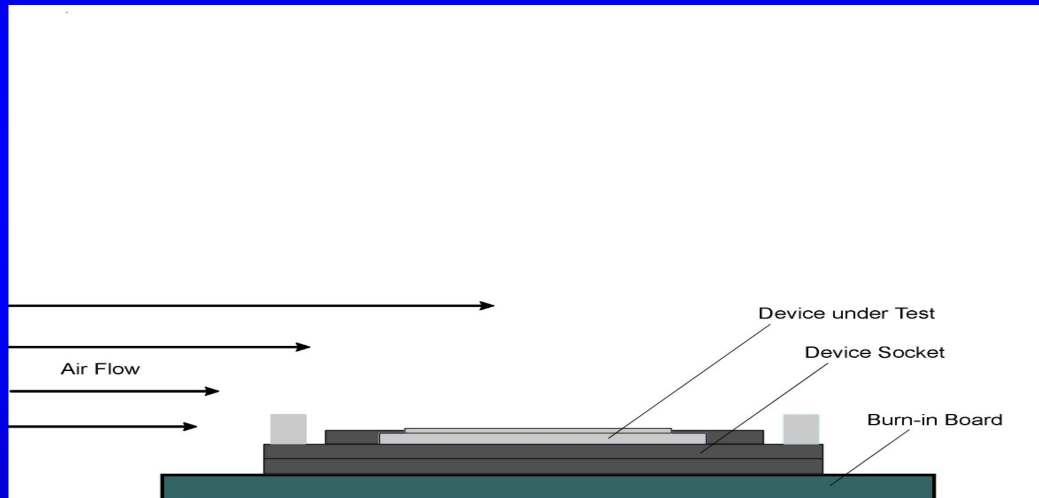
Semiconductor Problems

- New VLSI and Microprocessor devices are dissipating higher power during burn-in.
- New semiconductor technologies draw high currents when applying accelerated voltages during burn-in.
- Active thermal control during burn-in is required to manage all of the environmental and production yield variables.

New burn-in problems

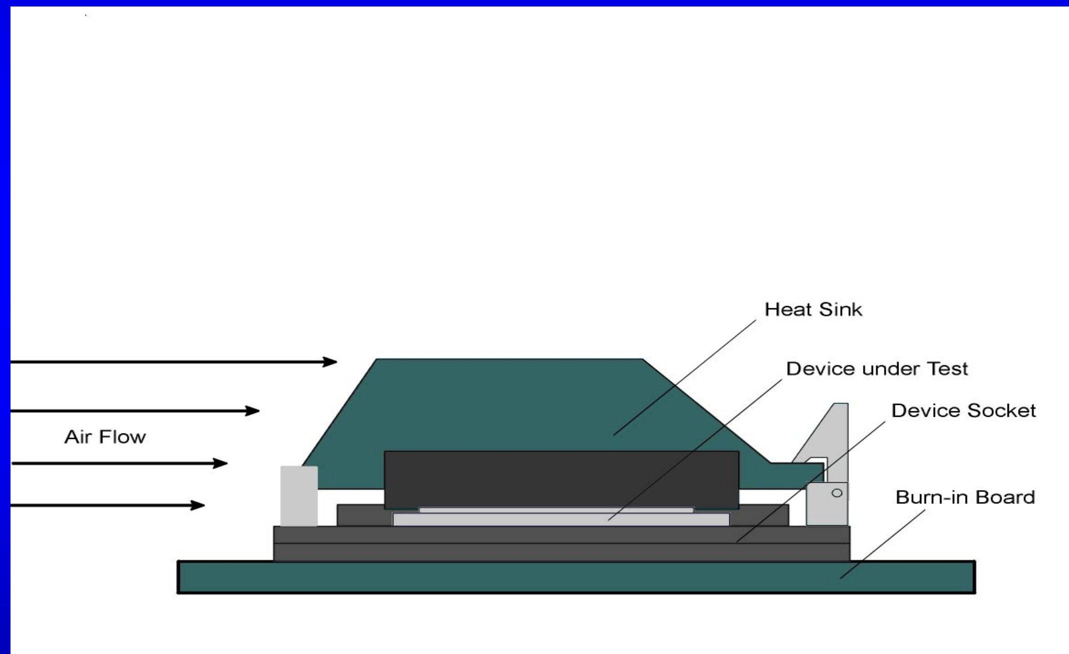
- Power dissipation: How do you add and remove heat?
- Temperature control: How do you control DUT temp so that all devices are aged equally?
- DUT to DUT power variations: How do you control +/- 50% DUT power variations?
- DUT to DUT thermal resistance variations: Imperfections of DUT and heat sink surfaces produce differences in thermal resistances.

0 to 5 Watt Burn-in



- Low power
- Unlidded socket, no heat sink.
- Oven air flow used to heat DUT.
- Difficult to control uniform DUT temp.

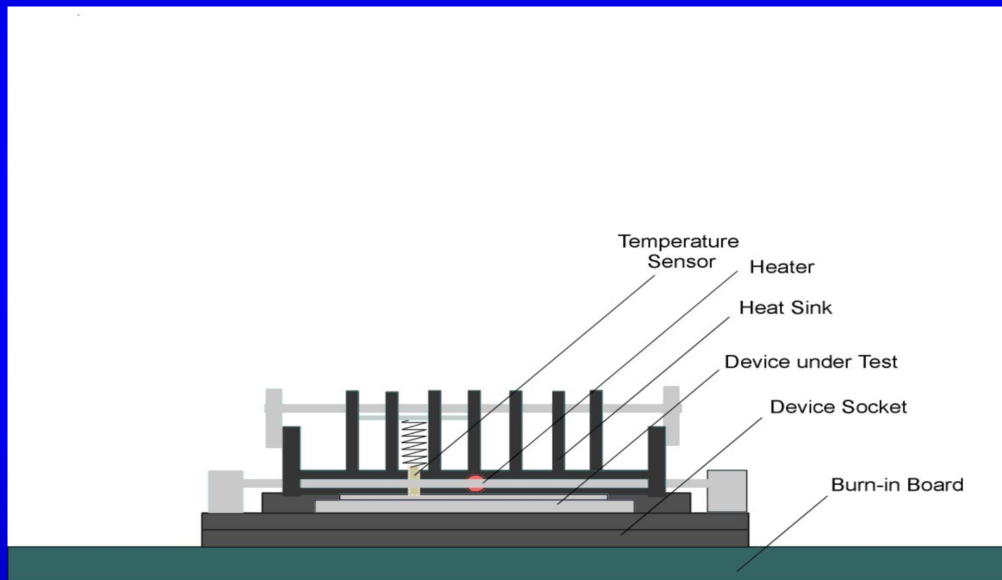
0 to 10 Watt Burn-in



- Lidded socket with a heat sink.
- Oven air flow used to heat DUT.
- Difficult to control uniform airflow +/- 20% typical
- Power per DUT is not uniform +/- 50%

0 to 25 Watt Burn-in

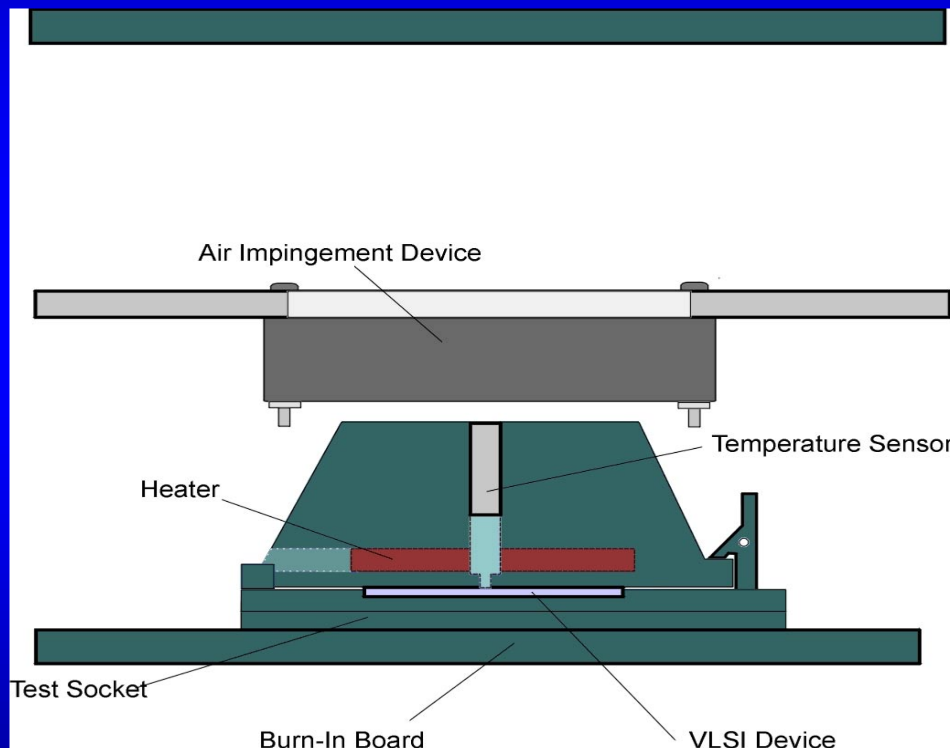
Active thermal control



- Lidded socket with a heat sink,temp sensor, heater, and PID controller per DUT
- Oven air flow used to cool DUT.
- Non-uniform airflow is compensated for by individual DUT heaters.

0 to 50 Watt Burn-in

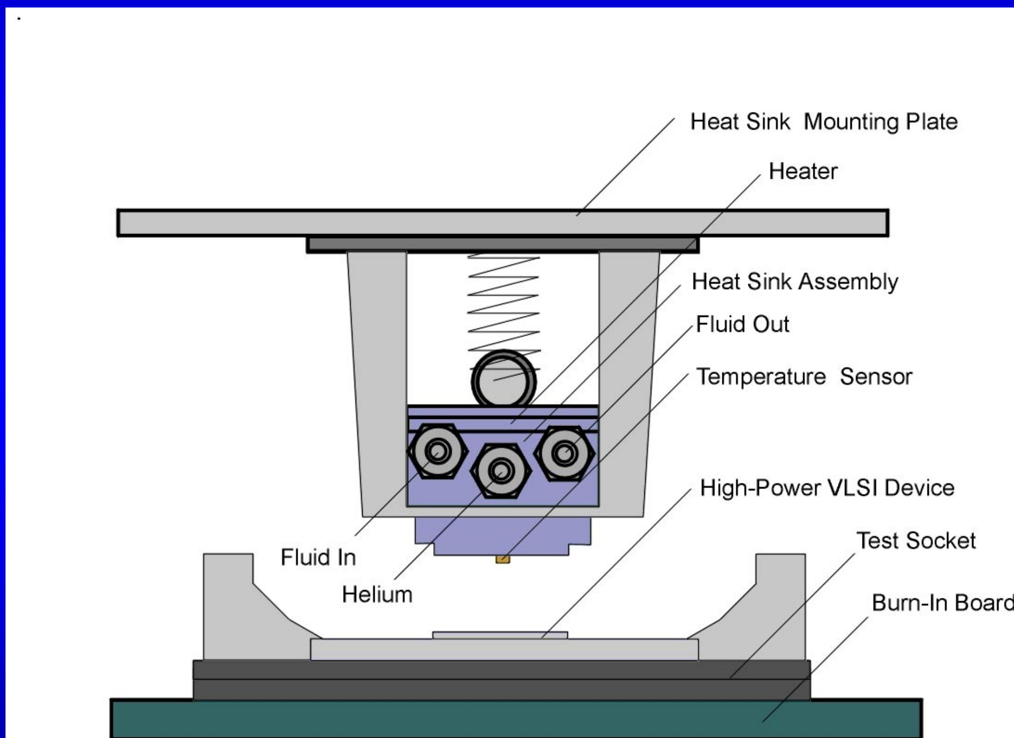
Active thermal control



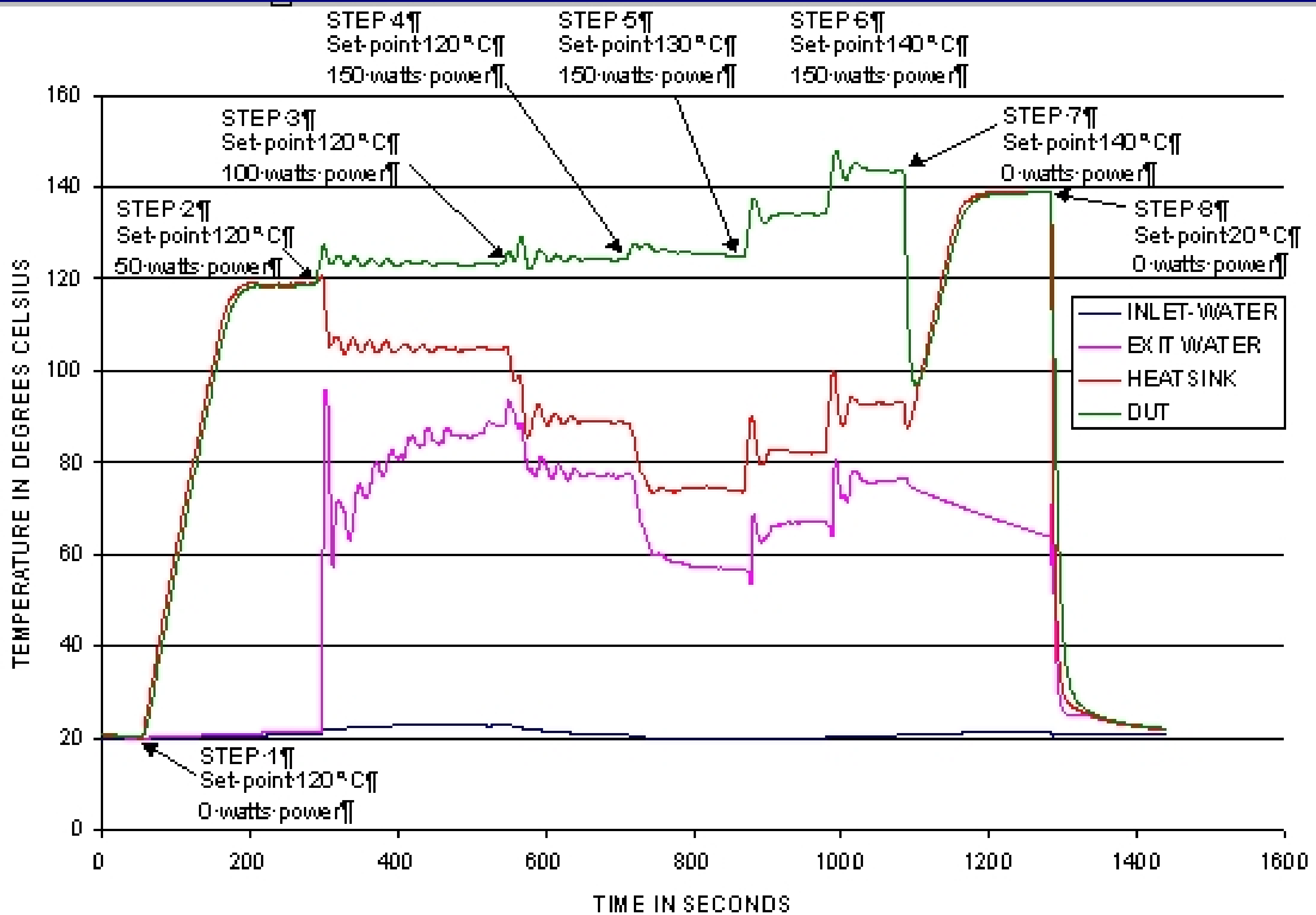
- Lidded socket with a heat sink,temp sensor, heater, and PID temp controller per DUT
- Individual DUT air flow control
- High current regulators required (25 amps per DUT)

0 to 150 Watt Burn-in

Active thermal control



- Liquid cooled heat sink.
- Individual DUT temp control
- Low thermal resistance
- High current regulators (75 to 100 amps per DUT)


STEP 4¶
Set-point 120 °C¶
150 watts power¶
STEP 5¶
Set-point 130 °C¶
150 watts power¶
STEP 6¶
Set-point 140 °C¶
150 watts power¶
STEP 3¶
Set-point 120 °C¶
100 watts power¶
STEP 7¶
Set-point 140 °C¶
0 watts power¶
STEP 2¶
Set-point 120 °C¶
50 watts power¶
STEP 8¶
Set-point 20 °C¶
0 watts power¶
STEP 1¶
Set-point 120 °C¶
0 watts power¶
INLET WATER
EXIT WATER
HEAT SINK
DUT
TEMPERATURE IN DEGREES CELSIUS
TIME IN SECONDS
0
20
40
60
80
100
120
140
160
0
200
400
600
800
1000
1200
1400
1600

Temperature Control @50 W

$R_t = (T_1 - T_2)/P_{watts}$

- Dut Case temperture **without** active thermal control with uniform airflow.
- 30 watt DUT +/- 50 %, R_t = 1°C/Watt +/- 20%.
- Worst case DUT temp distribution 48°C (+30°C,-18°C).

- Dut Case temperture **with** active thermal control.
- 30 watt DUT +/- 50 %, R_t = 1°C/Watt +/- 20%.
- Worst case DUT temp distribution +/-5°C

Temperature Control @100 W

$R_t = (T_1 - T_2)/P_{watts}$

- Dut Case temperture **without** active thermal control. Liquid cooled heat sink.
- 100 watt DUT +/- 50 %, R_t = .8°C/Watt +/- 20%.
- Worst case DUT temp distribution 112°C (+64°C,-48°C).

- Dut Case temperture **with** active thermal control.
- 100 watt DUT +/- 50 %, R_t = .8°C/Watt +/- 20%.
- Worst case DUT temp distribution +/-5°C

Conclusions

- Air and liquid cooled heat sinks are required for high power burn-in.
- Active thermal control is required to compensate for airflow variations.
- Active thermal control is required to compensate for DUT to DUT power variations.
- Active thermal control is required to compensate for variations in thermal resistance between DUT and heat sink.
- Active thermal control is required to maintain +/- 5° C case temperature uniformity.

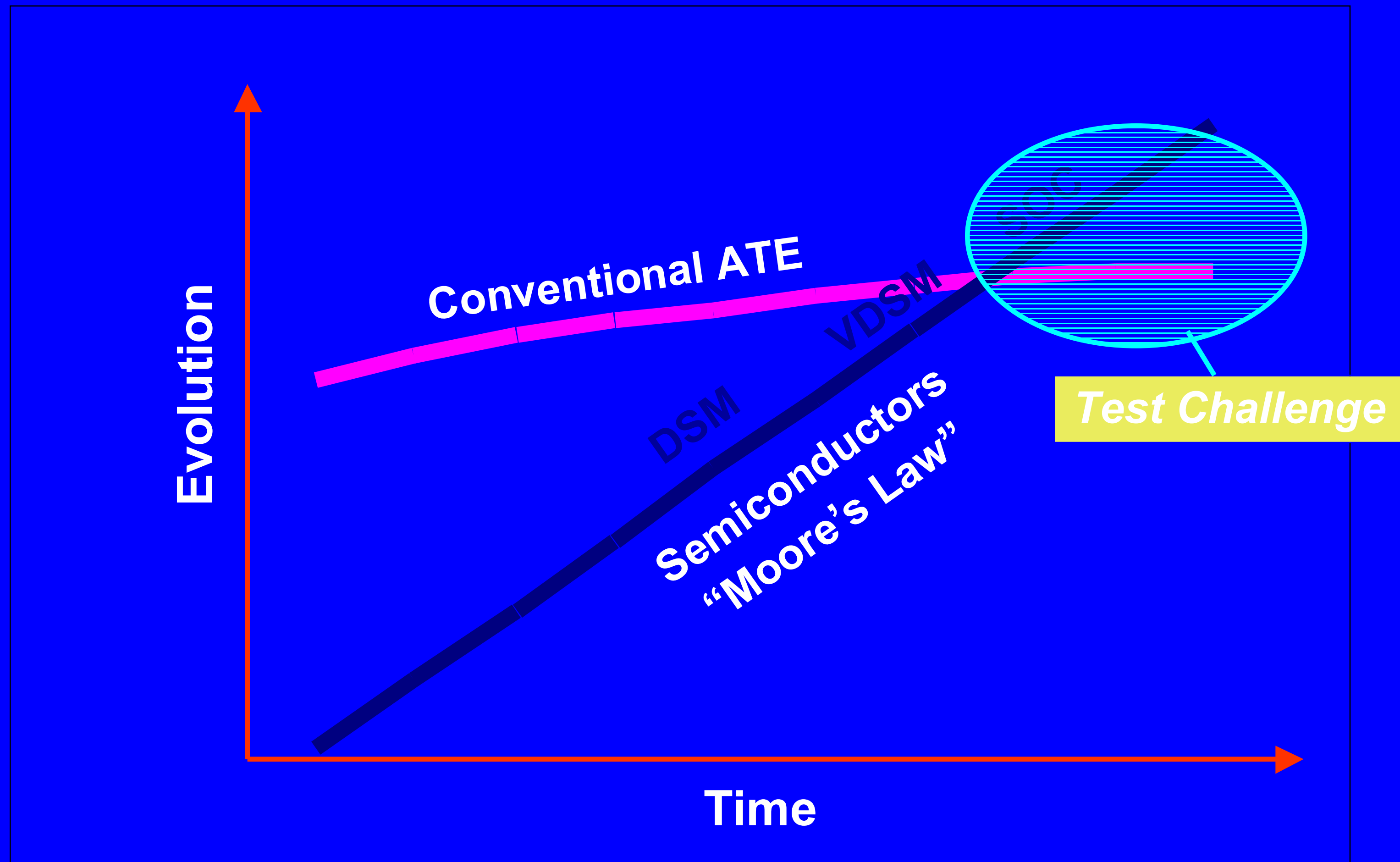
Embedded Test Solution for Burn-In

Charles McDonald
LogicVision, Inc.
email:charlie@lvision.com

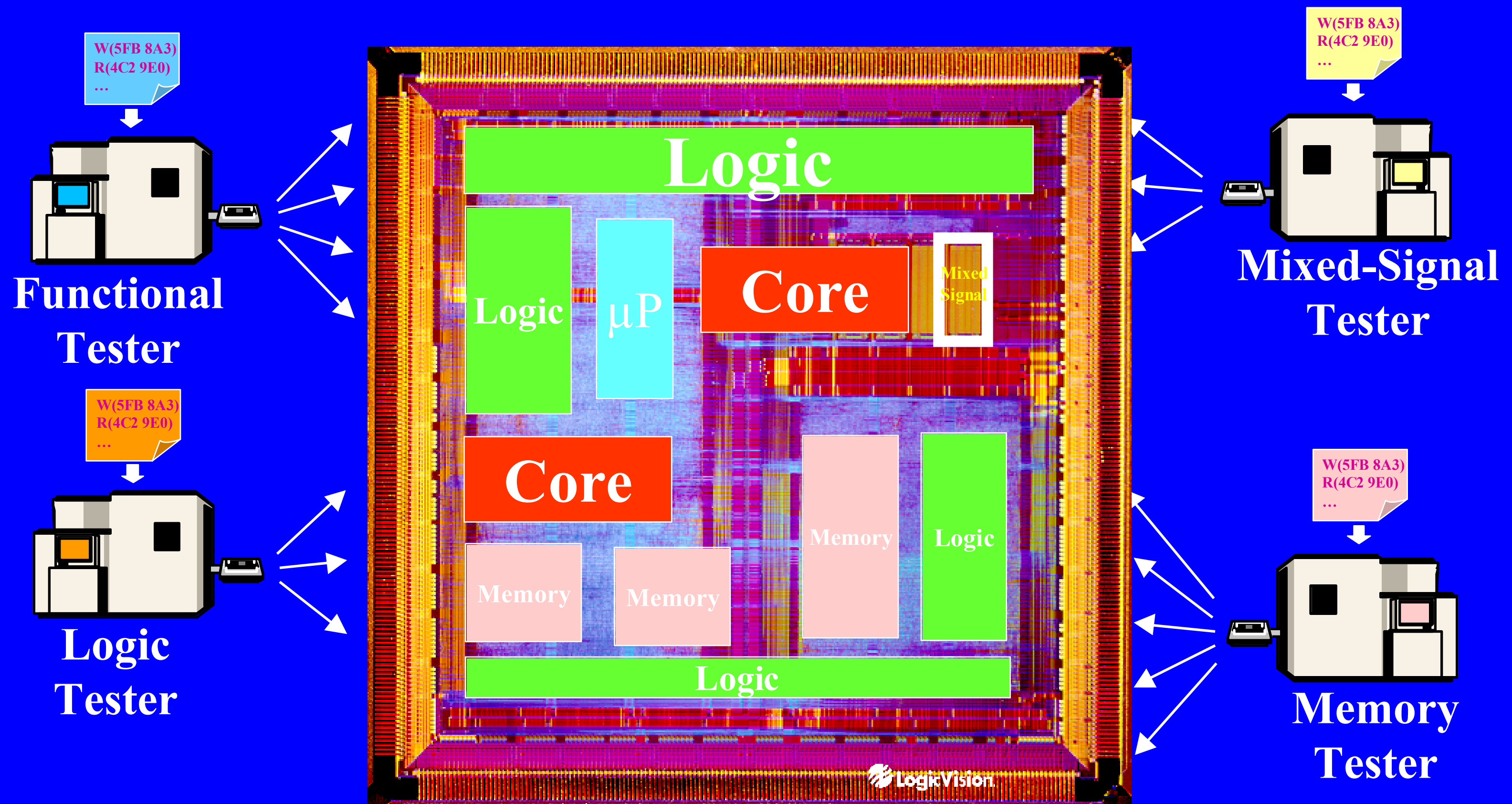
Agenda

- What is Embedded Test?
- How can Embedded test enhance Burn-In
- Cost Savings with embedded test
- Hardware Implications
- Summary

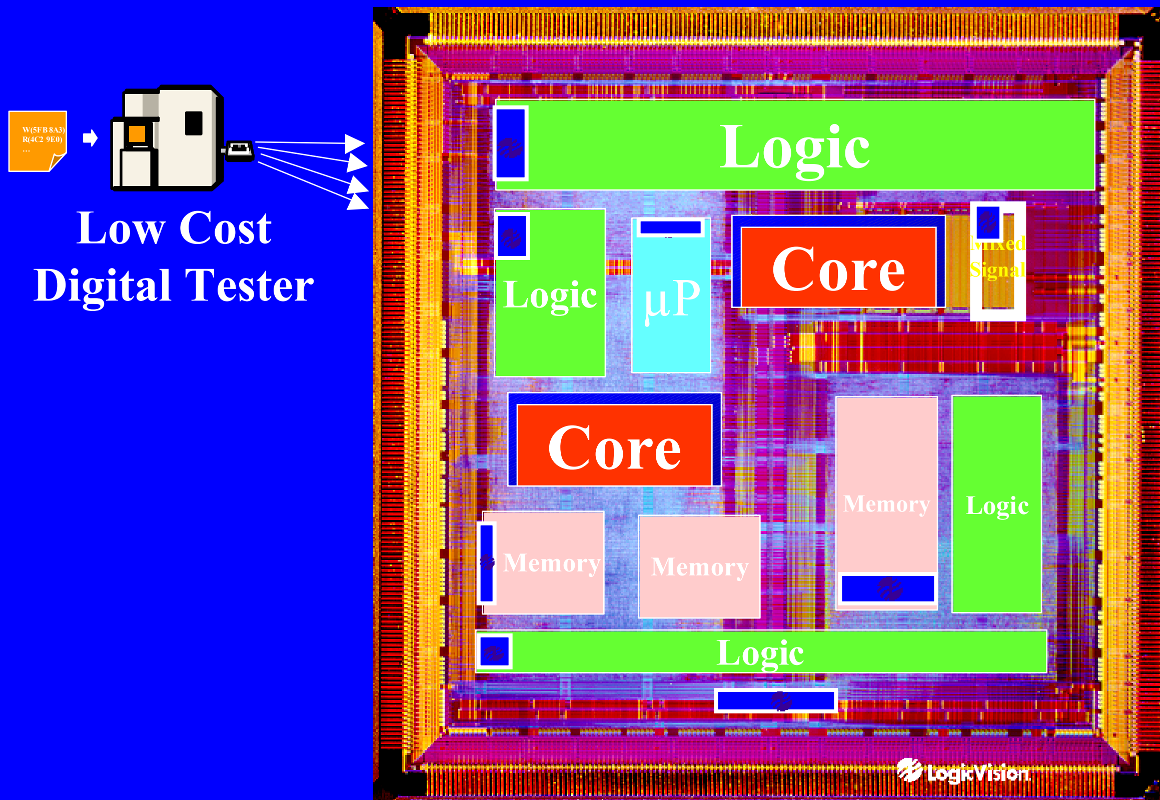
The Challenge for Semiconductor Testing



SOC Test Requirements

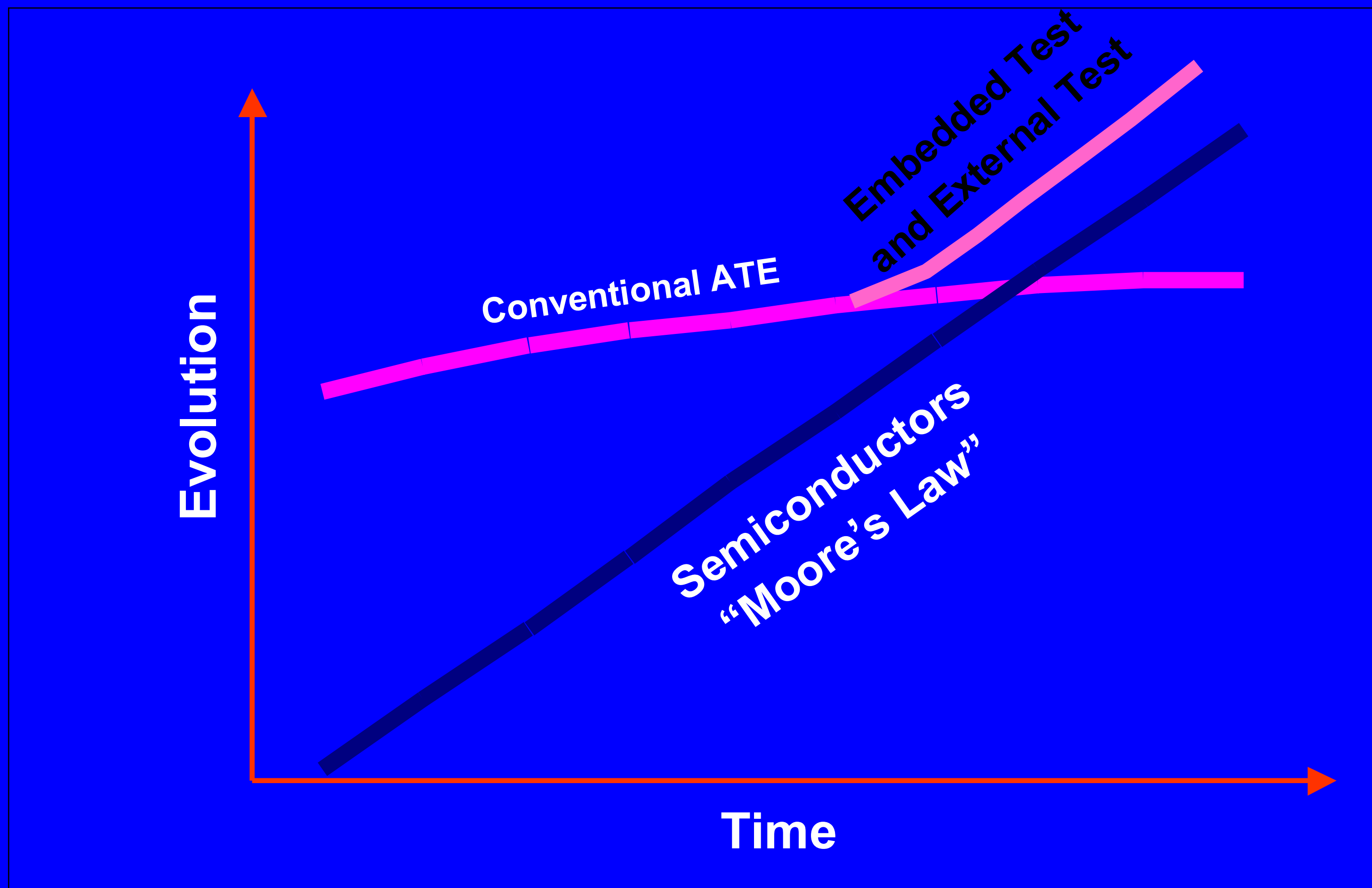


SOC Test - Embedded Test Solution

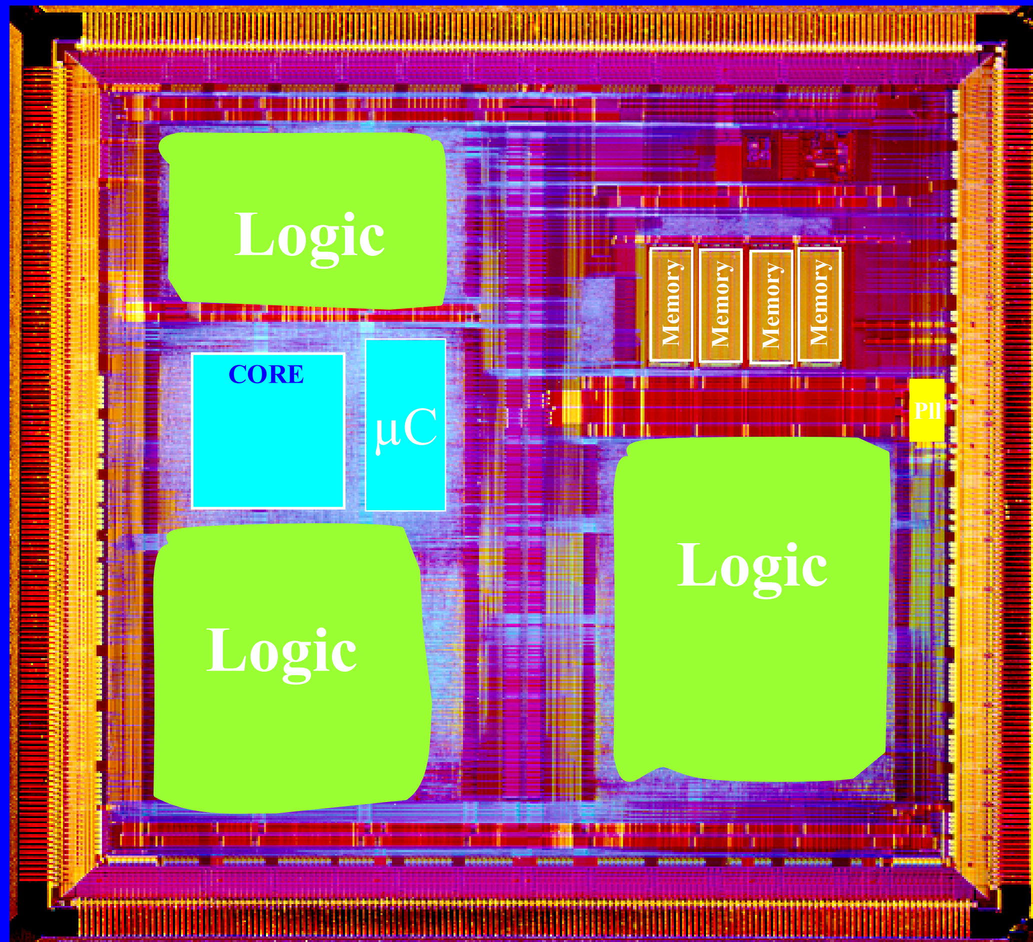


- Test is embedded during the front end of the design process
- Allows "divide-and-conquer" approach
- Each embedded test controller costs about 1,000 gates of silicon penalty

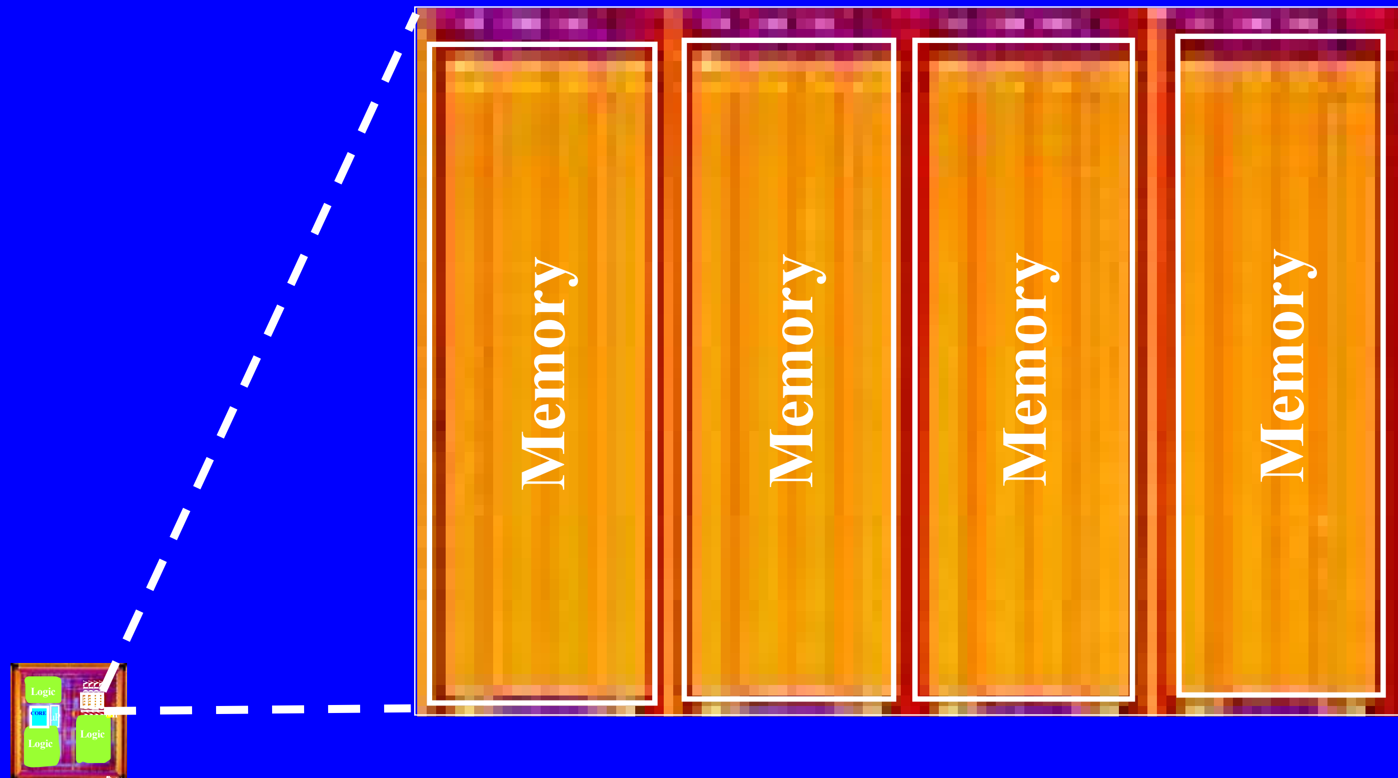
The Solution for Semiconductor Testing



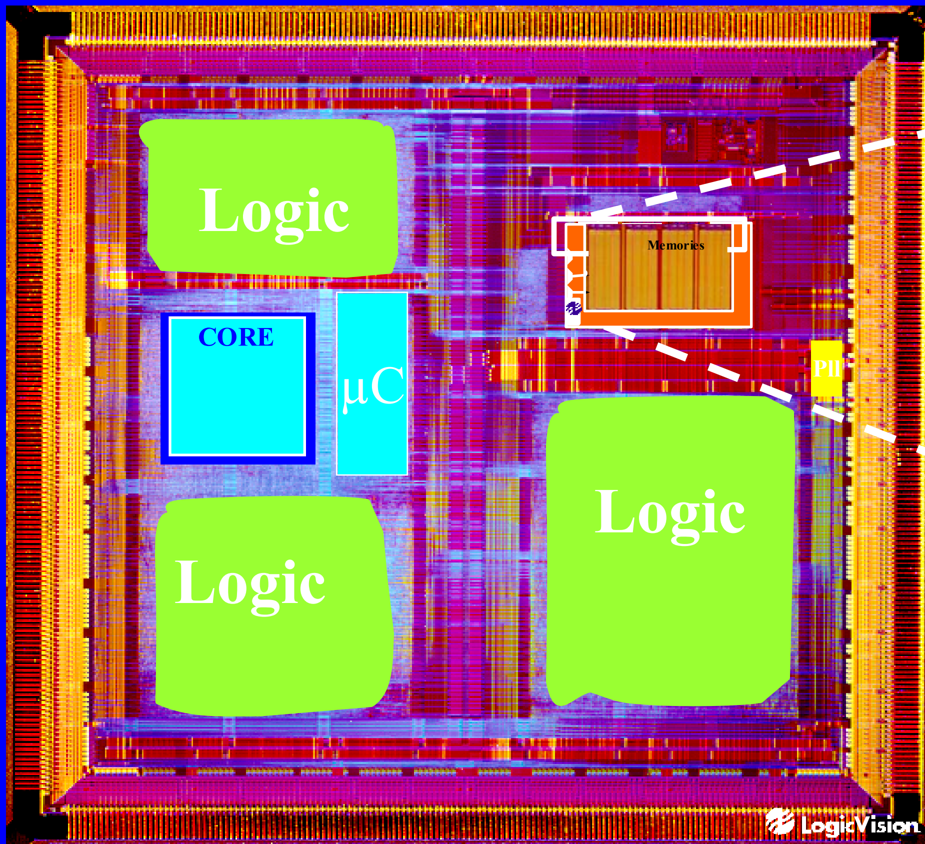
ASIC/SOC Test Solution

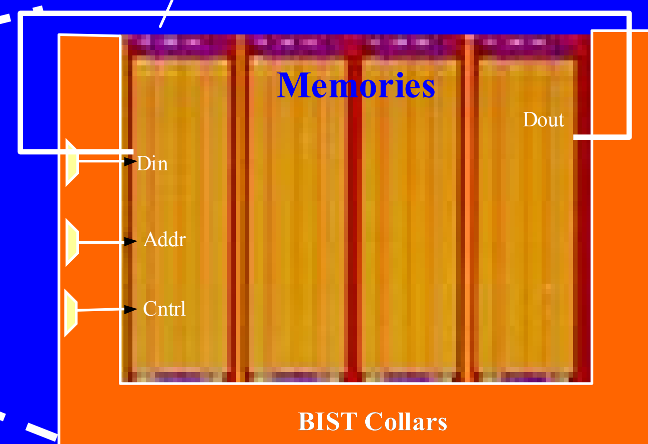


Embedded Memories

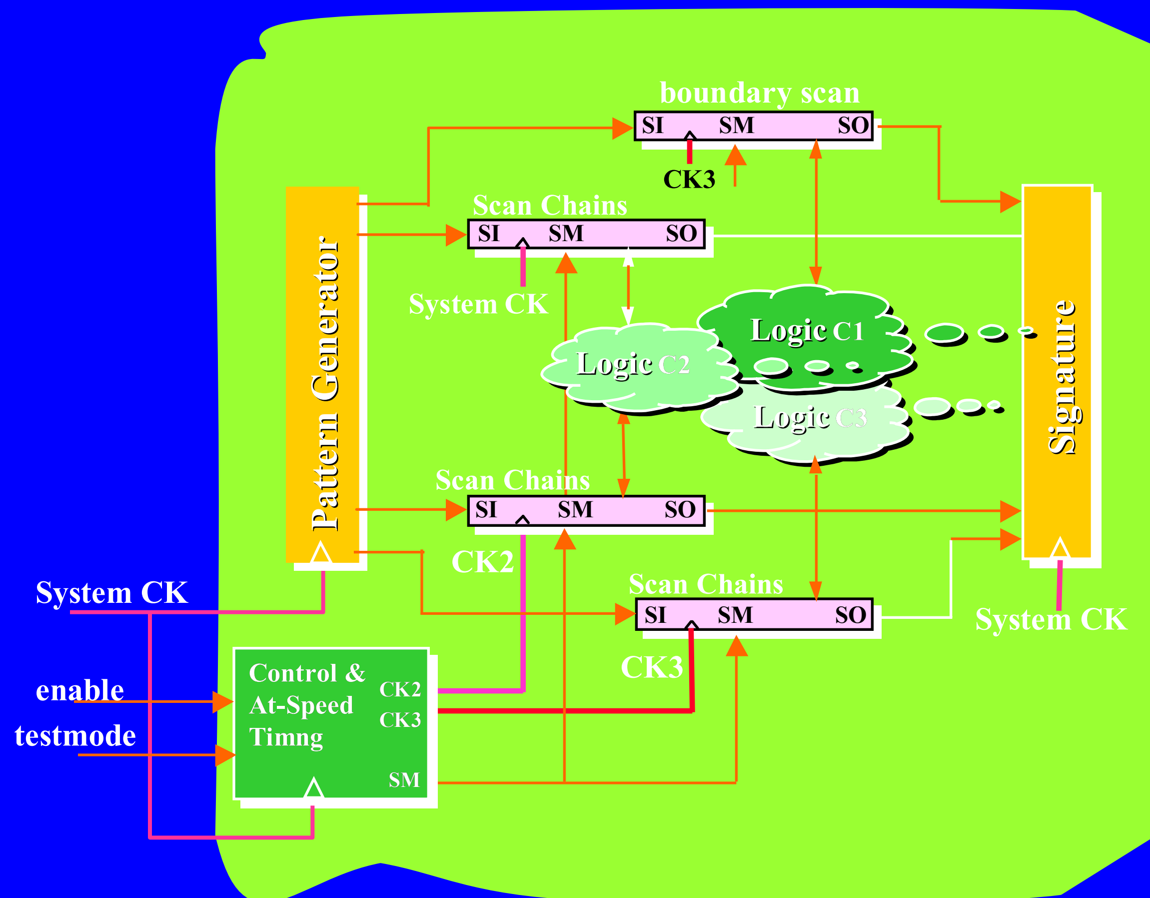


ASIC/SOC With Embedded Memory Test

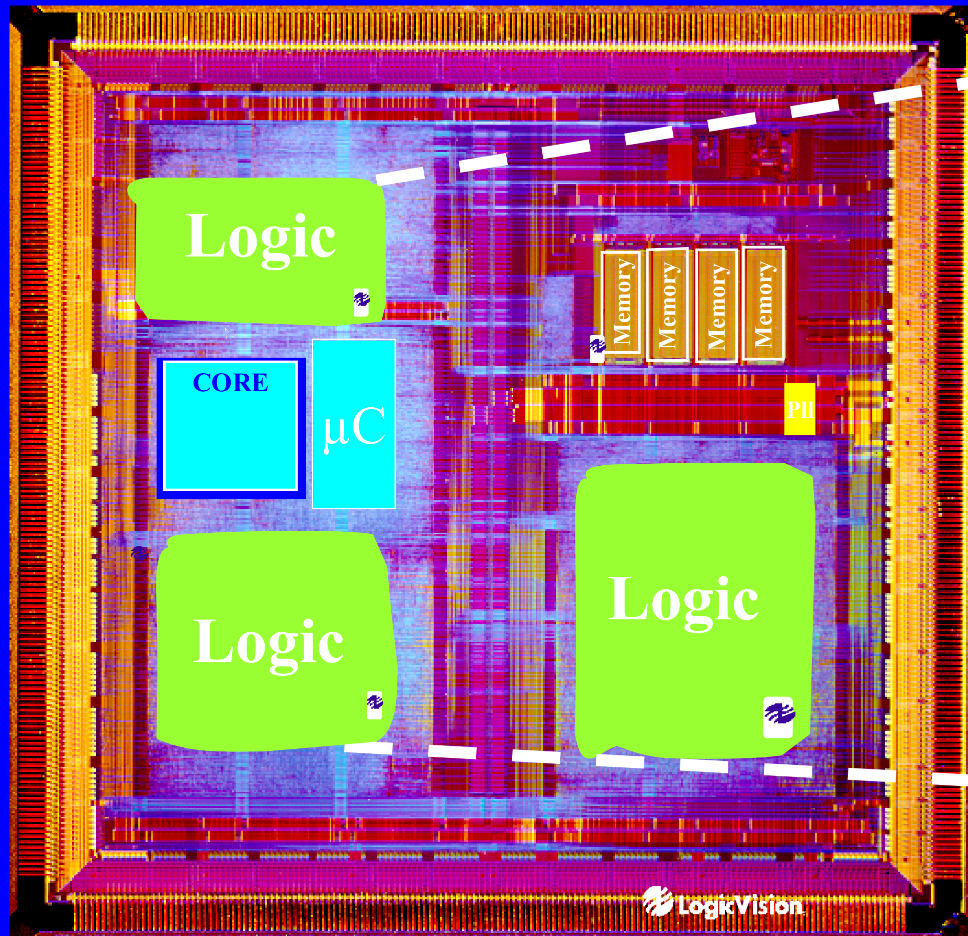


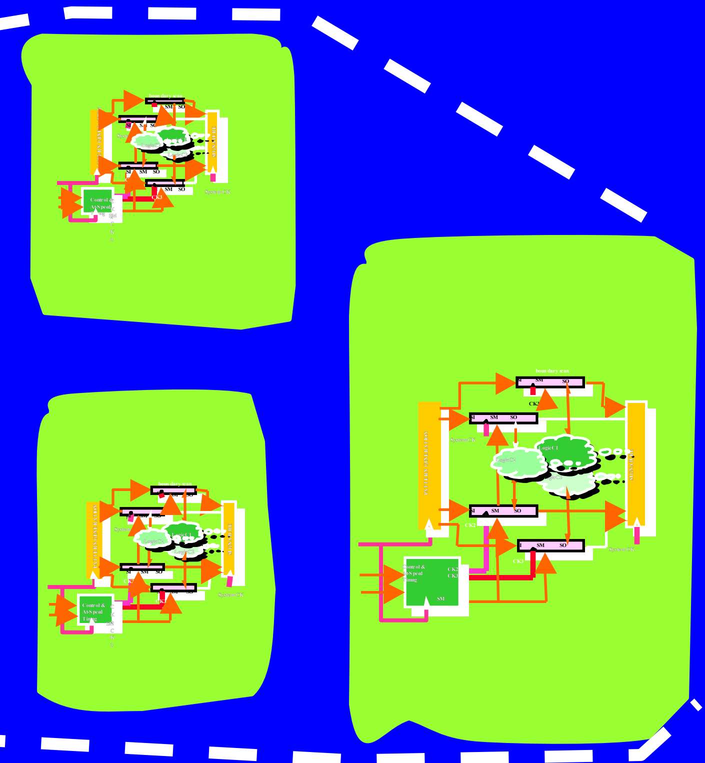


logicBIST™

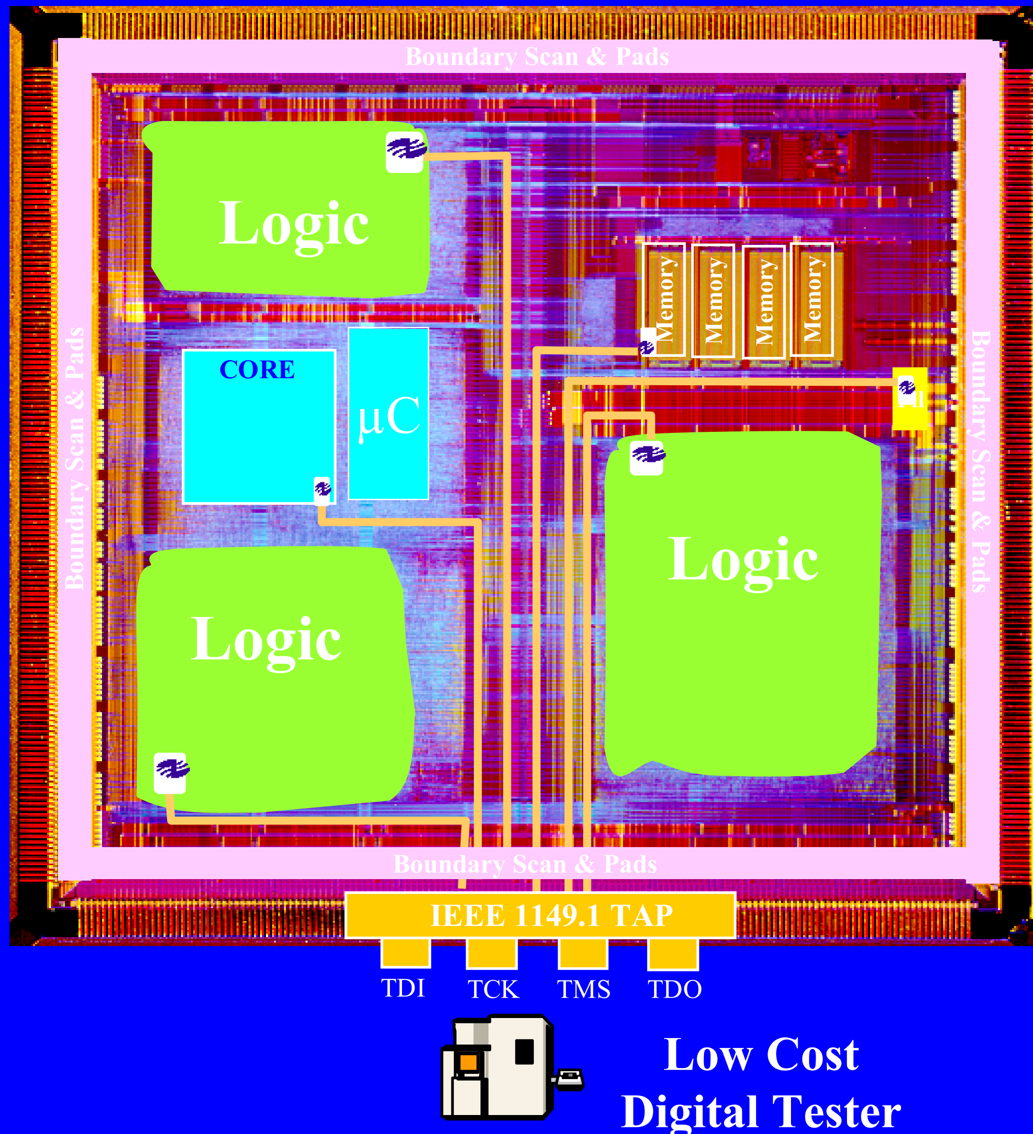


ASIC/SOC With Embedded Logic Test





Test Access



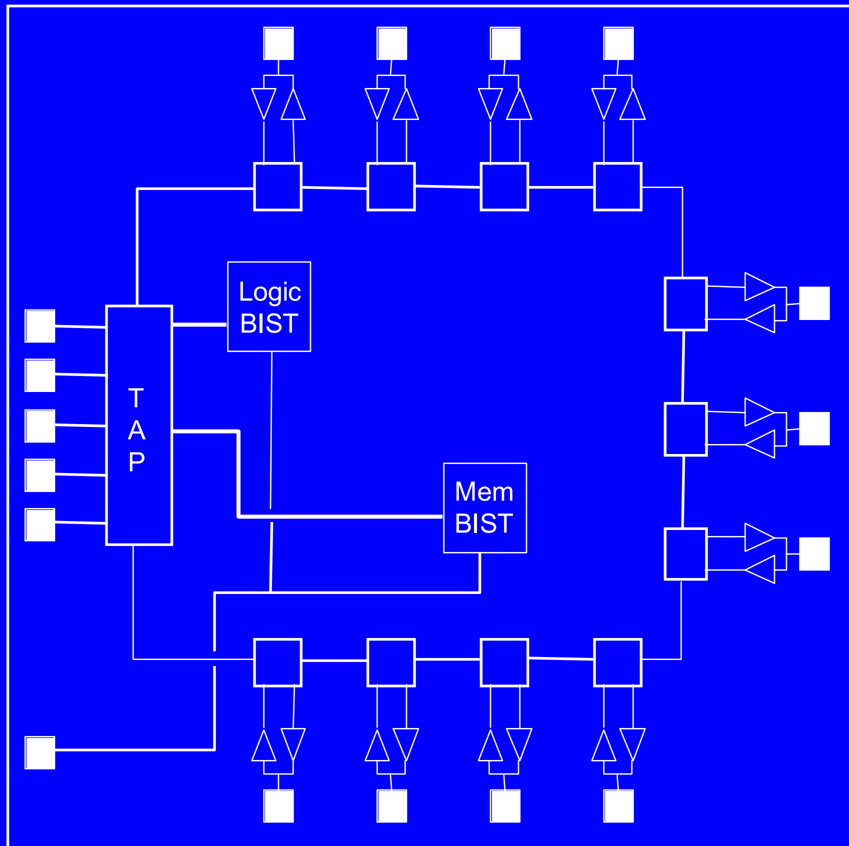
Automatic Generation and Assembly of Boundary Scan Cells and Pads

Automated Hook-up from Embedded Test Controllers

IEEE 1149.1 TAP Controller with Embedded Test Controller Instructions

Low Cost Digital Tester

Customer Test Case



- 500K Gates
- 503 I/O Pins
- 150MHz fmax
- Full Boundary Scan
- 95% Bi-directs
- 99.6% LogicBIST coverage

ATE Comparison

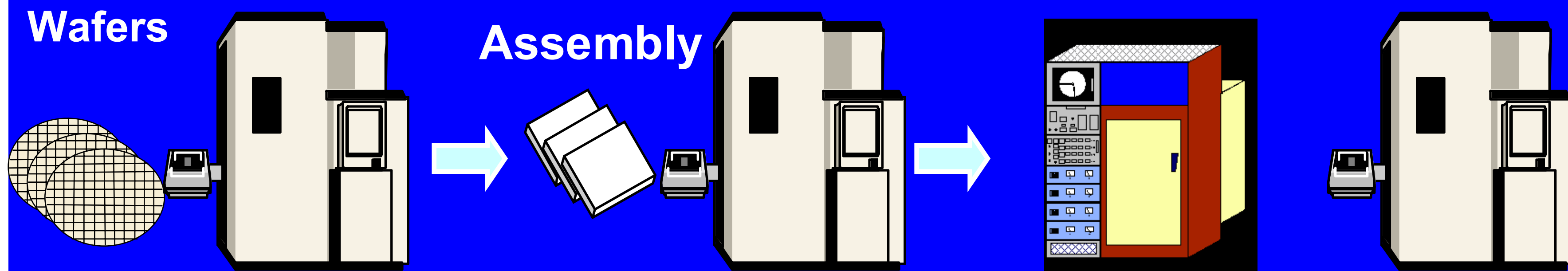
Burn-In Tester?

Capability	Functional	Structural
Pins	512	5
Vector Memory	8M	100K
Scan Memory	128M	0
PMU's	512	1
EPA	175ps	2ns
Frequency	400MHz	20MHz *
ATE Cost	>$3M	<$100K

** 300MHz High speed Clock card*

Burn-In Conventional Test Flow

Wafer Sort Test	Pre-B.I. Test	Burn-In	Final Test
IX9000	IX9000		IX9000
• 512 pin	• 512 pin	• clock	• 512 pin
• 400MHz	• 400MHz	• dc drivers	• 400MHz



Wafer Sort Flow	Pre-B.I. Test Flow	Burn-In Flow	Final Test Flow
• Logic/MemBist	• Logic/MemBist	• toggle	• Logic/MemBist
• Low Speed Funct	• At-Speed Funct	•serial scan	• At-Speed Funct
• ATPG	• ATPG		• ATPG
• DC I/O	• DC I/O		• DC I/O
• Iddq	• Iddq		• Iddq

Burn-In Embedded Test Flow

Wafer Sort Test

Low Cost ATE
- 30 pin
- 20MHz channel
- 300MHz Clock
- High Current PS

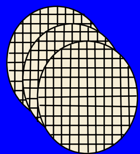
Burn-In

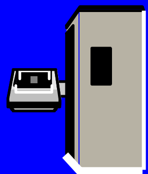
Burn-In System
- clock
- vec memory

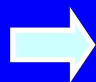
Final Test

High End ATE
- 512 pin
- 400MHz

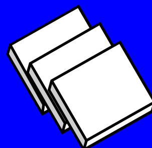
Wafers

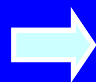


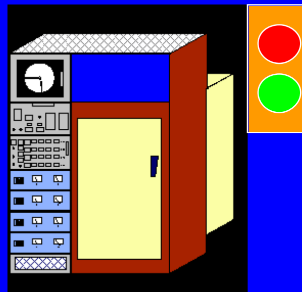


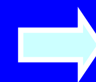


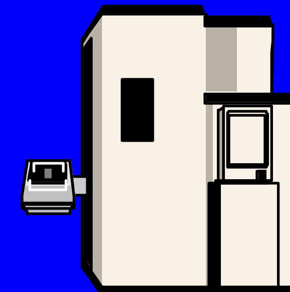
Assembly











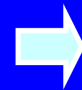
Wafer Sort Flow
- logic/Mem BIST
- I/O Structural
- I/O Leakage
- Static Idd

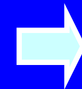
Burn-In Flow
- logic/membist
- membist
- I/O structural

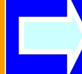
Final Test Flow
- Logic/membist
- At-Speed Funct
- ATPG
- DC I/O
- Iddq

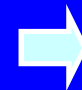
Embedded Test Burn-In Test Flow

Time0 — Load Units

Time0.1hrs — Room Temp At-Speed Test  Go/NoGo +Yield info

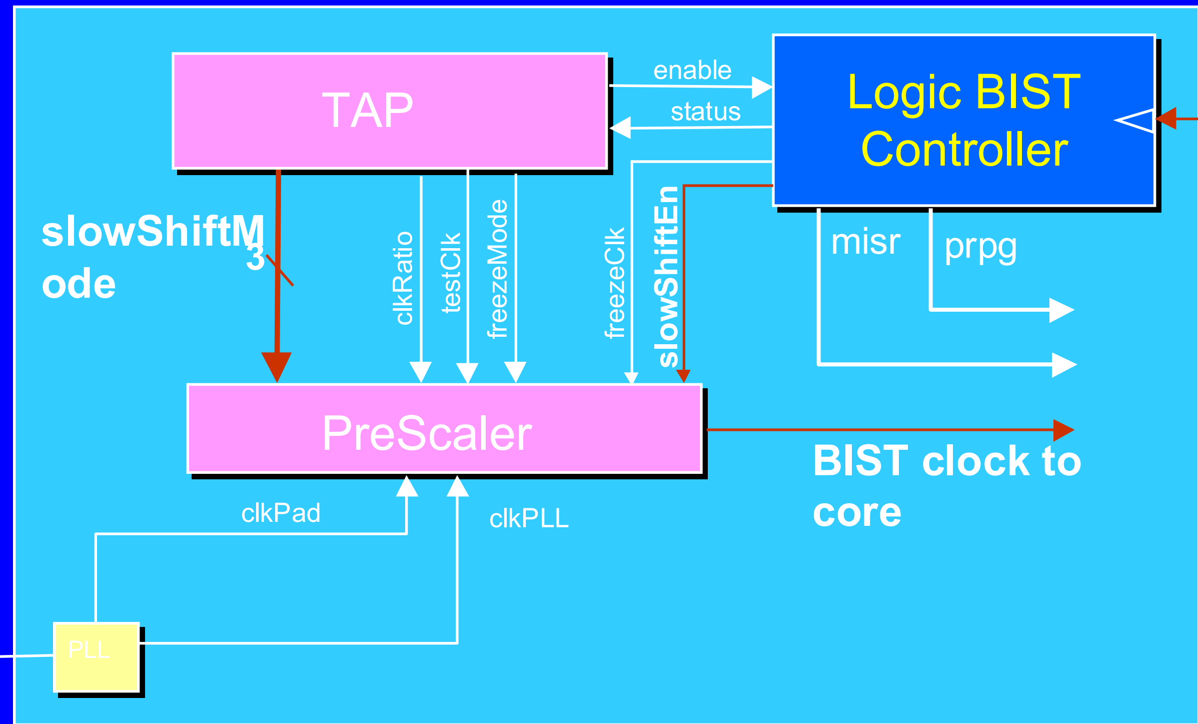
Time0 + 24hrs — Low Speed Structural test  Complete Cycle

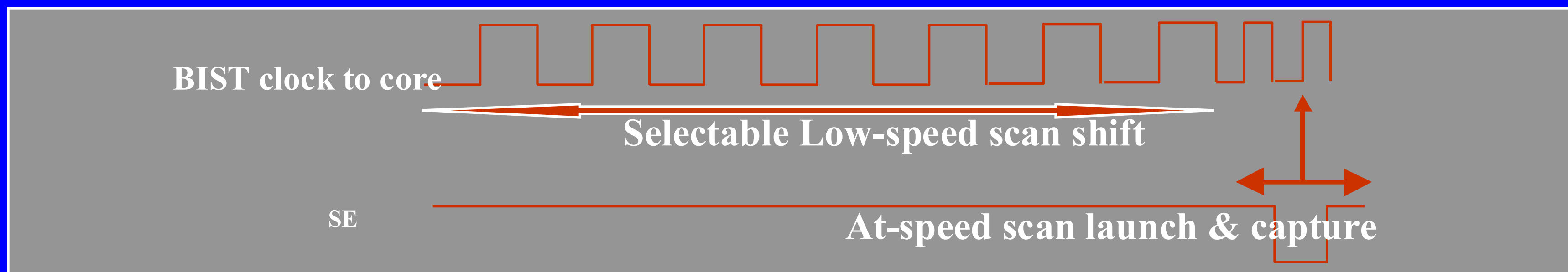
Time0 + 24.1hrs — Room Temp At-Speed Test  Go/NoGo & Diagnostics

Unload  Final Test

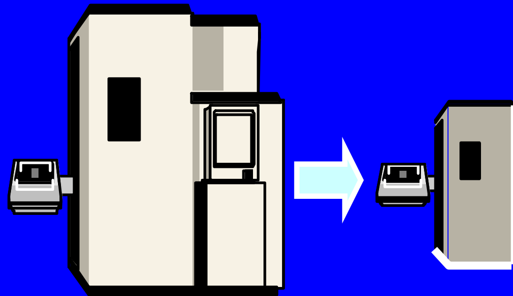
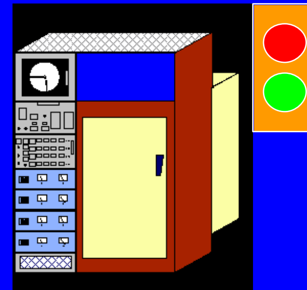
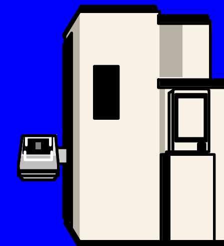
Logic BIST Low Power Mode

slowShiftMode			
0	0	0	7/8 speed
0	0	1	3/4 speed
0	1	0	5/8 speed
0	1	1	1/2 speed
1	0	0	3/8 speed
1	0	1	1/4 speed
1	1	0	1/8 speed
1	1	1	Full speed





Savings with Embedded Test Flow

Wafer Sort Test		Pre Burn-In Test	Burn-In	Final Test
				
· $450/hr · Test time · up-time	· $150/hr · < Test time · > Up-time		· Early Detection · At-Speed Test · Go/No-Go · Diagnostics	· Reduced Config · < Test Time
$1.00		+$1.30	+$0.20	+$0.20
				Total $2.70

Hardware Implications

- IC Hardware
  - Logic and MemoryBist
  - Bi-directs on I/O's
  - Global latched PASS/FAIL signal
- Burn-in Hardware
  - 10K vector memory 100K to initialize JTAG
  - 100K vector memory for diagnostics
  - Embedded Test Software for diagnostics
  - High Speed Clock for at-speed test
  - Use of existing JTAG on board O.K.

Summary

- Embedded Test allows for real at-speed testing during burn-in
- Implementation of embedded test reduces overall test costs
- Process steps can be reduced or eliminated with embedded test
- Manufacturing defects through burn-in can be detected earlier in process
- Expensive Final test ATE resources can be implemented at burn-in test

AMD Athlon

Next Generation Burn-in & Test System for Athlon Microprocessors : "Hybrid Burn-in"

Mark Miller

Sr. Member of Technical Staff

Athlon Product Development

Advanced Micro Devices

What Is “Hybrid Burn-in” ?

- **New generation of burn-in technology at AMD that has evolved due to the unique requirements of the Athlon and Duron microprocessor product lines**
  - More electrical features than “traditional” burn-in (minus ovens)
  - Individual DUT temperature, voltage, and frequency control
  - Able to execute X86 code and BIST code individually
  - Failed units can be shutdown individually to prevent damage
  - Real time individual data collection and communication to host
- **“HBI” is actually a multiple position, independently programmed, low pin-count, *tester* that is able to economically run long test times (burn-in durations) at unique burn-in conditions**

The Purpose of Burn-in Is Not New :

- There is always a quality driven requirement to accelerate various silicon failure mechanisms so that infant mortals can be removed from the general population before shipment to customers

  - Silicon failure acceleration methods include :

    - Temperature
    - Voltage
    - Circuit test / node toggle coverage
    - Current density (frequency)

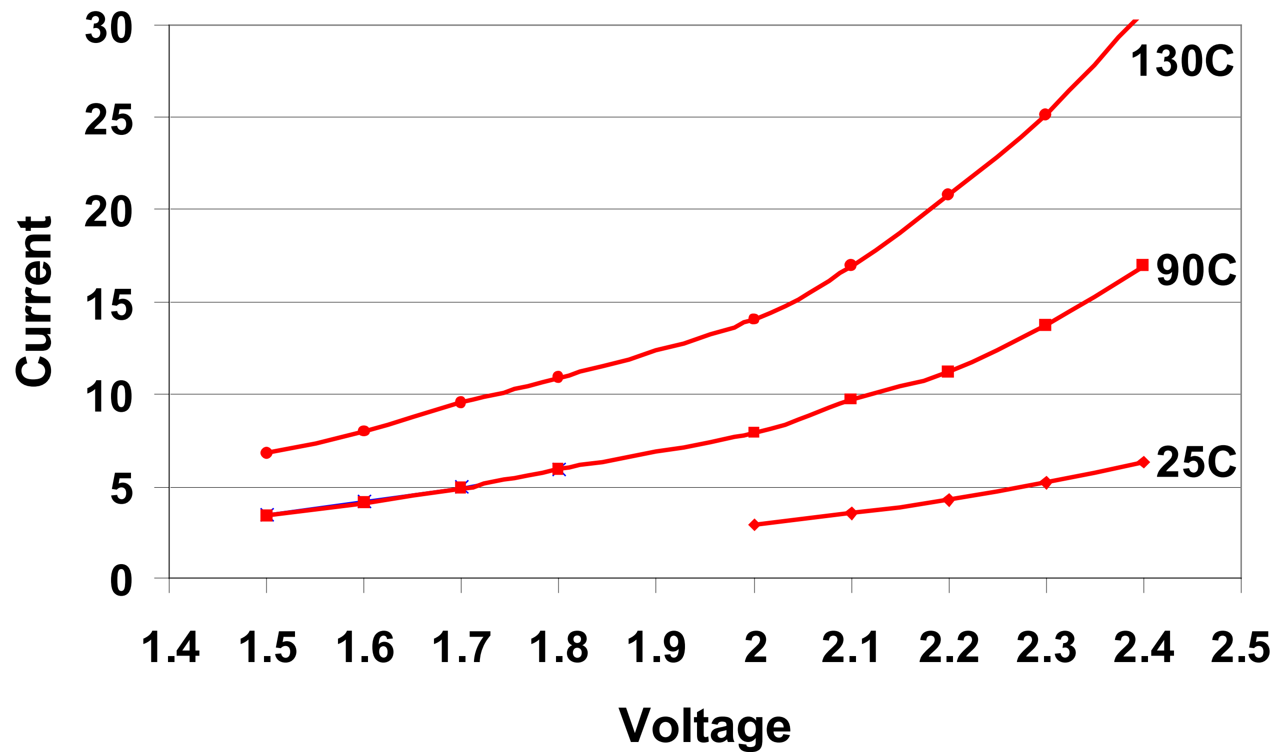
Why Hybrid Burn-in ?

- New silicon technologies and high product transistor counts (>>50 million!) preclude the use of traditional methods to accelerate failure mechanisms during burn-in
  - Wide variations of static power (Δ10W+ across wafer lots)
  - High device currents at burn-in conditions (up to 30A)
  - Sensitive C4 chip-attach technology needs tight temp control
  - Lower voltages with tighter tolerances are required by products
  - Higher frequencies. External : 100-200MHz. Internal : >1 GHz
  - Complex test interfaces require more flexible "drivers" to control BIST, SCAN, JTAG interfaces, and X86 code execution
  - Data collection required to support product qualifications and to measure continuous improvement.

Transistor Leakage History

AMD Microprocessor Static Leakage

Temperature and Voltage Effects



Thermal Runaway

- **Thermal runaway is a destructive positive feedback condition that can occur when inadequate thermal control is combined with a silicon process technology where leakage increases exponentially with temperature**

Thermal Runaway

Increased Heating

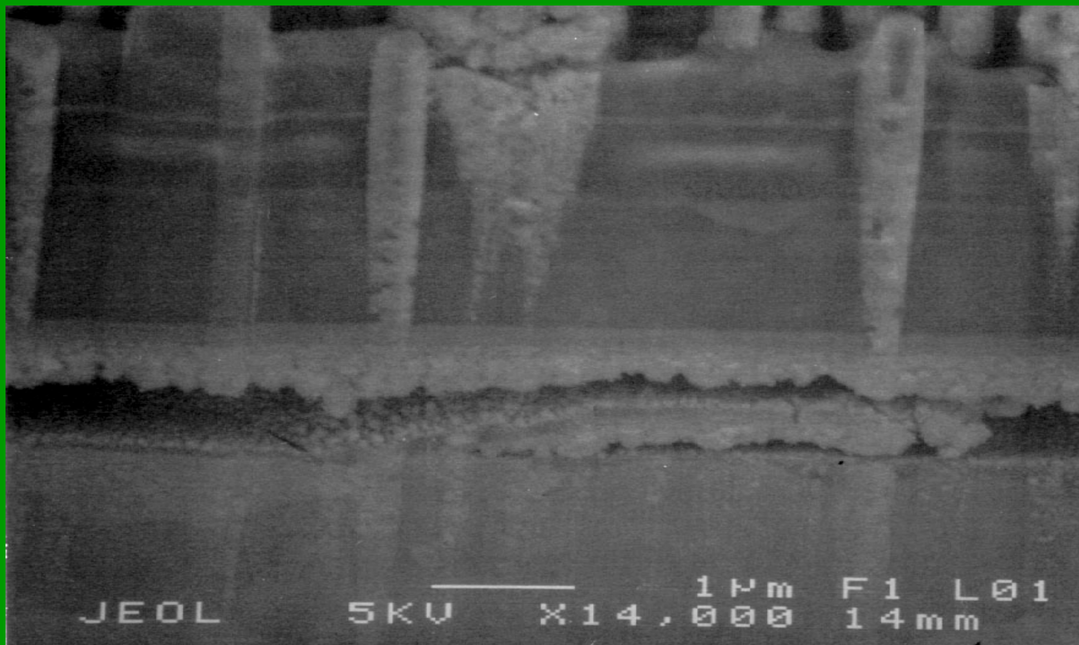
Higher transistor Leakage

Increased static ICC

Higher Power Dissipation

Overheating Causes Failures

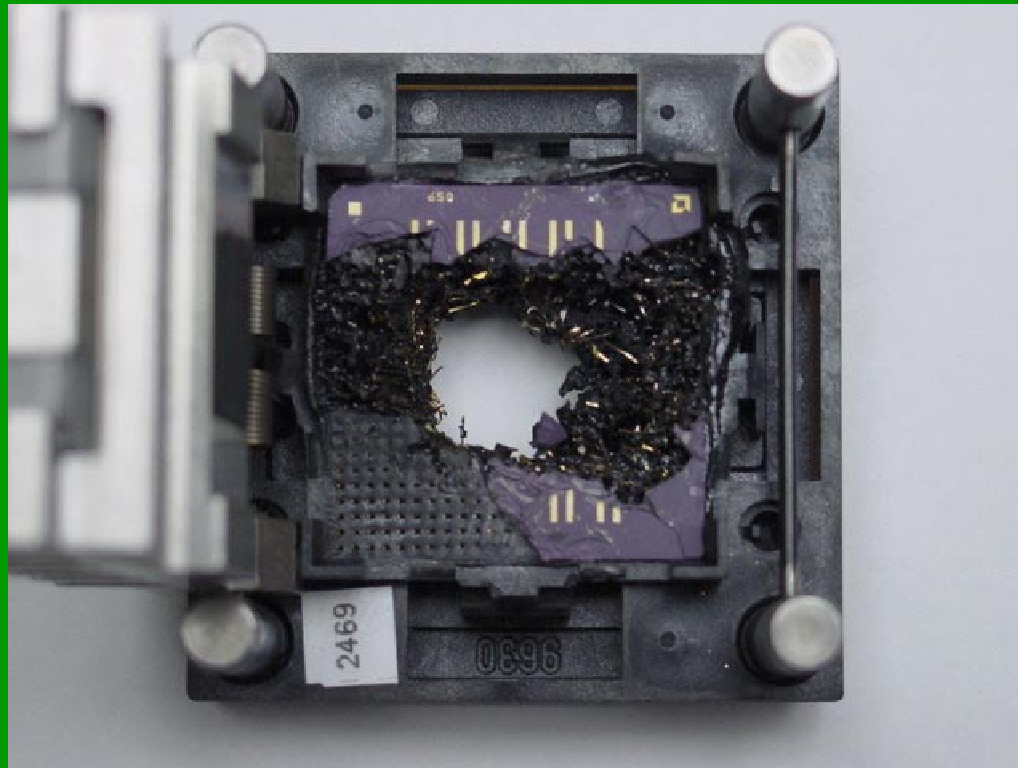
- The original Athlon qualification lots had failures due to thermally over-stressed C4 bumps. This was due to the wide variation in device leakage currents and inadequate (inflexible) thermal control during the accelerated life testing



< C4 bump delamination

Chernobyl Effect

Test sockets can be destroyed by thermal runaway. Active thermal control with constant die temperature feedback insures stable temperature and prevents product or hardware damage



What's Different ?

- 35 amps per DUT available vs. ~2 amps in traditional BI
- Individual Vcc control from 1 V – 3 V
- Individual thermal control from 25C - 140C
- Additional test access through JTAG and AMD special test modes
- Ability to run ATPG patterns through SCAN port with special clocks
- Independent test programming capability with visual C control code
- Directed testing with X86 code that is loaded to Athlon's cache
- Higher node toggle coverage possible with tester interface
- More tightly controlled temperature allows shorter BI duration
- Individual voltage stress is possible
- Real time data collection per unit

Burn-in Specs Drive Test Costs

- Inadequate thermal capability at burn-in can force a product's back-end flow to include an expensive VLSI test insertion to screen out units that might thermally runaway
- "Hybrid burn-in" customizes conditions per DUT and eliminates the requirement for a pre-burn-in test

Block Diagram of Traditional Burn-in System

DRIVER

Common Test Pattern Generation

Common Clock Generation

Single **Common** Power Supply for 100's of DUTs

BIB

Athlon

multiple DUTs

Athlon

Passive Heatsinks

Airflow

Oven Required

Block Diagram of Hybrid Burn-in System

- NO Oven Required -
Standard circuit boards and components are used

Fan

Control

Active Heatsink

Control

Independent Thermal Management Circuits

Independent Voltage Supply

Sense

Source

Athlon

Temperature Sense

Independent Frequency Control

Compare

Drive

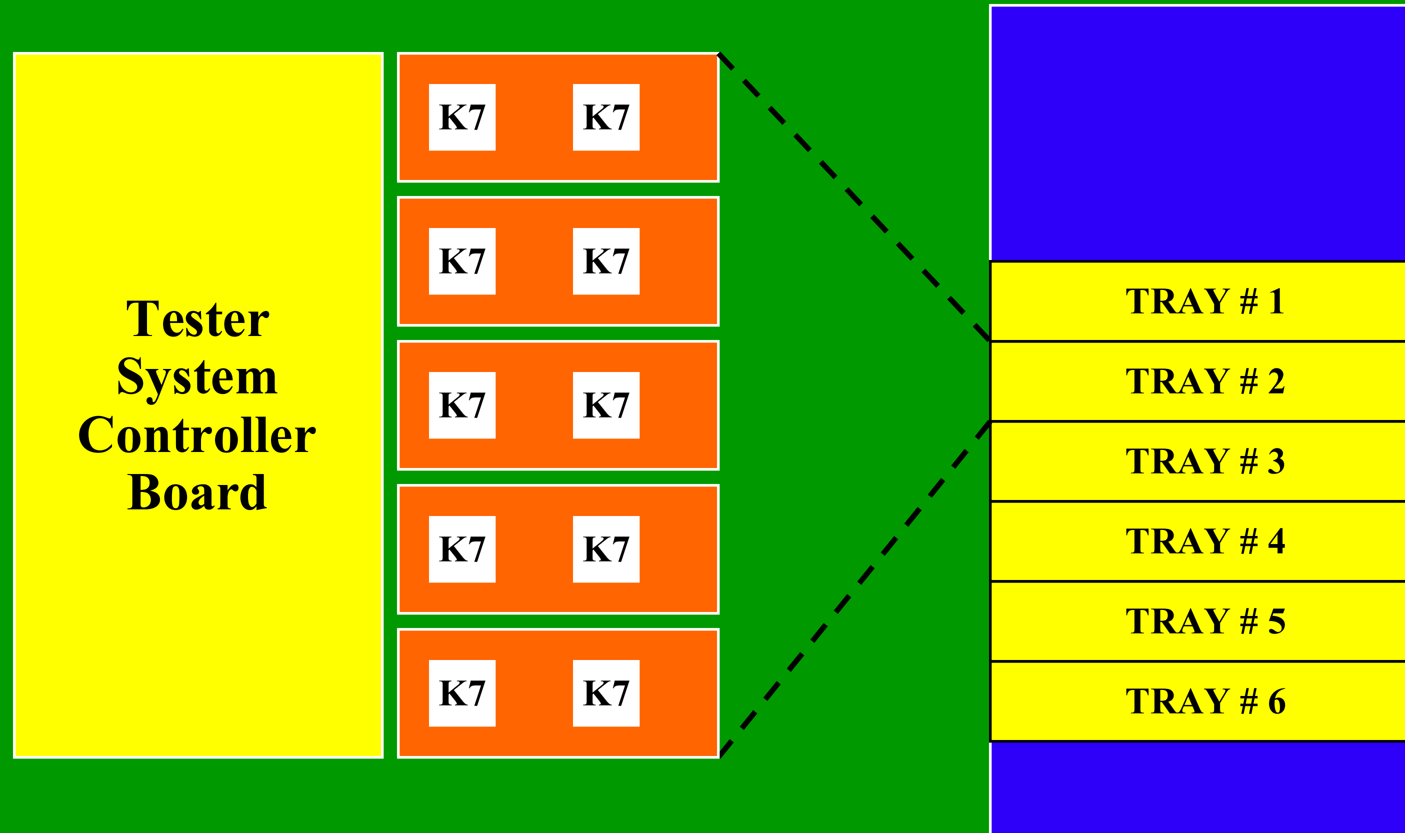
Independent Test Pattern Control

X86 based tester running standard C++ code independently controls Athlons DUTs and their support circuitry

Hybrid Burn-in Hardware Configuration

Tray
- 10 Athlons per tray
- Modular configuration

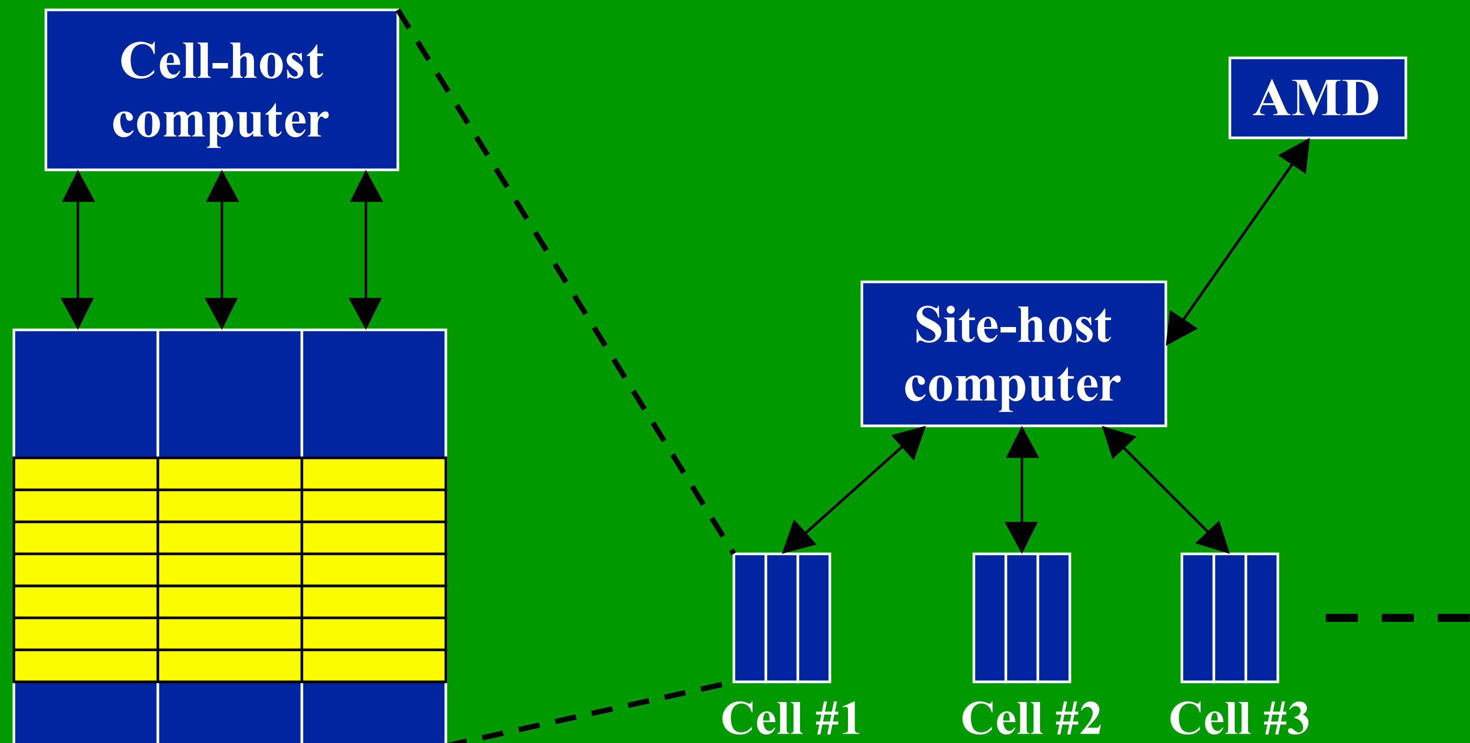
Rack
- 6-7 Trays per rack
- Ethernet access



Hybrid Burn-in System Configuration

Cell
- 3 racks / cell

Site
- 100s of cells per site



K7 Hybrid Burn-in Prototype Chassis

Operator Interface via Touch-screen

AMD Burn-in Facility

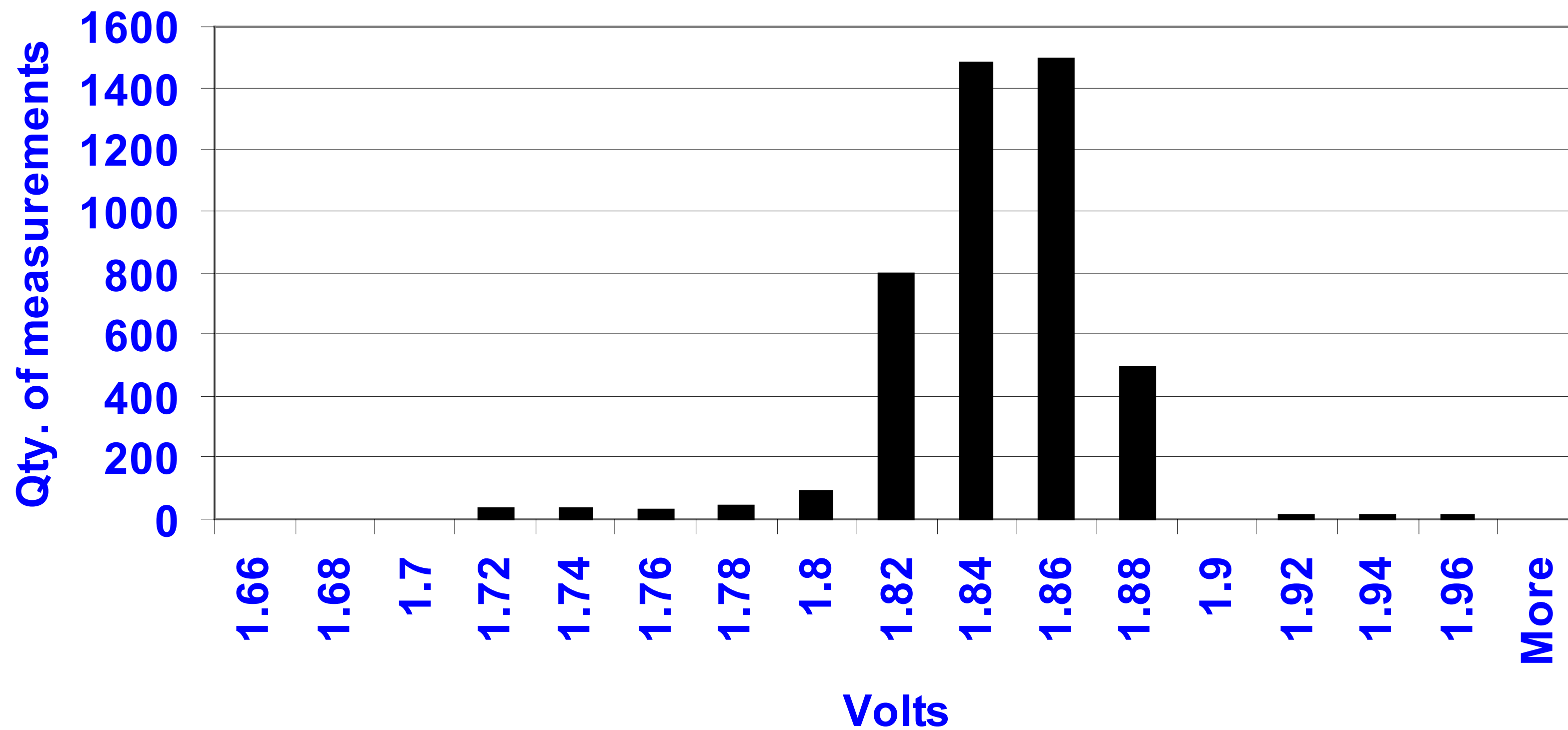
Hybrid Burn-in Benefits

- Handles very high leakage (fast $$) devices that otherwise could not be burned in
- Removes the need to prescreen parts based on power or thermal requirements. All types of parts are run together greatly simplifying production logistics and reducing cost
- Customized conditions for individual parts on the fly
- Able to detect over-temp and fail conditions so that individual DUTS can be shut off to insure that hardware is not damaged and neighbor parts are not affected. One failing unit cannot bring down the entire BIB
- Real time data collection on every unit at programmable time intervals allows a new level of insight to the real production conditions and the failure rates over time.

Benefits (Continued)

- Microsoft visual C++ test programming environment that is very similar to that used in many simple VLSI testers
- Higher capacity, better accelerations (therefore shorter durations) vs. traditional burn-in
- Improved quality : HBI is really another test insertion that is capable of detecting and excluding defective parts
- Quality is also improved because parts can be thoroughly tested at many temperatures during the burn-in/test cycle and this is usually impractical on short ATE test insertions
- Standard support components can be used since only the DUT and socket reach temperatures in excess of 50C.   No ovens or special high temperature rated boards are required

HBI Voltage Control Data



HBI Thermal Control Data

HBI Fail Tracking in Time

Hybrid Burn-in Failure Monitor Time Logs

Tradeoffs

- Initial capital cost is 3X higher than traditional burn-in but still significantly less expensive than most commercial full feature general purpose, burn-in systems
- Hardware reliability is worse simply because there are more complex active components to fail than traditional burn-in
- More complex setup and programming. No DIP switches! Need VLSI test engineers to develop C++ burn-in programs
- Need higher level of operator training at burn-in vendors due to more complex interfaces. This also increases per insertion cost charged by vendors
- Clean and fully air-conditioned facility is required
- Lead time to fabricate is 3X longer than traditional BI due to many long lead components (Tantalum caps, etc)

Status

- Hybrid burn-in is in full scale ramp at AMD with tens of thousands of positions up and running Athlon production
- Individual thermal, voltage, and frequency control has allowed many Athlons to ship that would have otherwise been unable to burn-in under a traditional set of conditions
- AMD has internally managed the design, procurement, and fabrication of the systems in order to achieve aggressive schedule and cost goals.

… Beyond Burn-in

- Demonstrating ATPG pass/fail testing to reduce high cost VLSI tester loading
- Implementing full temperature range tests that are not practical with high cost VLSI testers that must keep short test times
- Implementing more exhaustive commercial grade test flows that make full use of the burn-in hours to fully test products
- Demonstrating ATPG delay fault testing at rated product speeds so that full vector sets are covered at high frequency
- Exploring full potential of unlimited JTAG access. Athlon utilizes many private instructions that can be exercised during burn-in

Summary

- Sub-micron products widely variable power dissipation requires efficient thermal solutions with flexible feedback and control
- Ever lower voltages and higher DUT currents require dedicated voltage sources to compensate for the smallest voltage drops
- Higher product frequencies require site level clock generation
- Complex products require flexible, independent, pattern generators to allow true "test during burn-in".

- The challenge met by Hybrid Burn-in was to satisfy these new requirements of Athlon while providing a new cost effective burn-in architecture for the future

Acknowledgment

- **Hybrid burn-in is a design evolution based on years of previous work by earlier AMD K5 and K6 engineering teams in partnership with numerous sub-contractors and component suppliers who have performed superbly to accomplish this project within the required scope and schedule.**