Burn-in & Test Socket Workshop

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Session 4
Monday 3/05/01 3:30PM

Burn-in Board Design

"High Power BIB Power Plane Design And Decoupling Simulation"

Zamel Jaafar - Intel (Presenter)
Anthony Wong - Intel
Peter Ngaa - Intel

"Cost Effective Burn-in Board Design"
Frank W. Jurasek - IBM Microelectronics (Presenter)
Ralph J. Bernardini - IBM Microelectronics (Presenter)
James M. Brown - IBM Microelectronics (Presenter)

"High Speed & High Power Burn-in Board Design"
Hon-Lee Kon - Intel
Cher-Shyong Low - Intel
Presented By: **Zamel Jaafar** - Intel

High Power BIB Power Plane Design and Decoupling Simulation

2001 Burn-in and Test Socket Workshop

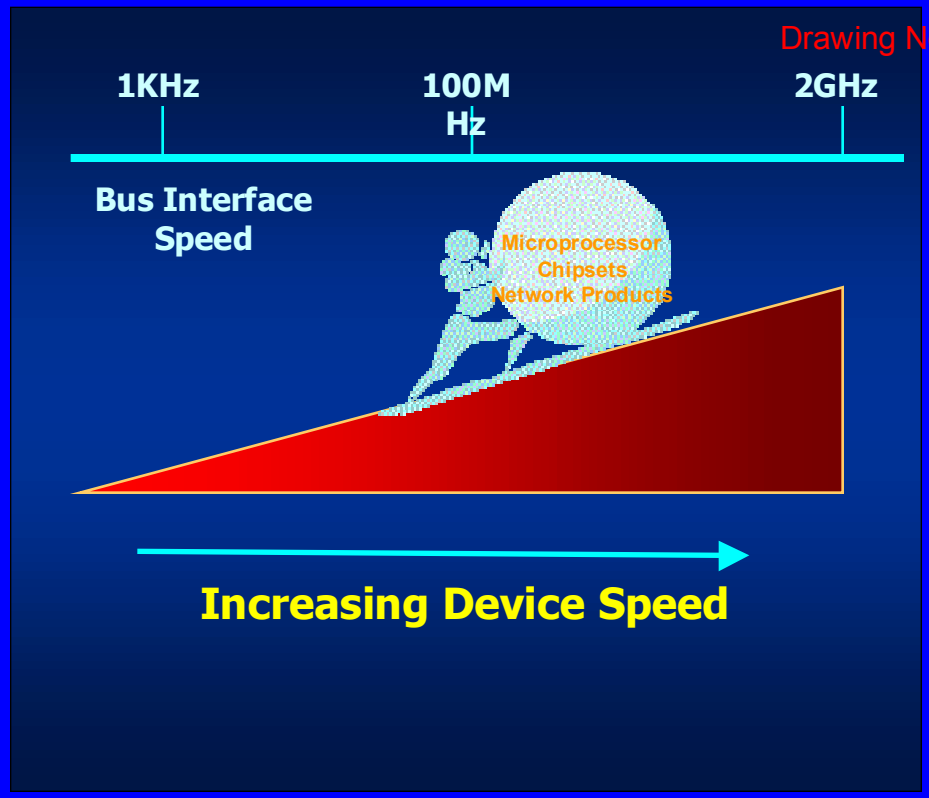
BiTS
BURN-IN & TEST SOCKET WORKSHOP

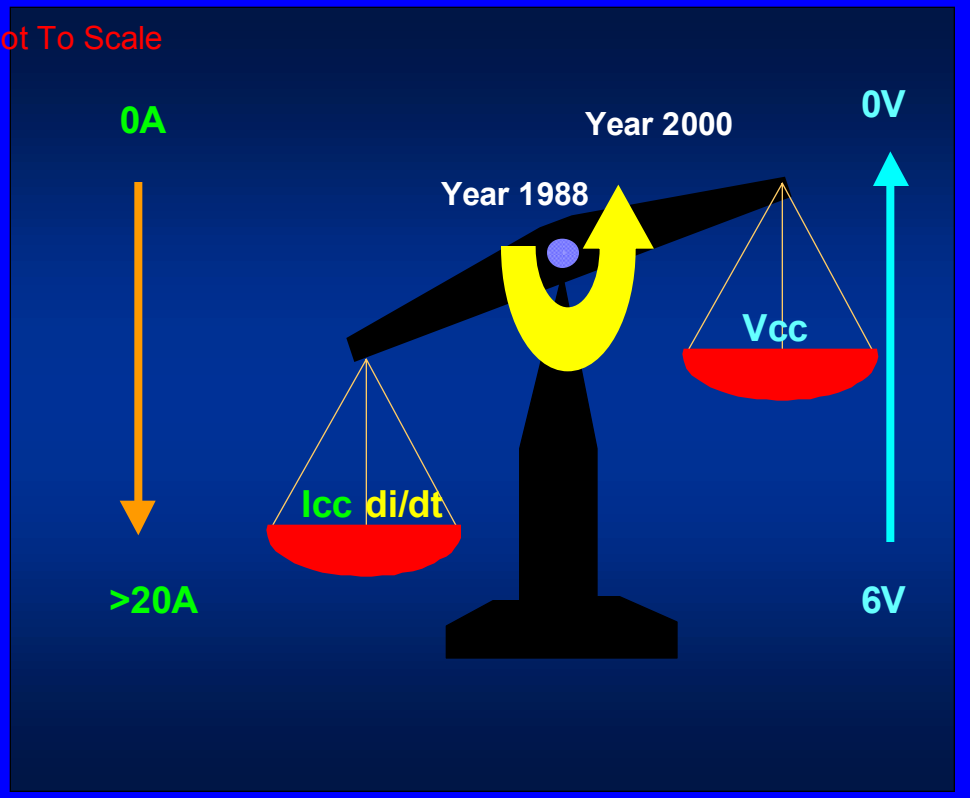
Zamel Jaafar/ Peter Ngaa/Anthony Wong
ITTO, Intel

Agenda

- Current trend of processor operation conditions
- Power Plane Design Considerations
- Decoupling Simulation
- Summary
- Acknowledgement

Current Device Operating Trend



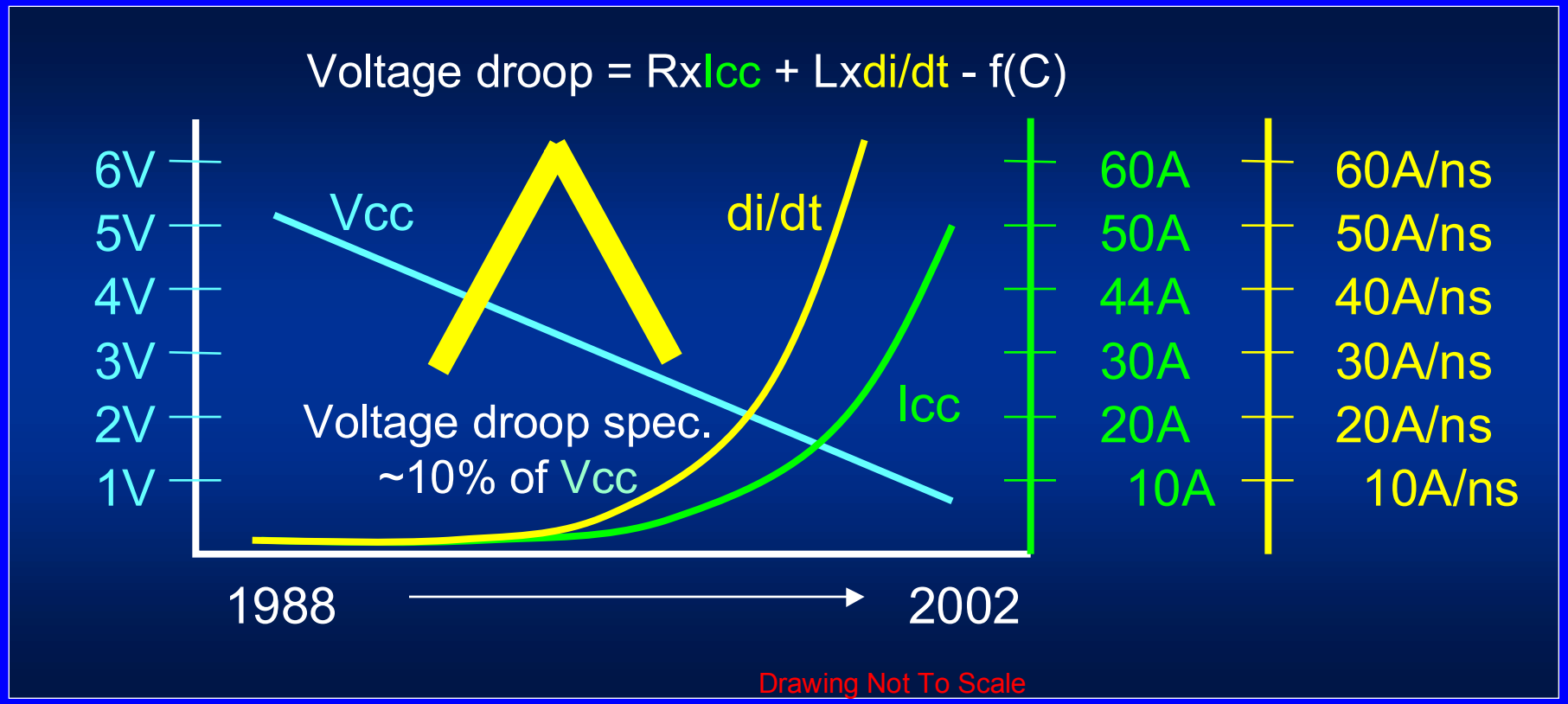


Device Operating Conditions Changed Drastically !

How does this impact us?

Device Power Trend During BI

- VCC is progressively dropping
  - Icc and Power are rising
    - Maximum di/dt is rising dramatically



BIB Power Plane Design Considerations

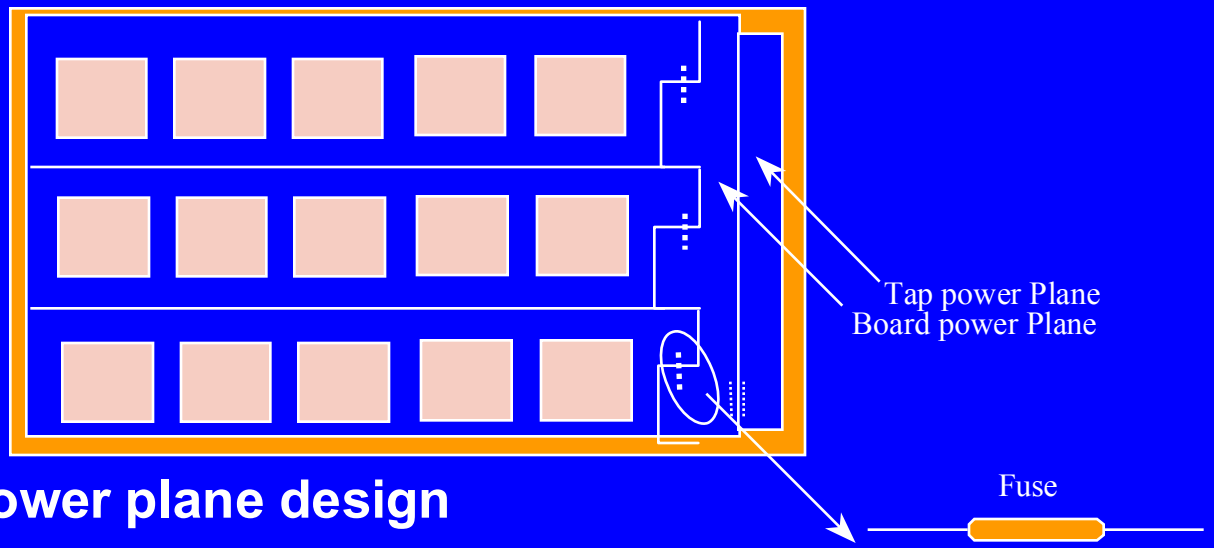
- Provide stable reference voltage for exchanging digital signal
- Distribution of power to all devices on BIB evenly.
- Maximum current carrying capability
- Maximize the capacitive coupling
- Minimize inductance and resistance

Voltage droop = RxIcc + Lxdi/dt - f(C)

Power Plane Design

- Basic Power Plane design
- High current power plane design and
- Very high power plane design.

1) Basic Power plane



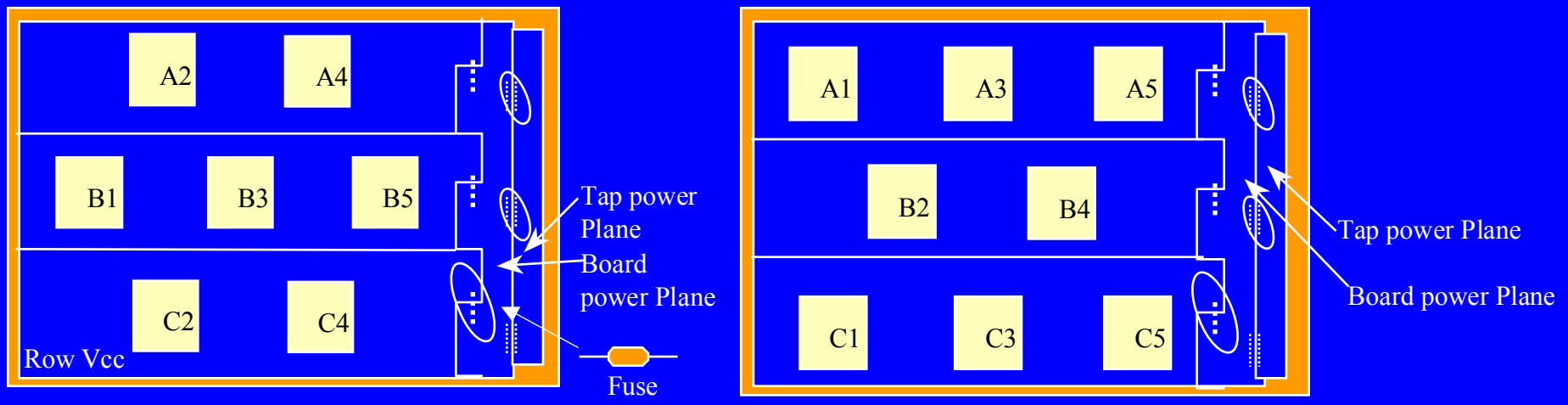
- Basic power plane design
- Very low Current capability < 15A per board with 6/8 layers PCB and 62.5 mils thickness.

Limitation of Basic power plane design.

- Unable to meet 10% VCC noise margin for low BI VCC (ie. <2.5V).
- Caused large Voltage drop across BIB
- Long power delivery path & high resistance along power delivery path for last DUT

2) High Current Power Plane Design

- 2 separate layer approached
- 2 separate fuses for alternate units per row
  - Enable higher current per DUT (>15 A per BIB)
  - Reduce Vdrop across the BIB.

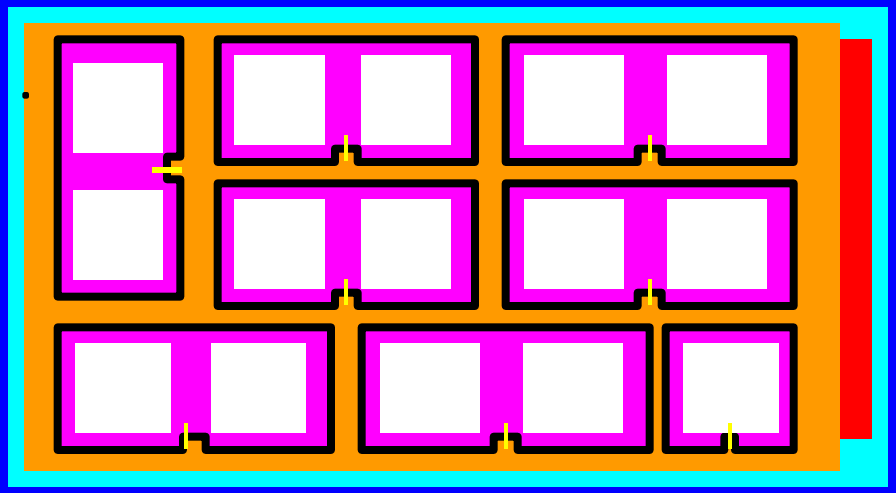


Limitation

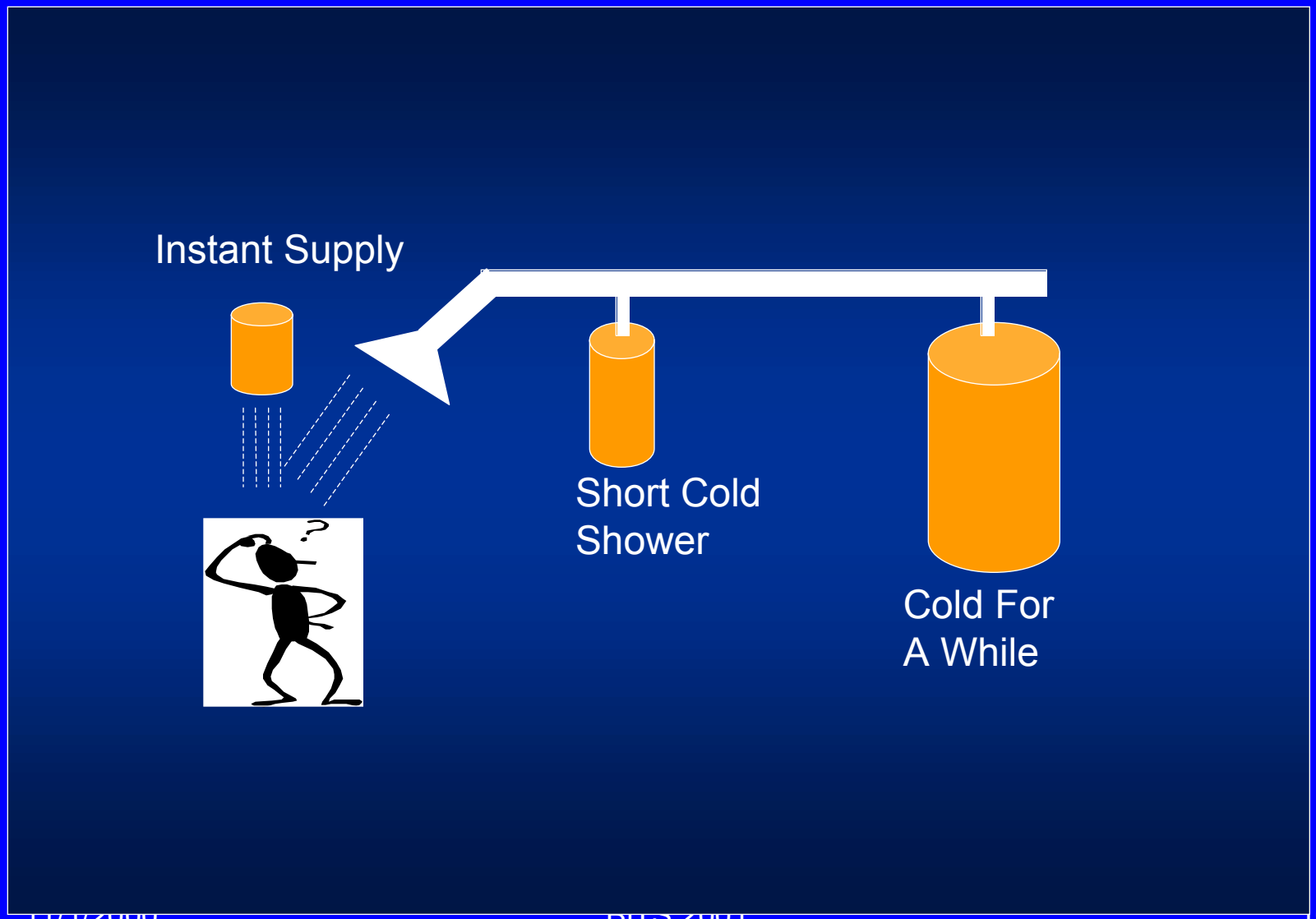
- **Unable to cater for extreme high current > 90A per board**
- **Unable to meet 10% VCC noise margin.**
- **Caused Voltage drop across BIB**
- **Still Long power delivery path and high resistance along power delivery path for last DUT**

3) **Very High Current Power Plane Design**

- 2 separate layer approached
  - One layer is a solid plane throughout whole BIB
  - One layer have a 2 device isolation island design.
  - 2 Dut per fuse
    - Enable higher current per DUT > 20A
    - Reduce Vdrop across fuse holder.
    - Able to meet 10% Vcc noise.
- 2X oz Cu plane to minimize resistance and to improve power delivery.
- Minimized resistance along power delivery path. Better power delivery

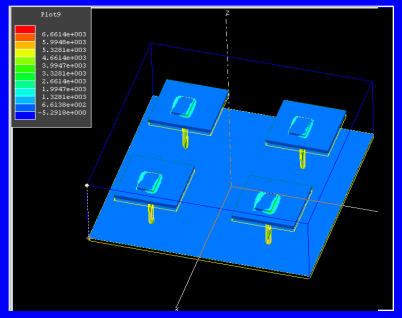


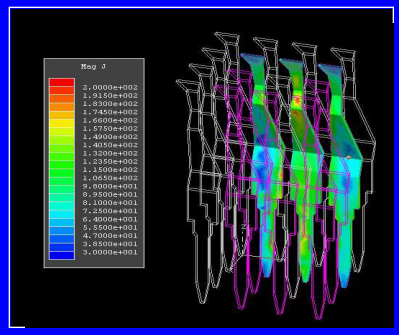
POWER DECOUPLING



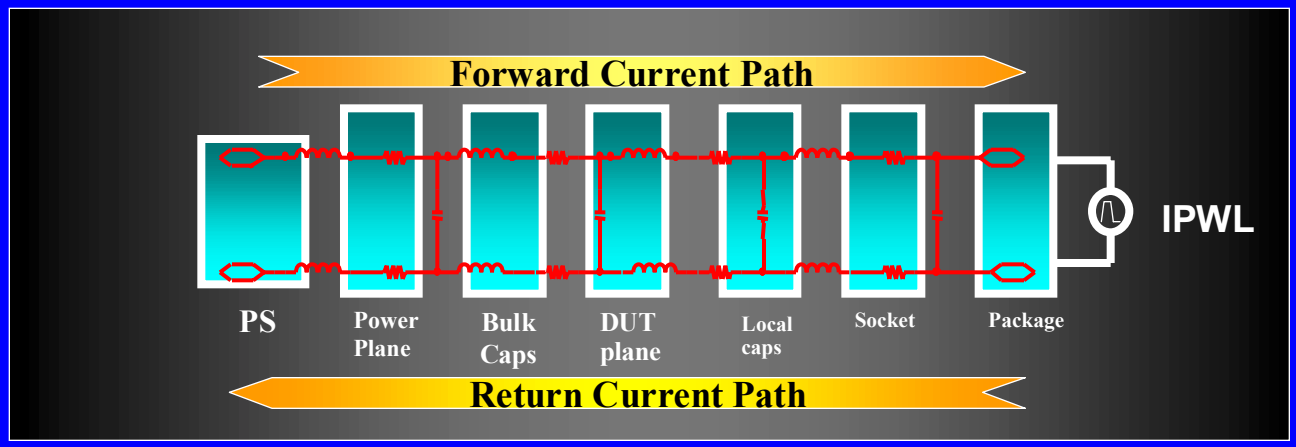
POWER ELECTRICAL PATH MODELING

3D Field Solver

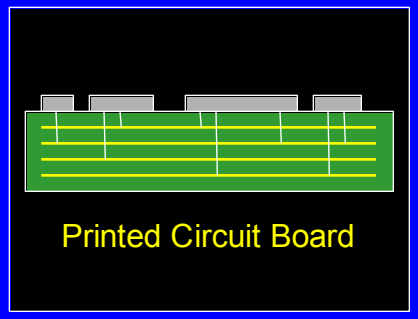


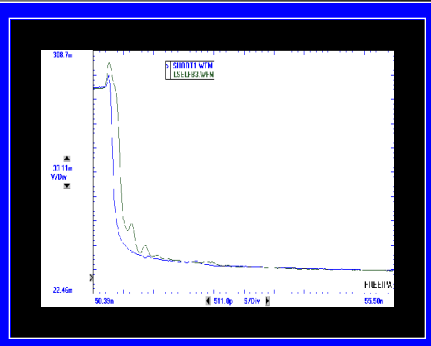


2D/3D Q-Static Solver



3D Modeling

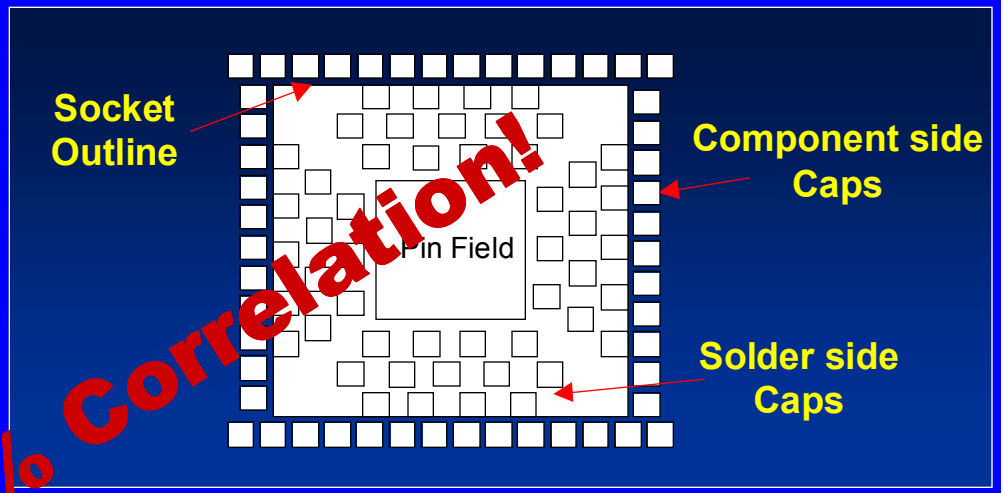




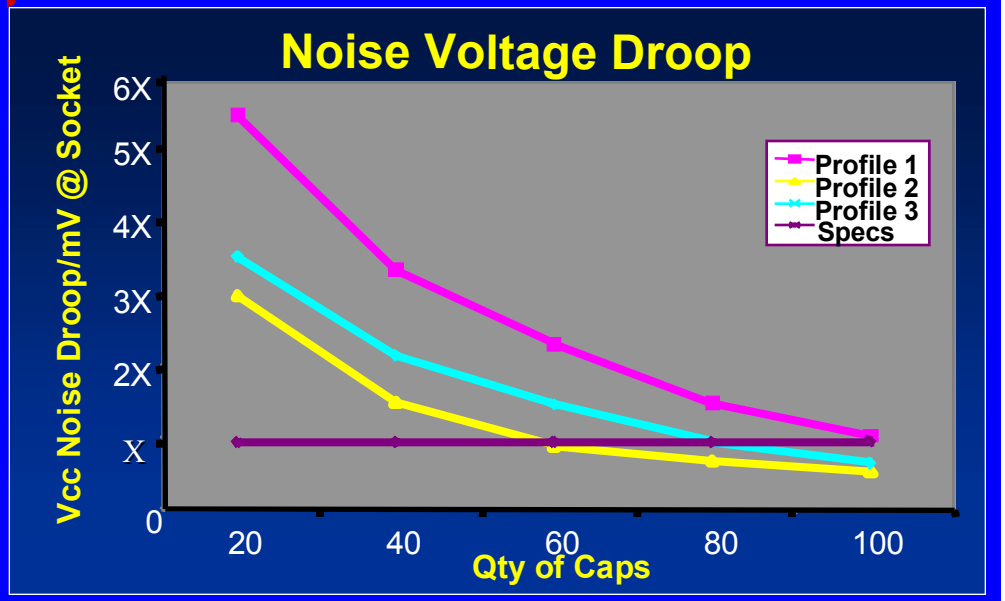
Time Domain Reflectometry

POWER DECOUPLING CONSIDERATION

- **Capacitors**
  - Main noise suppressor
  - Comp/Solder layer
  - Optimize real-estate
  - Plane capacitance
- **Noise Sensitivity Study**
  - Qty Caps vs. Noise
  - Qty Caps vs. Cost
- **PS Sense-line Feedback**
  - Monitor voltage compensation

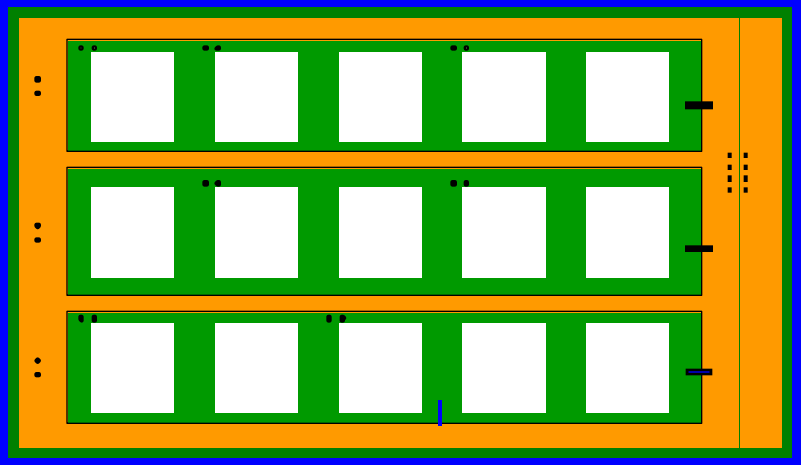


Achieved 75-88% Correlation!



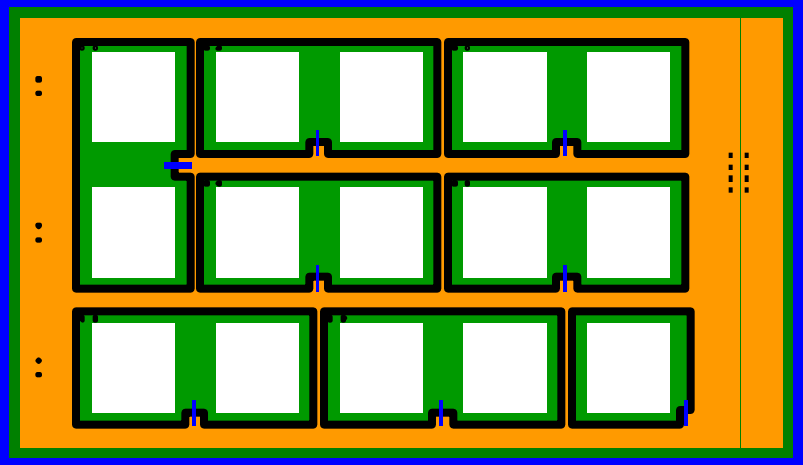
Simulation Results

BIB - ROW



Minus

BIB - ISLAND



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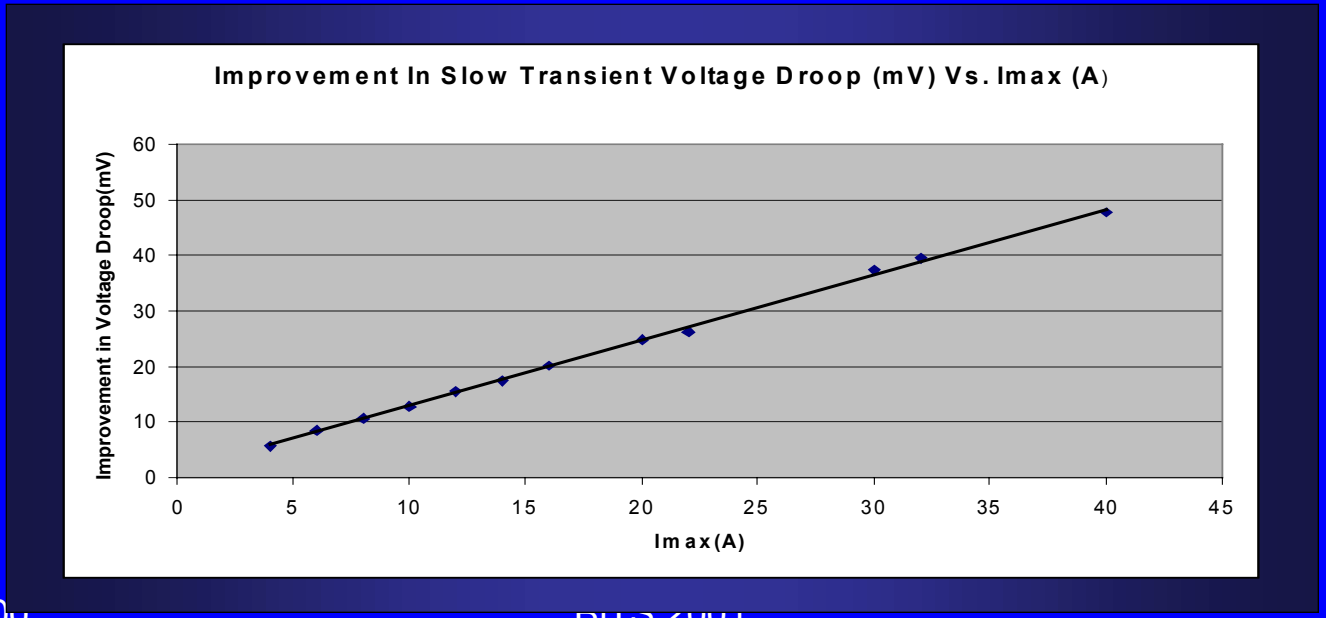


Conclusion

- As the VCC and ICC trend keep going to their extreme, BIB island power plane design provides a viable solution.
- Island power plane design has an improvement of 12% over the conventional power plane design.
- Island Power Plane Design is capable for future extreme high power device without venturing into new BIB design.
- Currently, this key learning has been proliferated to the future BIB design

THANK YOU

Q & A

Acknowledgement

The Authors would like to appreciate the contribution from Intel Test Hardware Development Group in this BiTS paper.

Cost Effective Burn In Board Design

IBM Microelectronics Division

Ralph J. Bernardini

Frank W. Jurasek

James M. Brown

In Today's Competitive World … The Market Demands

- **Quality**
- **Low cost**
- **On time deliveries**
- **Re- use .. burn in boards**
- **Efficiency**

Goal Of Design

- Have one burn in board to support all product types and test plans
- Program the configurations for maximum efficiencies
- Design modular configurations

This Presentation Addresses Reducing The Cost Of Ownership.. Through Burn In Board Design

- **Compressed data routing**
- **Universal board configuration**
- **Socket inter-poser solution**

Compressed Data Routing Design

(Data Interleave)

Data Routing (Conventional)

- Conventional burn in board designs route the same tool I/O across the row dimension of the burn in board
- This method may not route the burn in tool I/O to the burn in board in the most efficient manner

Conventional Routing

Data

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

Data Selects

R	1	2	3	4	5	6	7	8	9	A	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	1	2	3	4	5	6	7	8	9	10	T
R	11	12	13	14	15	16	17	18	19	20	T
R	11	12	13	14	15	16	17	18	19	20	T
R	11	12	13	14	15	16	17	18	19	20	T
R	11	12	13	14	15	16	17	18	19	20	T

Data Routing (Compressed)

- Compressed data routing molds the burn in tools I/O into an efficient burn in board I/O routing design
- This method allows the burn in tool I/O to be routed in an efficient manner
- Reduces the number of data selects required and improves test time

Interleave Routing

Data

R	A	A	A	A	A	A	A	A	A	A	T
	A	B	B	A	A	B	B	A	A	B	
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
	C	D	D	C	C	D	D	C	C	D	
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
	E	F	F	E	E	F	F	E	E	F	
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
	G	H	H	G	G	H	H	G	G	H	
R	H	H	H	H	H	H	H	H	H	H	T

Data Selects

R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T

Universal Burn In Board Configuration Design

(System Bus Utilization)

Conventional Approach

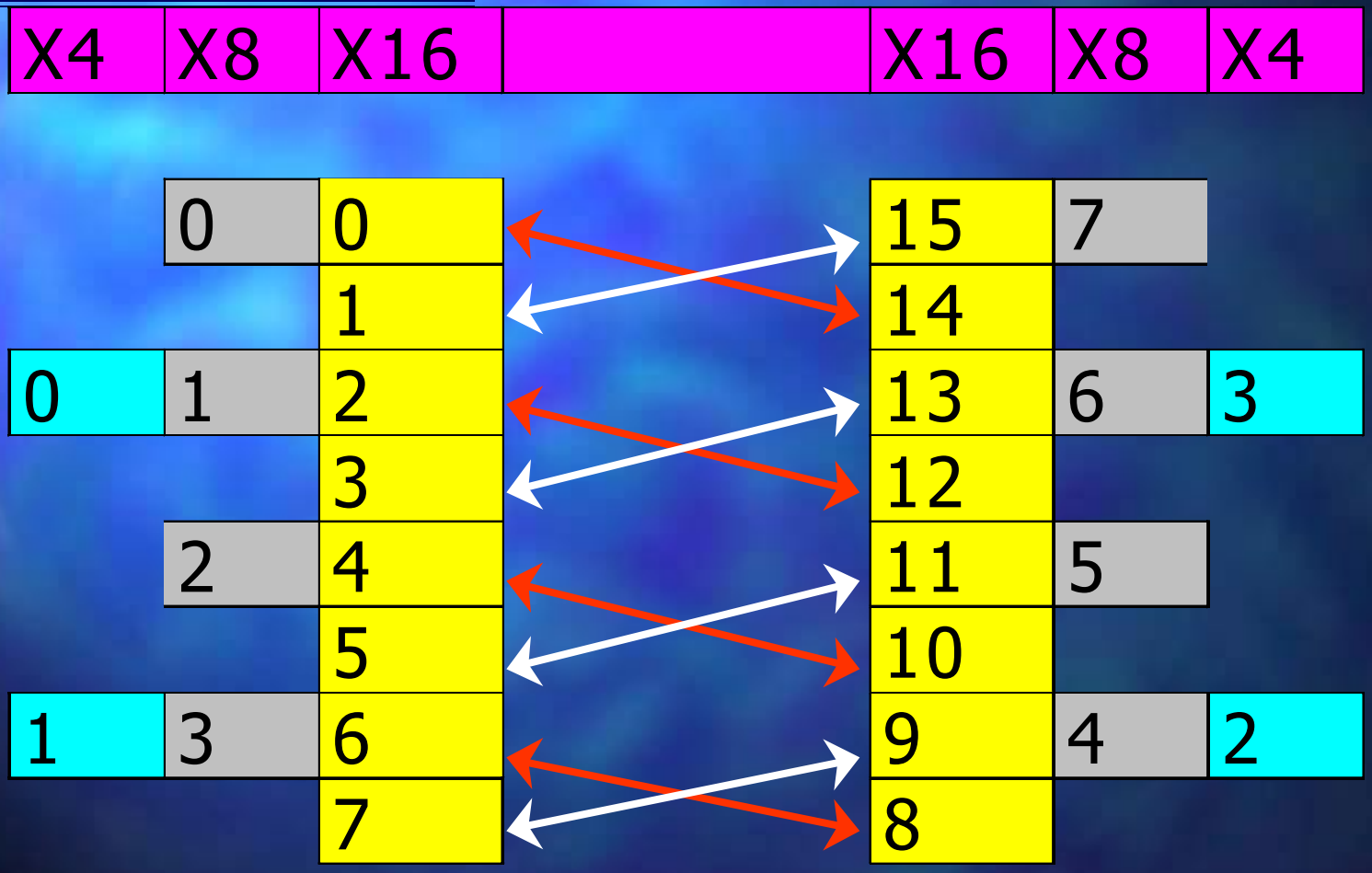
- Design burn in board as per product configuration (x32-x16-x8--etc)
- Design burn in board to route the maximum product I/O configuration to each device then mask out un-used product I/Os for lower configurations

Universal Approach

- For wide I/O product
  - I/O's are tied together on the Burn in Board
  - Use data selects to isolate product I/O's on the BIB
- For narrow I/O product
  - Route product I/O to use all tool I/O
  - Use dual data selects for scan bus efficiency

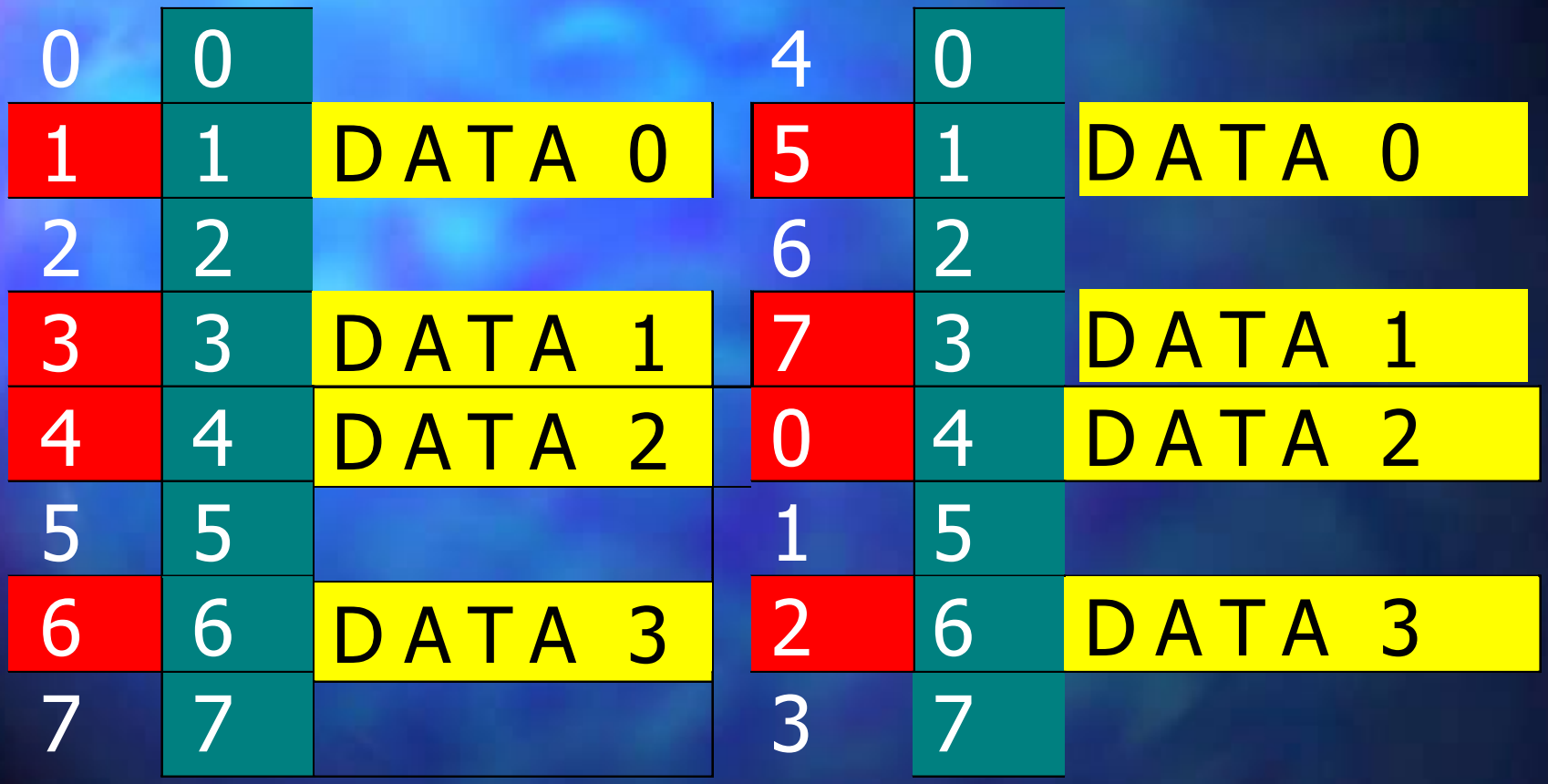
Three Configurations

8 tool I/O's Wired To Each DUT



Shorted I/O's .. 0-14, 1-15, 2-12, 3-13, Etc

X4 I/O Configuration Routing
Dual use of Tool I/O



Red Tool I/O

Yellow DUT I/O

X4 - Dual Selects Used For Each Scan

Data

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	A	A	B	
R	B	b	B	b	B	b	B	B	B	B	T
R	C	c	C	c	C	c	C	c	C	C	T
	C	D	d	c	C	D	d	C	C	D	
R	D	d	D	d	D	d	D	D	D	D	T
R	E	e	E	e	E	e	E	e	E	E	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	F	T
R	G	g	G	g	G	g	G	g	G	G	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	H	T

Data Selects

R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T

Data Select 1 and 2 First Scan

Data Select 3 and 4 Second Scan

X8 I/O Configuration

0	0	DATA 0	4	0	DATA 0
1	1	DATA 1	5	1	DATA 1
2	2	DATA 2	6	2	DATA 2
3	3	DATA 3	7	3	DATA 3
4	4	DATA 4	0	4	DATA 4
5	5	DATA 5	1	5	DATA 5
6	6	DATA 6	2	6	DATA 6
7	7	DATA 7	3	7	DATA 7

X8 Configuration

Data

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	A	A	B	
R	B	b	B	b	B	b	B	B	B	B	T
R	C	c	C	c	C	c	C	c	C	C	T
	C	D	d	c	C	D	d	C	C	D	
R	D	d	D	d	D	d	D	D	D	D	T
R	E	e	E	e	E	e	E	e	E	E	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	F	T
R	G	g	G	g	G	g	G	g	G	G	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	H	T

Data Selects

R	1	2	5	6	7	8	11	12	13	14	T
R	3	3			9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3			9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3			9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3			9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T

1 First Scan 2 Second Scan

3 Third Scan ...Etc

X16 I/O Configuration

Low I/O Scan

NOTE	0	0	DATA 0	0	14	DATA 14
I/O'S	1	1	DATA 1	1	15	DATA 15
LOW	2	2	DATA 2	2	12	DATA 12
HIGH	3	3	DATA 3	3	13	DATA 13
TIED	4	4	DATA 4	4	10	DATA 10
	5	5	DATA 5	5	11	DATA 11
	6	6	DATA 6	6	8	DATA 8
	7	7	DATA 7	7	9	DATA 9
SCAN	LO	DS	8 I/O			
SCAN				HI	DS	8 I/O

X16 I/O Configuration

Hi I/O Scan

NOTE	0	0	DATA 0	0	14	DATA 14
I/O'S	1	1	DATA 1	1	15	DATA 15
LOW	2	2	DATA 2	2	12	DATA 12
HIGH	3	3	DATA 3	3	13	DATA 13
TIED	4	4	DATA 4	4	10	DATA 10
	5	5	DATA 5	5	11	DATA 11
	6	6	DATA 6	6	8	DATA 8
	7	7	DATA 7	7	9	DATA 9
SCAN	LO	DS	8 I/O			
SCAN				HI	DS	8 I/O

X16 CONFIGURATION LO SCAN

Data

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	A	A	B	
R	B	b	B	b	B	b	B	B	B	B	T
R	C	c	C	c	C	c	C	c	C	C	T
	C	D	d	c	C	D	d	C	C	D	
R	D	d	D	d	D	d	D	D	D	D	T
R	E	e	E	e	E	e	E	e	E	E	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	F	T
R	G	g	G	g	G	g	G	g	G	G	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	H	T

Data Selects

R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T
R	1	2	5	6	7	8	11	12	13	14	T
R	3	3	4	4	9	9	10	10	15	15	T
R	1	2	5	6	7	8	11	12	13	14	T

SELECT 8 I/O ... WITH LOW ENABLES

X16 CONFIGURATION HI SCAN

Data

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	A	A	B	
R	B	b	B	b	B	b	B	B	B	B	T
R	C	c	C	c	C	c	C	c	C	C	T
	C	D	d	c	C	D	d	C	C	D	
R	D	d	D	d	D	d	D	D	D	D	T
R	E	e	E	e	E	e	E	e	E	E	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	F	T
R	G	g	G	g	G	g	G	g	G	G	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	H	T

Data Selects

R	16	17	20	21	22	23	26	27	28	29	T
R	18	18	19	19	24	24	25	25	30	30	T
R	16	17	20	21	22	23	26	27	28	29	T
R	16	17	20	21	22	23	26	27	28	29	T
R	18	18	19	19	24	24	25	25	30	30	T
R	16	17	20	21	22	23	26	27	28	29	T
R	16	17	20	21	22	23	26	27	28	29	T
R	18	18	19	19	24	24	25	25	30	30	T
R	16	17	20	21	22	23	26	27	28	29	T
R	16	17	20	21	22	23	26	27	28	29	T
R	18	18	19	19	24	24	25	25	30	30	T
R	16	17	20	21	22	23	26	27	28	29	T

SELECTS 8 I/O WITH HIGH ENABLES

Inter-poser Solution Design

(Sub Boards)

Standard Bib Designs

- **Standard burn in board designs solder sockets directly to the burn in board**
- **This method routes signals and resource to each socket**
- **The socket footprint used on this burn in board is fixed**

Inter-poser Bib Designs

- This method solders sockets to a inter-poser board that is directly plugged into the burn in board
- The main board routes the resources needed to the plug-able pins of each inter-poser (per test requirements)
- The inter-poser routes the resources directly to the socket pins

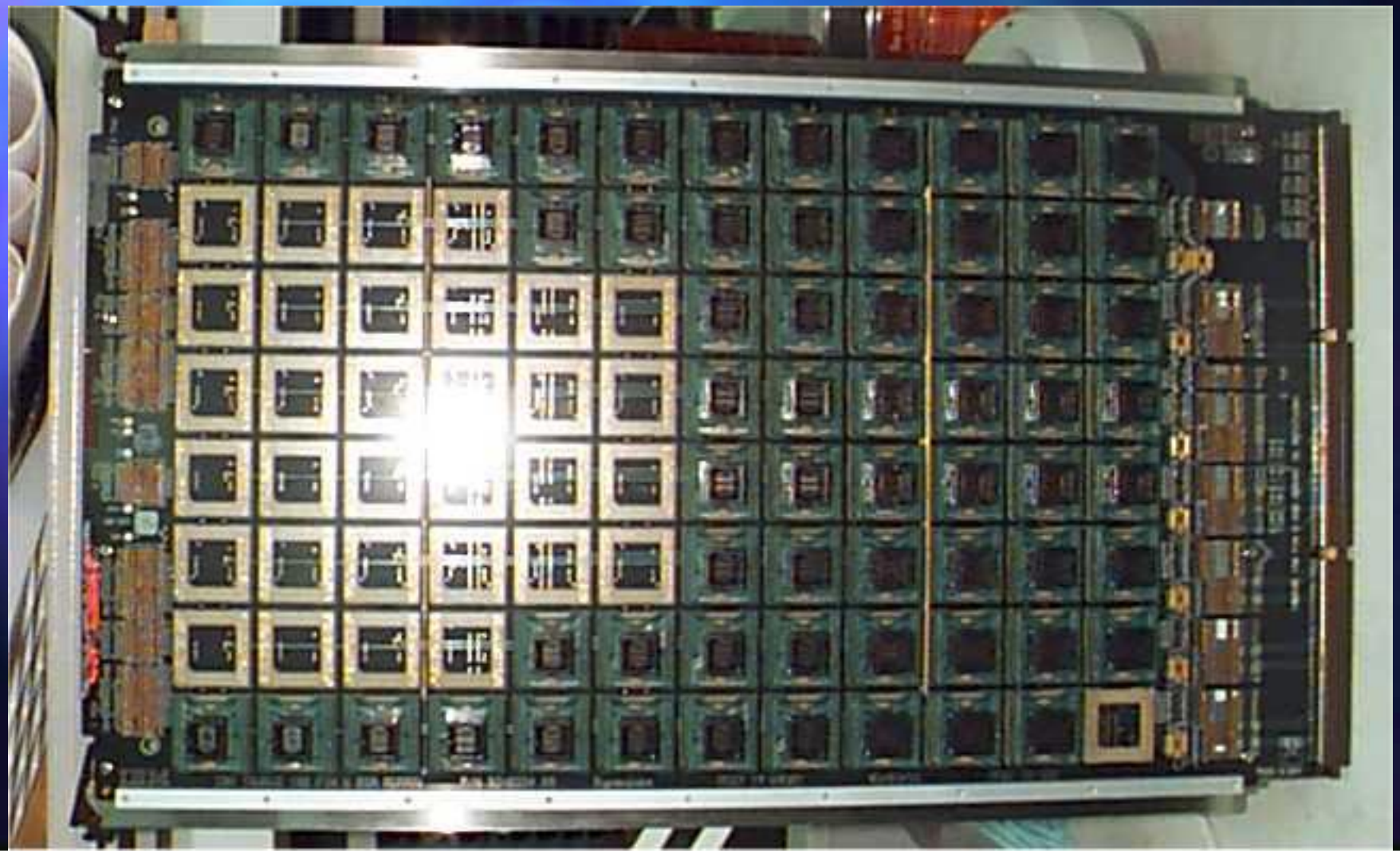
Goal Of Design

- Burn in board for all product regardless of socket or pin out differences
- High performance plug-able sub boards that configure to product type
- Resolve pitch and trace routing problems

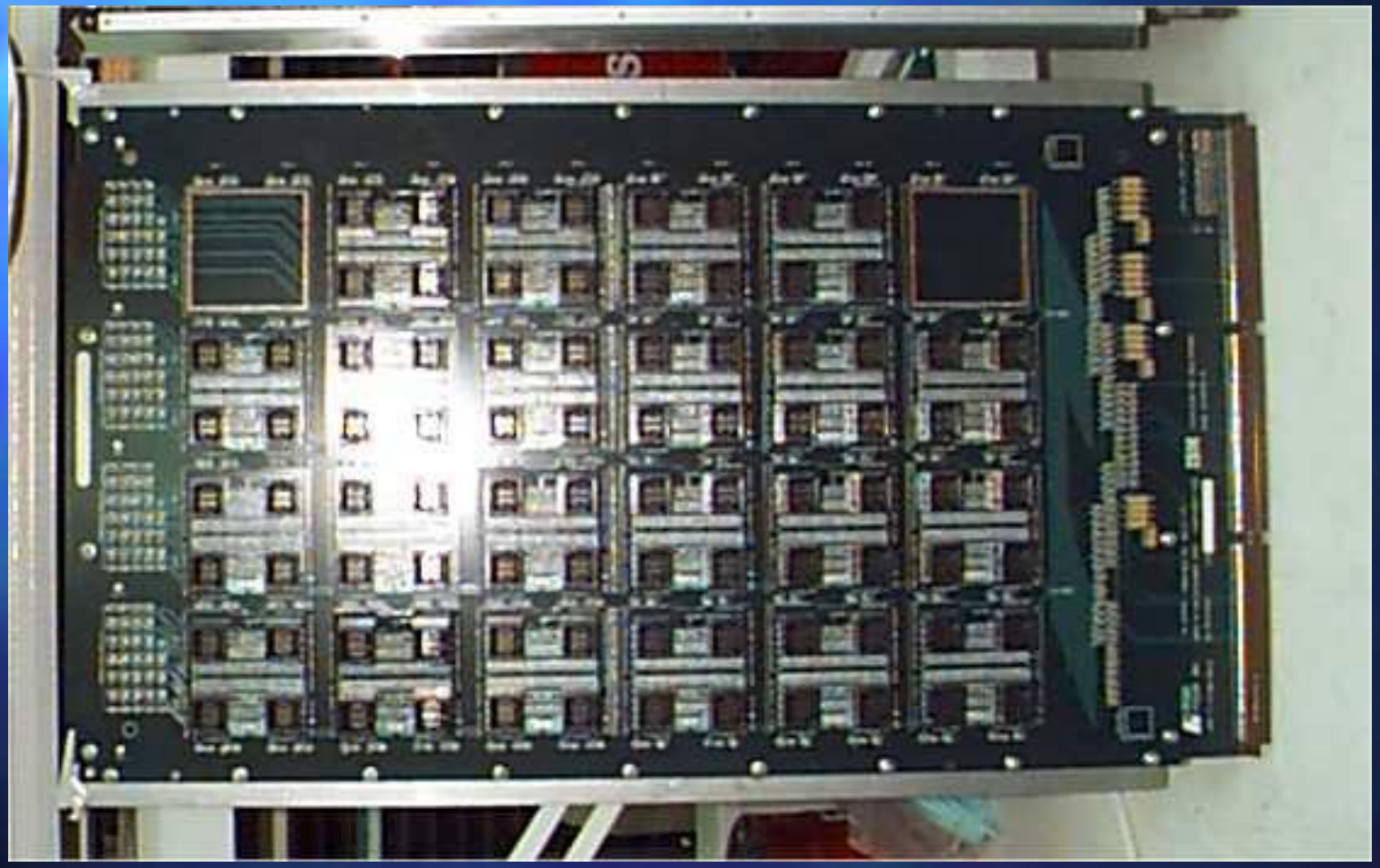
Goal Of Design

- Resolve / reduce temperature and power problems
- Protects the main burn in board
- Decrease board repair time

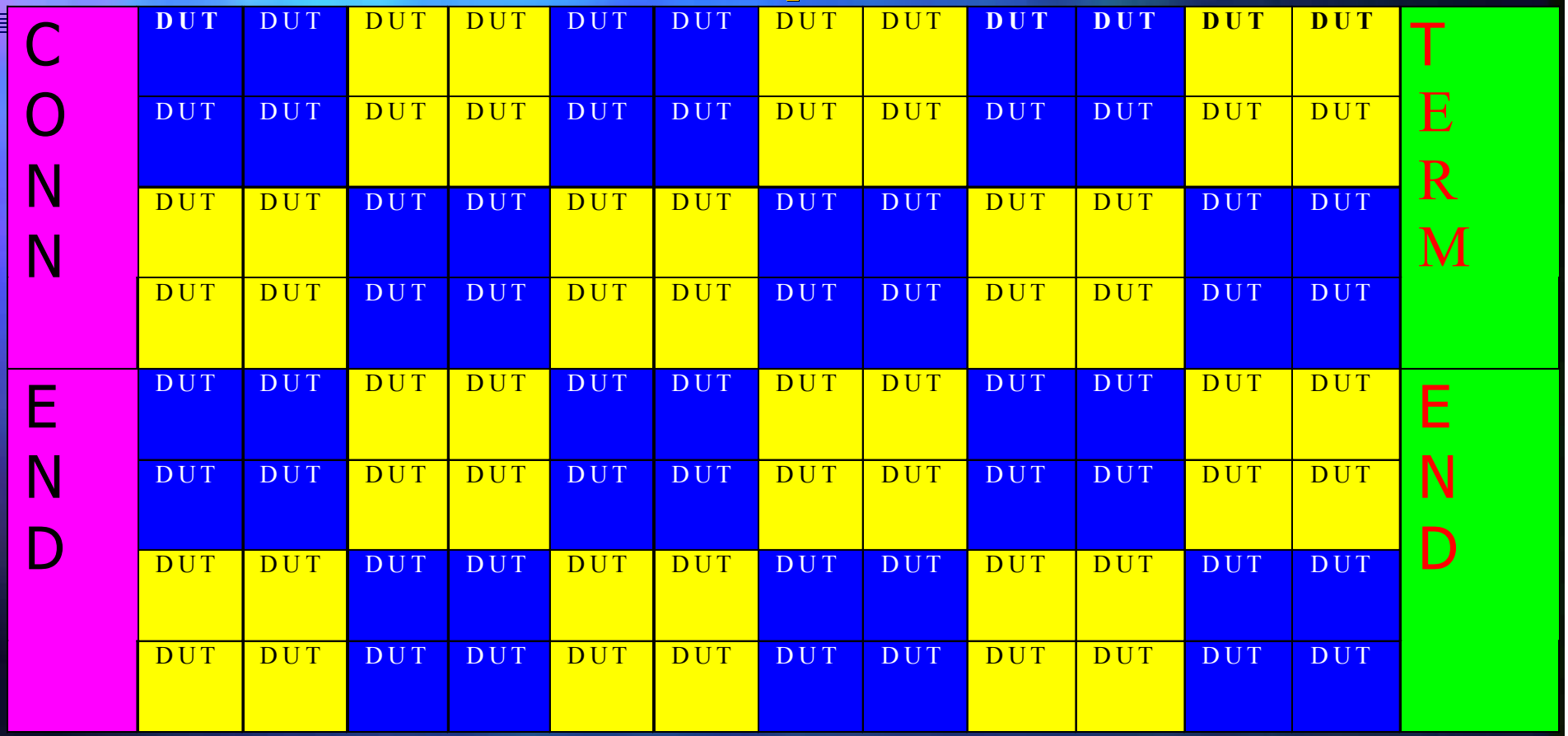
One Socket per Inter-Poser



Four Sockets per Inter-poser

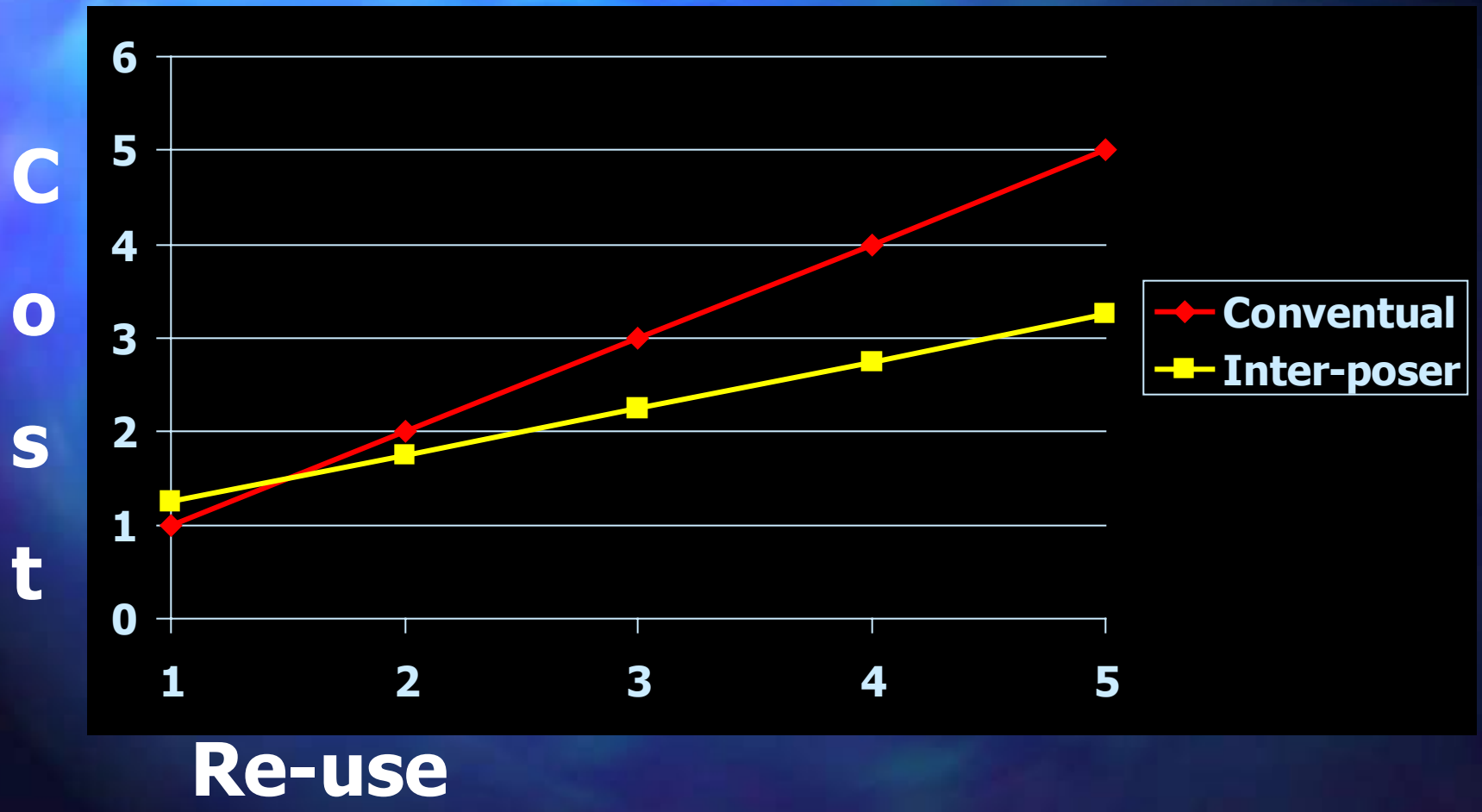


Sub Boards Have 4 Sockets



96 Duts Per Board

Cost to Re-use



Summary

- Improved BIB signal quality
- Improved test efficiency
- Better stress / Burn in duty cycle
- Less components and easier repair
- Reduced capital tooling

Summary

- **Inter-poser**
  - **One BIB with inter-poser concept supports**
    - **multiple form factors**
    - **different pin outs**
    - **Power control**
    - **Thermal control damage**
    - **Reduces socket pin pitch constraints**
- **Re-use of bib …. many / all product type**

I/O SCAN

01

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

01

R	A	a	A	a	A	a	A	A	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	E	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

LEFT SIDE CONVENTIONAL

02

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

02

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	C	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

RIGHT SIDE INTERLEAVE

03

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

03

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	C	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

LESS COMPONENTS

04

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

04

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

R = INPUT FILTER CKT

05

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

05

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

T= TERMINATOR CKT

06 06

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

STABILITY

07

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

07

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

LOWER CROSSTALK

08 08

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

LESS I/O LOAD

09

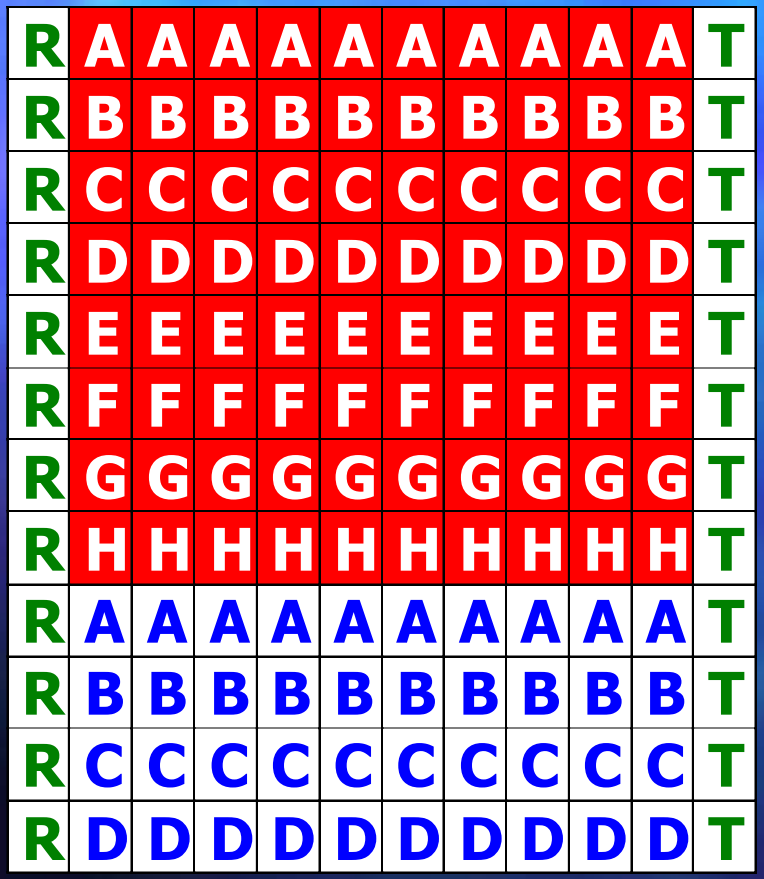
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

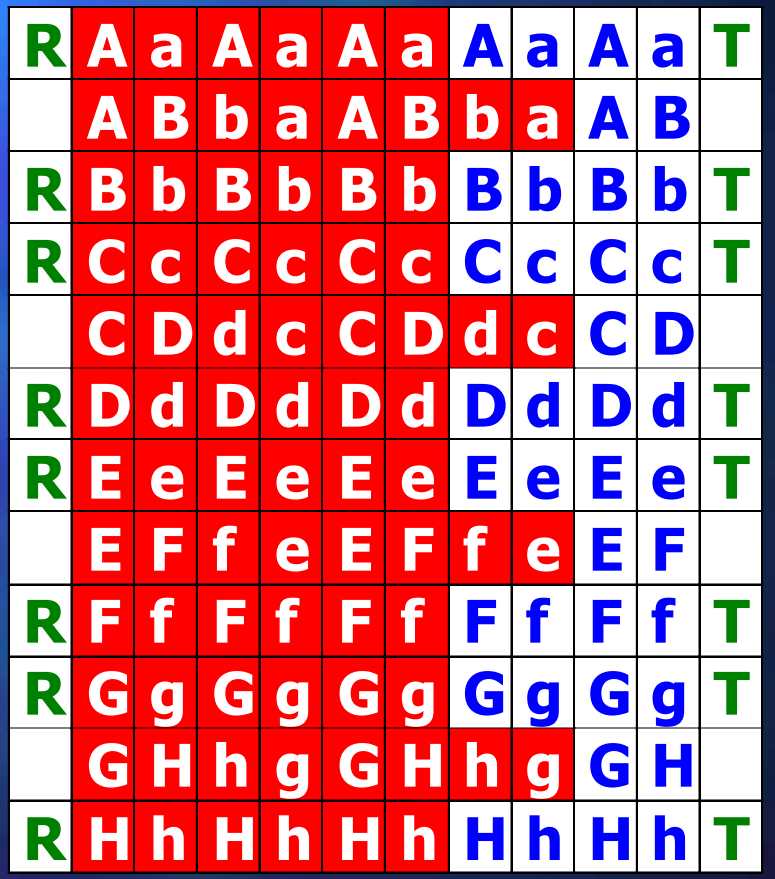
09

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	E	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

BETTER I/O DRIVE

10 10





LOWER SCANS

11

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

11

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

LOWER TEST TIMES

12

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

12

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

BETTER STRESS

13 13

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

IMPROVED DUTY CYCLE

14

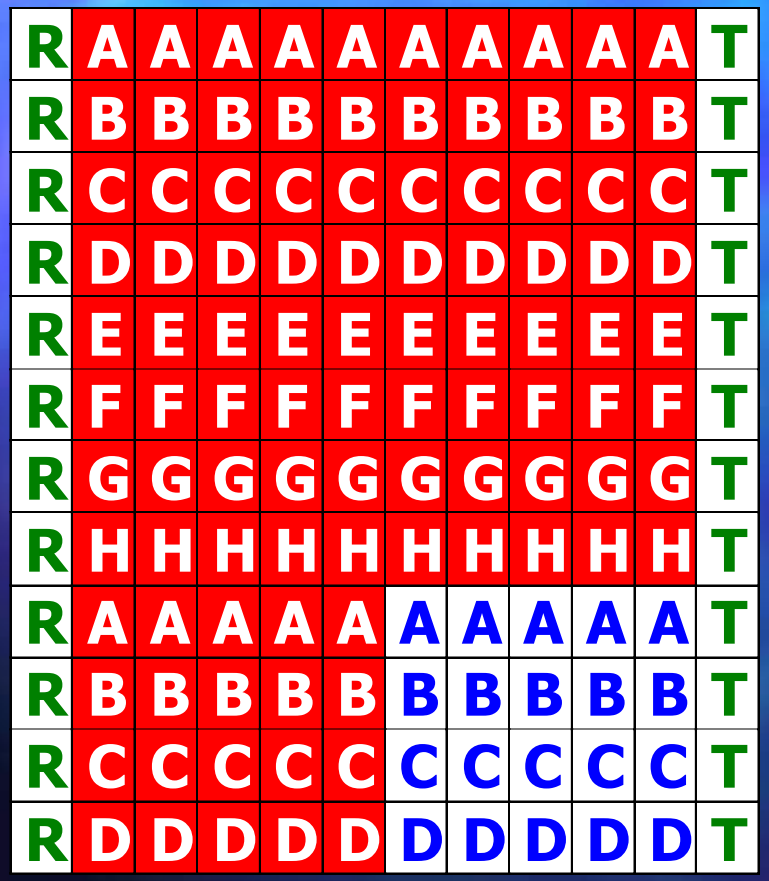
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

14

R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

3/4 DONE

15



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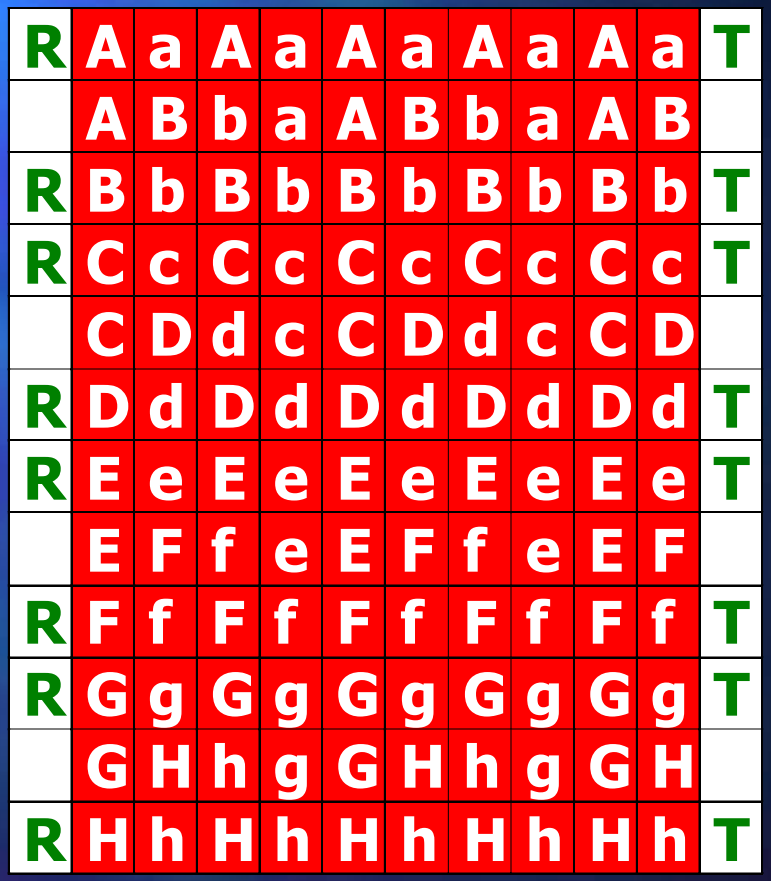
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

DONE

15



R	A	a	A	a	A	a	A	a	A	a	T
	A	B	b	a	A	B	b	a	A	B	
R	B	b	B	b	B	b	B	b	B	b	T
R	C	c	C	c	C	c	C	c	C	c	T
	C	D	d	c	C	D	d	c	C	D	
R	D	d	D	d	D	d	D	d	D	d	T
R	E	e	E	e	E	e	E	e	E	e	T
	E	F	f	e	E	F	f	e	E	F	
R	F	f	F	f	F	f	F	f	F	f	T
R	G	g	G	g	G	g	G	g	G	g	T
	G	H	h	g	G	H	h	g	G	H	
R	H	h	H	h	H	h	H	h	H	h	T

EXTRA CYCLES

16 + 01

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	A	A	A	A	A	A	A	A	A	T
	A	B	B	A	A	B	B	A	A	B	
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
	C	D	D	C	C	D	D	C	C	D	
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
	E	F	F	E	E	F	F	E	E	F	
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
	G	H	H	G	G	H	H	G	G	H	
R	H	H	H	H	H	H	H	H	H	H	T

FASTER READ CYCLES

17 + 02

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	A	A	A	A	A	A	A	A	A	T
	A	B	B	A	A	B	B	A	A	B	
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
	C	D	D	C	C	D	D	C	C	D	
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
	E	F	F	E	E	F	F	E	E	F	
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
	G	H	H	G	G	H	H	G	G	H	
R	H	H	H	H	H	H	H	H	H	H	T

BETTER TRACE SPEEDS

18

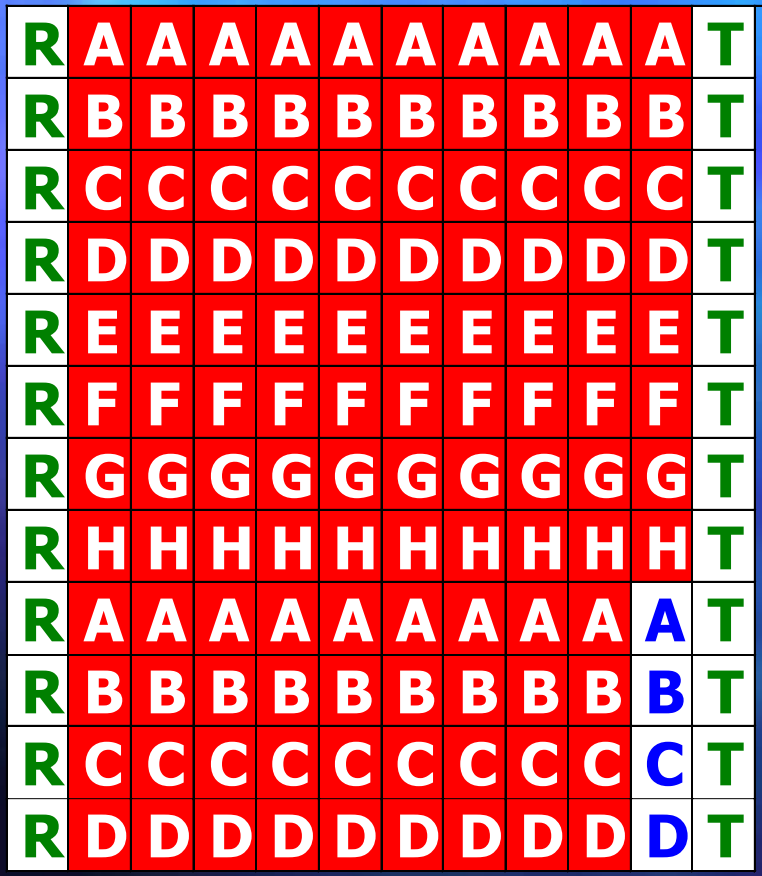
+ 03

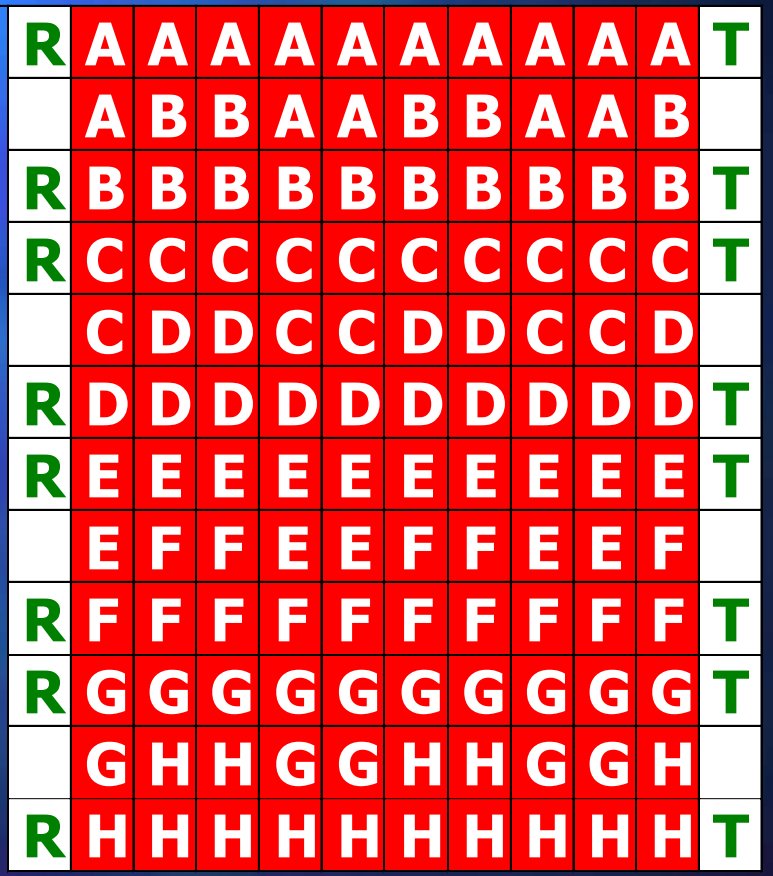
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	A	A	A	A	A	A	A	A	A	T
	A	B	B	A	A	B	B	A	A	B	
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
	C	D	D	C	C	D	D	C	C	D	
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
	E	F	F	E	E	F	F	E	E	F	
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
	G	H	H	G	G	H	H	G	G	H	
R	H	H	H	H	H	H	H	H	H	H	T

LESS DRIVER POWER

19 + 04





FINALLY !!

20 + 05

R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
R	H	H	H	H	H	H	H	H	H	H	T
R	A	A	A	A	A	A	A	A	A	A	T
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
R	D	D	D	D	D	D	D	D	D	D	T

R	A	A	A	A	A	A	A	A	A	A	T
	A	B	B	A	A	B	B	A	A	B	
R	B	B	B	B	B	B	B	B	B	B	T
R	C	C	C	C	C	C	C	C	C	C	T
	C	D	D	C	C	D	D	C	C	D	
R	D	D	D	D	D	D	D	D	D	D	T
R	E	E	E	E	E	E	E	E	E	E	T
	E	F	F	E	E	F	F	E	E	F	
R	F	F	F	F	F	F	F	F	F	F	T
R	G	G	G	G	G	G	G	G	G	G	T
	G	H	H	G	G	H	H	G	G	H	
R	H	H	H	H	H	H	H	H	H	H	T

High-Speed & High-Power Burn-In Board Design

Authors:
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Cher-Shyong Low (cher.shyong.low@intel.com)

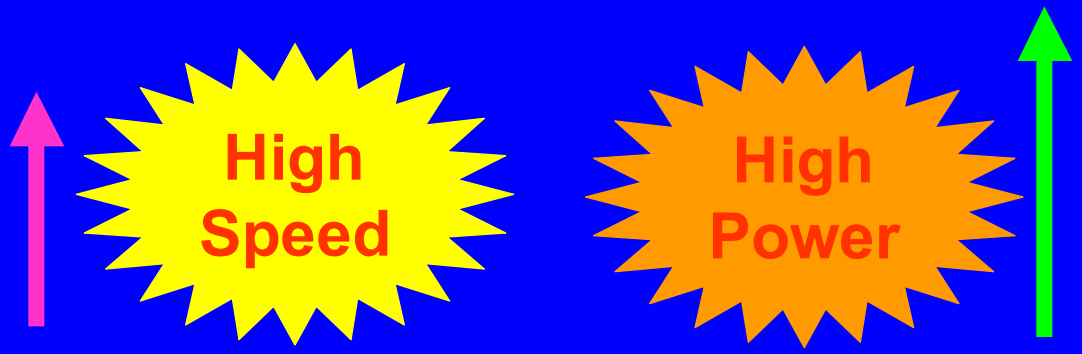
BURN-IN & TEST SOCKET WORKSHOP

Agenda

- Introduction
  - Next Generation BIB Design Challenges
- High-Speed Design (Signal Integrity)
  - Routing Topology & Termination Technique
  - Trace Impedance & Length Compensation
    Signal Integrity Simulations Setup
- High-Power Design
  - Delivery System
  - Decoupling Modeling
  - Vdroop Reduction
- Summary

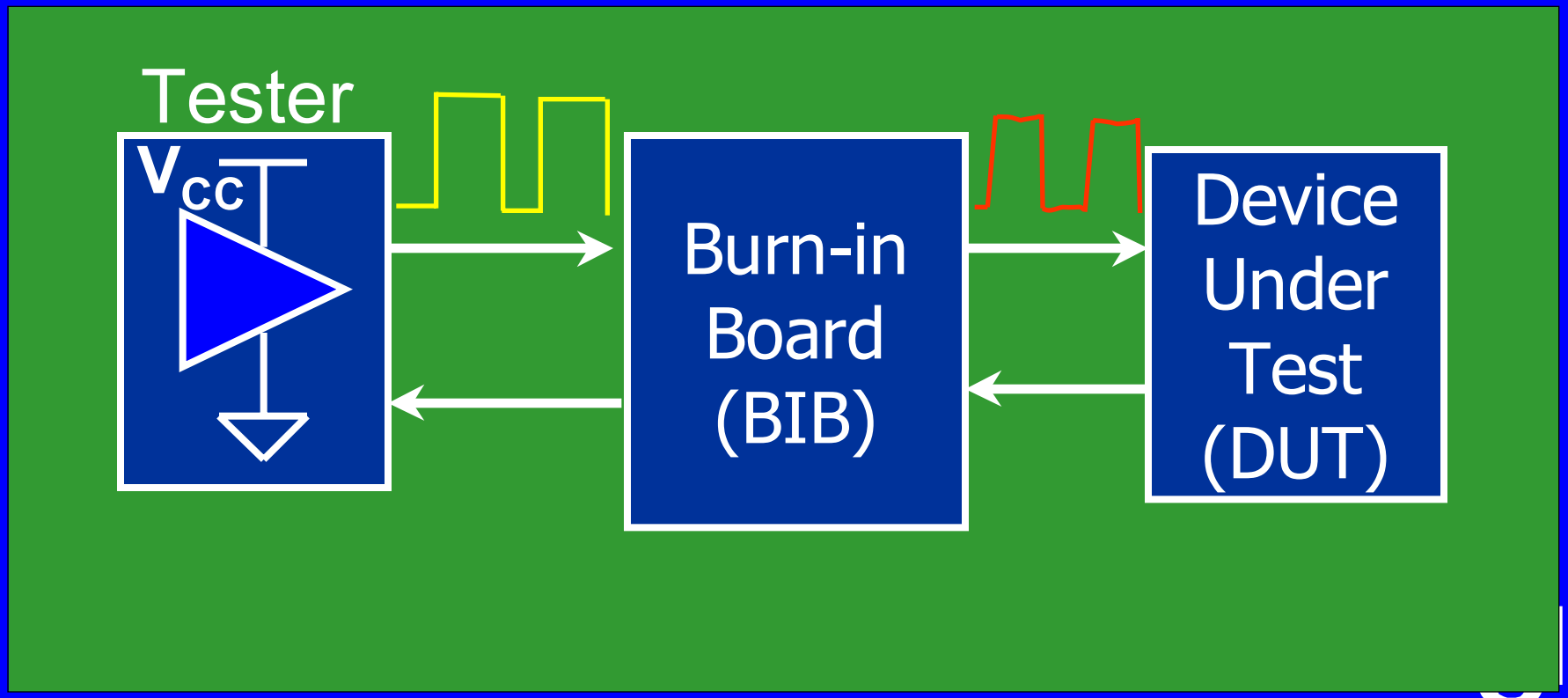
Next Generation Burn-in Board Challenges

- Advanced microprocessor blazes into the Gigahertz spectrum
  - –Burn-in board design has become more complex
- Two major key challenges

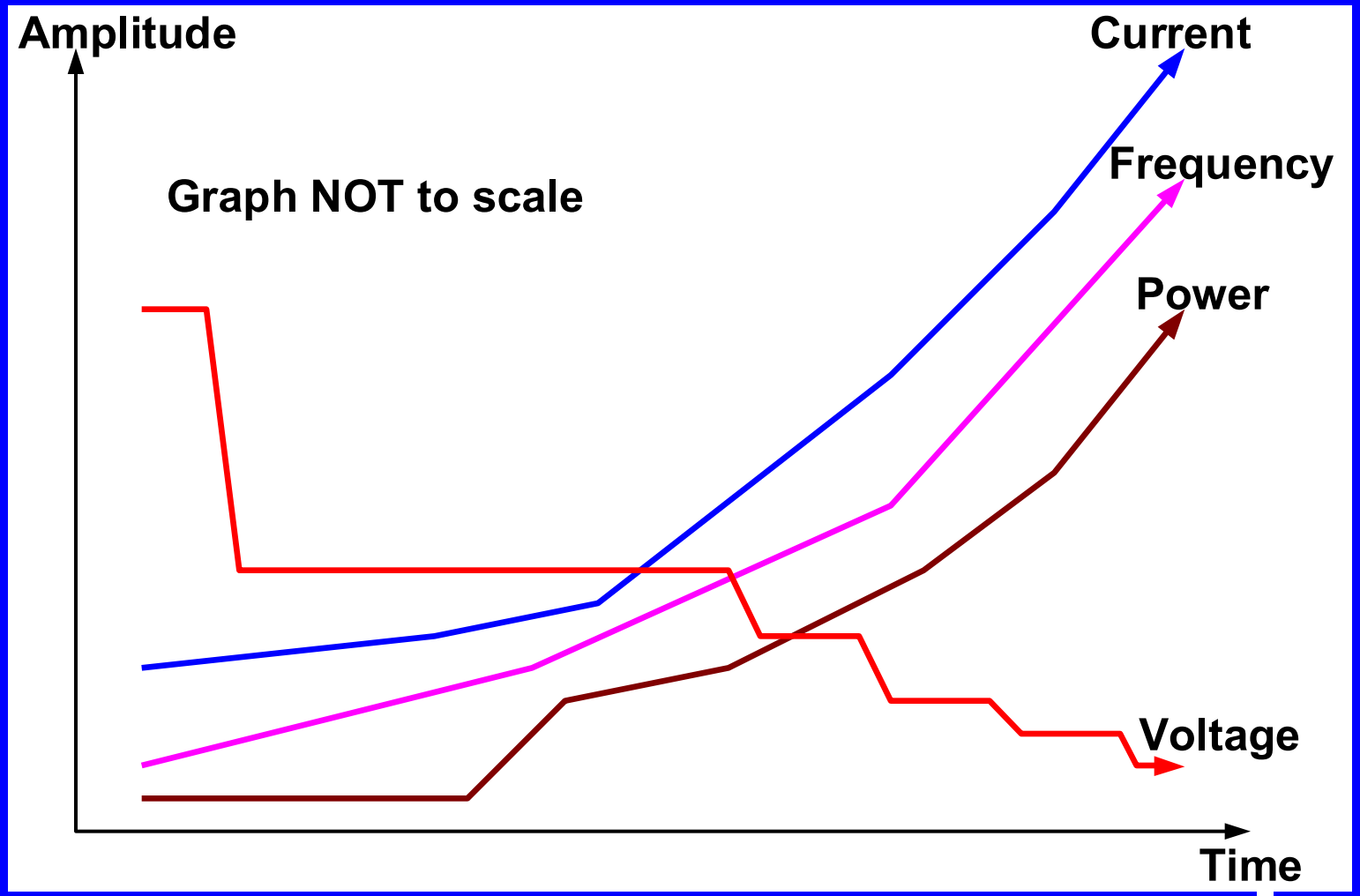


INTRODUCTION

- Two key attributes in Burn-in board design:
  - Deliver clean signal quality and stable voltage
  - Deliver continuous current



Environment Trend



What is High-Speed Design ?

- Problem faced in High Speed Design
  - When $T_{pd} > T_r/2$, signal trace will exhibit high speed effects.
  - Affecting signal integrity.
- In BI arena, typical signal trace length exhibits long T_{pd} ($> T_r/2$).
- Consideration
  - Routing topology
  - Termination technique
  - Trace impedance compensation
- Pre-Design Simulation helps to make selection

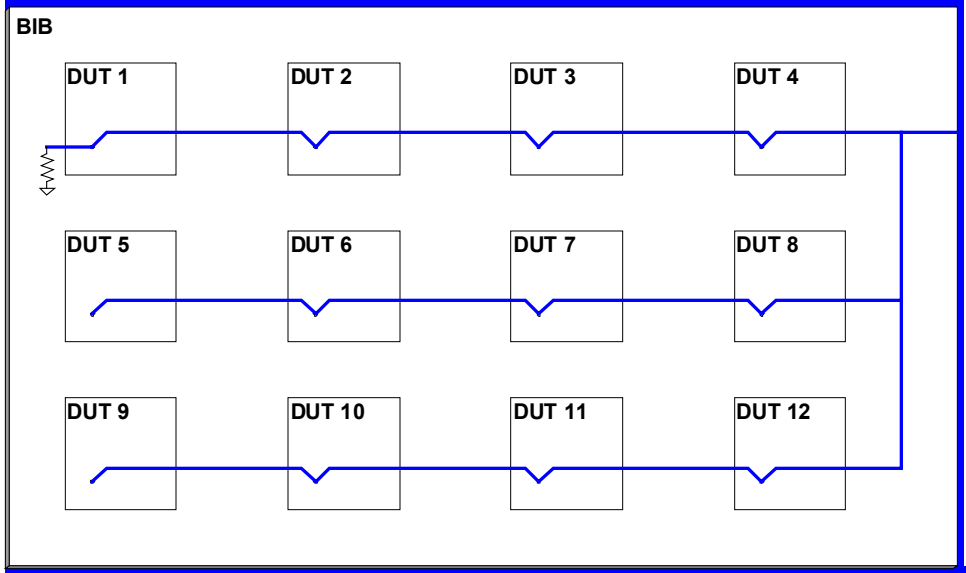
Routing Topology Concepts & Attributes

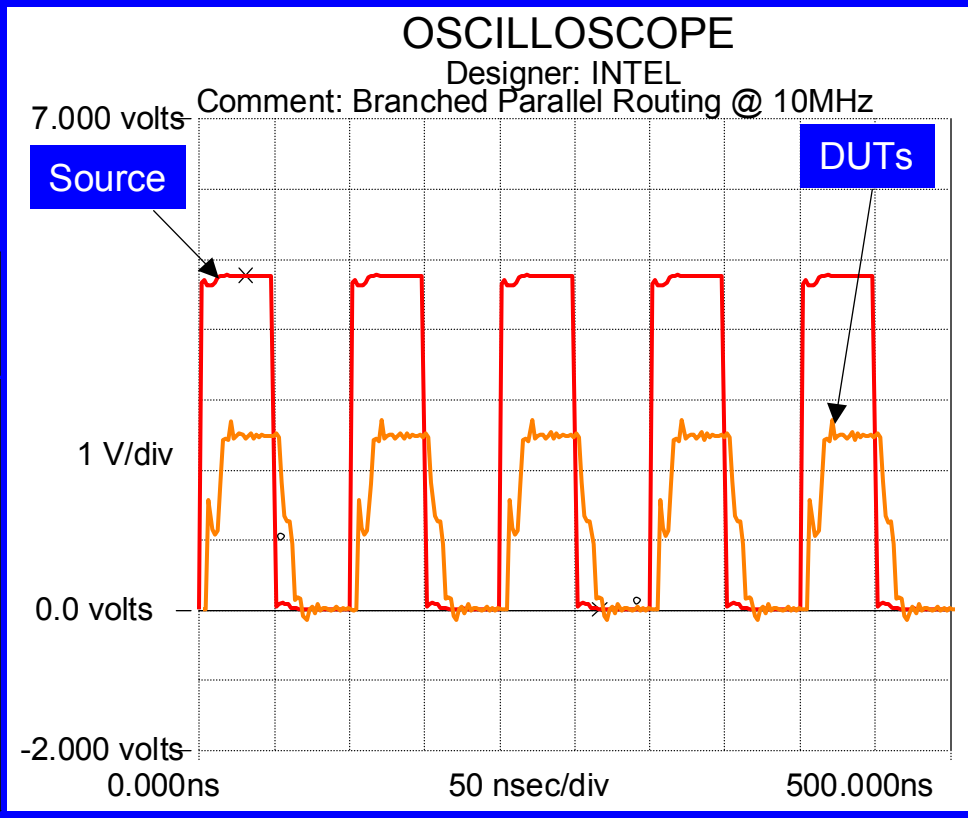
- General routing guidelines :
  - Branch Parallel routing
  - Continuous Serpentine Terminated routing
  - Individual Row Terminated routing
  - Dual-Drop Terminated routing
  - Point-to-Point Terminated routing

Branched Parallel Routing

Routing properties :

- Only a single channel per signal is needed
- Exhibit bad signal integrity at high speed

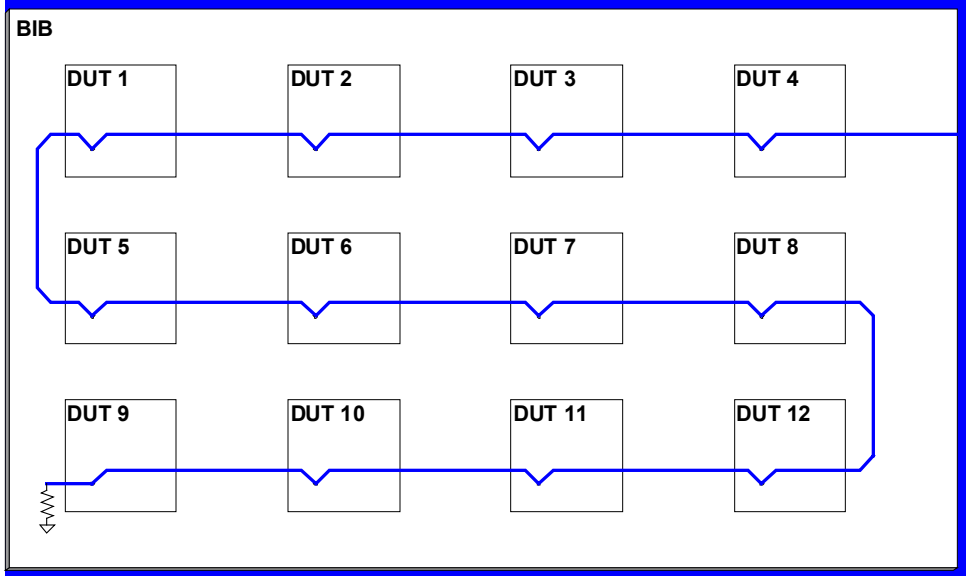


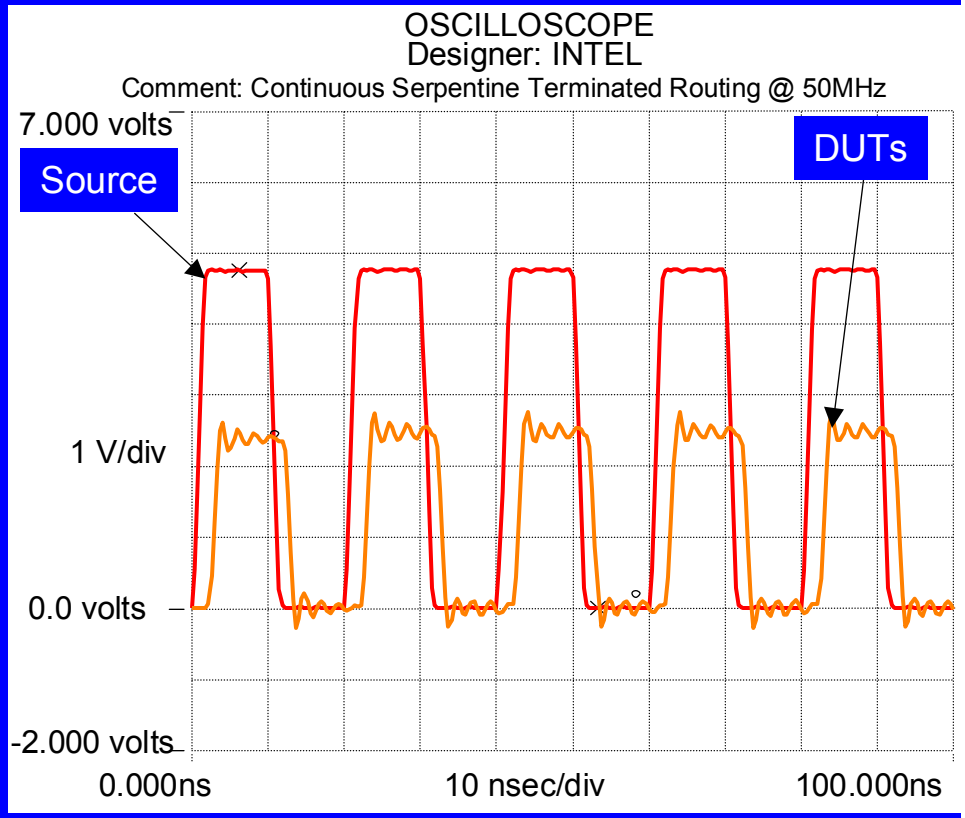


Continuous Serpentine Terminated

Routing properties :

- Only a single channel per signal is needed
- Has very long trace line (>6’), transmission line reflection is prominent.
- Exhibit bad signal integrity at high speed

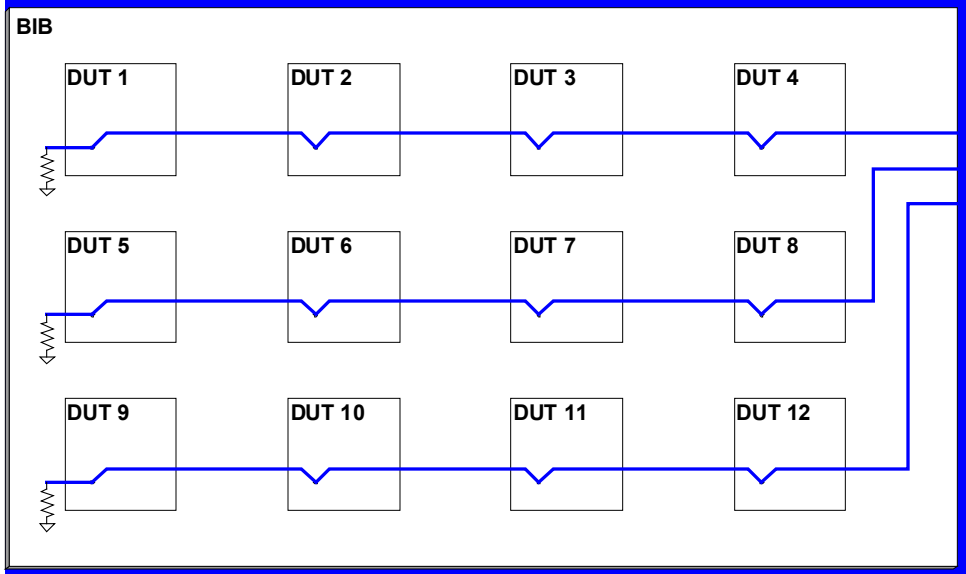


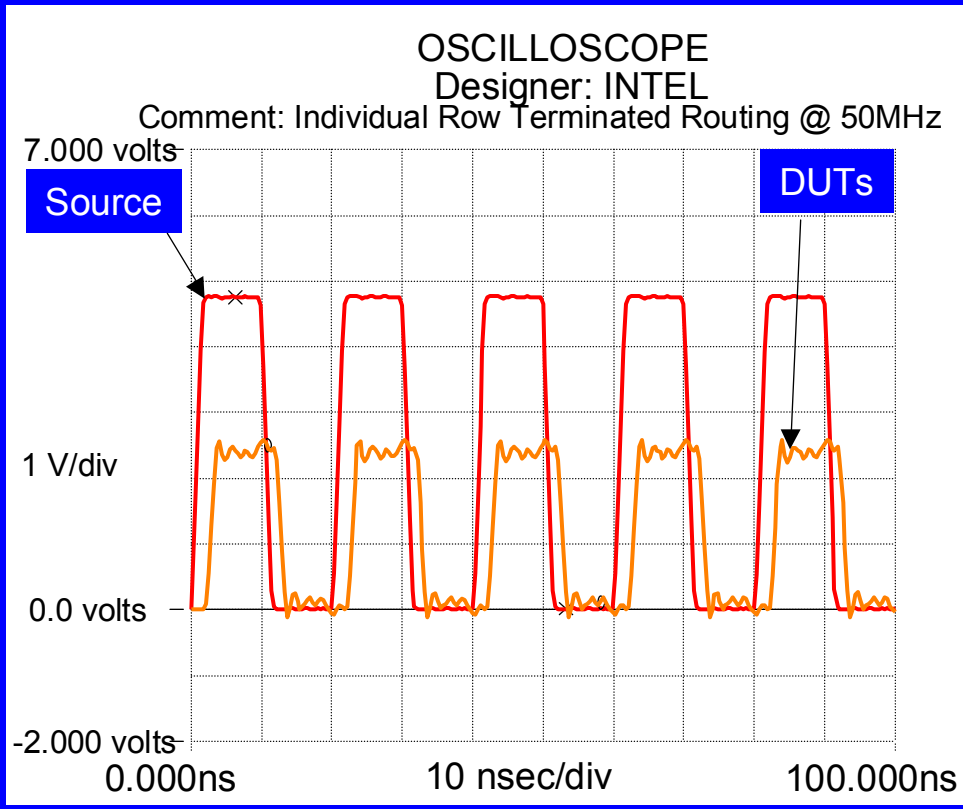


Individual Row Terminated Routing

Routing properties :

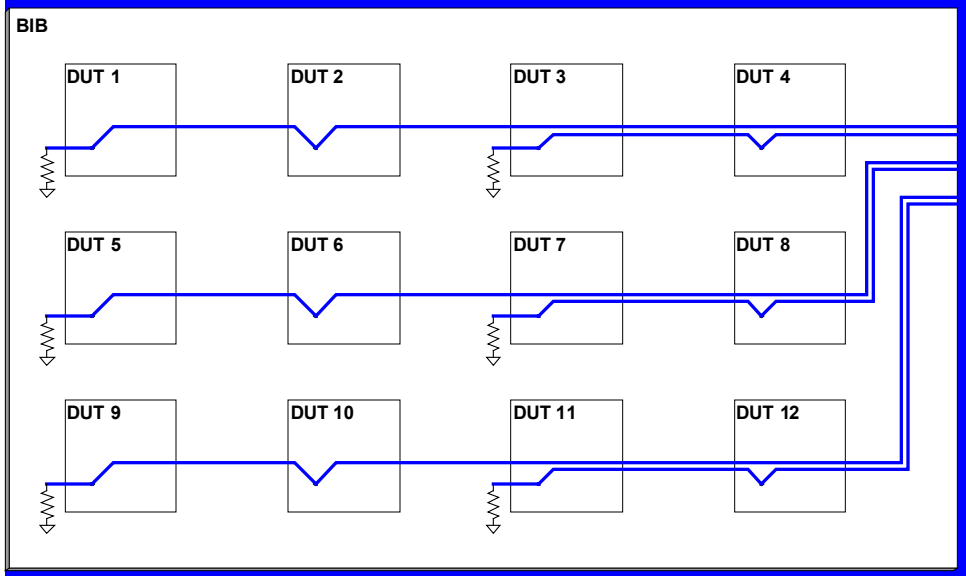
- Short trace length – OK for high speed board
- Minimized timing delay
- Requires X fold (where x=# of rows) of channels
  - # driver channel = # row of DUTs on BIB.

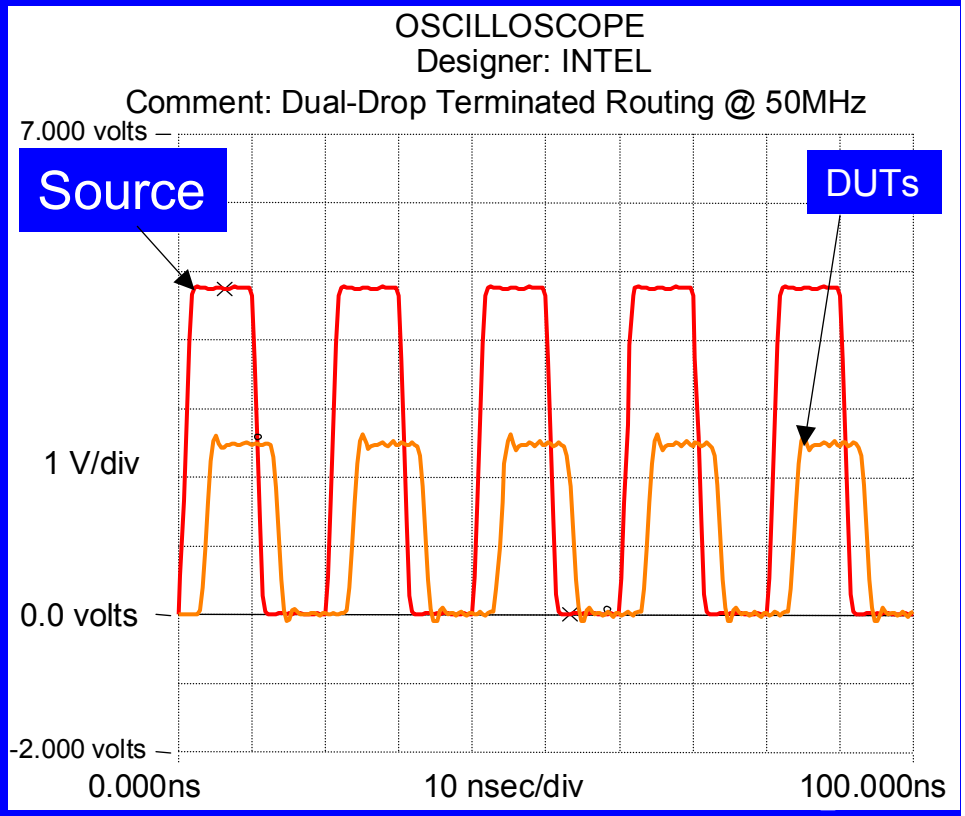




Dual-Drop Terminated Routing

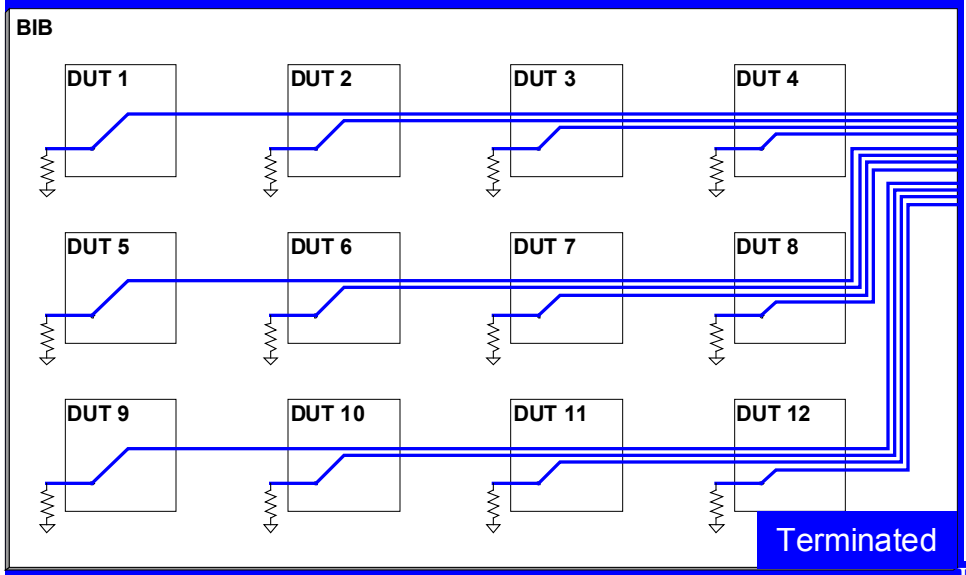
- Exhibit good signal integrity
- Recommended for high speed signal
- Uses more driver channel

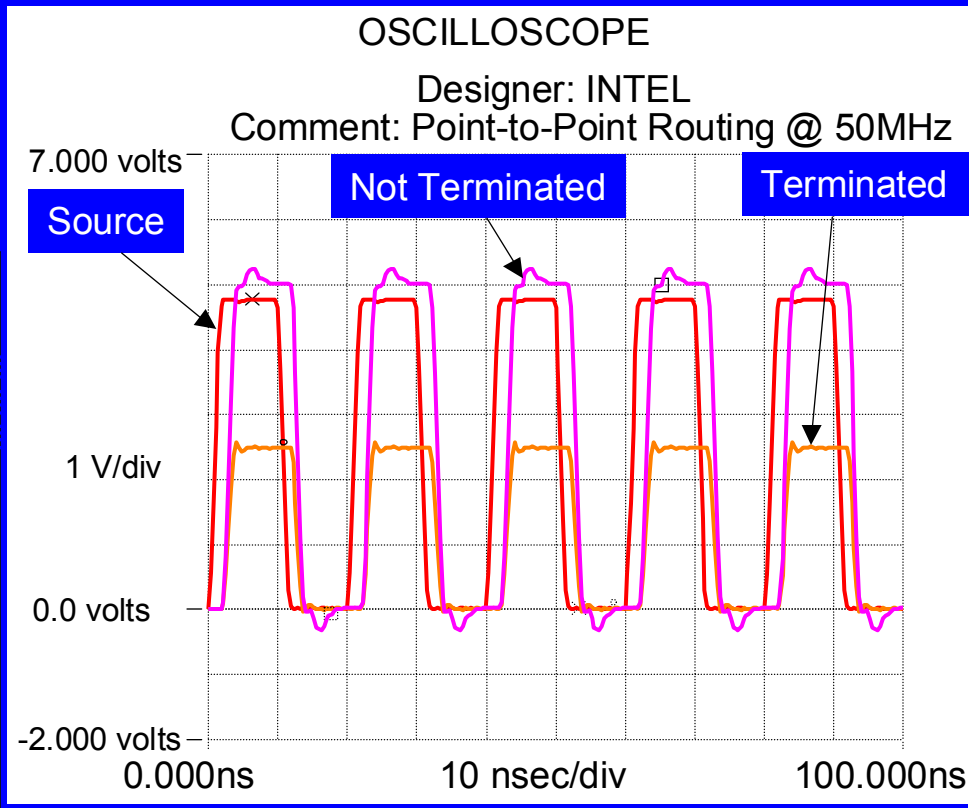




Point-to-Point Routing

- The preferred method for high-speed line.
- # driver channel = # DUTs on BIB.



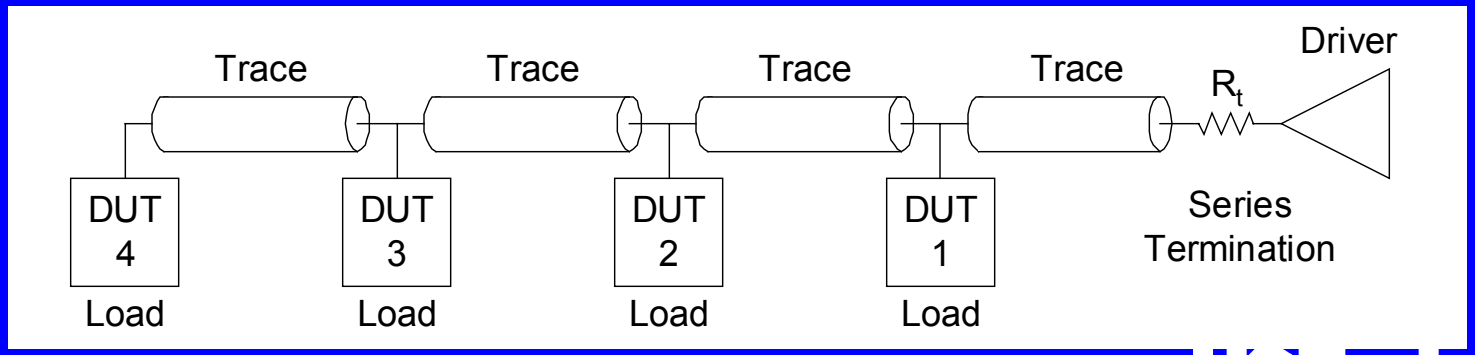


Termination Techniques

- Two common termination scheme in BIB design:
  - Source Termination/Series Termination
  - End Termination/Parallel Termination
- No standard termination works universally
  - Complexity of layout geometry
  - Power consumption
  - Component count
  - Combination of termination scheme
- Termination scheme selection is base on SI simulation

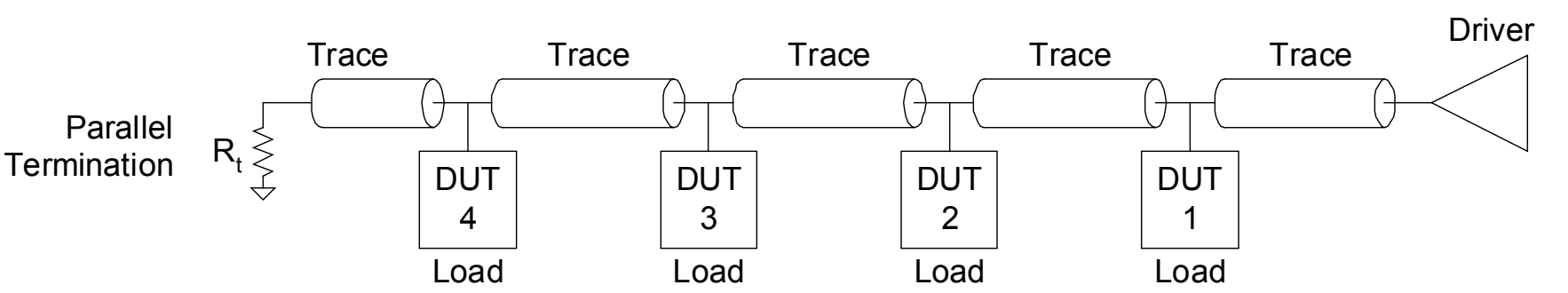
Source/Series Termination

- In series between driver output and transmission line.
- To eliminate signal reflection from the source.
- Slower signal rise time.
- Termination resistor, $R_t = Z_o - R_o$
  - Z_o = Characteristic Impedance of trace
  - R_o = Driver output resistance



End/Parallel Termination

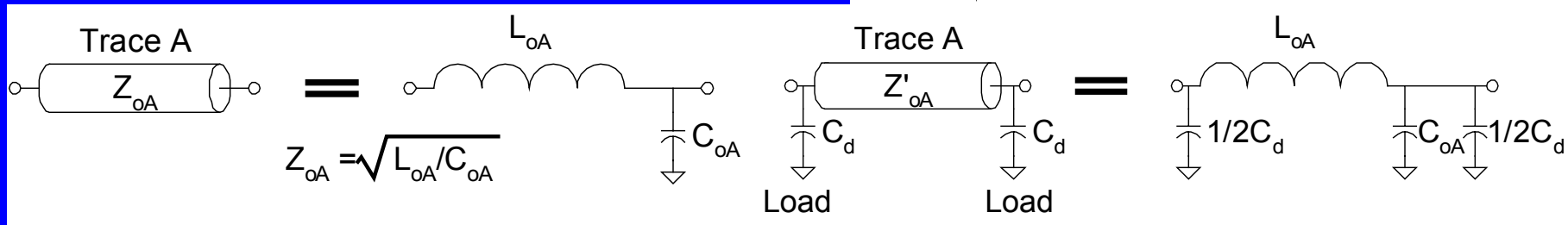
- Located at the receiving end.
- Higher power consumption.
  - Driver must able to source enough current to drive this terminator.
  - Signal level will be halved.
- Termination resistor, $R_t = Z_o$

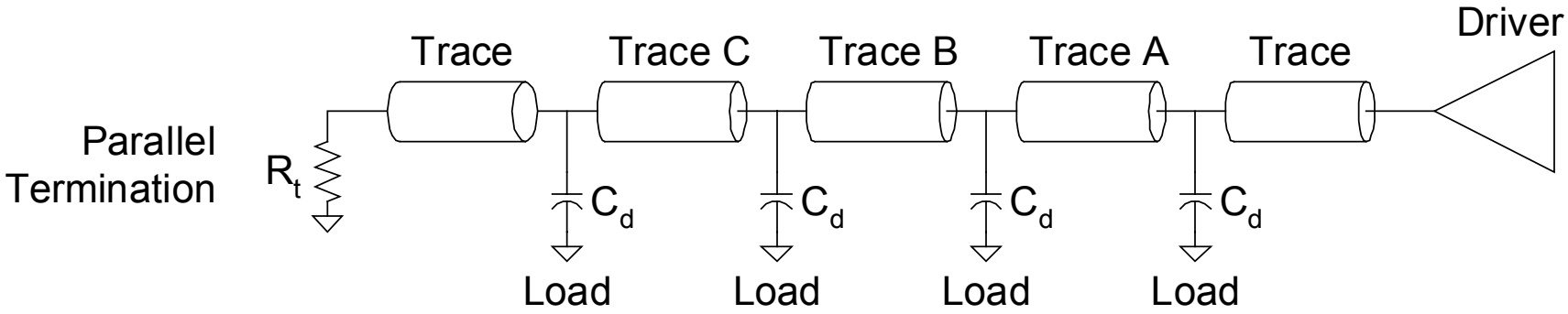


Impedance Compensation

- Existence of DUT's capacitance loading effect reduces the effective Z_o.
- To compensate the loading effect, trace impedance is increased > Z_o.

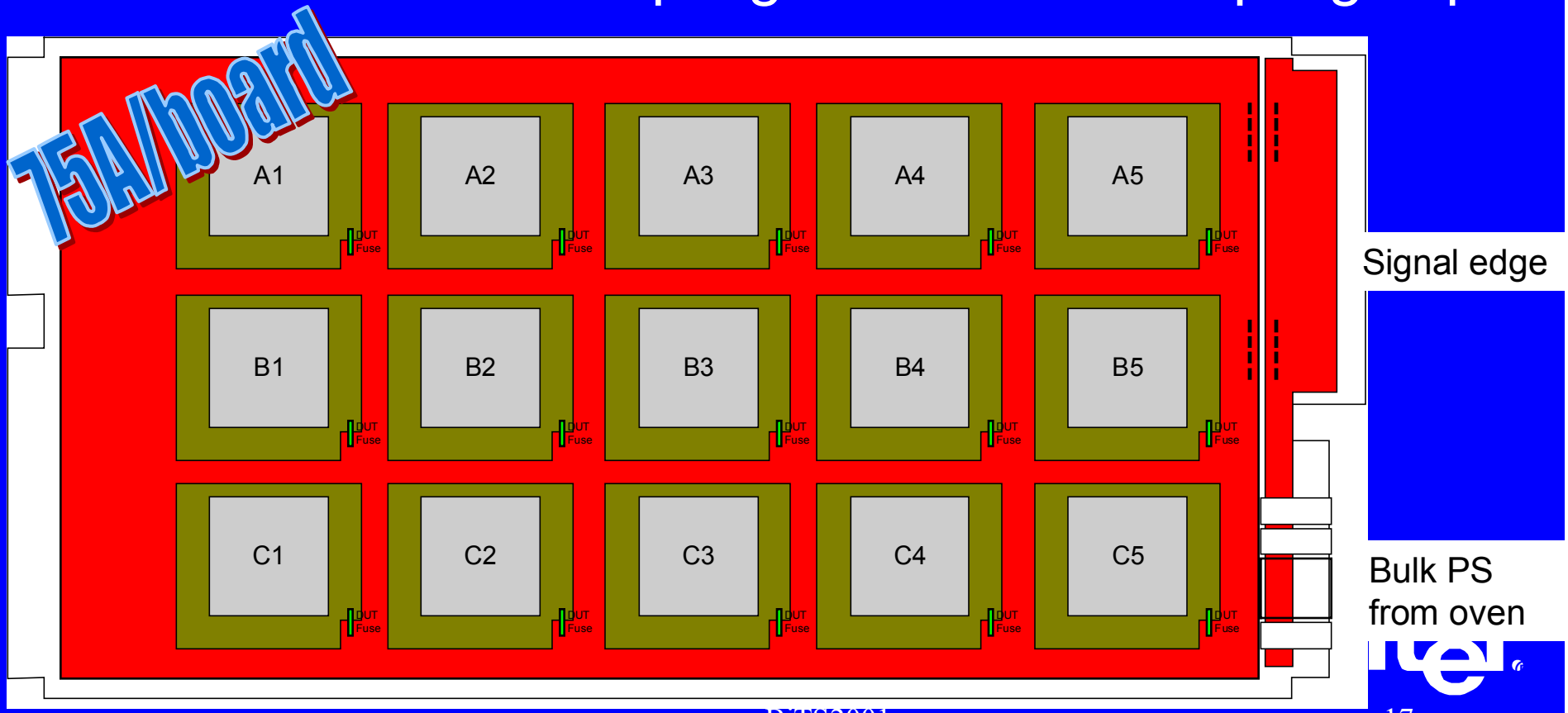
$$Z'_{oA} = \sqrt{\frac{L_{oA}}{(C_{oA} + C_d)}} = \frac{Z_{oA}}{\sqrt{(1 + C_{oA}/C_d)}} < Z_{oA}$$





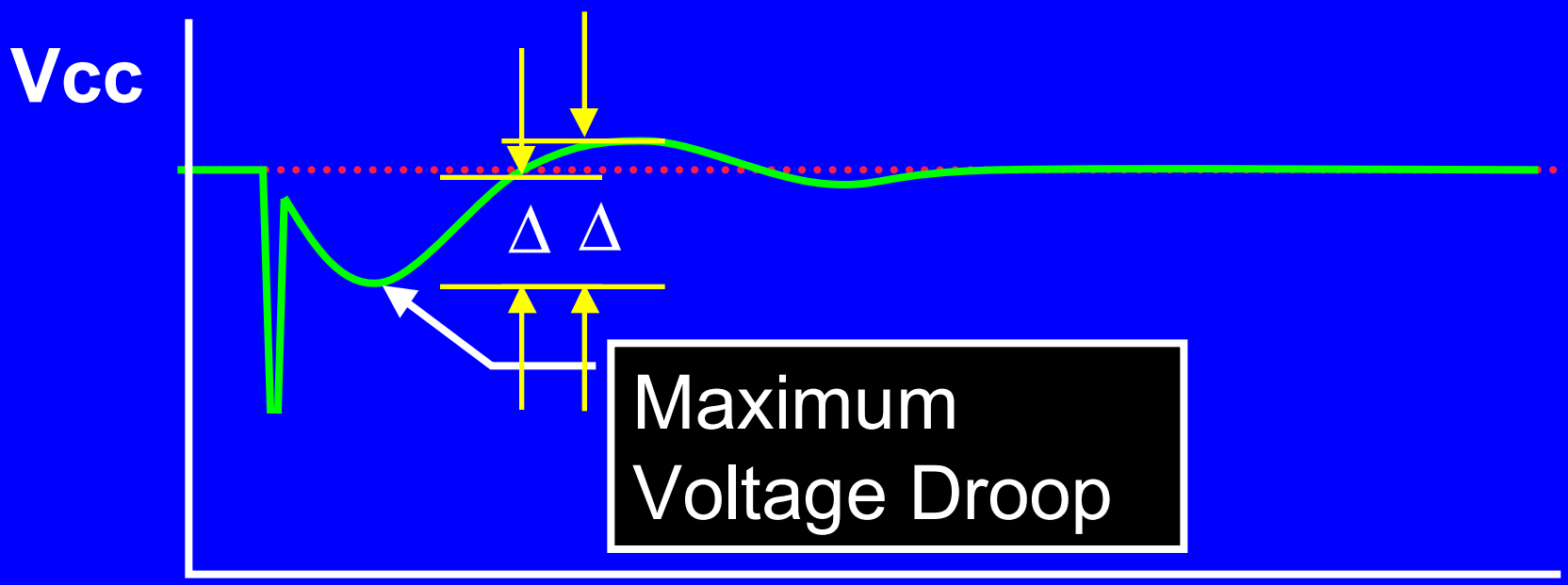
Burn-in Board Power Delivery System

- Common bulk power supply to entire board
- Row or Individual DUT partitioning
- Utilize Bulk decoupling and local decoupling caps



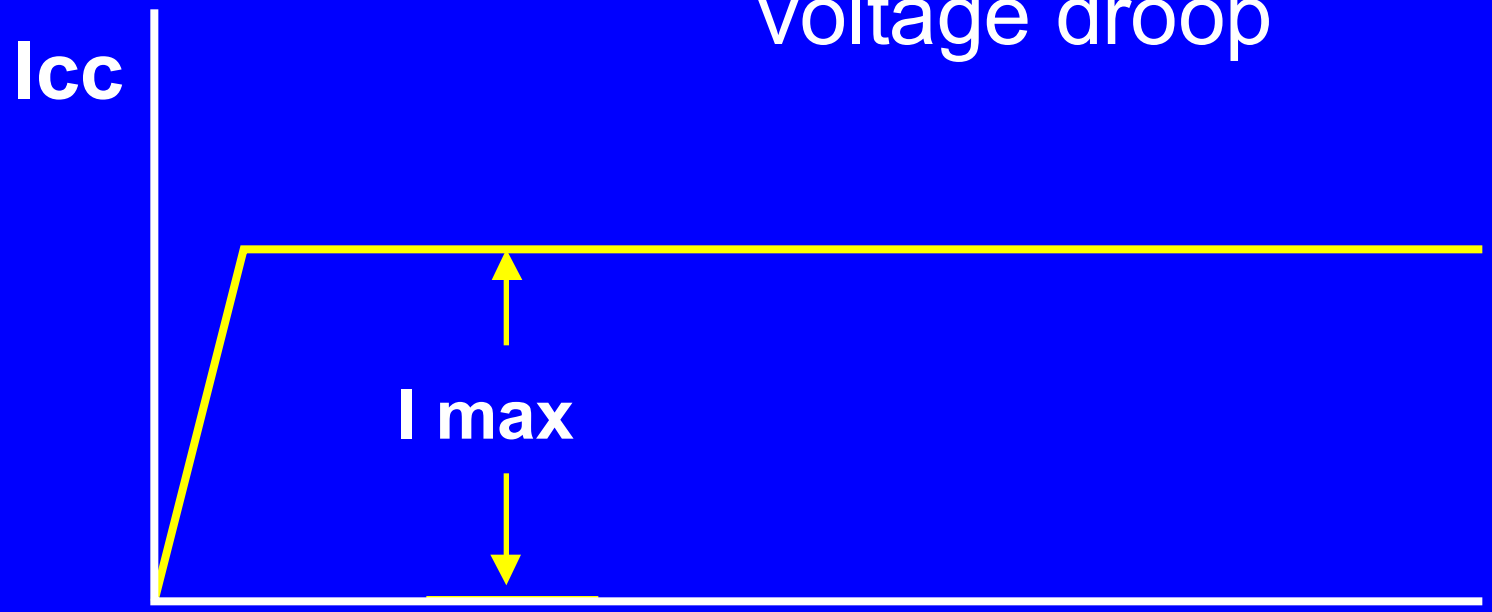
Power Delivery Performance

- 3 key indicators in power delivery performance
- Vcc → Voltage droop specs



Power Delivery Performance

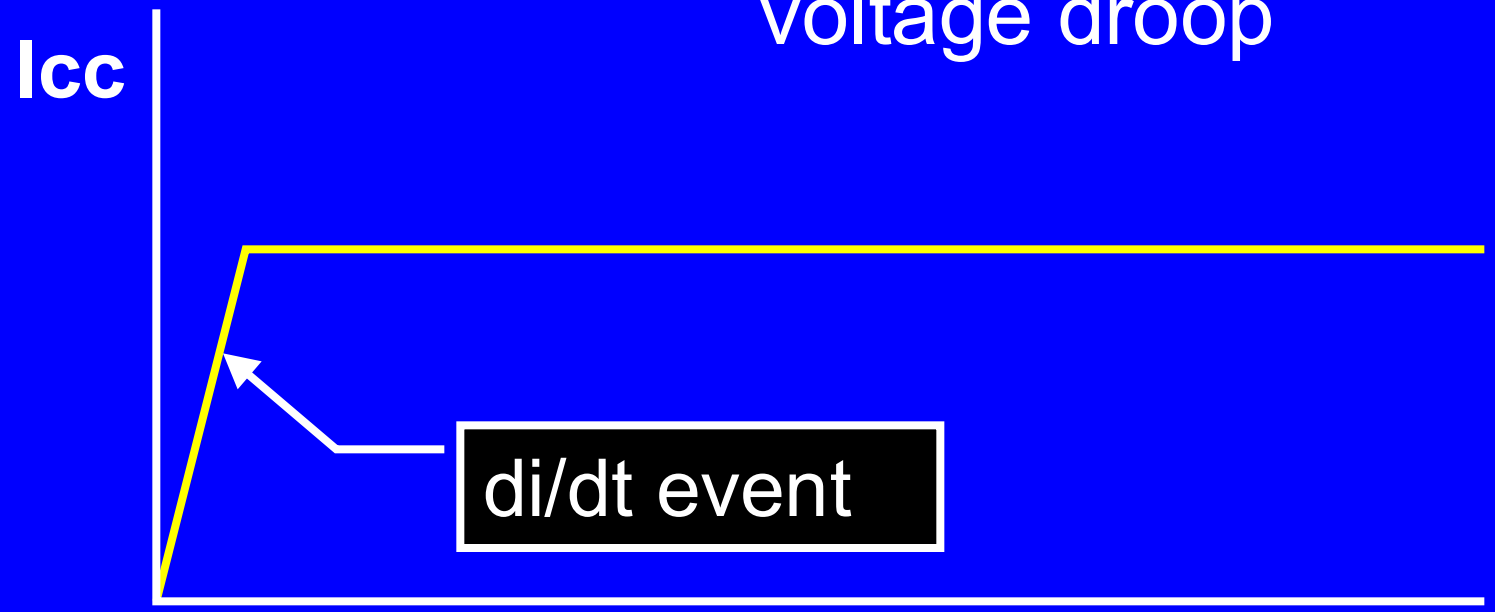
- Imax → Impacts slower transient voltage droop



Every 1X Amp increase will incur extra 10mV drop / Imax

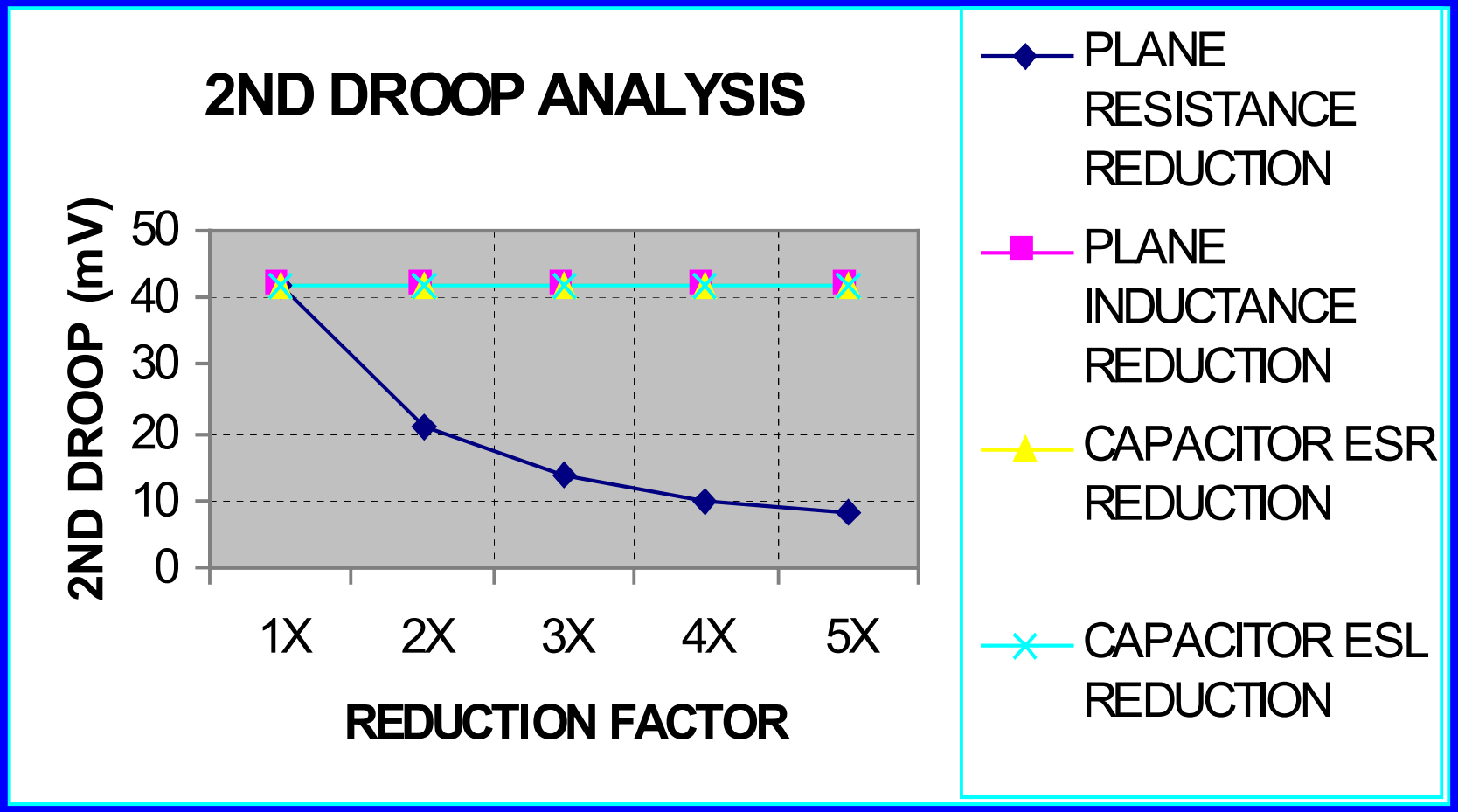
Power Delivery Performance

- di/dt → Impacts fast transient voltage droop



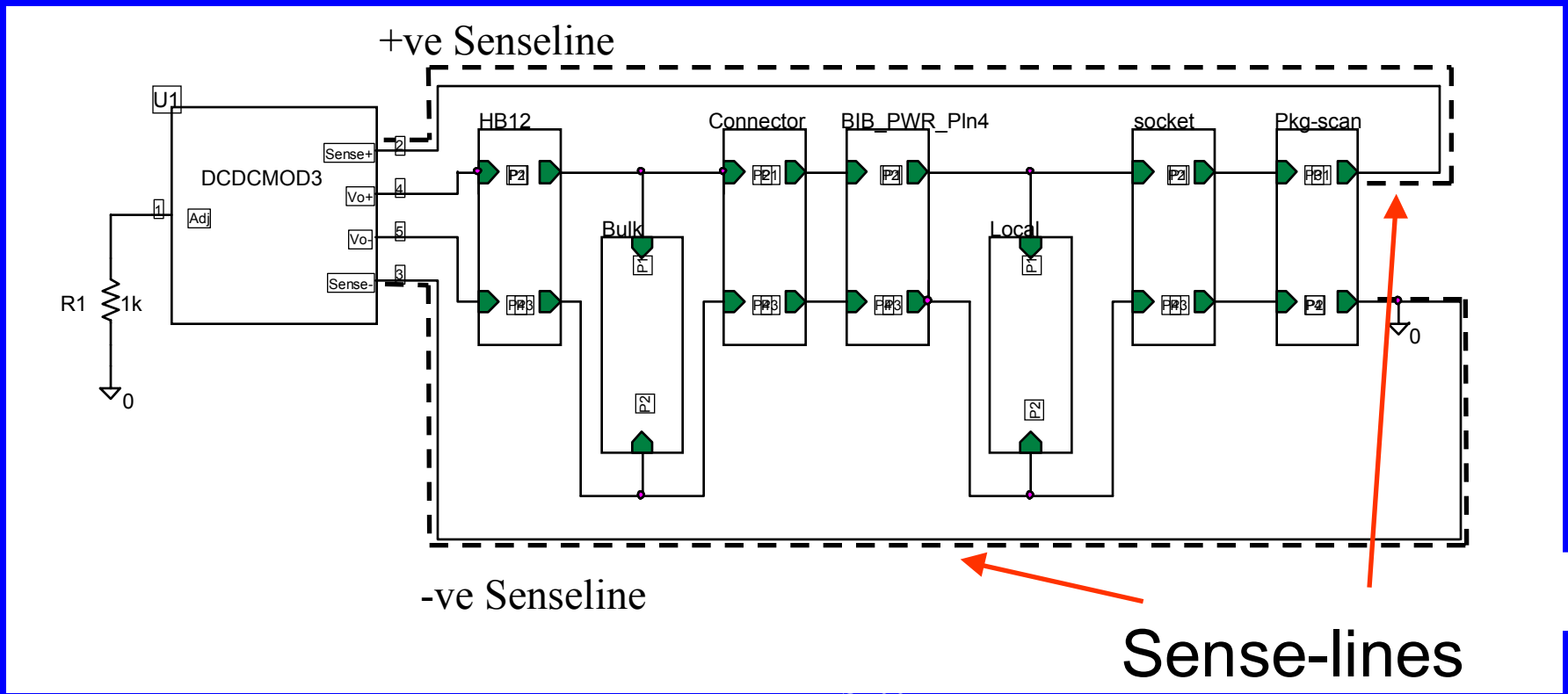
Every 1X A/ns increase will incur extra 10mV drop / 1pH

DROOP ANALYSIS



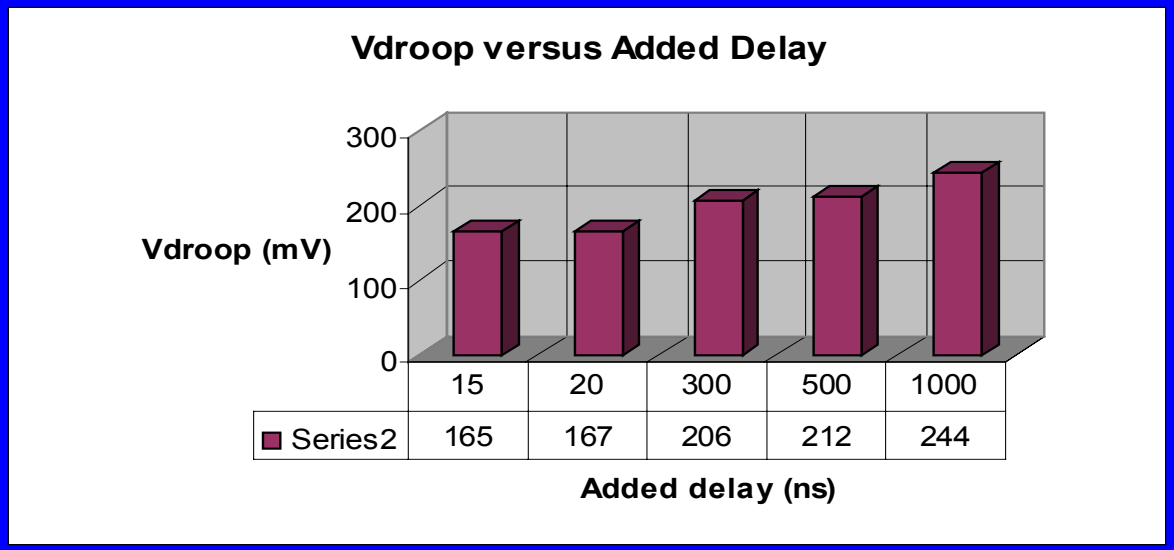
Vdroop Reduction Techniques

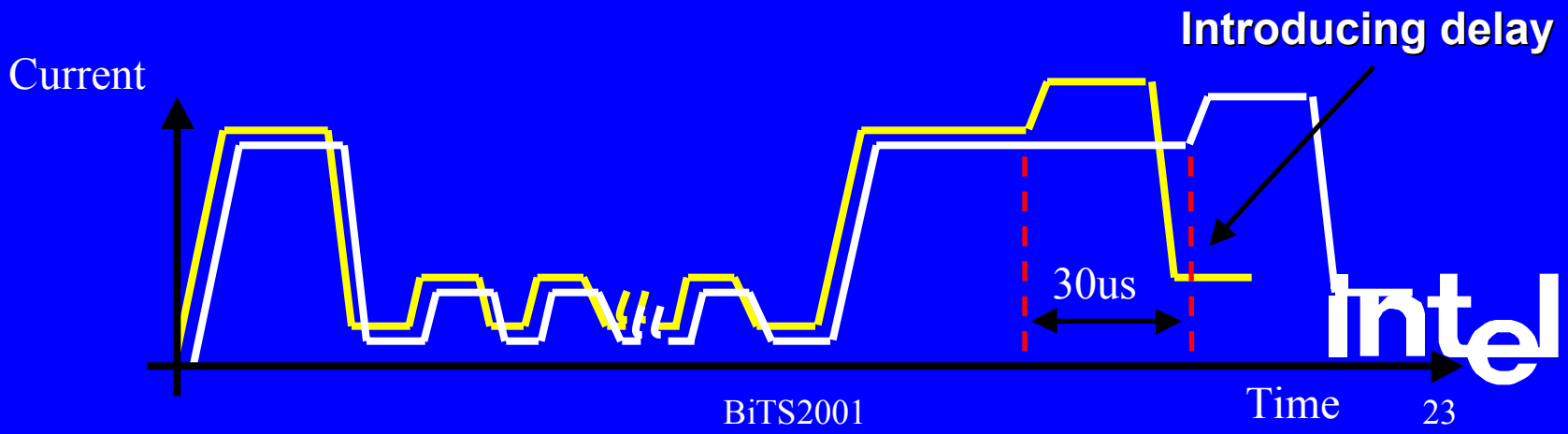
- Close loop model
  - Die level Vdroop activity can be sensed and feedback to the converter.
  - Voltage compensation is closely monitored.



Vdroop Reduction Techniques (con't)

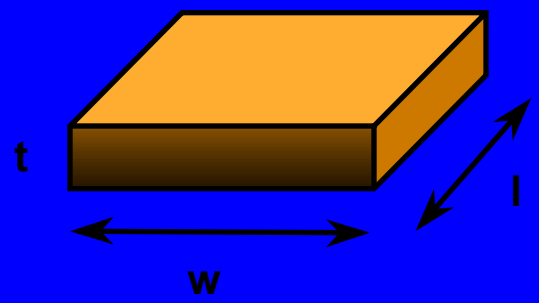
- Optimizing DUT I profile
  - Introducing delay aids in voltage recovery and thus reduces Vdroop





Vdroop Reduction Techniques (con't)

- 2oz Plane
  - –2.76 mil thick (2X thicker v.s. 1-oz laminates)
  - –Effective cross-section resistance (DC): Rdc = 0.25 ohm (in/in)



$$R = \rho\frac{l}{A} = R_{sheet}\frac{l}{w} = (2.459x10^{-4})\frac{l}{w}$$

$$\rho = 6.787x10^{-7} \text{ (Copper resistivity)}$$

SUMMARY

- High-speed and high-power design methodology is essential for next generation BIB.
- Signal integrity simulation and routing methodology are vital to preserve signal integrity
- Paradigm shift is needed in power delivery system for high-power design.
- 2-oz plane effective to solve droop issue.
- Close loop modeling helps to reduce/minimize Vdroop.

THANK YOU

Q & A

ACKNOWLEDGEMENT

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