



Burn-in & Test Socket Workshop

March 4 - 7, 2001
Hilton Mesa Pavilion Hotel
Mesa, Arizona

IEEE

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Technical Program

Session 3

Monday 3/05/01 1:00PM

Electrical And Mechanical Modeling And Analysis

“Review Of Burn-in Socket Contact Platings”

Thomas A. Bradley - Agere Systems

“A Finite Element Analysis Of Solder Balls On A BGA Package In Sockets During Burn-in”

Alfred Sugarman - Loranger International Corp. (Presenter)

Ariane Loranger - Loranger International Corp.

“SPICE Model Extraction From S Parameter Data For Test Contactors”

Valts Treiberis - Everett Charles Technologies

“Least Squares Analysis Of Composite True Position Specification”

Alex Owen - Wells-CTI

BiTS 2001 Workshop

Review of Burn-in Socket Contact Platings

By: Thomas A. Bradley

AGERE Systems

Formerly Lucent Technologies Microelectronics
Group in Allentown, PA

Introduction

- Contact Materials - Gold or Nickel Boron
- Device Materials - Solder Balls
- Test Temperatures - 125C and 150C
- Times - 9 hours up to 1100 hours
- Tests - Visual up to 10X magnification
Contact Resistance in Ohms

Test Summary

- BGA Test Package - 60/40 solder balls
- Socket Conditions - Loose or on Boards
- Socket types
 - 225 pin with tapered hole contact
 - 352 pin with flat surface contact
- Test 1 - 9 Hours at 150C
- Test 2 - 9 Hours at 125C
- Test 3 - 24 Hours at 150C
- Test 4 - 24 Hours at 150C
- Test 5 - 1100 Hours at 150C

Gold Contacts Test Results

- 9 Hours at 125C
10% of contacts contaminated with solder material, corresponding device balls missing chunks of solder
- 24 Hours at 150C
100% of contacts contaminated with solder material, all device balls missing chunks of solder

Nickel Boron Contacts Test Results

- 9 Hours at 125C
- 24 Hours at 150C
- 1100 Hours at 150C
- No sign of any contact contamination at any of the above conditions, good connections

Intermetallic Alloys

Per Charles A. Harper`s Handbook of Wiring, Cabling and Interconnects for Electronics

- Gold* alloys with tin & lead to form intermetallic compounds Au_6Sn , $AuSn$, $AuSn_2$, $Au_{19}Sn_4$, Au_2Pb and $AuPb_2$
- Solder becomes brittle when gold alloys exceed 5%, contact intermittents & opens develop when alloys reach 10 to 15%
- Alloys grow extremely slowly at 25C but are greatly accelerated by heat and pressure
- * Similar alloys grow for other materials

Impact of Intermetallics

- When alloys build up on socket contacts the connections become unreliable due to high resistance and opens
- When alloys develop on the device contacts, device solderability suffers due to gold embrittlement

Other Contact Materials

- Several other common contact materials were tested
- All exhibited the same results as gold
- Even NiB failed when the temperature approached 183C (solder liquidus)
- NiB also failed when exposed to flux

Conclusions

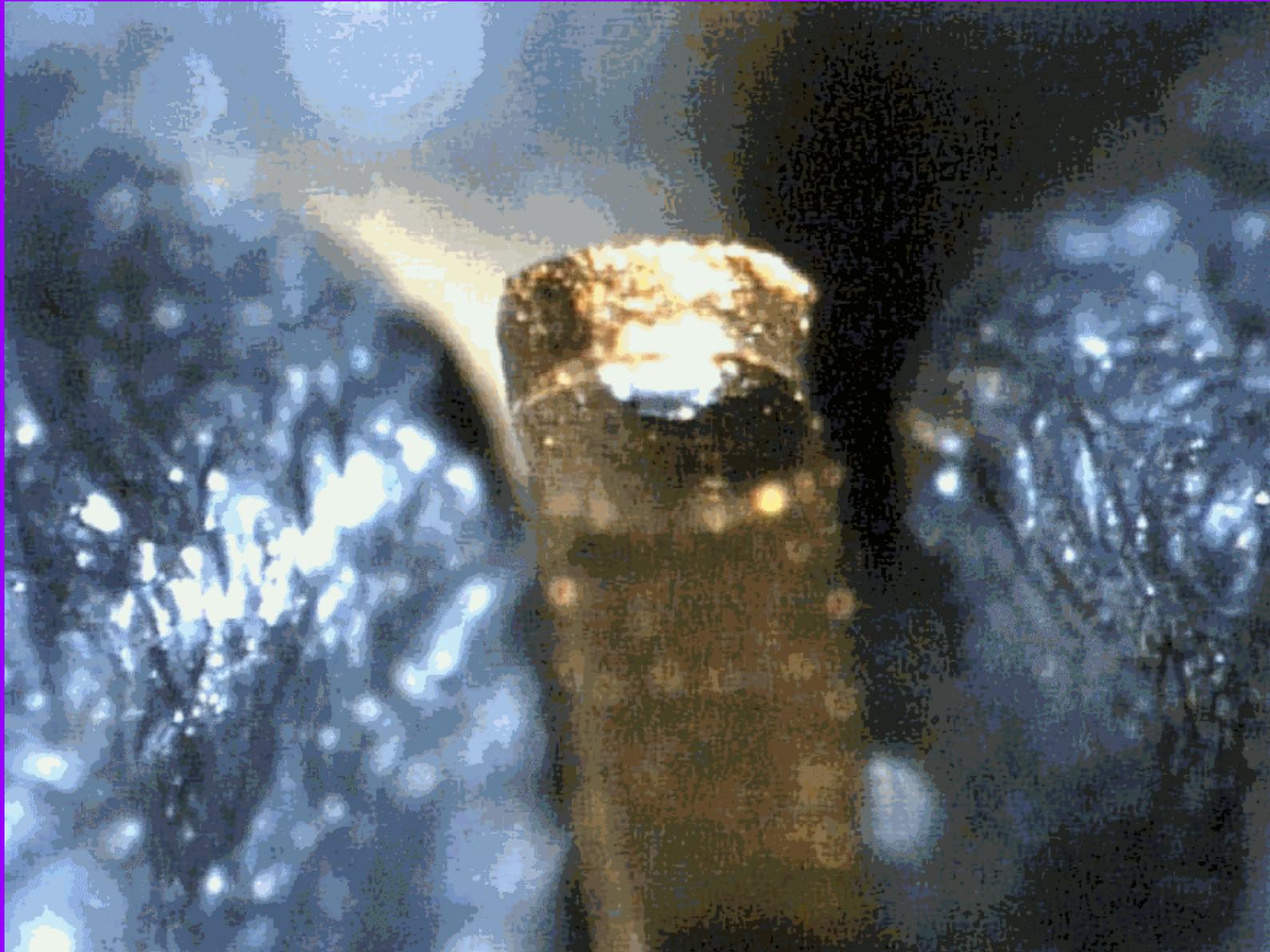
- Only NiB contact plating has been found to eliminate contamination due to alloy growth
- Applies to BGAs and any device with solder dipped or plated contacts
- Applies at 125C and 150C
- Questionable at 100C
- Does not apply for short term use at 85C
- Work arounds include:

Burn-in of BGA before solder ball attach

Reducing temperature to 85C (3X time)

Don't look - don't ask - don't tell

Photo of Solder on Gold Contact





A FINITE ELEMENT ANALYSIS OF SOLDER BALLS ON A BGA PACKAGE IN SOCKETS DURING BURN-IN

By
Alfred Sugarman
Ariane Loranger

Presented at
BiTS Burn-In & Test Socket Workshop
March 4-7, 2001
Mesa, AZ



PURPOSE

- Analyze stresses and strains during burn-in on the solder ball/package interface for 3 different styles of contacts.
- Evaluate possible failure modes for the solder balls from the evaluated stresses and strains.

REVIEW AND SCOPE

- Analysis of stresses (tensile and shear), strains (tensile and shear), displacements in the solder ball at the package/ball interface for more than 2 weeks at 125°C for socket contact styles that include compression, single arm tweezers and double arm tweezers.
- Comparison of FEA data with creep models
- Comparison of conditions of stress, strain, time and temperature during burn-in and conditions leading to grain boundary sliding.
- Analyzed tensile stresses in the interface region of the solder ball to the package body which could contribute to tensile creep and failure.



WHAT IS FINITE ELEMENT ANALYSIS (FEA) AND HOW IS IT DONE

- Finite Element Analysis is a computer based simulation of the effects of stress and strain on the solder balls in a BGA package after they are stressed under burn-in conditions in a socket.
- Basis of FEA is the elastic (Hooke's Law) and plastic response of an element (e.g., a cube). This study used nonlinear analysis methods to evaluate plastic creep.
- FEA of the solder ball was performed by breaking the solder ball into hundreds of thousands of little geometric elements and analyzing with a computer the effect of contact load and burn-in temperature on each element. FEA also analyzes the interaction between each element and its neighbor.



WHAT IS FINITE ELEMENT ANALYSIS (FEA) AND HOW IS IT DONE (continued)

- FEA does not allow for differences in microstructure (e.g., grain size, colony size, porosity) or changes in microstructure during burn-in.
- FEA is a good way of examining effects from stresses and strains from burn-in on the solder ball over a range of conditions. With FEA experimental error can be eliminated. Going beyond these results to an understanding of their underlying reasons (e.g., increasing or decreasing strain with time, why strain is greater in one case than in other case) is beyond the scope of this work.

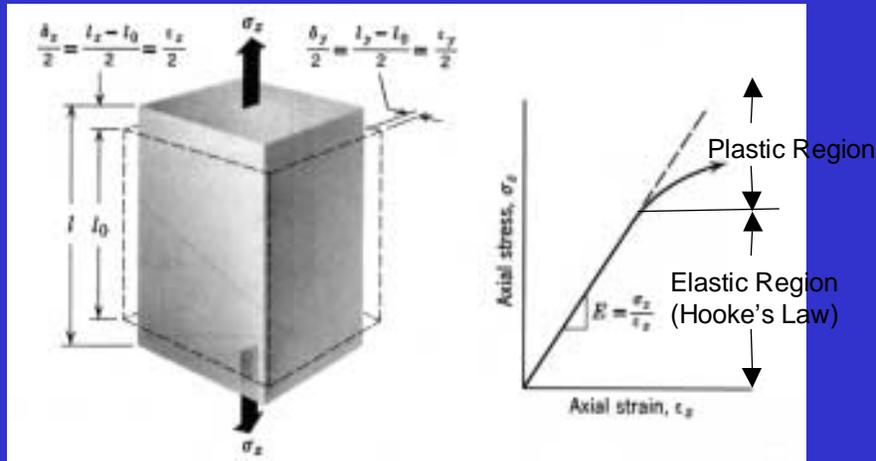


Figure 1. Example of tensile stress and strain. The elastic region is described by Hooke's Law.

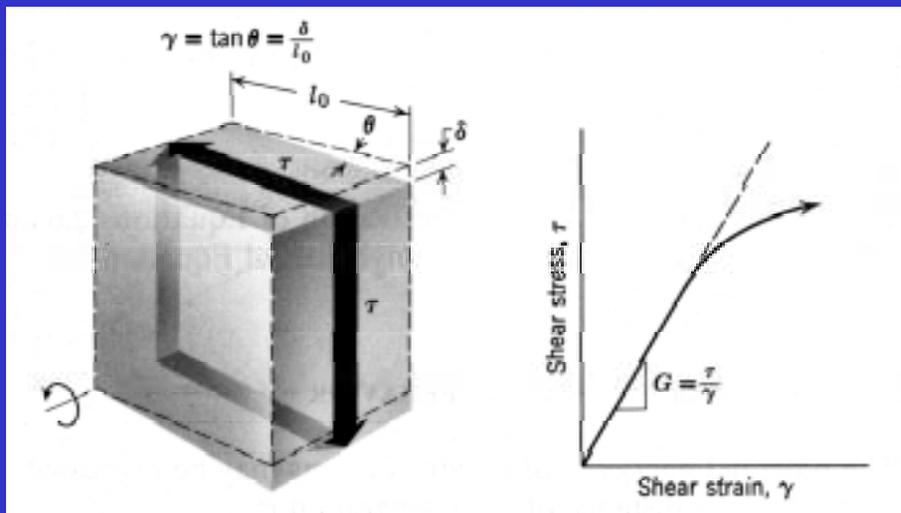
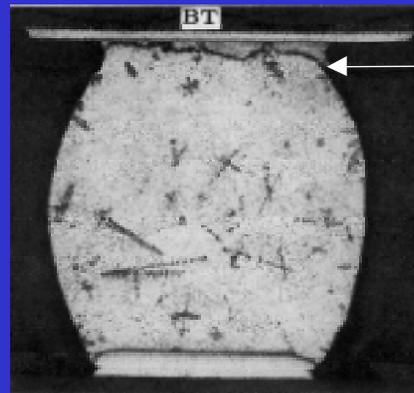


Figure 2. Example of shear stress and strain

HOW DO SOLDER JOINTS FAIL

- Creep in solder balls during burn-in can cause strain at the solder ball/package interface weakening this area.
- Cracking at solder ball/package interface can lead to lost balls or open connection as shown below.
- Temperature cycling and mechanical fatigue testing that simulate the field environment show the predominant failure mode is cracking in the solder ball leading to an open.



Crack in solder ball near package interface

Figure 3. Solder ball with crack at package interface. The interface is where the FEA was performed.

CONDITIONS FOR GRAIN BOUNDARY SLIDING

- High temperatures & low strain rates which occur during burn-in conditions are appropriate conditions for promoting sliding between the colonies and/or grains in the solder. (See schematic below)

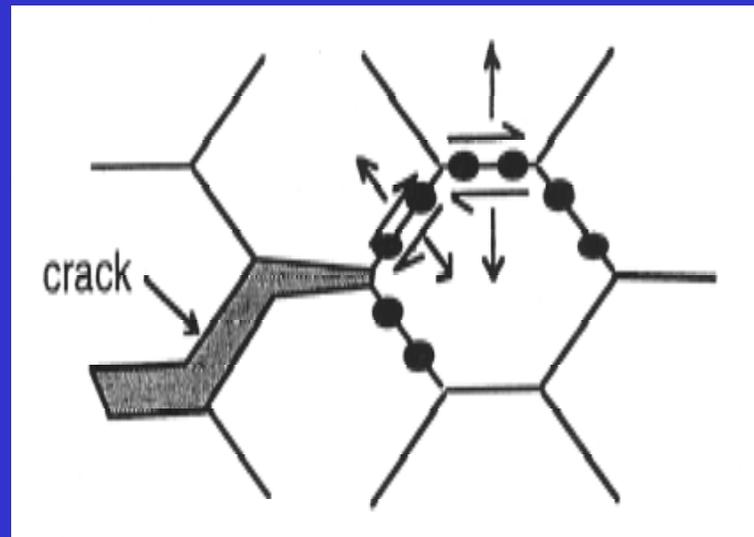


Figure 4. Schematic showing grain boundary sliding which creates cavities between the grain resulting in cracking.



Inputs To Finite Element Analysis Model

	Single Arm Tweezers	Double Arm Tweezers	LIC Compress Contacts
SOLDER BALL MATERIAL			
Alloy	63Sn37Pb	63Sn37Pb	63Sn37Pb
Young's Modulus (MPa)	21,000	21,000	21,000
Poisson's Ratio	0.4	0.4	0.4
Yield Stress at 125°C (MPa)	9.5	9.5	9.5
Temperature	125°C	125°C	125°C
Coefficient of Thermal Expansion	NA	NA	NA
SOLDER BALL GEOMETRY			
Diameter of ball	.0295 in	.022 in	.022 in
Diameter of ball at pkg interface	.024 in	.018 in	.018 in
CONTACT (see Note 1)			
Contact Force	40g	15g	18g
Bend Angle In Contact	21°	21°	N/A
Width	.05 in split	0.10 in	N/A
Spring Constant of Contact	NA	NA	NA
Coeff of Thermal Expansion	NA	NA	NA
CREEP MODEL INPUTS (see Note 2)			
Creep Activation Energy, ΔH	0.494 eV	0.494 eV	0.494 eV
Freq Constant, C^* (1/sec-MPa)	.2046	.2046	.2046
Boltzmann Constant, k (eV/°K)	8.63e-5	8.63e-5	8.63e-5



Notes For Table Of Inputs:

Note 1. Sourced from literature

Note 2. Power Creep Law

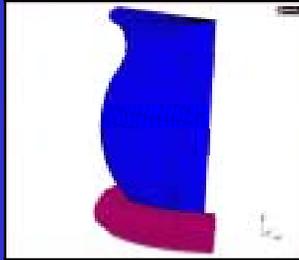
$$\dot{\gamma} = C^* \tau^n \exp\left(-\frac{\Delta H}{kT}\right)$$

Where:

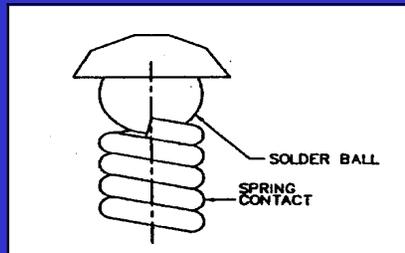
- $\dot{\gamma}$ = creep rate (1/sec)
- C^* = frequency constant (1/sec-MPa)
- τ = shear stress (MPa)
- n = exponent
- ΔH = activation energy (eV/°K)
- k = Boltzmann's constant (eV/°K)
- T = temperature (°K)



FEA OF COMPRESSIVE STYLE CONTACTS



FEA model of Loranger contact style. 1/4 model.



Schematic of Loranger style contact.



Witness marks created by compression style contacts.

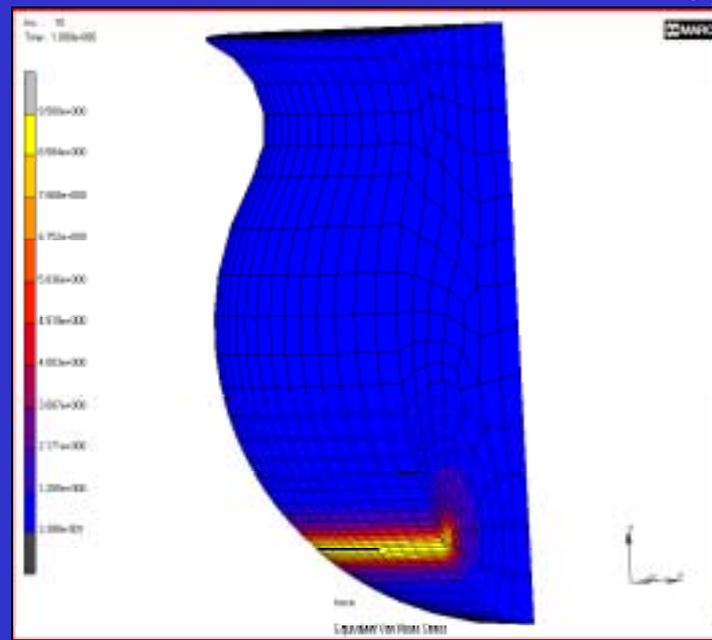
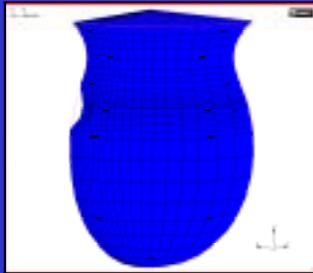
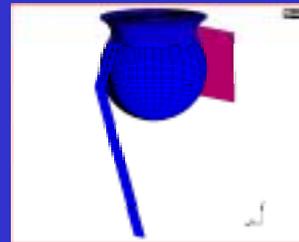


Figure 5. LIC design (1/4 model). Static stress at 0 hrs. Magnitude of stress is indicated by color and density of grid on surface.

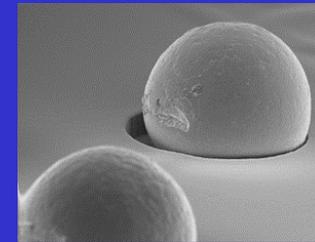
FEA OF SINGLE ARM TWEEZERS



Single arm tweezers design.
Deformation created in solder ball.
(1/4 model).



Model used for FEA of single arm
tweezers contact style.



Witness mark created by single arm
tweezers style contacts after burn-in
125°C for 9 hours.

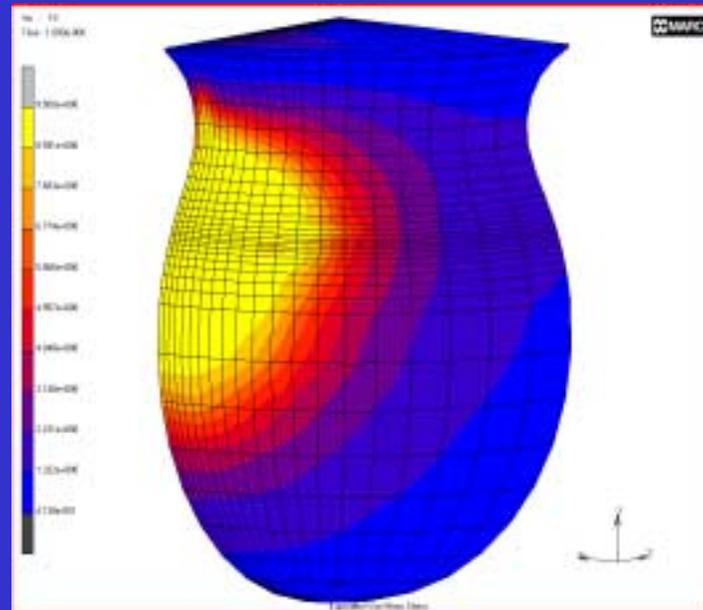
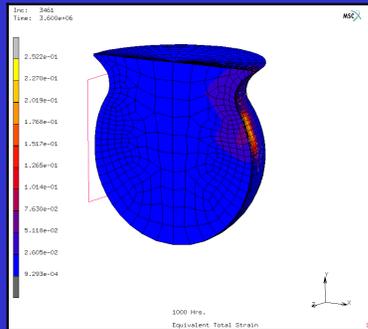


Figure 6. Single arm tweezers design (1/4 model). Static stresses at 0 hours and 125°C.

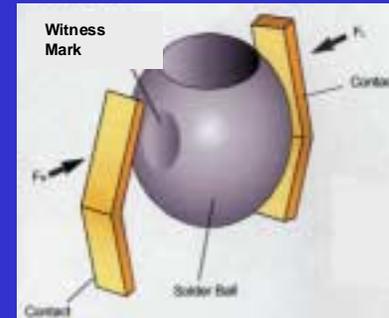
FEA OF DOUBLE ARM TWEEZERS STYLE CONTACTS



Two arm tweezers design. Total Strain after 42 days (1/2 Model)



Two arm tweezers design. Model used for FEA of double tweezers design



Schematic of two arm tweezers style contact.

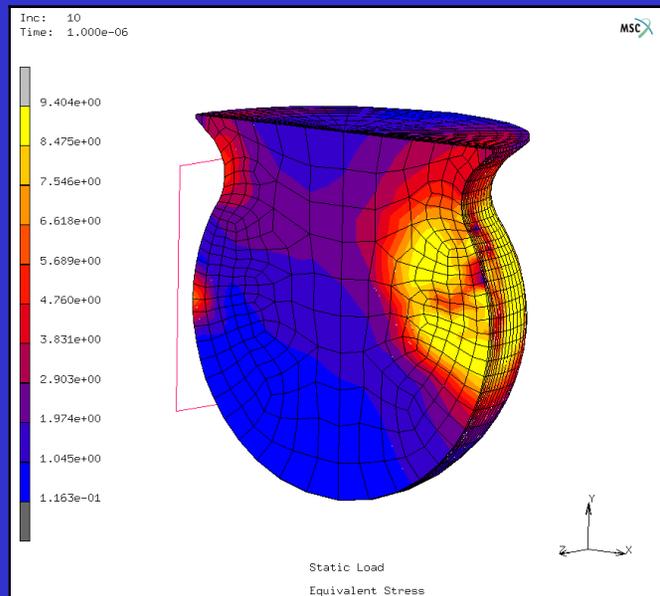
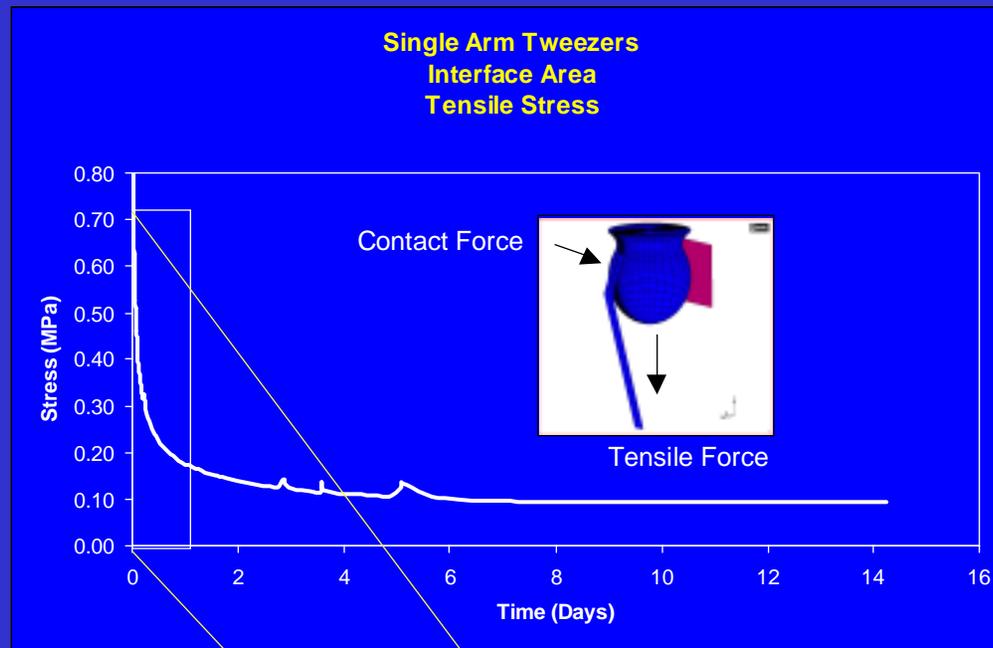
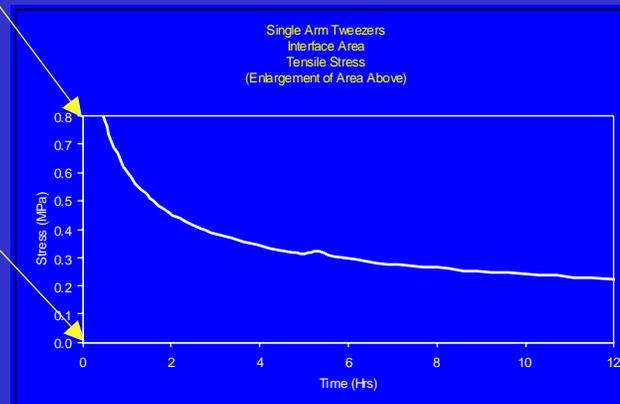


Figure 7. Two arm tweezers design (1/2 Model). Equivalent Stress Static Load at 0 hours and 125°C.

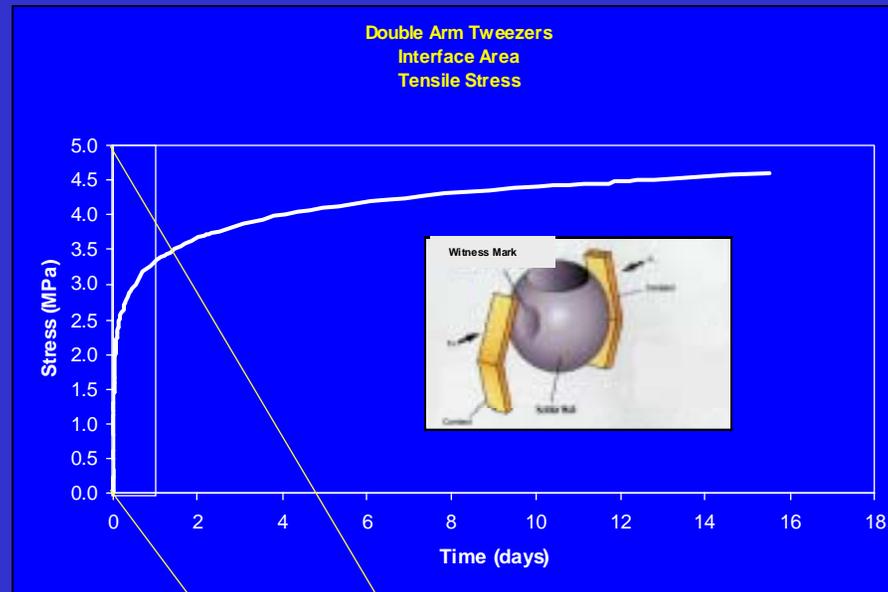
FEA OF SINGLE ARM TWEEZERS STYLE



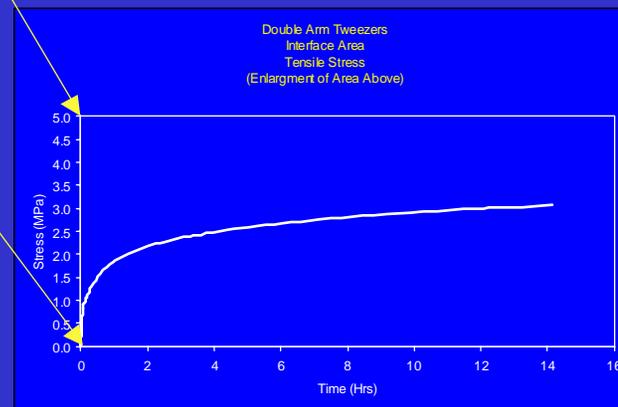
Enlargement of chart area



FEA OF DOUBLE ARM TWEEZERS STYLE



Enlargement of chart area



GRAIN BOUNDARY SLIDING

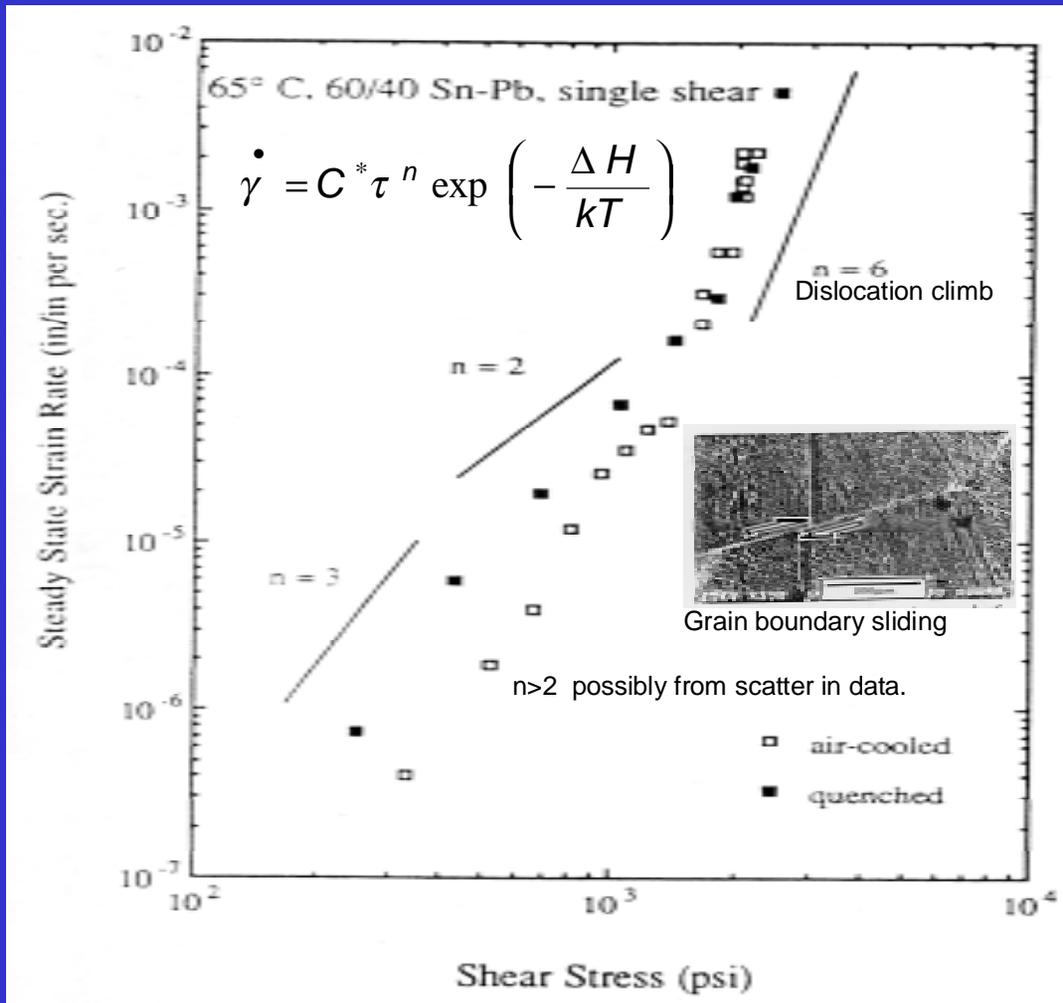


Figure 8. Steady state strain rate vs shear stress determined with conventional creep tests at 65°C on single shear specimens with air-cooled and liquid nitrogen quenched solder joints. Photomicrograph on chart shows grain boundary sliding in Pb-Sn eutectic solder as predicted when n=2.

In equation above

$\dot{\gamma}$ = shear strain rate,

τ = shear stress

n = stress exponent

C^* = frequency constant,

ΔH = activation energy

k = Boltzmann's constant

T = temperature (°K)

STRESS EXPONENT WHICH IS CHARACTERISTIC OF THE CREEP MECHANISM DOES NOT CHANGE

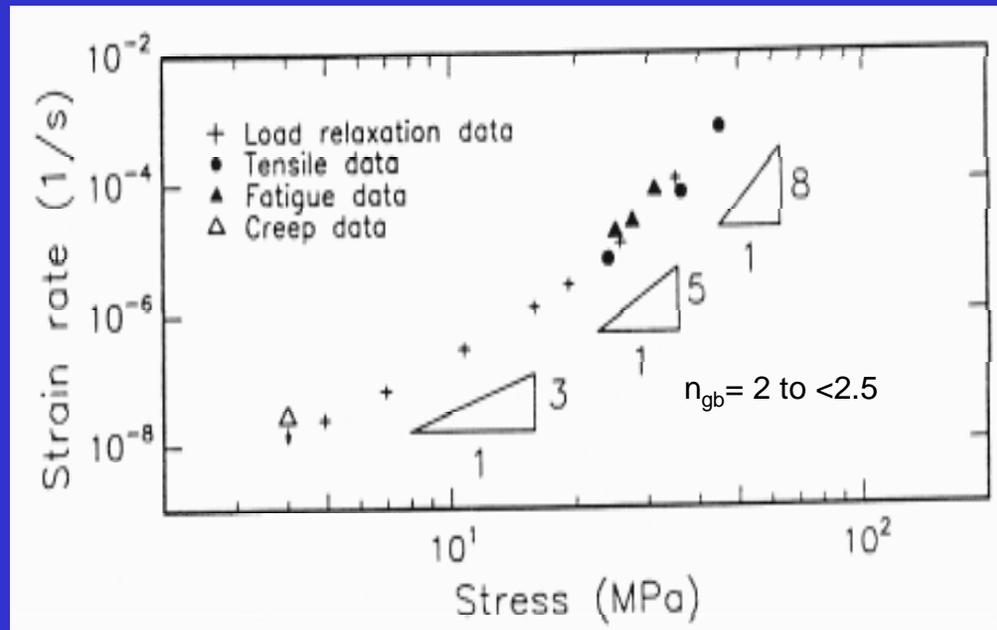


Figure 9. Test data by different methods from Pb-Sn eutectic solder showing stress exponent change over a range of stresses and strains. $1 \leq n_{gb} \leq 2.5$ corresponds to grain boundary sliding. This data confirms $n=2$ corresponds to grain boundary sliding regardless of how strain rate is measured.



STRESS EXPONENT ANALYZED FROM FEA OF SINGLE ARM AND DOUBLE ARM TWEEZERS CONFIRMS GRAIN BOUNDARY SLIDING



Figure 10. Shear strain rate vs stress for data from Finite Element Analysis for single arm tweezers. The slope, 2.2512 in the expression above for a best fit line is the stress exponent, n in the creep equation.

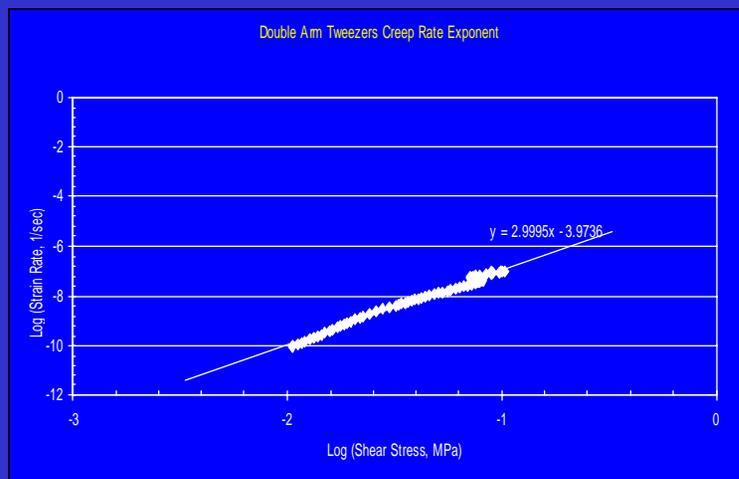


Figure 11. Shear strain rate vs stress for data from Finite Element Analysis for double arm tweezers. The slope, 2.9995 in the expression above for a best fit line is the stress exponent, n in the creep equation.

NOTE: Since the LIC compression contact style socket does not apply tensile shear stress or strain to the solder ball no graph is shown for this style and there is no fear of grain boundary sliding creating tensile strains.



Results Summary

Design	Contact Force	Tensile Force	Tensile Stress At Interface After 1 Day	Tensile Strain At Interface After 1 Day	Stress Exponent* (n)
LIC Compression Style	18g (compression)	N/A	N/A	N/A	N/A
Single Arm Tweezers Gripping Style	40g	12g	0.176 MPa (26 psi)	5.68×10^{-4}	2.3
Double Arm Tweezers Gripping Style	15g	10g	3.3 MPa (479 psi)	2.45×10^{-4}	3.0

*n=2.0 to 2.5 indicates grain boundary sliding which can promote porosity and cracking at the solder package interface.



CONCLUSIONS:

- Significant tensile forces at the solder ball package interface are created by tweezers style contacts. These tensile forces cause small tensile stresses and strains at the interface between the ball and package.
- Weak areas which existed before burn-in may grow during burn-in because of tensile stresses pulling down on the solder balls.
- For single arm tweezers the stress exponent is $n=2.3$ showing grain boundary sliding is dominant mechanism for deformation in the solder ball/package interface.

For double arm tweezers the stress exponent is $n=3.0$ showing grain boundary sliding may not be the only mechanism for deformation in the solder.

- Tweezers style contacts may increase the risk of BGA failures (e.g., lost balls, failure of solder joints) in the field and during processing by customer.



REFERENCES

1. "Solder Joint Reliability of BGA, CSP, Flip Chip and Fine Pitch SMT Assemblies" p 201 by John H. Lau and Yi-Hsin Pao, McGraw-Hill 1997
2. S.A. Schroeder and M.R. Mitchell, "Observations Of In Situ Creep Crack Propagation In 63Sn/37Pb" Proceedings of the NEPCON West'97. Part 1 (of 3), Anaheim, CA 1997.
3. Final Report for BGA Socket Design Comparison by MSC.Expert Solutions Group, Costa Mesa, CA October 16, 2000.
4. "Solder Joint Reliability of BGA, CSP, Flip Chip and Fine Pitch SMT Assemblies" op.cit. Table 4.9.
5. *Photo of witness mark from James Forster, "Performance Drivers for Fine-Pitch BGA Sockets", HDI pp34-37, December 1999.*
6. *Chart from Z. Mei, J.W. Morris, Jr., M.C. Shine "Superplastic Creep Eutectic Tin-Lead Solder Joints", Journal of Electronic Packaging Vol. 113 pp 109-114 June 1991*
7. *Photomicrograph from S.M. Lee and D.S. Stone, "Grain Boundary Sliding In As-Cast Pb-Sn Eutectic", Scripta Metallurgica et Materialia, Vol 30, No. 9 pp1213-1218 1994.*



SPICE Model Extraction from S Parameter Data for Test Contactors

Valts Treibergs
Everett Charles Technologies
March, 2001

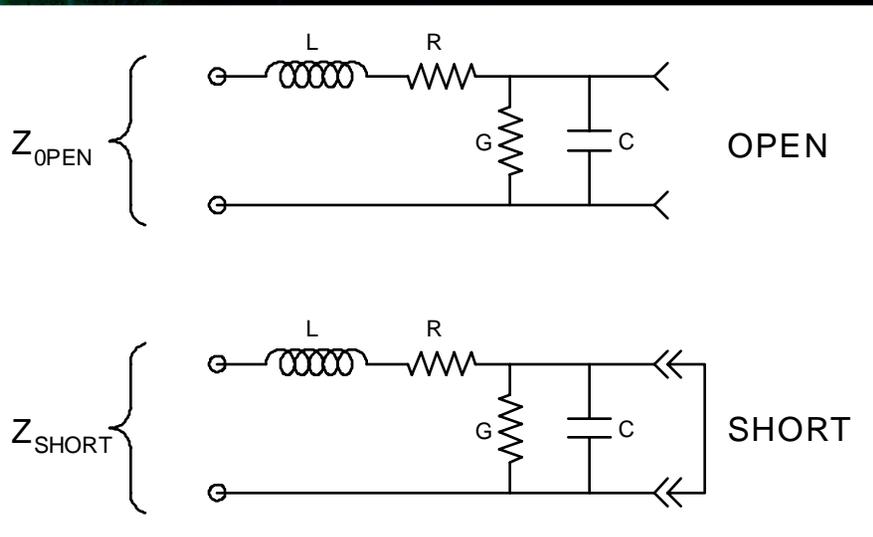


Topics

- Contactor RF Parameter Measurement Methodology
 - Reactance and Open & Short Circuit Measurement
- SPICE Model Topology
 - Individual Pin Parameters (Ls, Cs, Rc)
 - Coupled Pin Parameters (Cc, Lm)
- Probing & SPICE Model Parameter Extraction
 - Individual Pin Parameters (Ls, Cs, Rc) - Open & Short
 - Coupled Pin Parameters (Cc, Lm) - Crosstalk Open & Short
 - Model balancing
 - Example Results
- Transmission (S_{21}) Considerations
 - Comparison of models for Loop Through and Direct S_{21} responses
- Benefits of this Modeling Technique
- References / Bibliography

Measurement Methodology

- Short circuit impedance measurements isolate inductive reactance.
- Open circuit impedance measurements isolate capacitive reactance.
- Through measurements (perfect 50Ω load) are used for transmission and reflection parameters.
- Impedance is calculated directly from reflection response (S_{11} Parameter data).
- Crosstalk S_{31} responses are used to derive coupling parameters (mutual inductance and coupling capacitance).

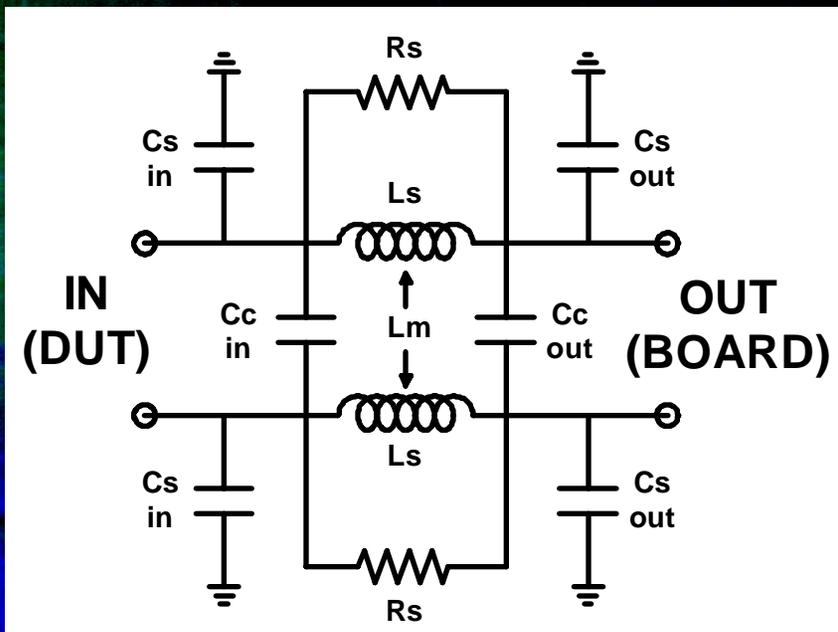
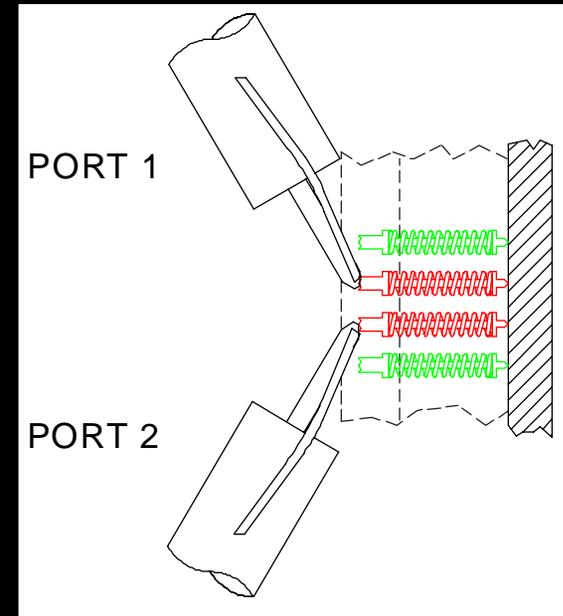


$$Z_{OPEN} = \frac{1}{G_{OPEN} + j\omega C_{OPEN}}$$

$$Z_{SHORT} = R_{SHORT} + j\omega L_{SHORT}$$

SPICE Model Topology

- Model topology is based on actual crosstalk test configurations - both area array and peripherally-leaded configurations are covered.
- High frequency effects of inductors are accounted for with parallel resistances.
- Some contactors may not be symmetric on input and output sides (QFP type, elastomer type).



L_s - Series Inductance (nH)

C_s - Shunt Capacitance (pF)

$$= C_{s\ in} + C_{s\ out}$$

L_m - Mutual Inductance (nH)

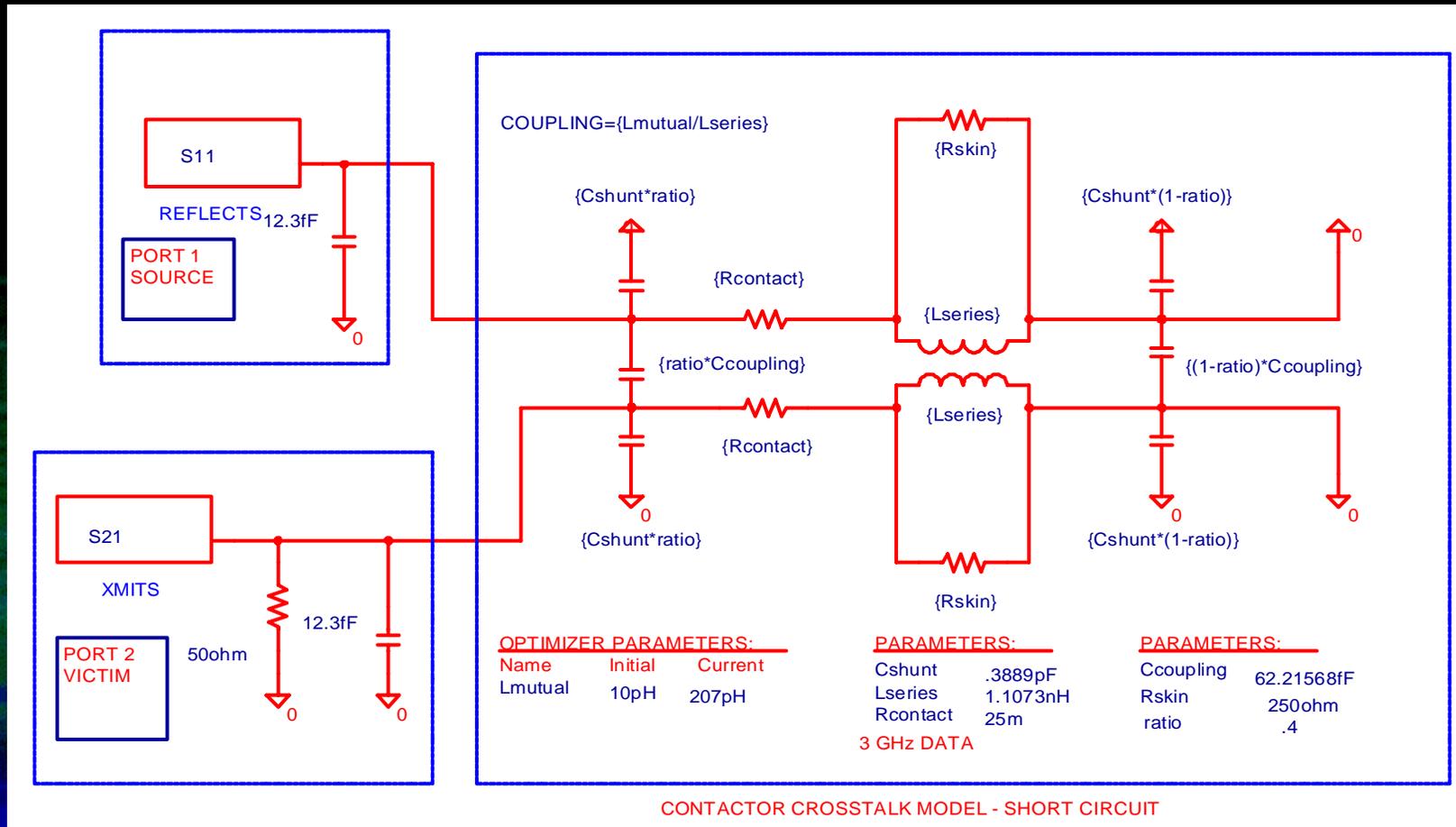
C_c - Coupling Capacitance (pF)

$$= C_{s\ in} + C_{s\ out}$$

R_s - High Frequency Loss (Ω)

SPICE Model for Short Circuit Crosstalk Measurement

- Both source and victim ports are terminated on the same side
- Circuit other end is shorted to ground



SPICE Model Parameter Extraction

- R_{contact} is not used.
- C_{shunt} and L_{series} are derived from S_{11} measurements on single contact pins.
- L_{mutual} and C_{coupling} can be derived using an iterative technique, fitting open circuit and short circuit crosstalk (S_{31}) data until both conditions are completely satisfied.
- R_s can be estimated or derived empirically.
- If contactor is not balanced on the board and DUT side, C_{shunt} and C_{coupling} must be split, fitting to the open circuit crosstalk response.

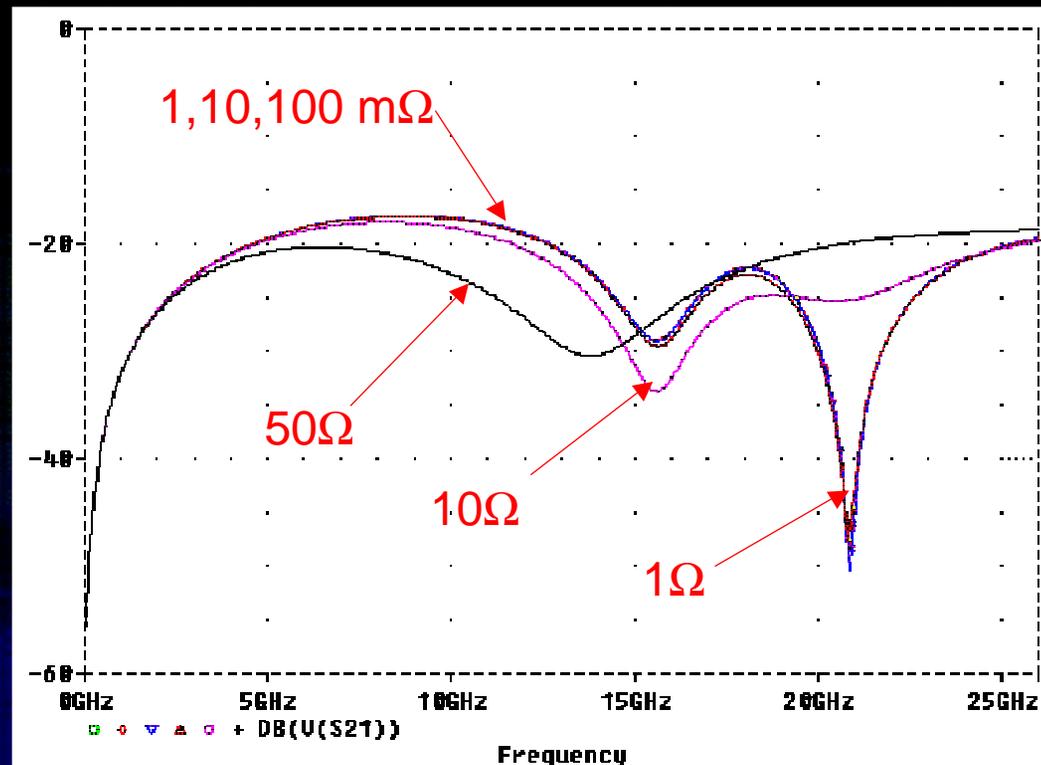


DC Contact Resistance - Is it Needed in SPICE?

- DC contact resistance only is significant in contactor SPICE models when $> 1\Omega$.
- Consider adding contact resistance in the total system model - it may interact with other active components in the simulation.

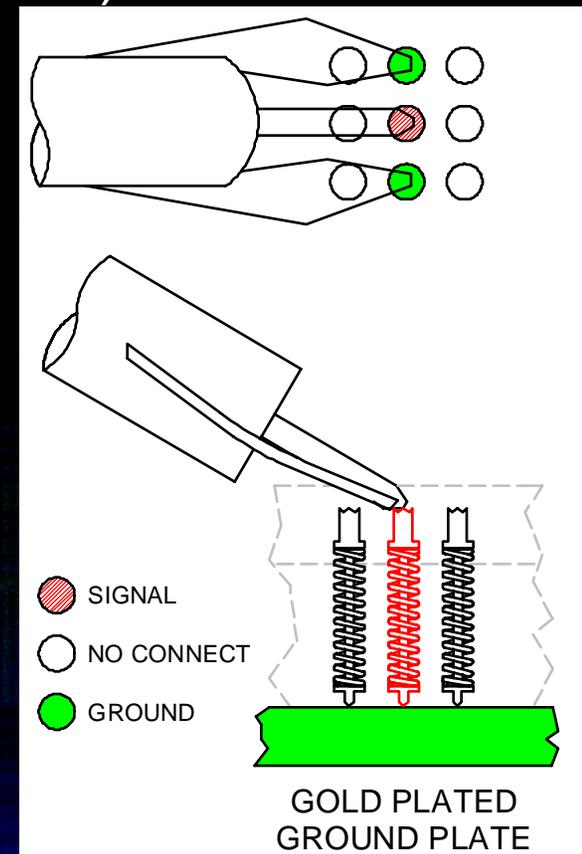
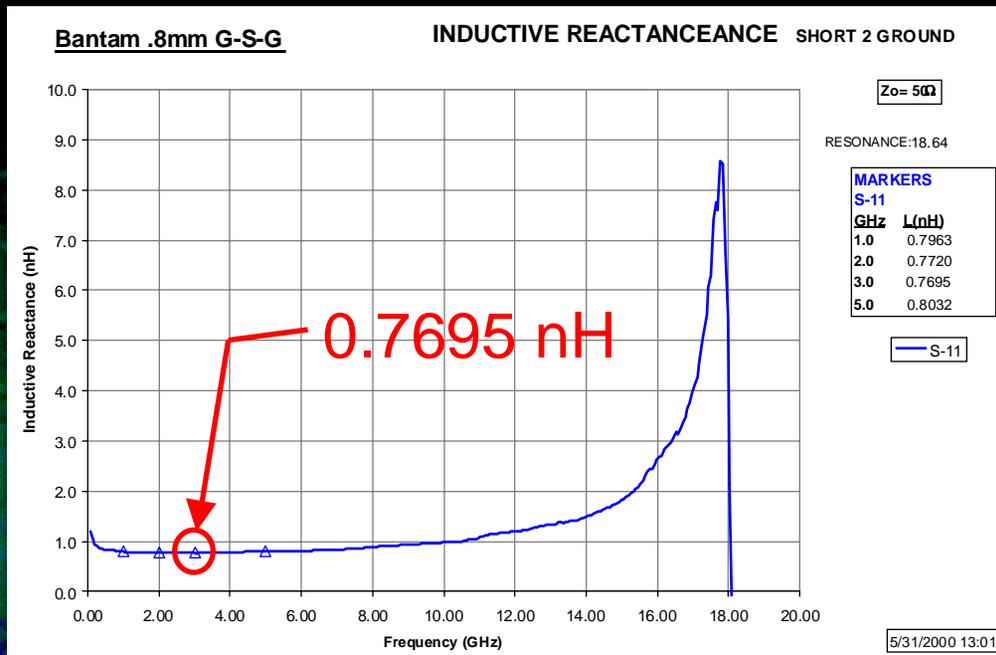
Example:

Open circuit S_{21}
crosstalk model
simulation - R_{contact}
varies from $1\text{ m}\Omega$ to
 50Ω .



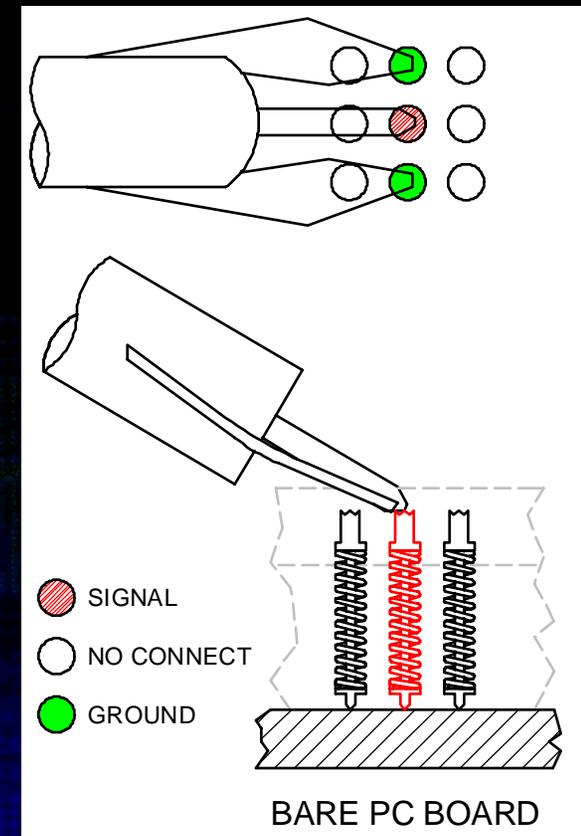
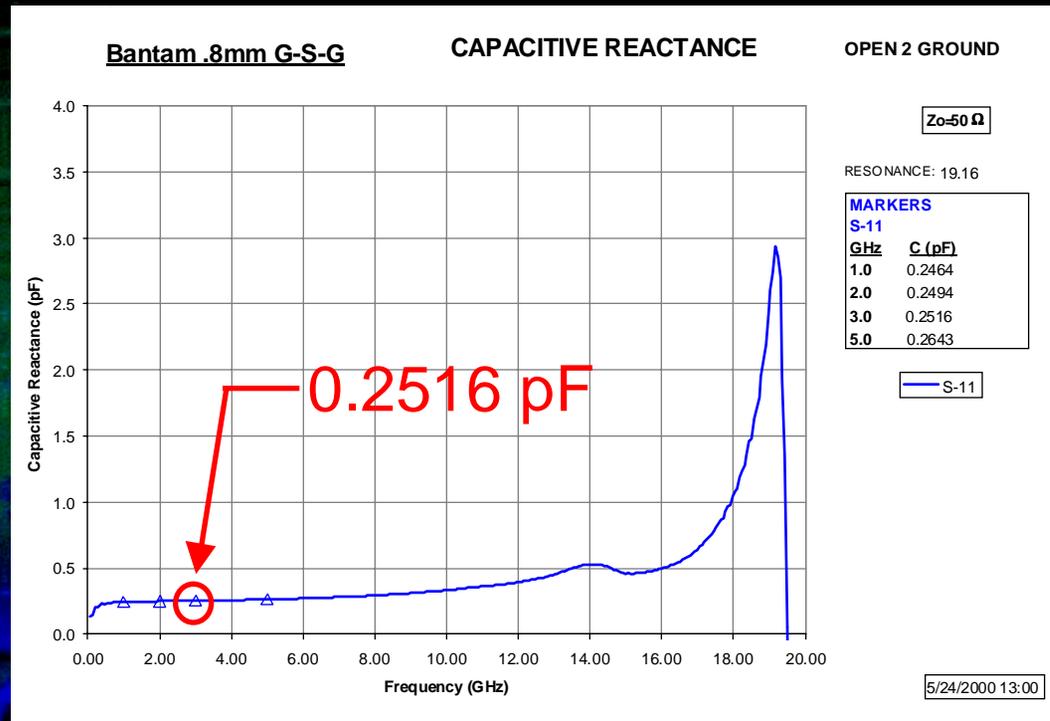
LS - Series Inductance Extraction

- Short circuit S_{11} is measured on a single pin as shown.
- Series inductance is selected at a 'typical' frequency point on derived reactance plot (example 3 GHz).



Cs - Total Shunt Capacitance Extraction

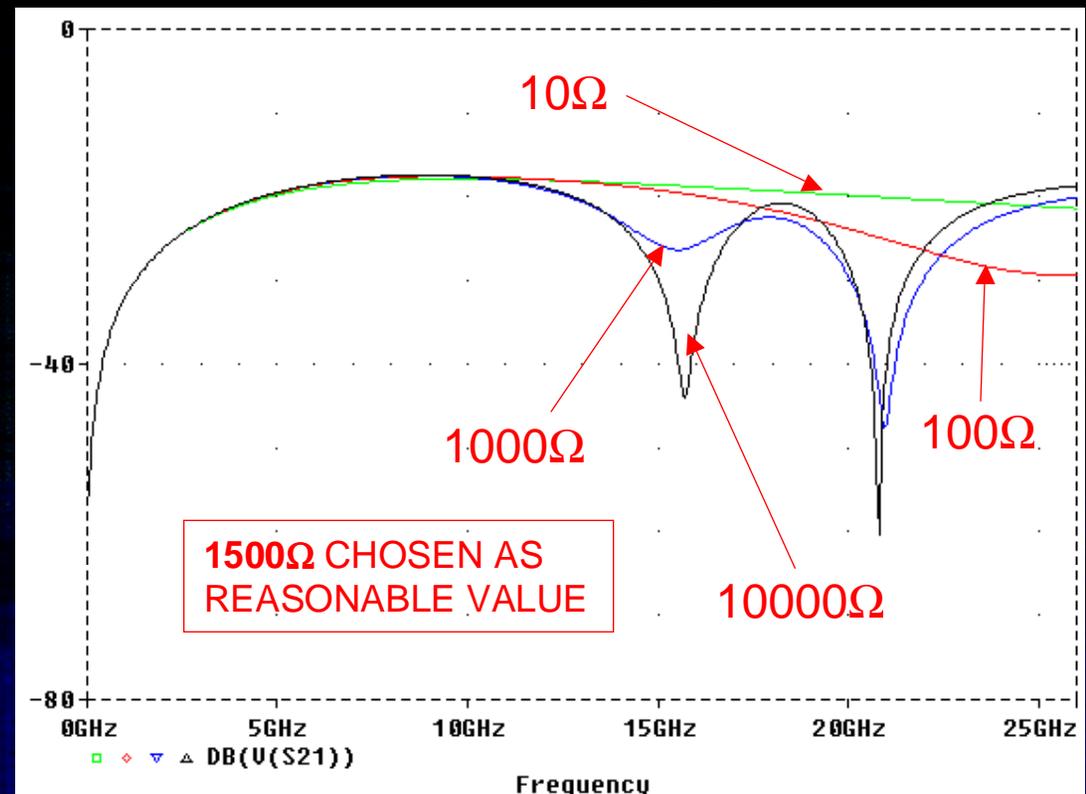
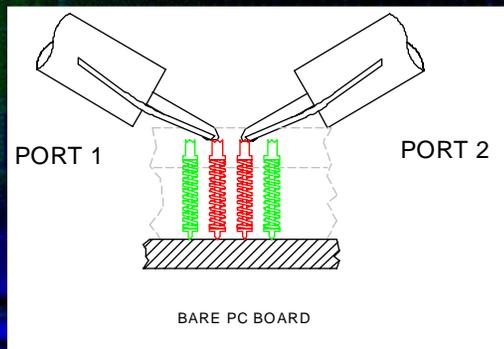
- Open circuit S_{11} is measured on a single pin as shown.
- Shunt capacitance is selected at a 'typical' frequency point on derived reactance plot (example 3 GHz).
- Cs is split: $C_s = C_{sin} + C_{sout}$. Ratio can be determined along with Cc extraction.



Rs - Resistive Loss

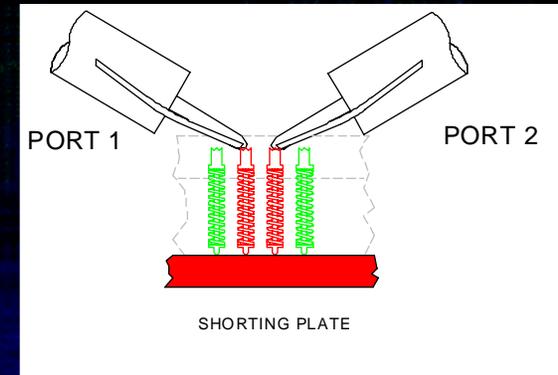
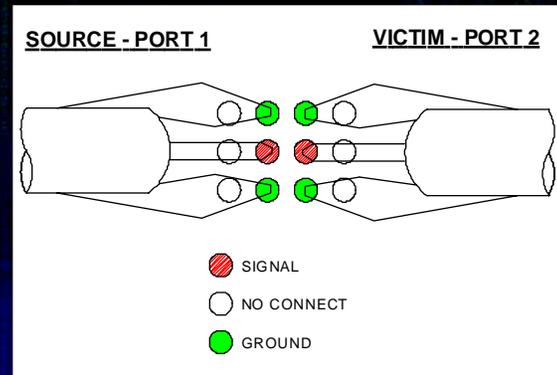
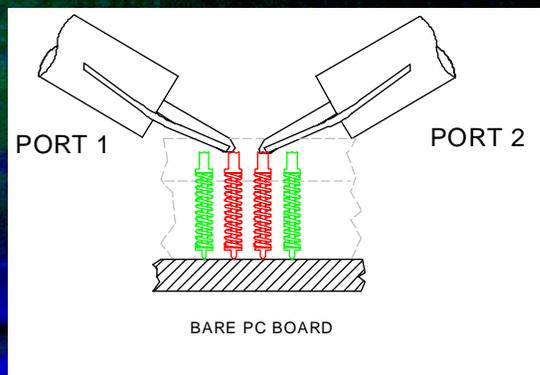
- A resistor is added in parallel with an inductor to correctly model the behavior of a 'perfect' inductor at higher frequencies ($> 1\text{GHz}$).
- R_s is approximately the impedance (Z) of the inductor L_s at the frequency which Q begins to roll off.
- R_s can be estimated by fitting the model response curves, and watching for similar resonance patterns of the actual S_{31} crosstalk responses.
- Changes in R_s at lower frequencies have almost no effect on response.

Example: Open circuit S_{21} crosstalk model simulation, R_s varies from $10\ \Omega$ to $10\text{K}\Omega$.



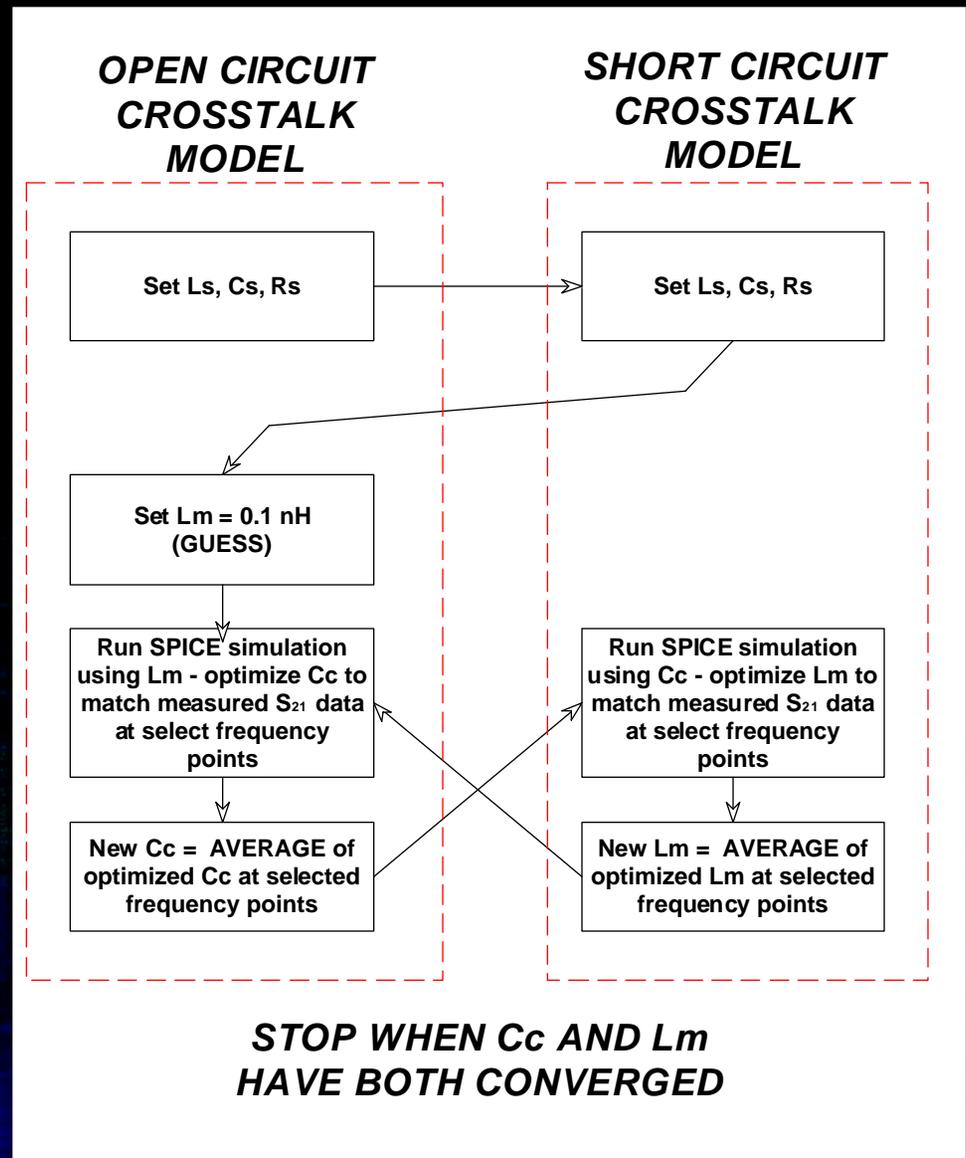
Cc and Lm - Coupling Capacitance and Mutual Inductance Extraction

- Lm and total Cc can be solved by fitting the SPICE model responses of open circuit and short circuit S_{31} data to measured crosstalk curves.
 - Ls and Cs are derived as presented earlier and loaded into each model (open and short crosstalk).
 - Rs should be set for high frequency performance.
 - In the open circuit crosstalk model, set Lm equal to 0.1 nH (initial guess)
 - $C_{s_{in}}$ and $C_{s_{out}}$ should be split evenly, as should $C_{c_{in}}$ and $C_{c_{out}}$
 - Alternate solving for either Lm or Cc, substituting the results of one simulation into the other until both values converge



Solving for L_m and C_c

- Simulation frequency values for optimization should be selected for the expected operating frequency of the contactor.
- Three or four points are usually adequate.
- Optimization usually converges to 2 decimal place accuracy (nH and pF) after two iterations.
- If convergence does not happen, vary $C_{s_{in}}/C_{s_{out}}$ ratio, try again.



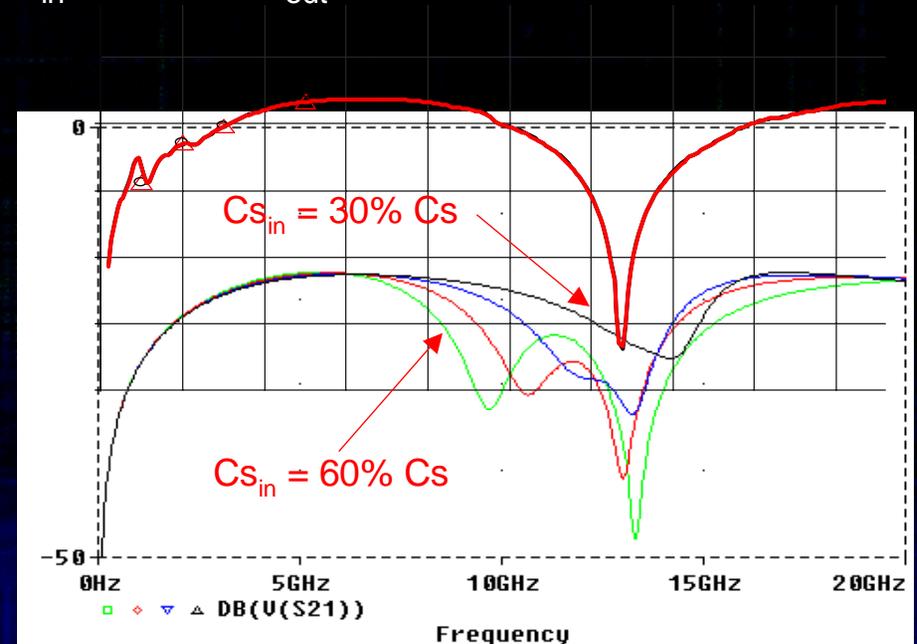
Splitting C_s and C_c

- Consider the contactor 'balance' in its construction:
 - Is the DUT or board side more capacitive?
 - Sometimes a TDR plot can help.
- Sweep the weighted C_s from 30-70% on each side of the model. Fit the open circuit crosstalk model to the actual data. Look at the higher frequency range for the curve resonances.
- Use the same split ratio for $C_{c_{in}}$ and $C_{c_{out}}$.

Example: Open circuit S_{21} crosstalk model simulation of elastomer based contactor - C_{sin} varies from 20%-80% of C_s .

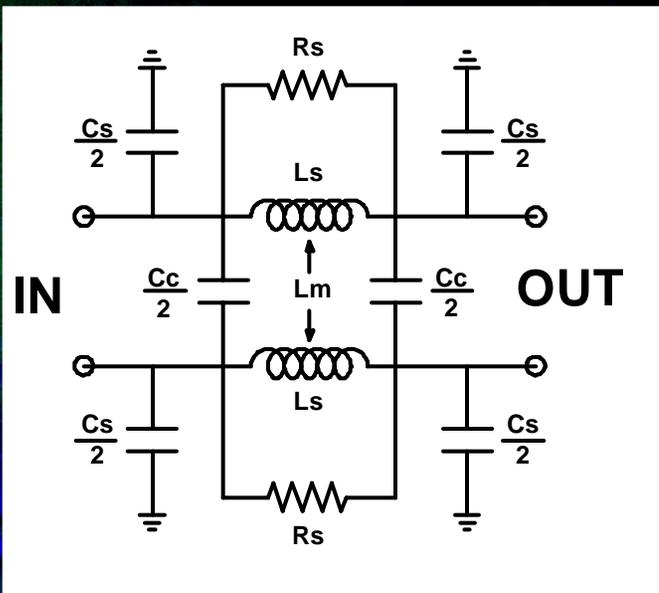
$$(C_s = C_{s_{in}} + C_{s_{out}})$$

Result: C_{sin} best fits 40% C_s



Example Solution - ECT 0.8mm Bantam-Pak[®] Test Contactor

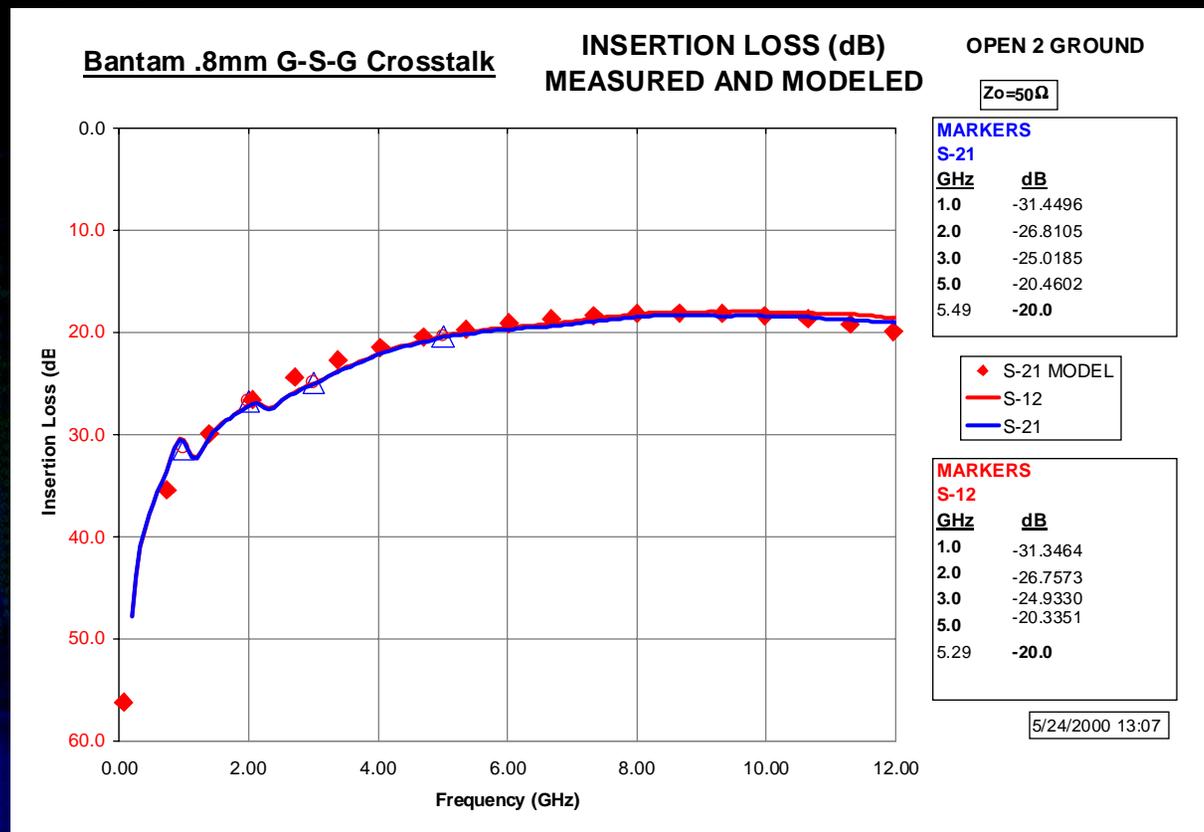
- The following frequency points were used for model fitting:
 - 3 GHz for L_s and C_s from S_{11} open and short data.
 - 1,3, 5, 8, 12 GHz for L_m and C_c for S_{21} open and short crosstalk data.
 - R_s was optimized with all other parameters fixed .
 - Contactor fairly balanced, C_c and C_s are equal on both input and output sides (50%).



L_s	Series Inductance	0.77 nH
C_s	Shunt Capacitance	0.25 pF
C_c	Coupling Capacitance	0.04 pF
L_m	Mutual Inductance	0.10 nH
R_s	Resistive Loss (high frequency effect)	1500 Ω

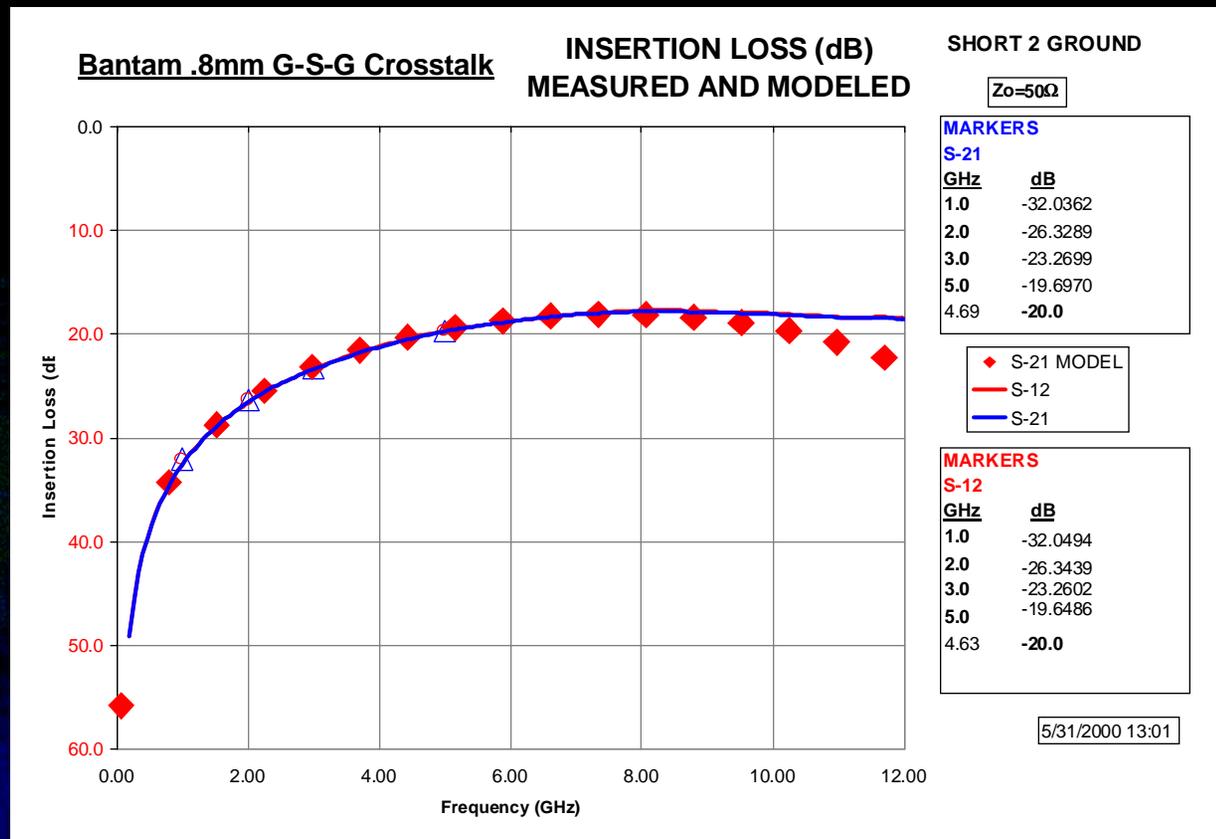
Example Results - Open Circuit Model and Actual Response

- Open circuit model response agrees to 2% of actual measured response up to -1db S_{21} bandpass frequency.
- Model only deviates from measured response at highest frequencies.



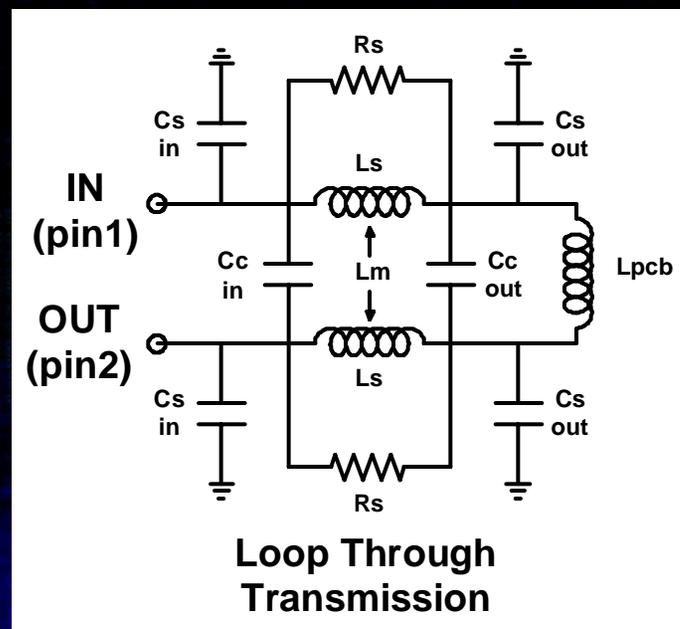
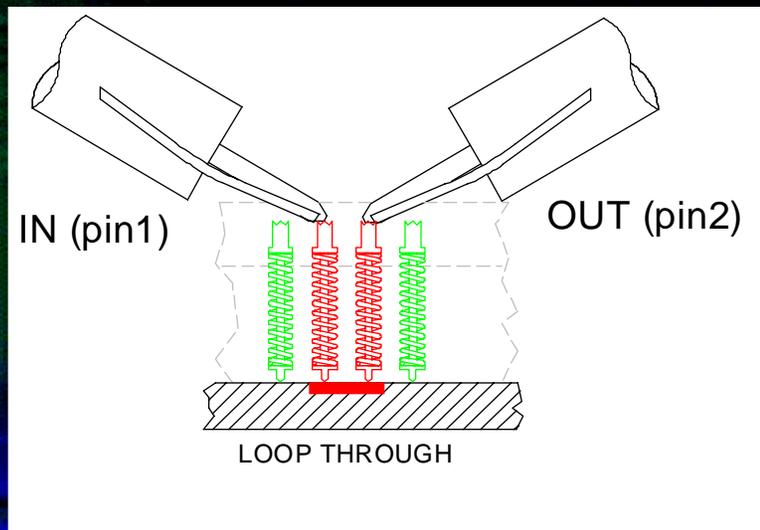
Example Results - Short Circuit Model and Actual Response

- Short circuit model response agrees to 2% of actual measured response up to -1db S_{21} bandpass frequency
- Model only deviates from measured response at highest frequencies



S_{21} in SPICE Models - Loop Through

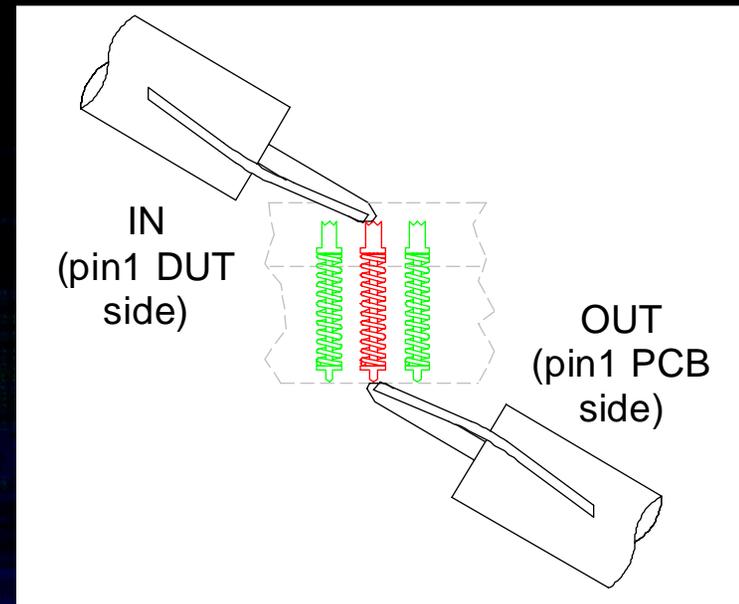
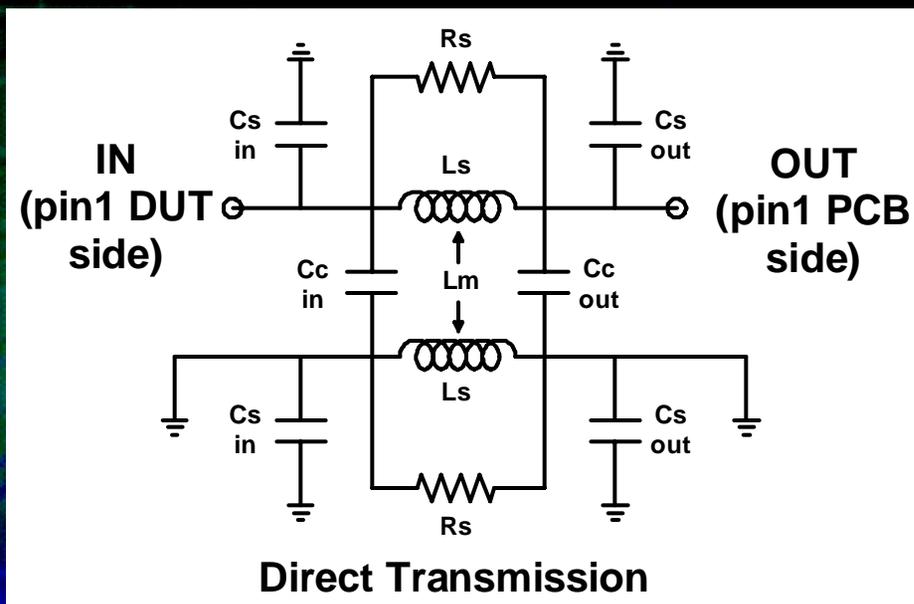
- Loop through S_{21} measurements
 - Measure the response of two adjacent contacts and a surrogate PC board trace, including coupling.
 - Inductance of PC board must be included.
 - Shunt capacitance must be included in model.
- Most common way to report insertion loss and bandwidth.



S_{21} in SPICE Models - Direct Measurement

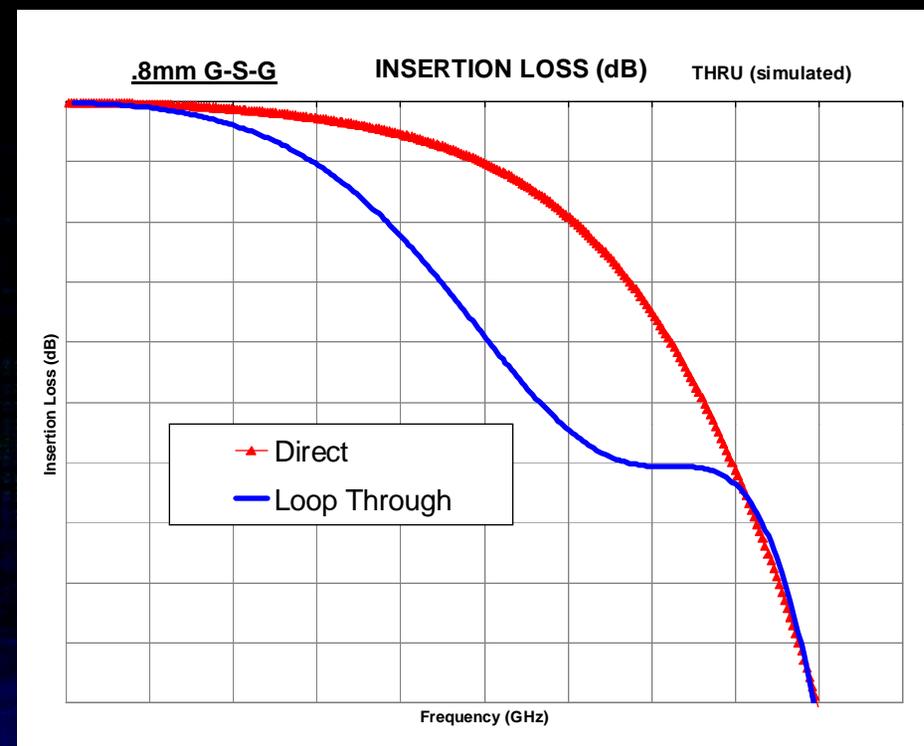
■ Direct S_{21} Measurements

- Measure transmission loss of a single pin configuration.
- Adjacent pin must be grounded or terminated.
- PC board not used in measurement.



S_{21} in SPICE Models - Comparison

- Loop through response can differ from direct response
 - More than double the inductance of a single pin.
 - Coupling effects induce more of a complex response.



Benefits of this Modeling Technique

■ Accurate:

- Measurements are very repeatable.
- Parasitics from PC boards and surrogates are eliminated.

■ Simple to do:

- Coplanar probes and standards available 'off the shelf'.
- No custom PC boards or surrogate devices need to be designed - open and short structures are simple and uniform from test to test.

■ Cost effective:

- All data manipulation and optimization can be done in Excel and freeware P-SPICE. - expensive modeling software is not required.
- Data acquisition is not needed - raw VNA floppy disk data is used.

■ Fast:

- Probing and fixturing is easy to set up.
- Only 2 data sweeps are required in 2 probe-pair touchdowns for area array contactors for each pin-pair configuration. A third sweep adds all S_{21} data (Attenuation, Return loss, BW, delay, phase, etc.)



References / Bibliography

- M. Honda: *The Impedance Measurement Handbook*, Hewlett-Packard 1989
- *Understanding the Fundamental Principles of Vector Network Analysis*, Hewlett-Packard, Application Note 1287-1
- *Obtain S-Parameter Data from Probe*, MicroSim design Source Newsletter, April 1994
- *S-Parameter Techniques for Faster, More Accurate Network Design*, Hewlett-Packard, Application Note 95-1
- *8 Hints for Making Better Network Analyzer Measurements*, Hewlett-Packard Application Note 1291-1
- David Ballo: *Network Analyzer Basics*, from 'Back to Basics Seminar', Hewlett-Packard 1998
- David Dascher: *Measuring Parasitic Capacitance and Inductance Using TDR*, Hewlett-Packard Journal, 1996
- *Gaining the Wireless Edge*, Agilent Technologies
- Various WWW resources



Least Squares Analysis of Composite True Position Specification

2001 Burn-in and Test Socket Workshop



Alex Owen
WELLS-CTI

Composite TP specification

- **Feature relationship with :**
 - External set of datums
 - To the pattern formed by the features themselves

Where is the pattern?

- **By definition, cannot determine pattern location until features are measured**
- **Once measured, the “best fit” pattern location is established.**
- **“Best Fit” is defined as placement of pattern to minimize variance to nominal**

Least squares analysis

- **Assuming:**
 - **Process metric exhibits normally distributed random variation about a mean**
- **Then:**
 - **Distribution of difference between actual and nominal is characterized thru variance**
- **Therefore:**
 - **Adjusting position and orientation of the pattern to minimize the sum of the squares of difference between measured and nominal will minimize the variance of the final error terms**

Least squares analysis (cont)

- **Given :**
 - Set of feature location measurements
 - Set of corresponding specified nominal locations
- **Determine:**
 - Adjustments to the location and orientation of the nominal pattern so as to minimize “total error”

Derivation - Step 1

- **Define:**
 - Y_{mi}, X_{mi} = Measurement in Y, X direction
 - Y_{bi}, X_{bi} = Basic specification in Y,X direction
 - Y_{ci}, X_{ci} = Y_{mi}, X_{mi} measurement transformed to best fit grid location
 - Y_0, X_0 = Translation of best fit grid relative to measurement grid
 - Θ = Rotation of best fit grid from measurement grid

Derivation - Step 1 (cont)

$$XM_i = X0 - YC_i * \sin \theta + XC_i * \cos \theta$$

$$YM_i = Y0 + YC_i * \cos \theta + XC_i * \sin \theta$$

⇒

$$XC_i = (XM_i - X0) * \cos \theta + (YM_i - Y0) * \sin \theta$$

$$YC_i = (YM_i - Y0) * \cos \theta - (XM_i - X0) * \sin \theta$$

Derivation - Step 2

- Define total error term
- Take partial derivative with respect to adjustment parameters
- Establish values required to minimize error

Derivation - Step 2 (cont)

$$\varepsilon = \sum_{i=1}^N \left[(XC_i - XB_i)^2 + (YC_i - YB_i)^2 \right]$$

Find $\frac{\partial \varepsilon}{\partial X_0}$, $\frac{\partial \varepsilon}{\partial Y_0}$, $\frac{\partial \varepsilon}{\partial \theta}$

set equal to 0

solve for X_0 , Y_0 , θ

Derivation - Step 2 (cont)

$$X_0 = \frac{\sum_{i=1}^N X_{Mi} - \cos \theta * \sum_{i=1}^N X_{Bi} + \sin \theta * \sum_{i=1}^N Y_{Bi}}{N}$$

$$Y_0 = \frac{\sum_{i=1}^N Y_{Mi} - \sin \theta * \sum_{i=1}^N X_{Bi} - \cos \theta * \sum_{i=1}^N Y_{Bi}}{N}$$

$$\theta = a \tan \frac{\sum_{i=1}^N X_{Bi} * Y_{Mi} - \sum_{i=1}^N X_{Mi} * Y_{Bi} - \frac{\left[\sum_{i=1}^N X_{Bi} * \sum_{i=1}^N Y_{Mi} - \sum_{i=1}^N X_{Mi} * \sum_{i=1}^N Y_{Bi} \right]}{N}}{\sum_{i=1}^N X_{Bi} * X_{Mi} + \sum_{i=1}^N Y_{Bi} * Y_{Mi} - \frac{\left[\sum_{i=1}^N X_{Bi} * \sum_{i=1}^N X_{Mi} + \sum_{i=1}^N Y_{Bi} * \sum_{i=1}^N Y_{Mi} \right]}{N}}$$

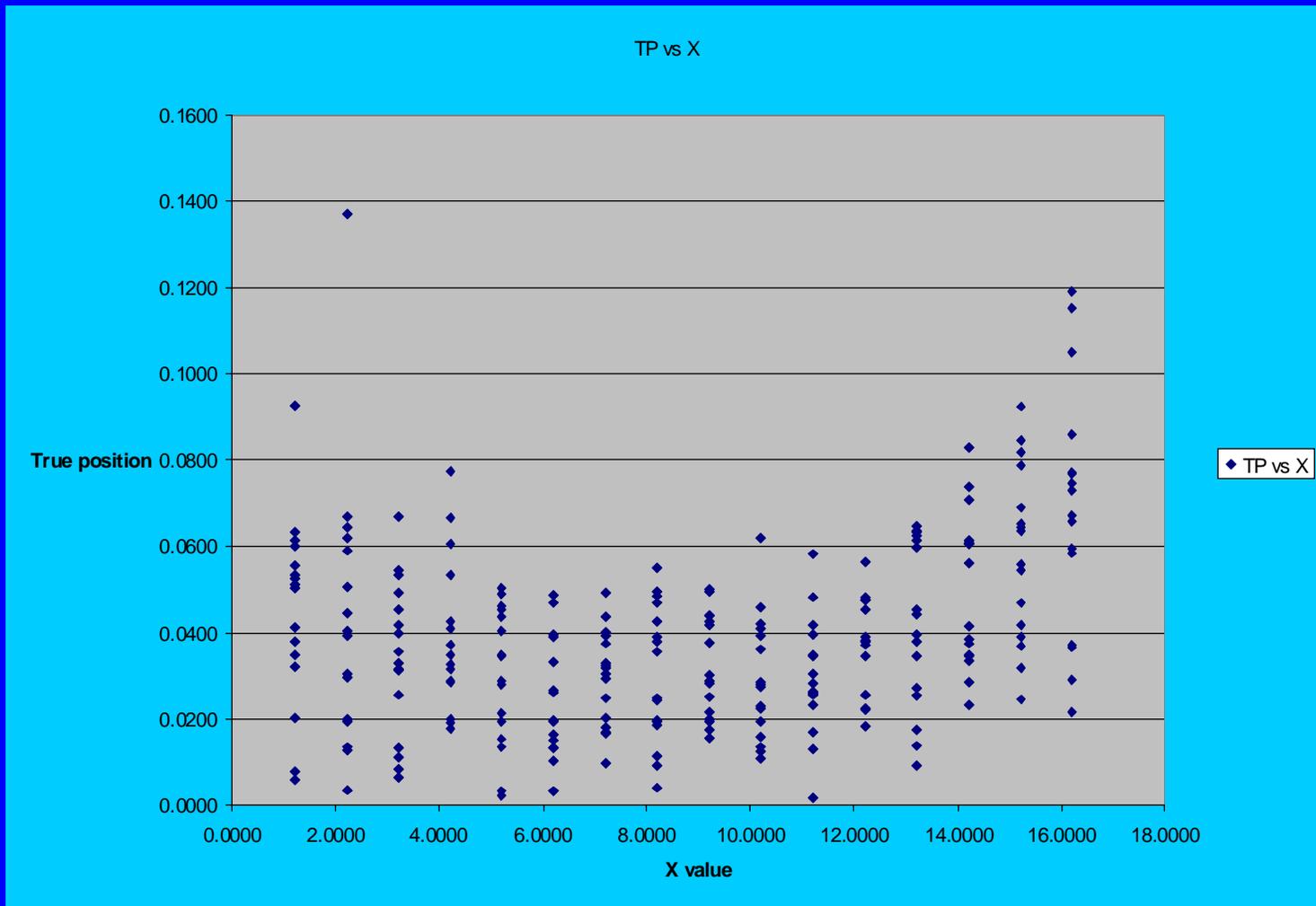
Spread sheet - set up

X_B	Y_B	X_M	Y_M	X_C	Y_C	$X_B * Y_M$	$X_M * Y_B$	$X_B * X_M$	$Y_B * Y_M$	X error	Y error	TP
$\sum X_B$	$\sum Y_B$	$\sum X_M$	$\sum Y_M$			$\sum X_B * Y_M$	$\sum X_M * Y_B$	$\sum X_B * X_M$	$\sum Y_B * Y_M$			

Example Data analysis

- Grid matrix part to engage 256 position BGA package on 1.0 mm pitch
- Data taken with View machine
- Example graphs of error vs position
- $X_0 = 0.115$
- $Y_0 = 0.124$
- $\text{Theta} = -0.013$ degrees

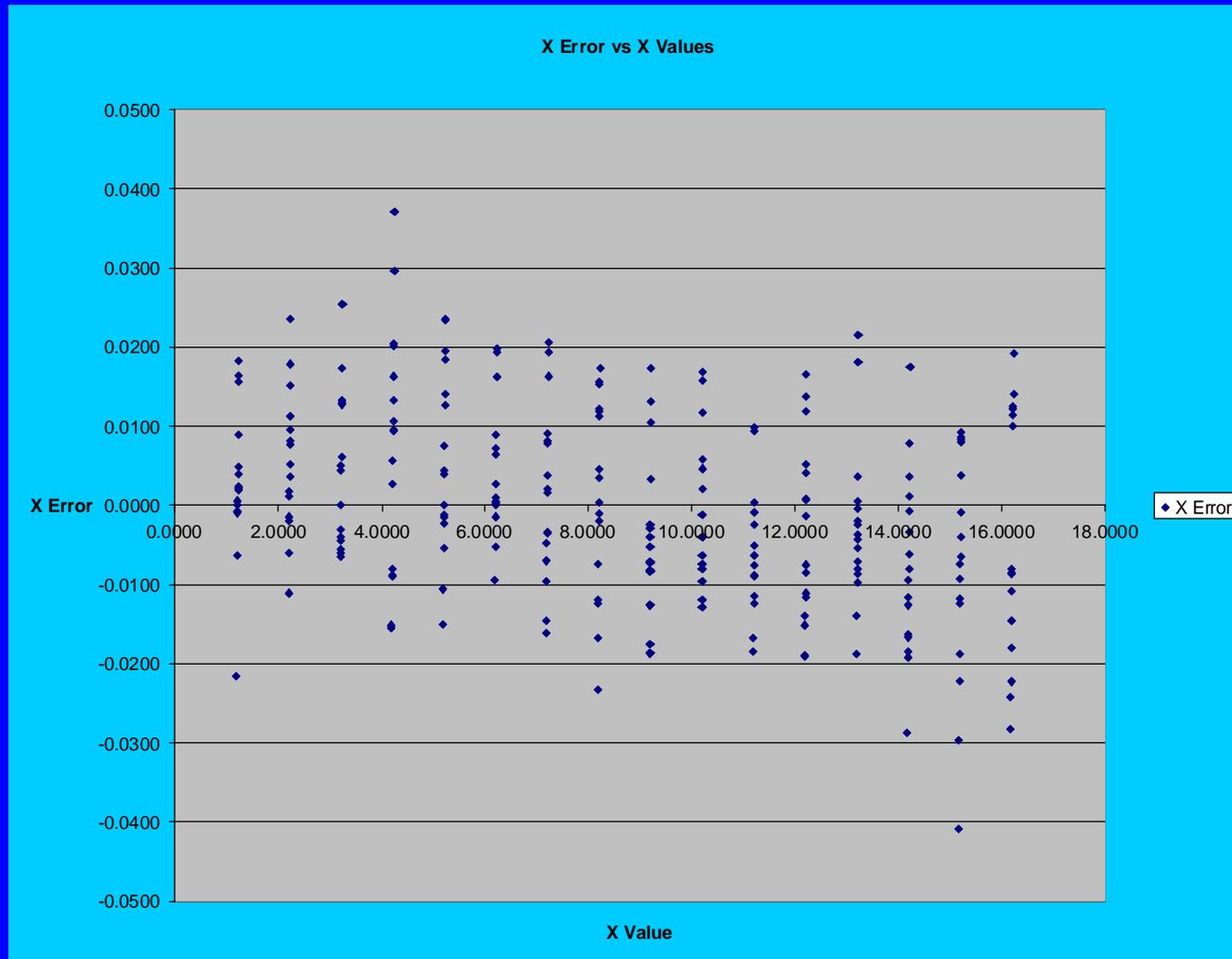
TP vs X Value



TP vs X Value

- Determine if pattern TP requirements met
- Deviation tends to increase at either end of part

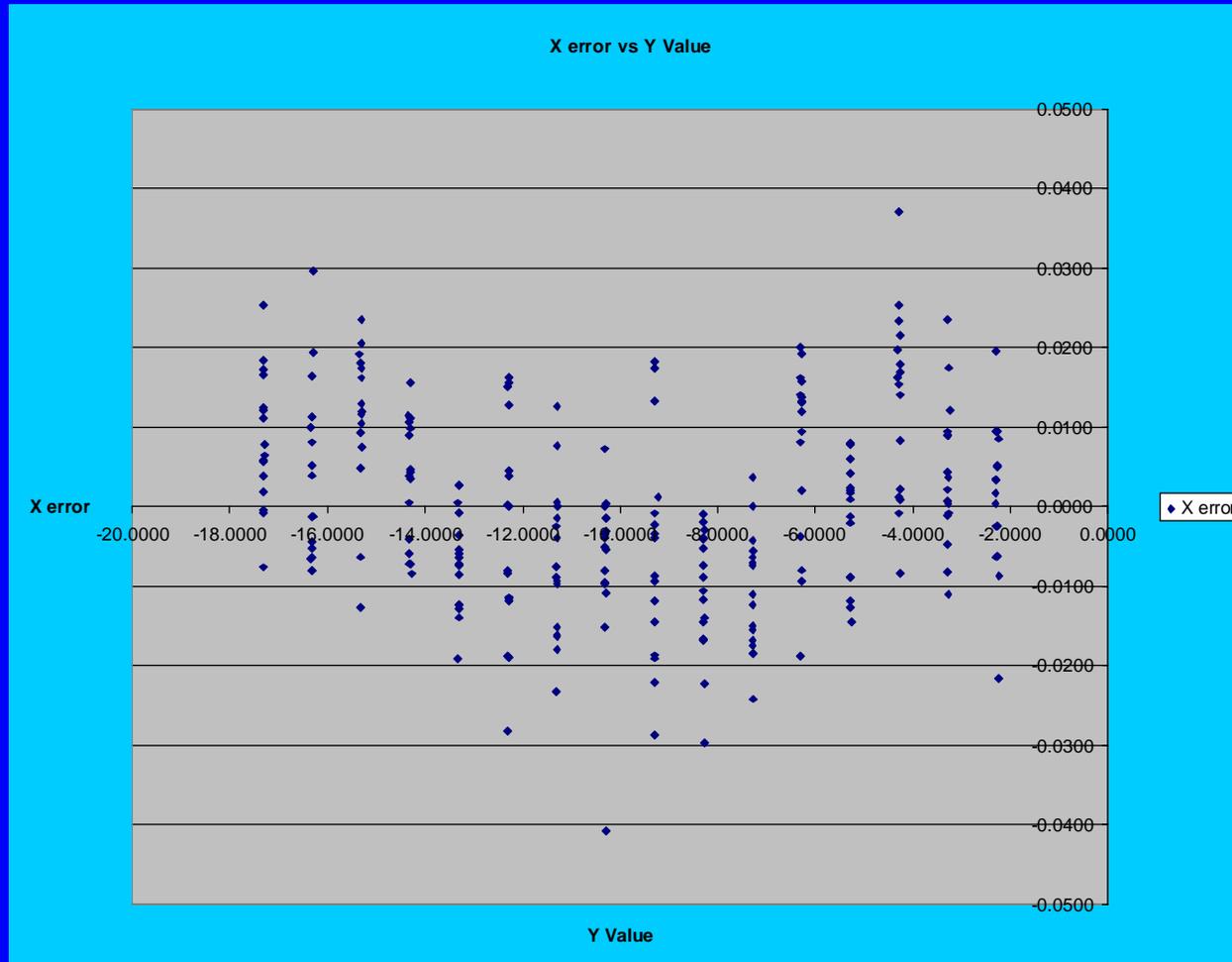
X error vs X Values



X error vs X Values

- Grid may be slightly oversized in X direction
- May need to alter gating/process/material parameters to correct

X error vs Y Values



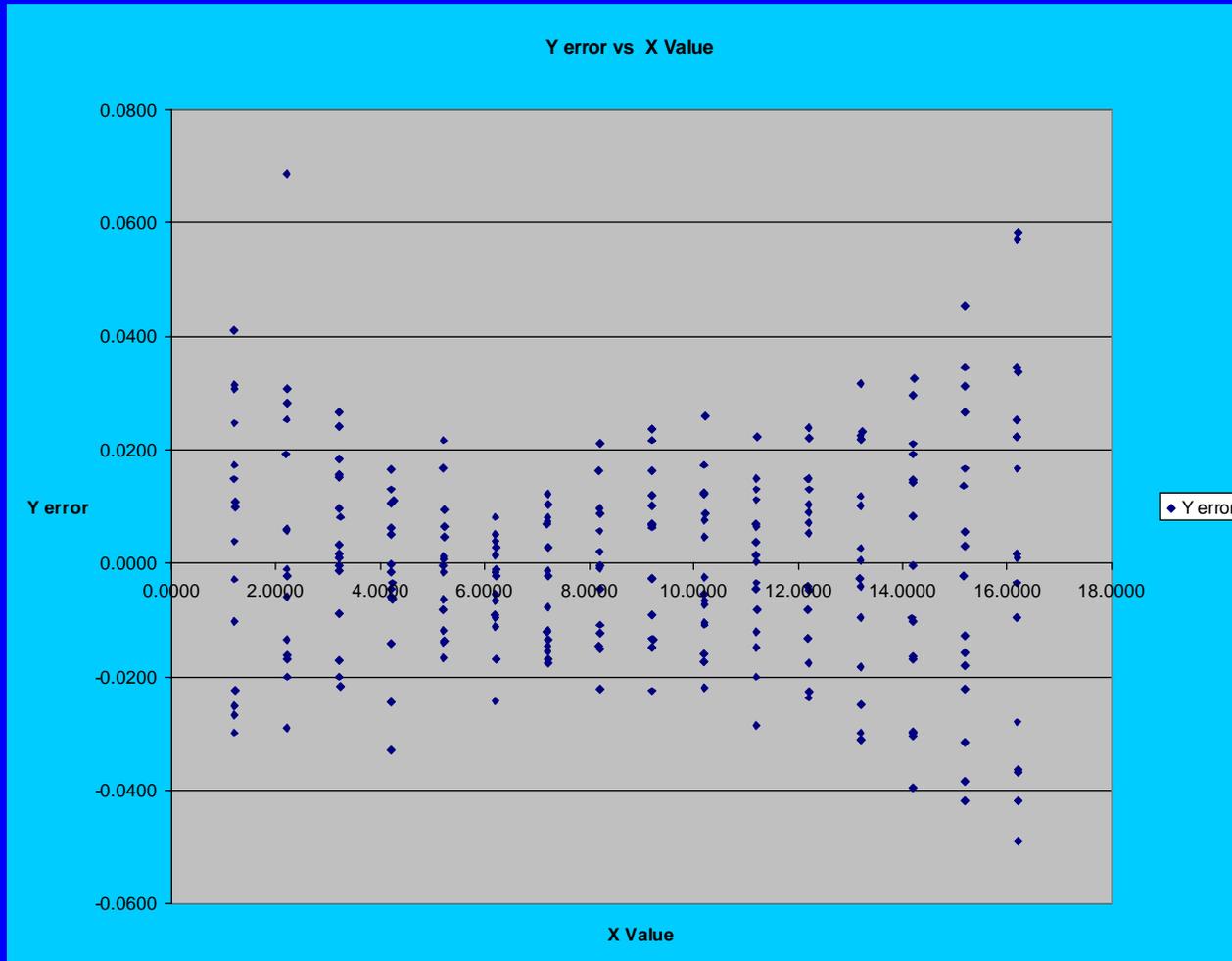
X error vs Y Values

- Differential shrink transverse to X direction
- May need to alter gating/process/material parameters

Y error vs Y Values

- Part oversized in Y direction
- More pronounced than in X direction
- May need to alter process parameters to correct

Y error vs X Values



Y Error vs X values

- Fairly well centered about mean
- Increase variation at ends could be due to other issues identified

Indicated Actions

- Investigate outliers
- Correct differential shrinkage in X and Y direction
- Re-measure part from new process
- Make steel corrections as indicated
- Verify part

Conclusions

- **Permits repeatable measurement**
- **Removes operator dependency on set up**
- **Measurement and reporting automated**
- **Support systematic issue identification and resolution**