Burn-in & Test Socket Workshop

March 4 - 7, 2001
Hilton Mesa Pavilion Hotel
Mesa, Arizona

IEEE

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Technical Program

Session 2
Monday 3/05/01 10:30AM

<u>Directions In Test Socketing</u>

"Spring Contact Probes For IC Device Testing"
Tim Dowdle – Synergetix

"Strip Test - Evolution, Considerations And Resources"
Brian Crisp - Everett Charles Technologies

"Lowering The Cost Of High Performance Test And Burn-in"
James Rathburn – Gryphics, Inc.

Spring Contact Probes for IC Device Testing

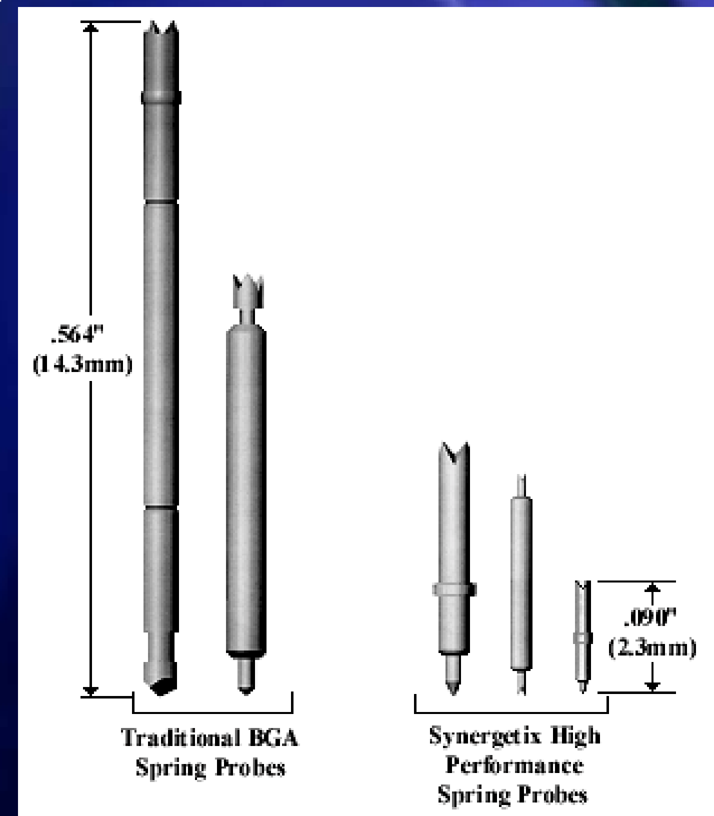
Presented by
Tim Dowdle

Proven Spring Contact Probe Simplifies Testing of IC Devices

- True Vertical Probing
- Customizable Geometry
- Ease of Manufacture
- Cost Effective
- Extreme Duty Capable

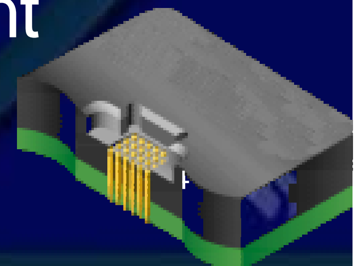
Disproving the Myth

- Long signal path length and high inductance spring contact probes do not make the optimum test socket contact.
- Test engineers were forced to build their own sockets borrowing a readily available technology.
- Spring contact probes originally designed for *printed circuit board* (PCB) testing fill the need.



Disproving the Myth

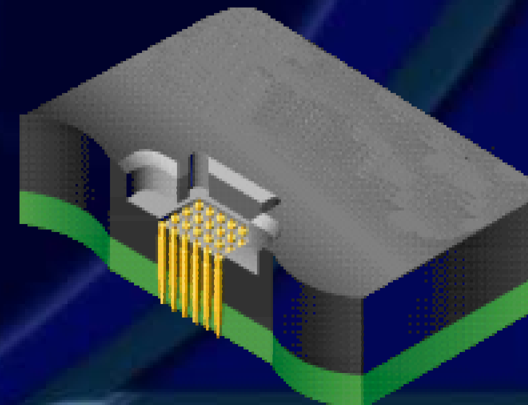
- The PCB probe commonly used in the past cannot support the testing requirements for the new generation of fine-pitch, high-speed devices, such as BGA and CSPs.
- Miniaturization down to .25mm (.010”) and test speeds well above 1GHz, drive manufacturers to develop contact designs which meet ultra-fine pitch requirements.
- By reducing size and length of the spring contact probe, it becomes essentially transparent in the electrical test path maintaining low, consistent contact resistance.



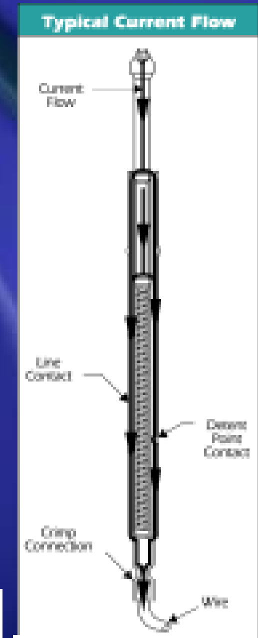
IDI

Spring Contact Probe Features

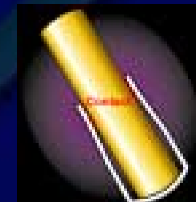
- Vertical probing motion.
- DUT board design is a true reflection of the device lead pattern.
- Spring probes are retained in test sockets with drilled holes offering unlimited capacity to customize sockets for specific applications.



Spring Contact Probe Features



- Gold plated crimped outer barrel, inner spring, with either one or two plungers.
- The spring is designed so that a “biasing” effect is created inside the barrel, forcing the plungers against the inner surface of the barrel.
- Utilizing this biasing feature, current flow follows a *plunger*–*barrel*–*plunger* path keeping the spring out of the conductive path.
- Reliable contact force and electrical performance in temperature extremes from 50°C to 150°C.



Reduced Cost of Ownership

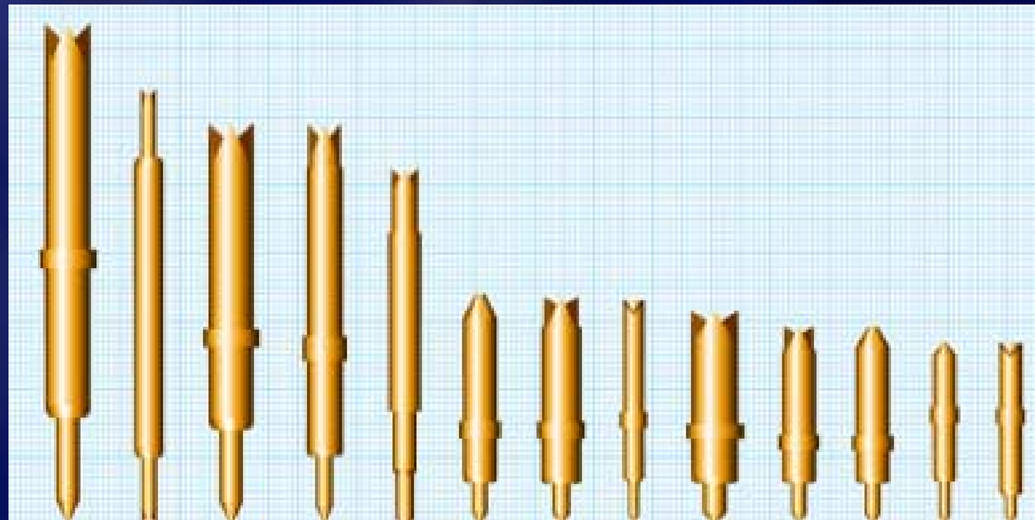
- When refurbishment is required the use of individual, self-contained contacts simplifies field replacement of a single contact or the entire array.
- High cycle life and easy refurbishment capability ***reduce the overall cost of ownership***.
- The spring contact probe allows versatility within the same test socket for use in automated test, engineering characterization, and custom burn-in tests.

Design Flexibility and Quality Management

- Socket manufacturers are dependent upon purchasing their contact technology from an outside supplier. Consequently, they are forced to develop the socket design around the existing features of that technology.
- Socket manufacturers who design and build their contact technology in house have a definite advantage.

Design Flexibility and Quality Management

- Device manufacturers are developing new CSP, BGA, LGA, and peripheral packages at a dizzying pace.
- Due to the variables involved in each package design and test methodology, a single spring contact probe will not be effective in every application.



Optimal Device Test Conditions

- High contact forces are becoming a critical concern for BGA devices.
- The contact force of the spring probe can easily be redesigned to avoid extreme forces in the handler and minimize the pressure against the devices and the DUT board, while maintaining the electrical and mechanical integrity.

Optimal Device Test Conditions

- BGA devices with a .5mm diameter solder ball on .8mm pitch may use a different spring contact probes than a device with a .75mm diameter solder ball on 1.27mm pitch.
- The probe tip will utilize a 4-point crown or other tip style to push the contact area away from the center of the ball. This will allow the probe tip to contact only the outer periphery of the ball avoiding all contact with the central keep-out area.

SEBM photo of witness marks left on a .75mm diameter ball using a four point crown tip style.

Optimal Device Test Conditions

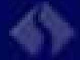
- It is imperative to use varying probe tip diameters and spring forces to achieve proper ball fit for each device under test.
- Factors involved in the selection of the contact are lead pitch, lead type, solder ball diameter, number of leads, available insertion force of the handling system, and rigidity of the DUT board.
- The spring contact probe offers many variable design factors that can be customized to improve the performance of the test socket.

Electrical Performance

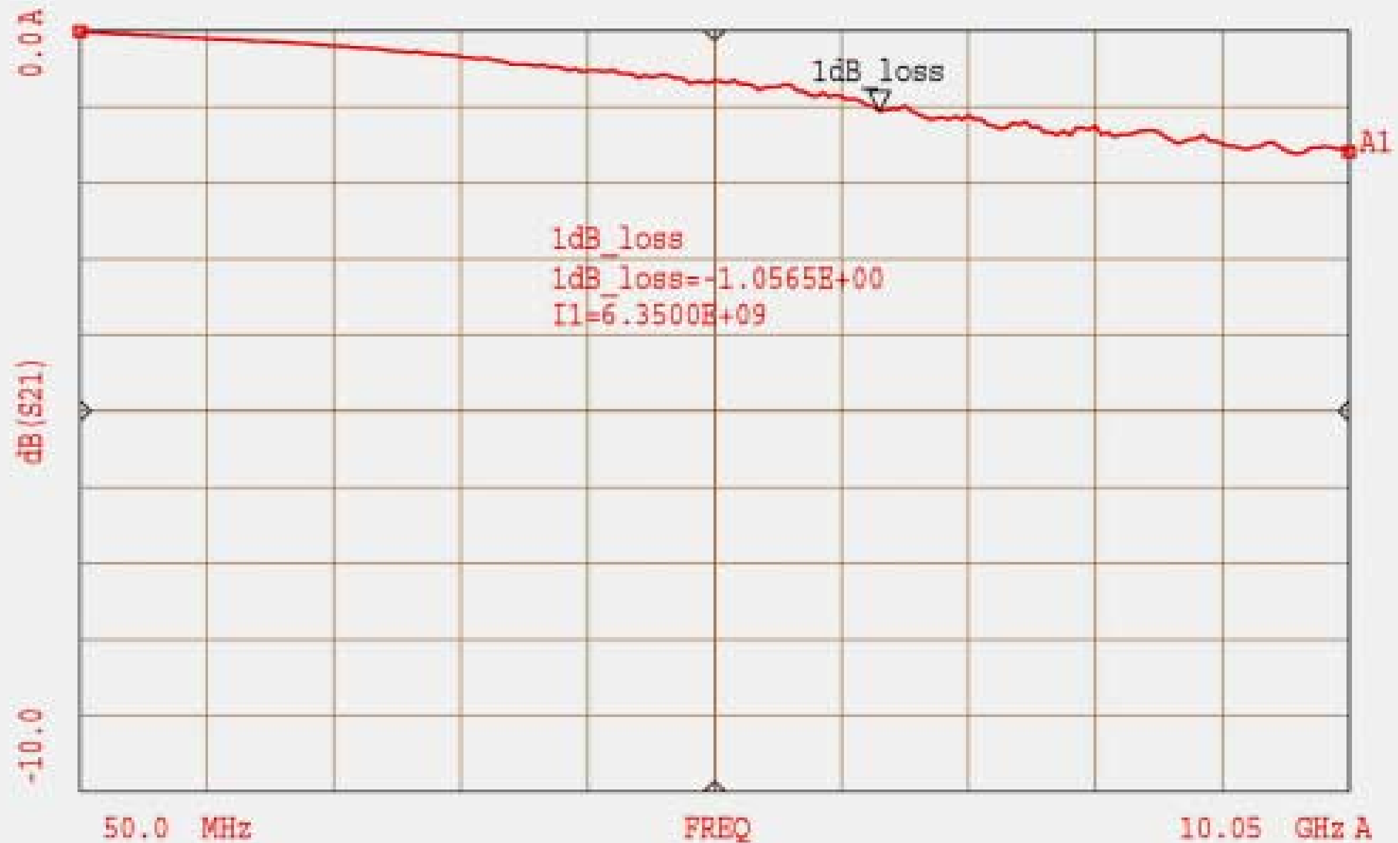
- Spring contact probes prove to be electrically superior to many other technologies. Test sockets utilizing this technology today, are characterized with *less than one nano Henry self-inductance*.
- These diminutive contacts excel in the areas of low contact resistance and electrical repeatability. A standard design threshold of less than 50mΩ is observed for most contacts of this style.
- Designs under development for new spring contact technologies will drive the contact resistance even lower.

probes	L1 & L2 (nH)	M21 (nH)	R1 & R2 (ohms)	C21a (pF)	C21b (pF)
field adjacent	0.50	0.06	80	0.040	0.050
field diagonal	0.50	0.01	90	0.007	0.008
edge adjacent	0.55	0.07	100	0.045	0.045
corner adjacent	0.67	0.08	115	0.050	0.050

Specifications subject to change without notice.
All measurements were taken at 0.50mm pitch.

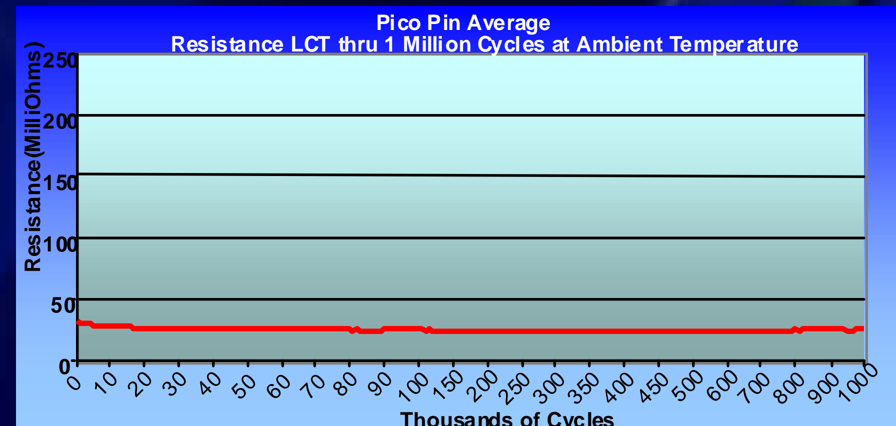


Electrical Performance



Long Life by Design

- The mechanics of a spring probe are largely contained inside the probe's barrel, essentially creating a closed contact architecture.
- Spring probes are an ideal choice for use in contaminated environments.
- Spring probes used in today's test sockets can last more than half a million cycles when manufactured to very tight specifications and properly cleaned and maintained in the handler.



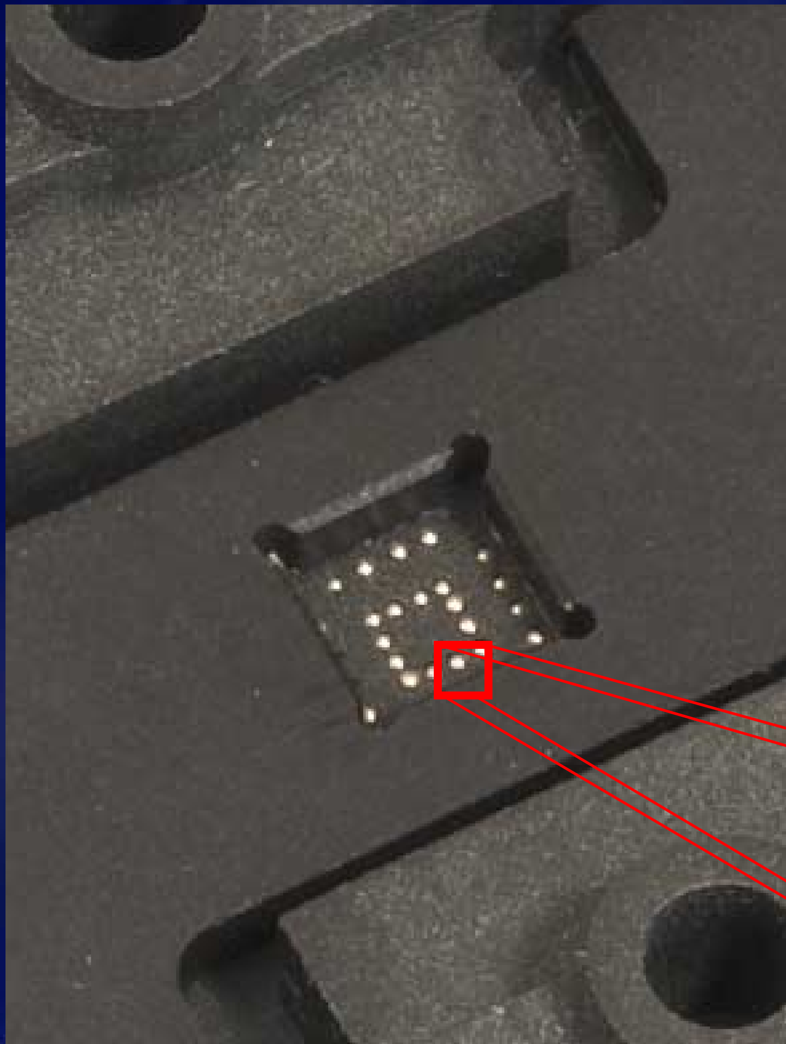
Future Socket Trends

- Test sockets are shrinking in size to accommodate smaller footprints.
- New high-speed devices above 1GHz will require the new generation of high frequency Chip Scale Probes utilizing signal paths shorter than .100" (2.54mm).
- *Strip testing* offers the CSP device manufacturer the opportunity to test earlier in the packaging process while the CSPs are still attached to their leadframe or strip, and have not been singulated.

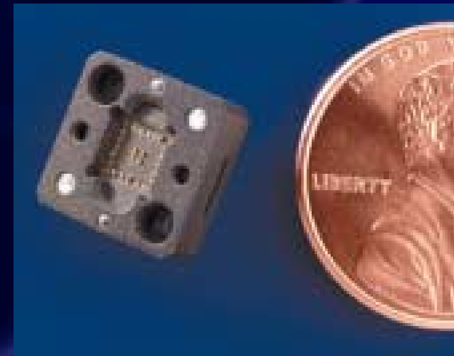
The Pico Pin

- Extremely short signal path
- Unique design boasts a .077” overall length with a compressed length of .059”.
- Made with advances in IDI spring-probe technology.

The Pico Pin

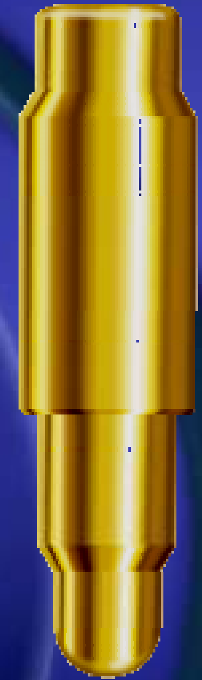


- Virtually eliminates signal loss and interference in high frequency testing environments.
- Provides invisible signal path for devices 0.65mm pitch and above.

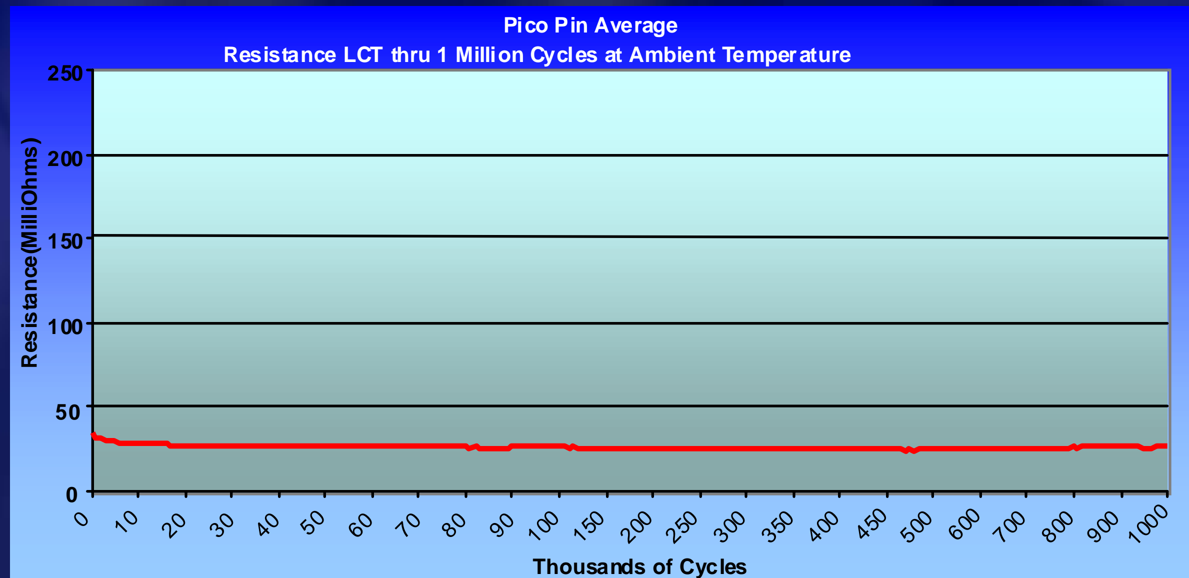


Patent Pending

The Pico Pin

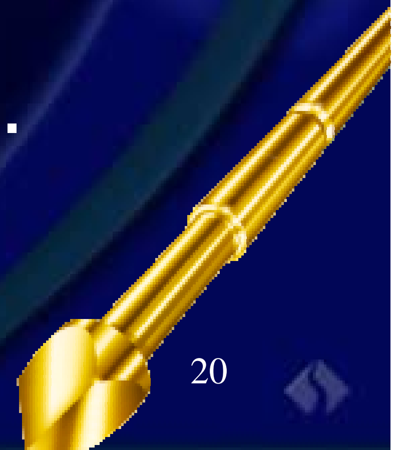


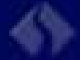
- .25 nH self-inductance!!
- Long Life
- Low Contact Resistance



Conclusion

- Spring Contact Probes are easily available with versatile design.
- Today, spring probes are designed with specific test socket applications in mind and offer the advantages of great electrical performance, extremely long life, and flexibility in design.
- Reliable and cost effective solution.





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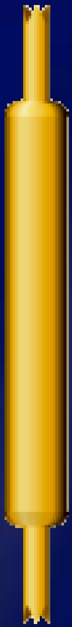

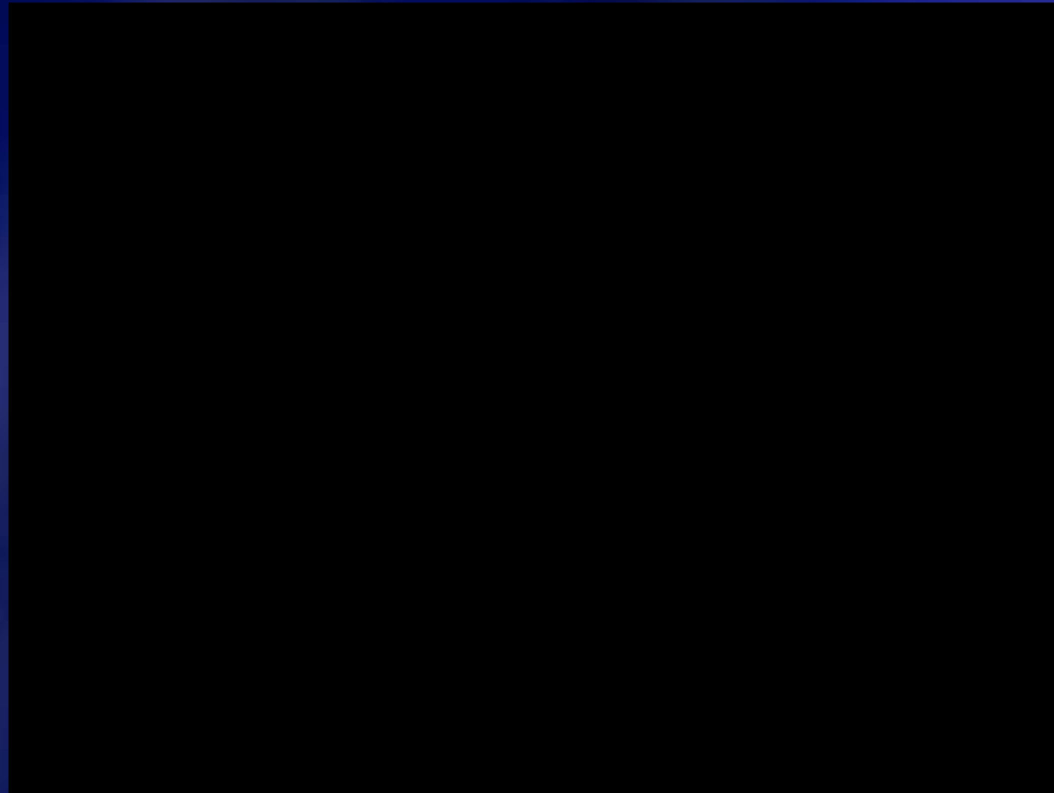

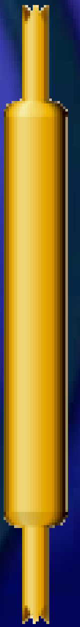

Evolution, Considerations, & Resources

Brian Crisp
Southwest District Sales Manager
Everett Charles Technologies
March, 2001

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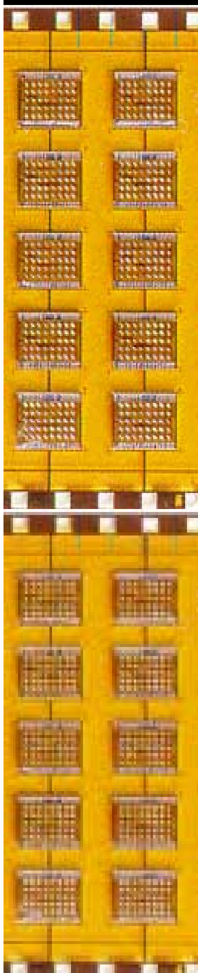
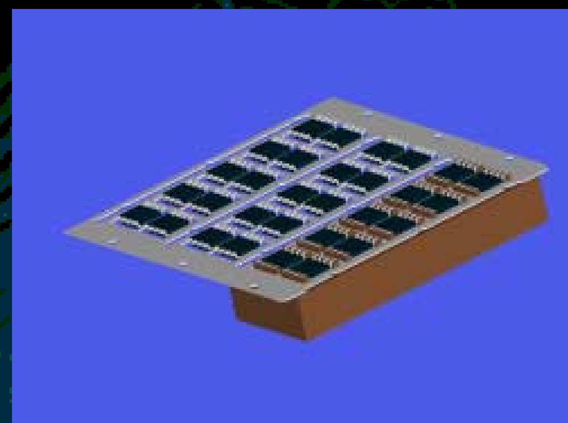
What is Strip Test?

A newly accepted method for simultaneous, massive, parallel testing

Strip Contactors





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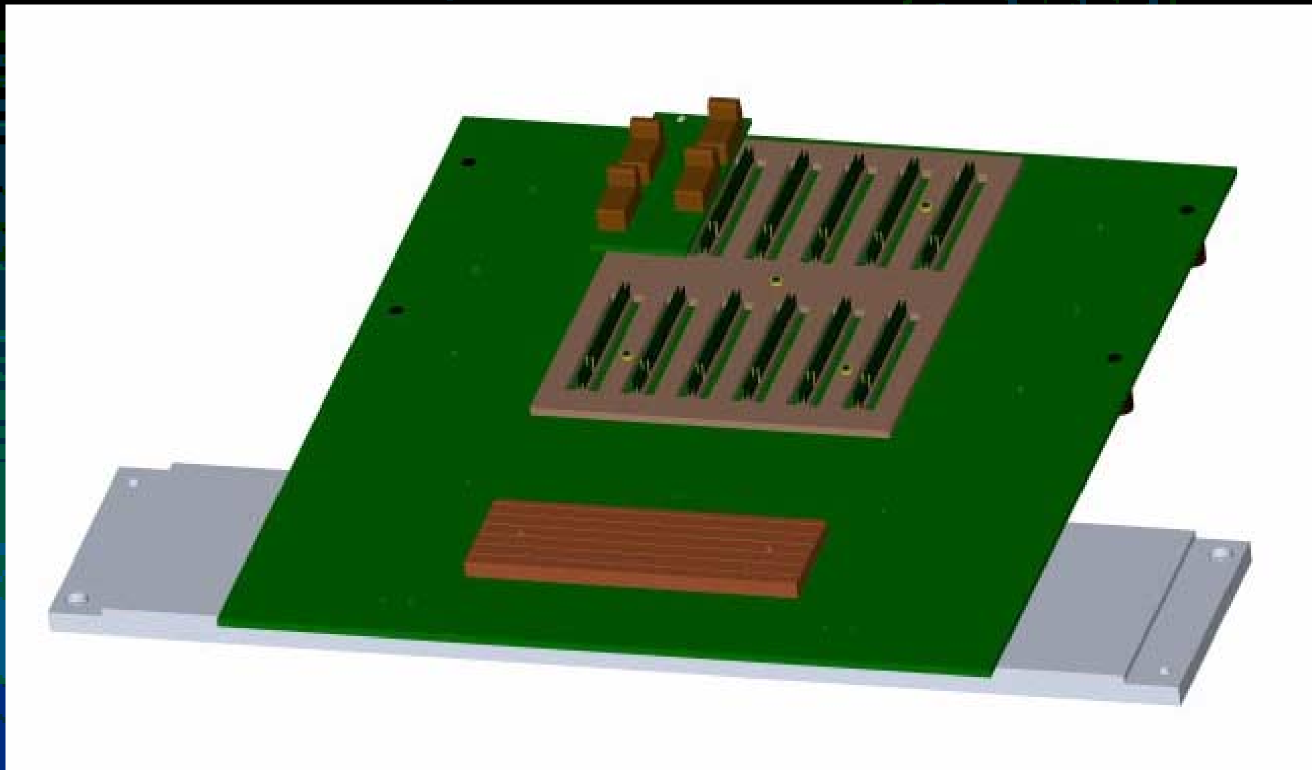
Strip Interface



48 Site Interface

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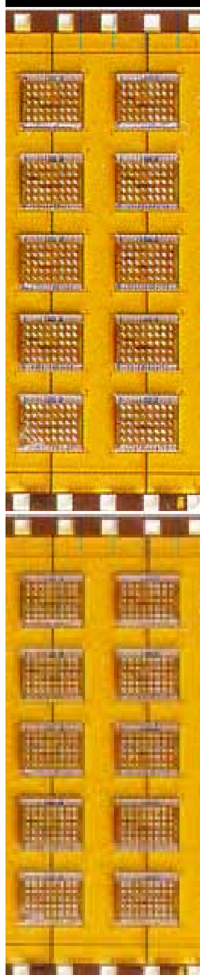
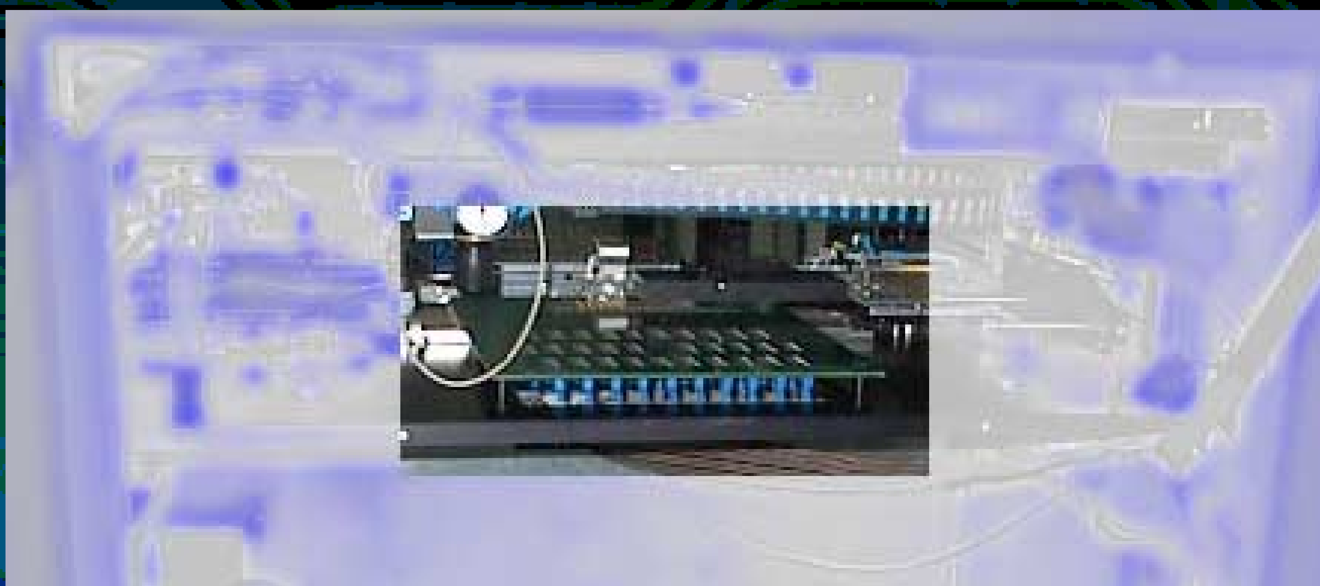
Strip Interface Installed





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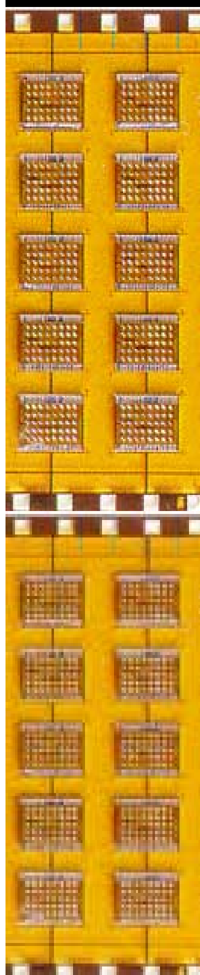
How Did Strip Test Evolve?



- First introduced in early 1990's on integrated lines
- Manufacturers either internally developed systems or turned to trim & form equipment manufacturers
- Now many major handler manufacturers either have, or are, introducing Strip and/or WLP Handlers

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Why is Strip Test Being Explored /Adopted?

- Test is the bottleneck
- Cost & productivity pressures
- Handling reduction
- New packaging technologies

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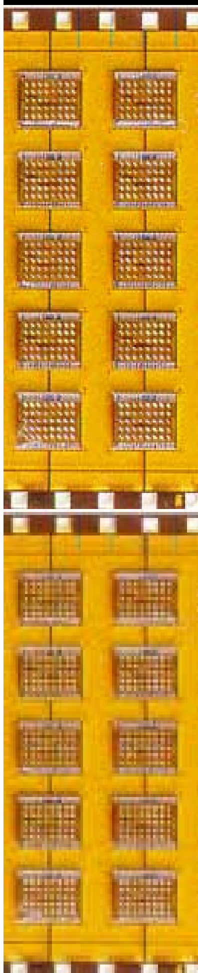
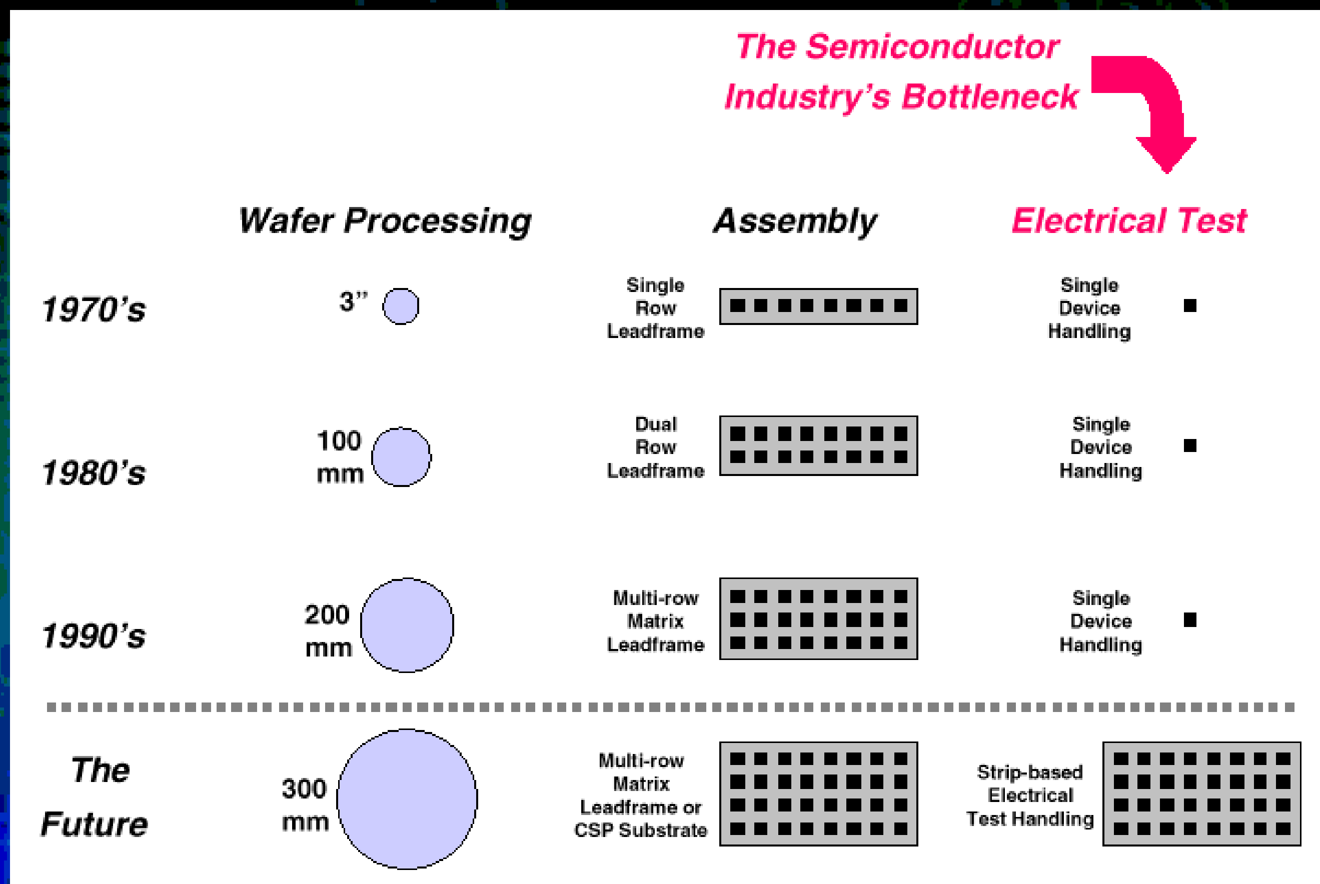
Test is the Bottleneck





Courtesy Tim Olsen, FICO America, Strip Based Test, Eighth Annual Manufacturing Test Conference SemiconWest 99

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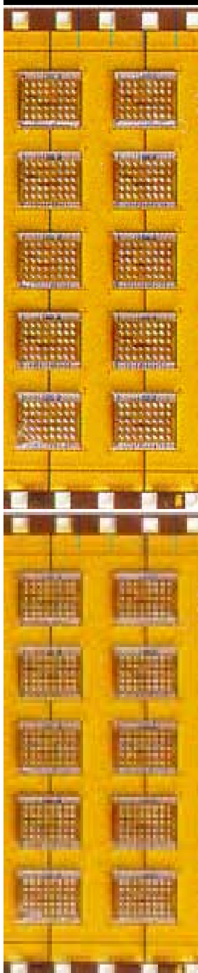
CSP Technology is Here!



There were greater than 50 CSP's in various stages of development or production at some 30 companies and institutions worldwide in 1998. It is estimated that there are now well over 100 CSP's under development.

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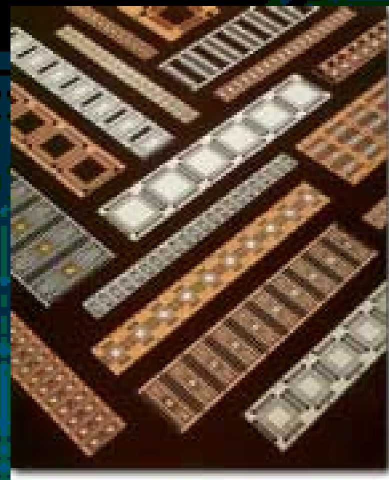
CSP Packaging at Wafer or Lead Frame

THE WAVE

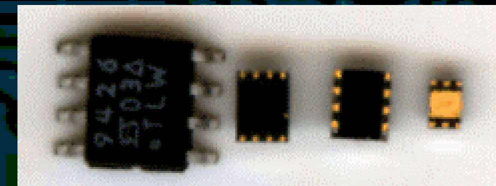
by Tessera

Wafer level packaging

Matrix Leadframes



Leaded Device Evolution



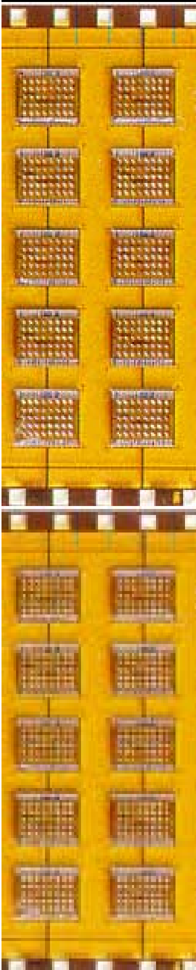
Fujitsu Super CSP

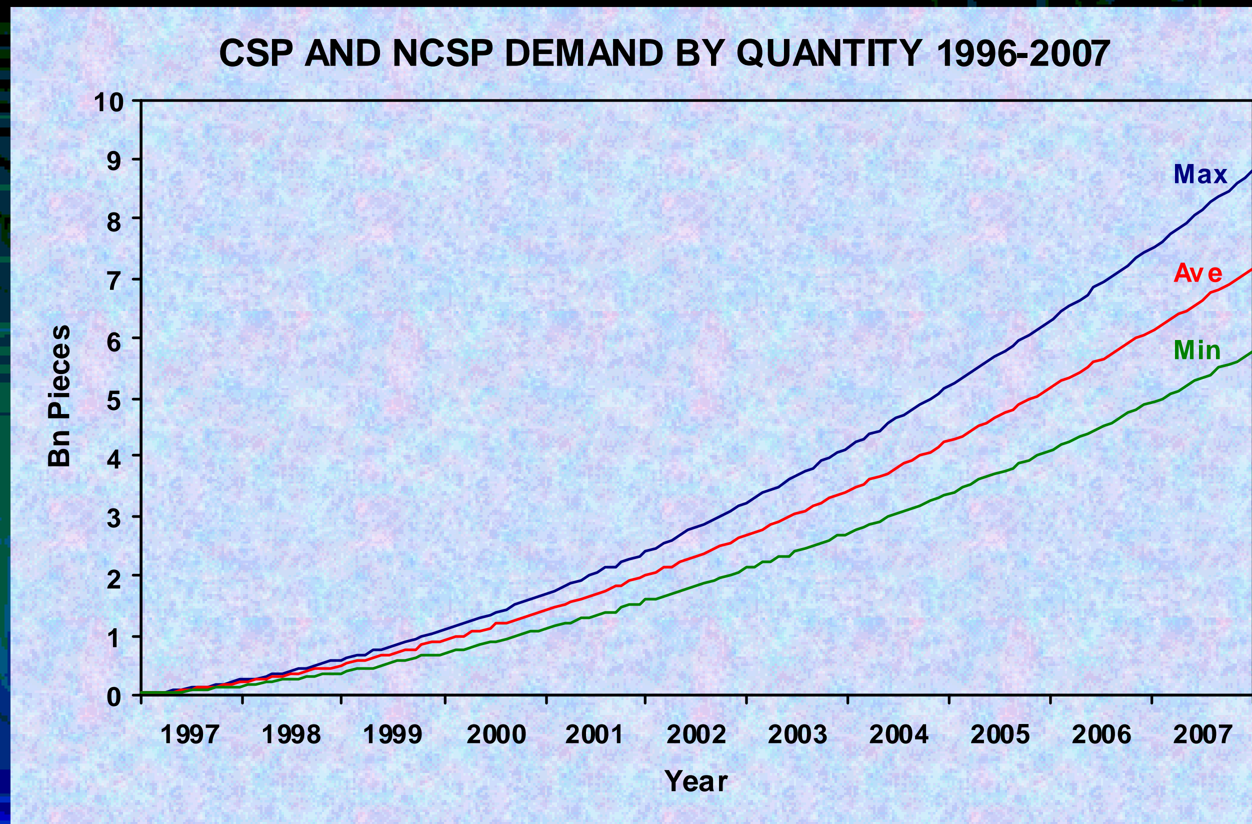
Except for solder ball transcription, all packaging is performed before dicing

Amkor MLF

Flush Leads

CSP Growth





Adapted from Chip-Scale Packaging vs. Flip-Chip By Mike Campbell, BPA Group Ltd.

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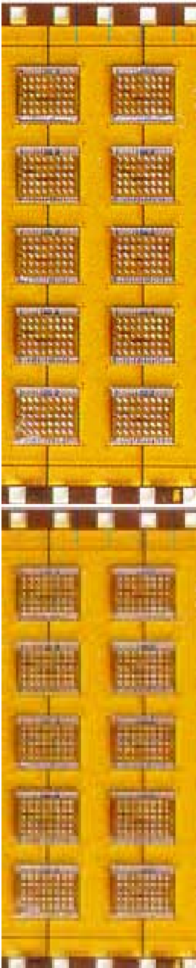
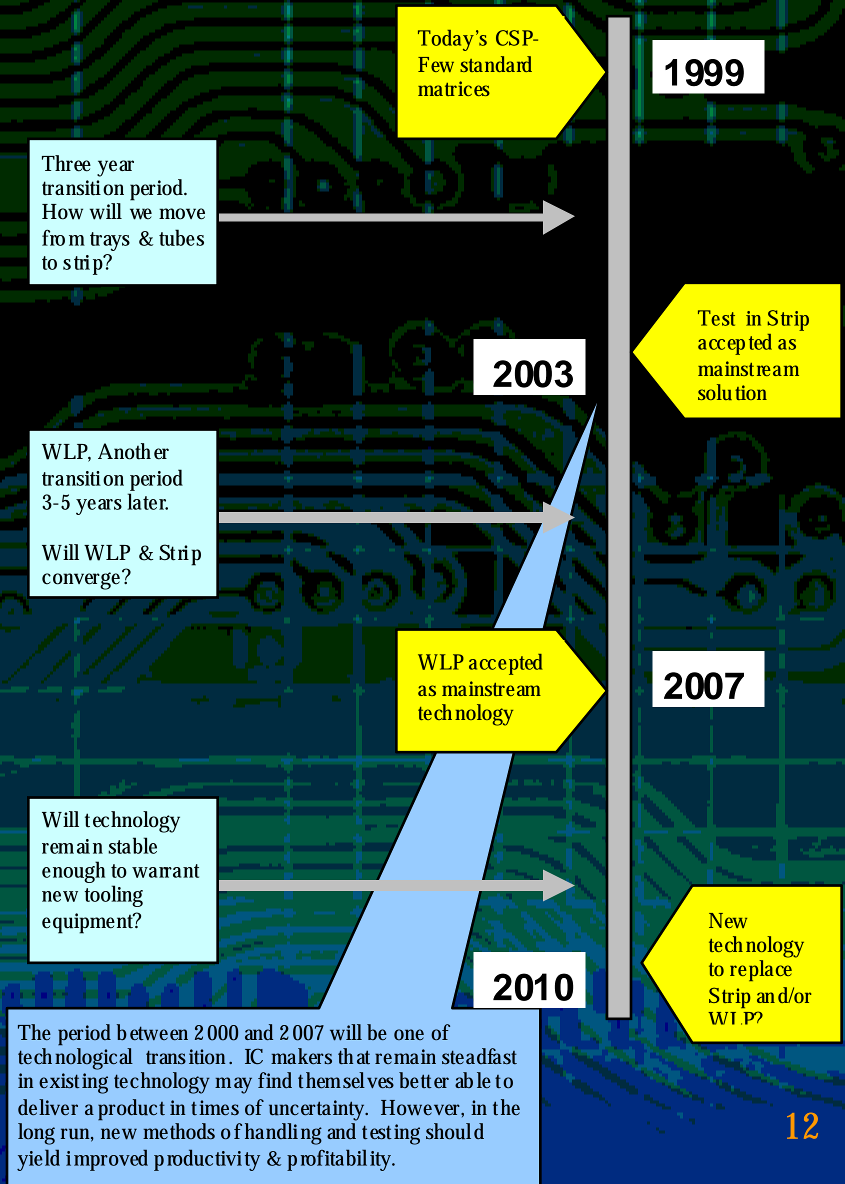


The Future?:
CSP & WLP Evolution



Adapted from: How Carrier Trays Are Shaping-Up for CSP Handling, By Ralph Henderer, Entegris Inc., Chip Scale Review Jan-Feb 2000

Key Benefits?

- Reduced Handling
  - less WIP
  - improved quality
  - faster time to market
- Productivity Gains
  - less equipment
  - less floor space
- Improved Profitability

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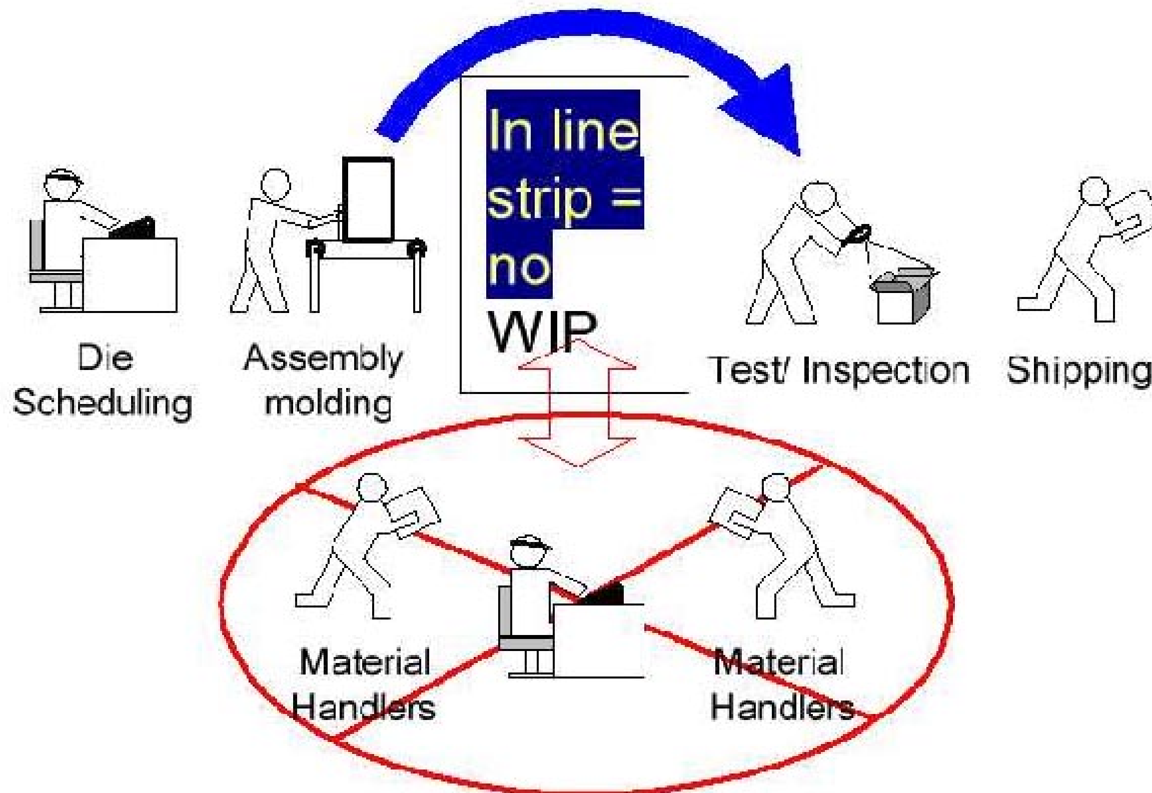
Reduced Handling



Adapted from Strip Test Update 99, Jack Kessler, Concepts Unlimited & Gordon Mackenzie, Delta Design, Test Assembly & Packaging Automation & Integration 99 Conference

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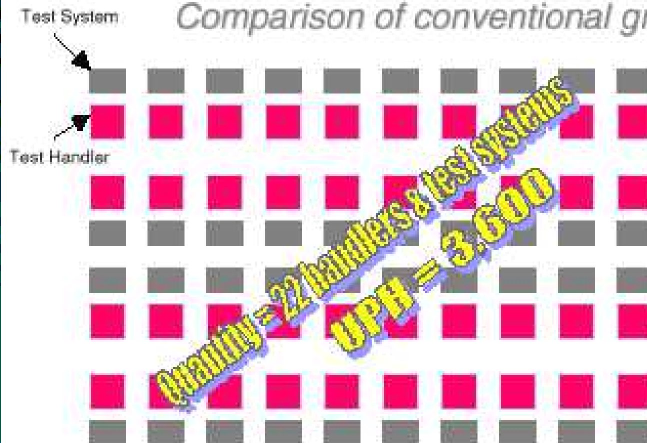
Productivity Gains

Comparison of conventional gravity handlers vs. strip-based handlers

Conventional Final Test Floor

(Example for singulated SOIC devices at 10 million/week)



Input Factors

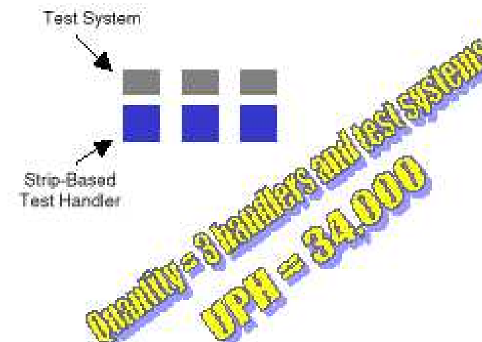
1.) 300 millisecond test time
2.) Conventional test system @ $100k
3.) Conventional singulated gravity handler @ $120K
4.) 75% utilization of equipment
5.) Index time of 0.70 seconds per device

TOTAL SQUARE FOOT
1,500 FT^2

Capital Cost	
22 Test Systems =	$2,200,000
22 Gravity Handlers =	$2,640,000
	$4,840,000

Strip-Based Test Floor

(Example for SOIC matrix leadframe devices at 10 million/week)



Input Factors

1.) 360 millisecond test time per 10 devices
2.) Parallel test system @ $350k
3.) New strip-based test handler @ $400K
4.) 75% utilization of equipment
5.) Index time of 0.70 seconds per 10 devices

TOTAL SQUARE FOOT
500 FT^2

Capital Cost	
3 Test Systems =	$1,050,000
3 Strip Handlers =	$1,200,000
	$2,250,000

Courtesy Tim Olsen, FICO America, Strip Based Test, Eighth Annual Manufacturing Test Conference, SemiconWest 99

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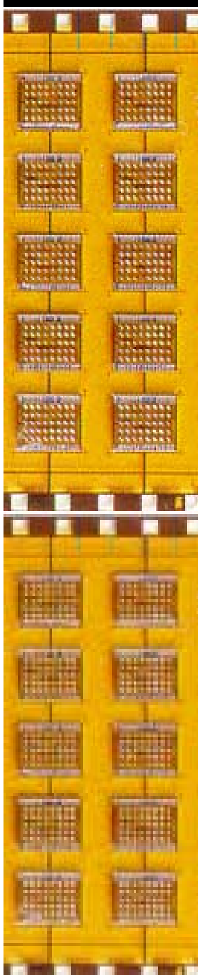
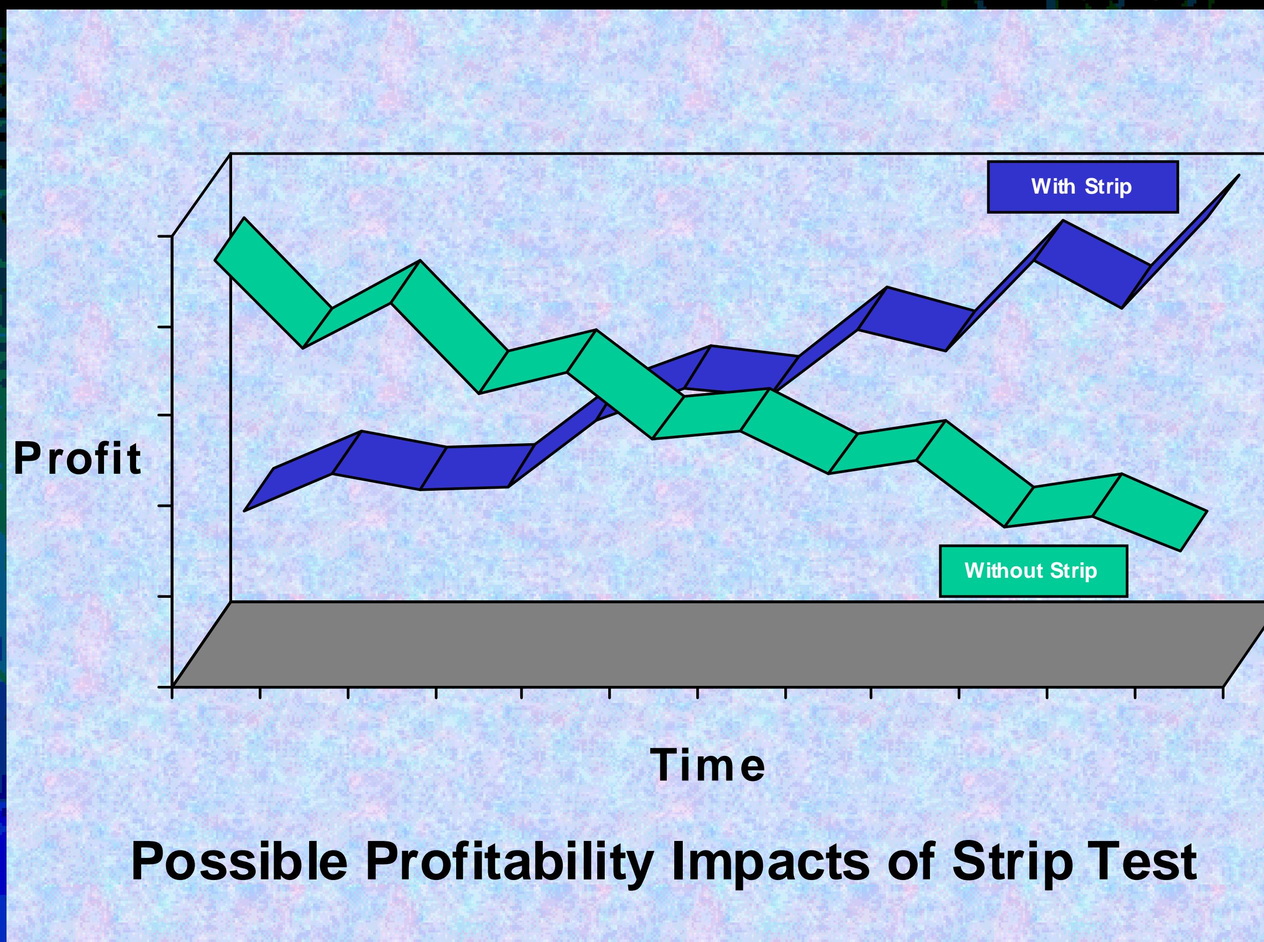
Improved Profitability





Possible Profitability Impacts of Strip Test

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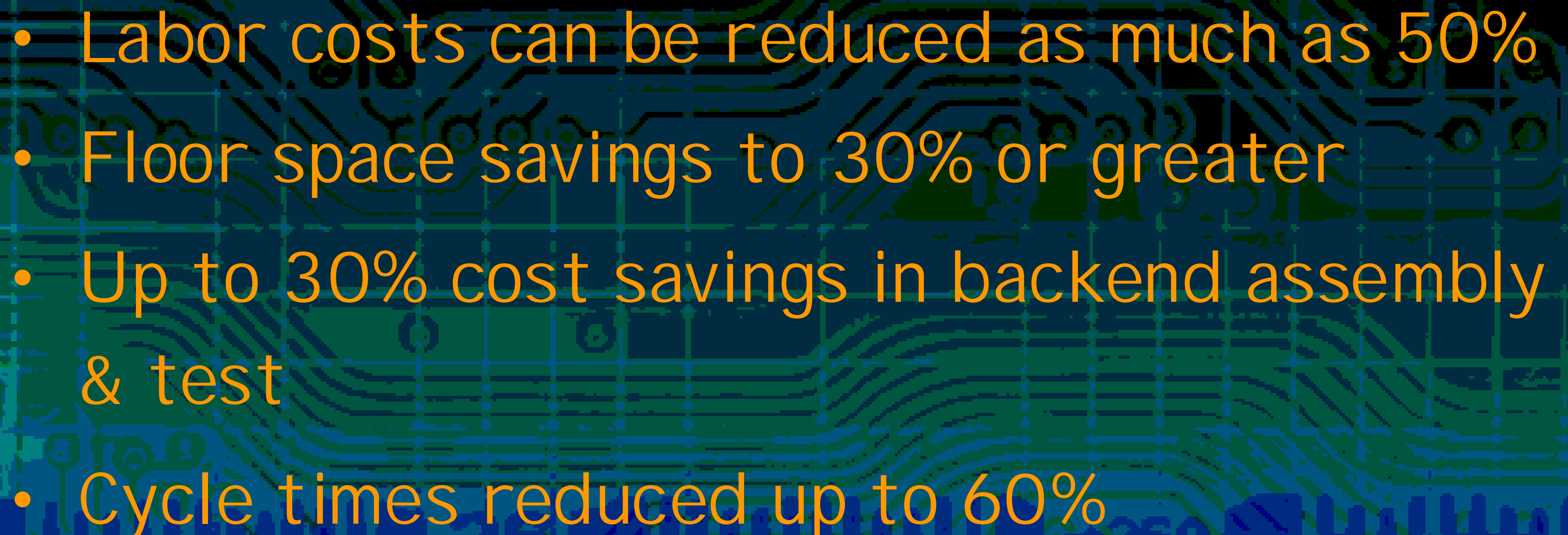
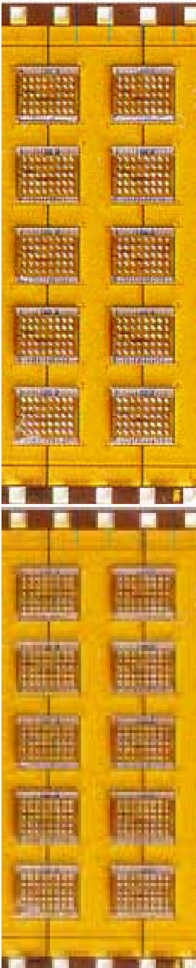
Some Statistics



- Labor costs can be reduced as much as 50%
- Floor space savings to 30% or greater
- Up to 30% cost savings in backend assembly & test
- Cycle times reduced up to 60%

Why isn't everyone using it?



- Product Dependent
  - lower pin count leaded devices & CSP's
- Production Issues
  - existing equipment for singulated product
- People Issues
  - resistance to change
  - empire protection
  - disconnection between assembly & test
- Test Issues
  - socket & performance board development

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Considerations

- Package Considerations
- Tester Considerations
- Handler Considerations
- Docking Considerations
- Contactor/Loadboard Considerations

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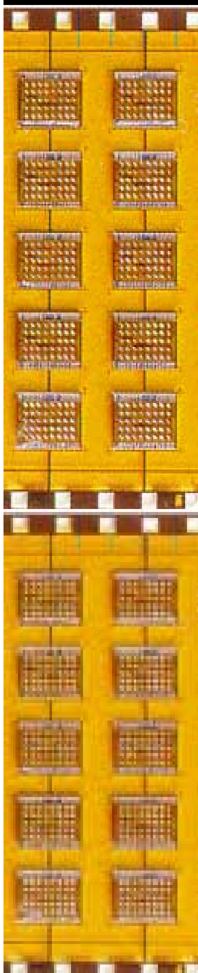
Package Considerations



- Pitch
- Density
- Strip/wafer coplanarity & flex
- Tooling
- Flash, resin bleed, & solder slivers

- Device targets
  - Leads
    - After trim condition
      - length
      - flatness
  - Lands
    - OSP's?
  - Solder Balls
    - Solder transfer rate
    - Witness marks

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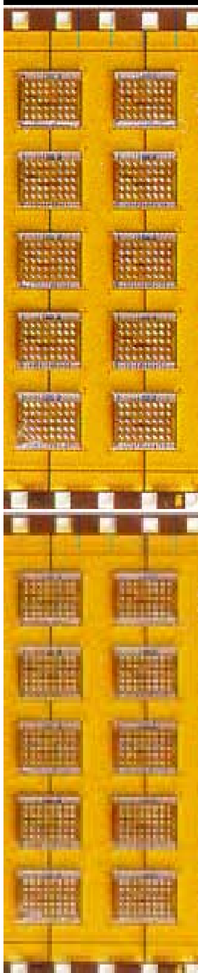
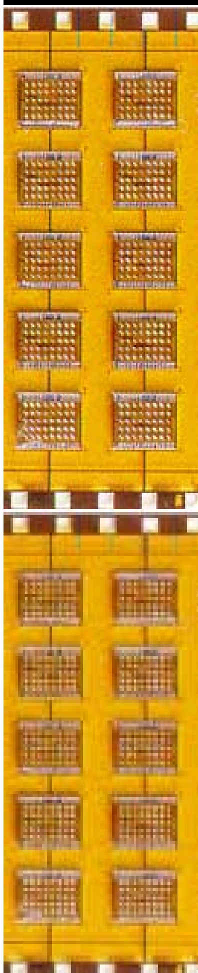
Tester Considerations



- Number of Devices Tested in Parallel
  - Tester resources
- Device Type
  - Memory
  - Mixed signal
  - Digital
  - RF
  - Etc.
- Functions Tested (DC, AC, functional)
- Device Testability
- Test Philosophy

Handler Considerations



- Nest/workpress to contactor coplanarity & alignment
- Nest/work press leadbacking
- Contactor/strip windows & placements
- Indexing capability
- Hardstop vs. programmable stop
- Ambient only vs. tri-temp
- Mechanical alignment vs. vision alignment
- Soak requirements
- Docking ease
- Multiple handler interfacing
- Handler maximum pin count

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Docking Considerations

Interface Interconnect Requirements

1. Direct Dock
   - High performance devices
     - RF products
     - Flash memory products
2. Cable Interconnect
   - Low performance devices
     - FET/Serial EE

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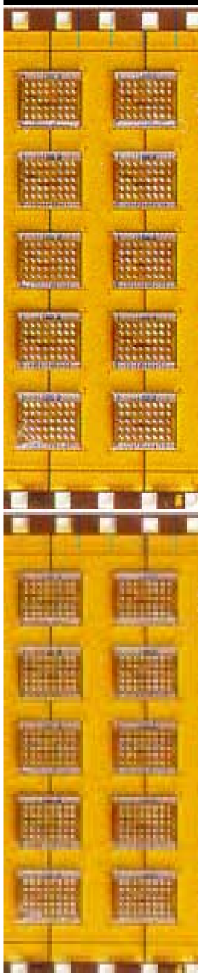
BURN-IN & TEST
SOCKET WORKSHOP

Contactor/Loadboard Considerations



- Load board/contactor complexity
- Ultra dependable contacts
- Contact Integrity
  - Redundant Contacts
  - High current
- Ability to easily assemble & maintain
- Cumulative error due to strip size
- Mechanical/optical alignment compatible
- Hand test requirements
- Interface flex and coplanarity
- Cost of test hardware

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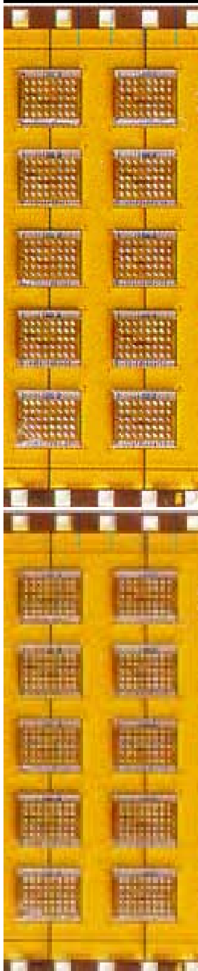
Order/Quote Considerations



- Package type
- Strip size
- Matrix size
- Pitch
- Lead count vs. contactor count
- Contact element type
- Handler make/model
- Load board requirements

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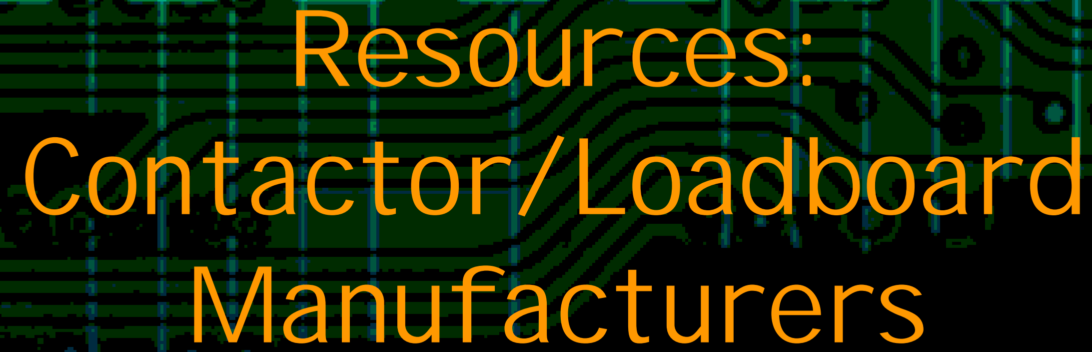
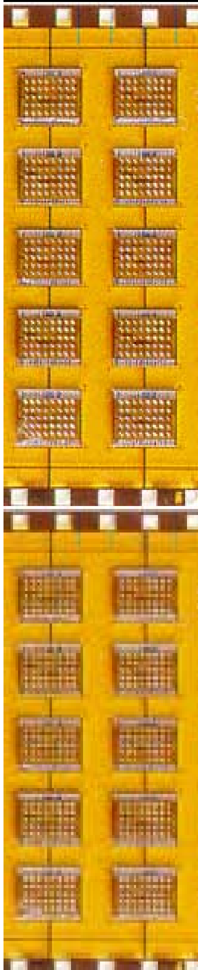
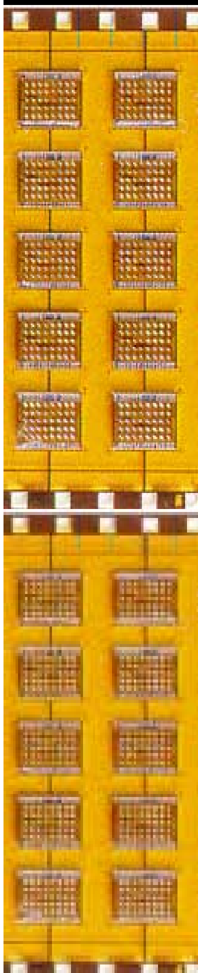


Resources: Contactor/Loadboard Manufacturers



- Select based on experience with strip test

Resources: Handler Manufacturers



- MCT/Aseco
- Delta Design
- Aetrium
- FICO
- Multitest
- HYAC Corporation
- ASM
- RVSI Systemation
- Ismeca
- Teradyne
- Hewlett Packard

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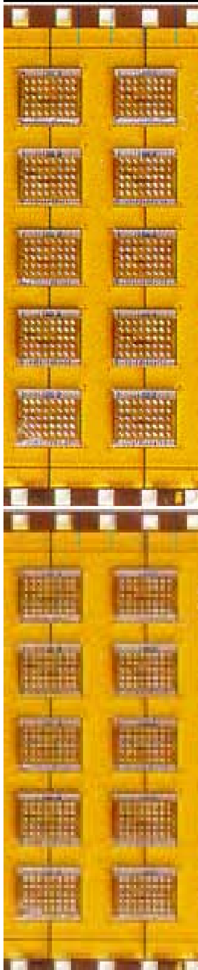
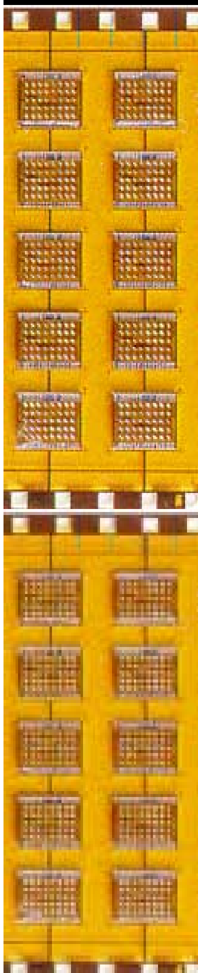
Resources: Tester Manufacturers



- Credence/TMT
- Eagle

Resources: Sub-Contract Assembly & Test



- Amkor
- STATS

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Summary

- Eliminate WIP
- Eliminate trays & tubes
- Conserve floor space
- Reduce cost of test
- Improve profits

STRIP

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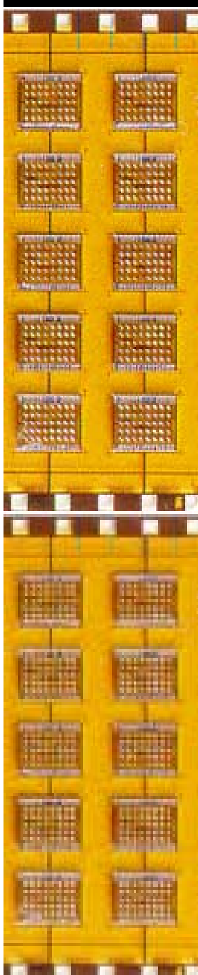
Bibliography/Resources



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  by Ron Leckie, Infrastructure
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  by Larry Klassen, Aetrium Inc
- Getting the Most From Your Handler, Parts 1 & 2
  by Jack Kessler, Concepts Unlimited
- Strip-Based Test, The Realities of Implementation
  by Tim Olsen, FICO America
- How carrier trays are shaping-up for CSP handling
  by Ralph Henderer, Entegris Inc.
- Integrated Massive Parallel Strip Test
  by Tim Gosnell, Amkor Technology
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  by Dennis Nelson, MCT
- Breaking the Assembly-Test Barrier
  by Tim Olson, FICO America

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BURN-IN & TEST SOCKET WORKSHOP

Lowering the Cost of High Performance Test and Burn-in

2001 Burn-in and Test Socket Workshop

James Rathburn
Gryphics, Inc.

Overview

- Introduction Question
- Market Trends Influencing Sockets
- Market Segments for Sockets
- The Life of an IC
- Cost vs. Performance Model
- Gryphics / Molex Development Program
- Conclusion

Introduction Question

- Why are there so many different types of Sockets?
    - Prototype and Emulation Sockets (PES)
    - Test
    - Burn-In
    - Production

Market Trends Influencing Sockets

- **Processors –**
  - uPGA, LGA, BGA packaging : 500 – 2000 I/O
- **High Performance ASICS and Chipsets –**
  - BGA, CGA packaging : 500 – 1500 I/O
- **Low Pin count High Speed ICs –**
  - FPLGA, CSP, MLF packaging : 5 - 250 I/O
- **Memory –**
  - TSSOP, CSP packaging : 50 – 150 I/O

Market Trends Influencing Sockets

- Systems – Operating above 1 –2 GHz
- Telecom / Datacom – Systems 1 – 10 GHz
- Portable Electronics – 2.5 to 10 GHz
- Memory – 200 MHz to 2 GHz

Market Segments for Sockets

- Prototype and Emulation Sockets (PES)
  - Historically BI Sockets or Pin and Header
  - Typically $1 to $2 per I/O
  - Mechanical Life Expectancy – 1 to 10 Insertions
  - Generally Soldered SMT
  - Unit Volumes ~ 1 to 1000

  - System speeds drive high performance due to Inductance of historical solutions

Market Segments for Sockets

- Burn-In Sockets
  - Historically Cantilever Beam or Stamped/Formed
  - Typically $0.15 to $2 per I/O
  - Mechanical Life Expectancy – 3K to 10K Insertions
  - Generally Soldered Thru Hole ; some Solderless
  - Unit Volumes ~ 500 to 100K

  - Market fragmentation drives cost and performance
    - Large volumes for MPU and Memory
    - Smaller volumes - sampling/qualification needs only

Market Segments for Sockets

- **Test Sockets or Test Contactors**
  - **Spring Probe, Fuzz Button, Elastomeric Based**
  - **Typically $3 to $20 per I/O**
  - **Mechanical Life Expectancy – 100K to 500K Insertions**
  - **Generally Solderless Compression Mount**
  - **Unit Volumes ~ 1 to 100**

  - **Cost, Ease of Use, Maintenance, Delivery**
    - All are increasingly important issues
    - Electrical Performance limits many technologies

Market Segments for Sockets

- Production or End User Sockets
  - Historically "Beam Based" Stamped or ZIF
    - Some Interposer types for LGA
  - Typically $0.01 to $0.05 per I/O
  - Mechanical Life Expectancy – 1 to 10 Insertions
  - Generally Soldered SMT – Interposer Compression
  - Unit Volumes ~ 100K to 100 Million

  - System speeds drive high performance due to Inductance of historical solutions
    - Cost and Reliability are Critical Parameters

The Life of an IC – Socket Mating

- Package Characterization
- Device Characterization
- System Development
- Device Test
- Device Burn-in
- System Level Test
- Production Socket

Cost vs. Performance Model

$$\frac{\text{Cost of Socket}}{(\text{Freq GHz})(\text{Insertion to Repair})} + \frac{(\text{Cost of Repair})(\#\text{ of Repairs})}{(\text{Insertion Count After Repair})}$$

Gryphics / Molex Development Program

- **Primary Goal**
  - Development of Next Generation MPU Socket Architecture – Device Speed drives LGA
  - Ramp High Volume, High Performance, Low Cost Production
- **Secondary Goal**
  - Apply the core technology used in low cost high volume applications to the lower volume
    - PES
    - Burn-In
    - Test

Gryphics / Molex Development Program

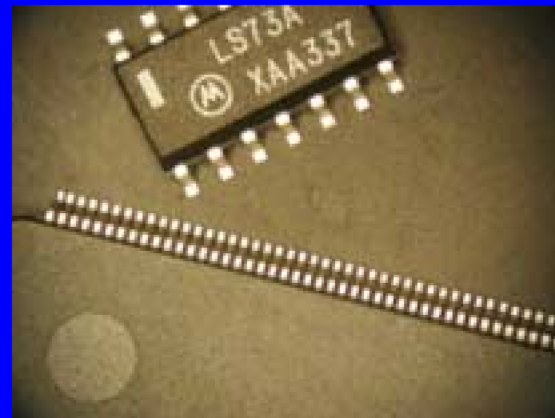
- Photos show one type of LGA production connector
  - Low cost
  - 1 db Loss @ 6 GHz
  - Solderless or SMT
  - Configured for 25 insertion count
  - Medium Normal Force

Gryphics / Molex Development Program

- Photos show the same contact configured for PES or Test for BGA
  - Low Cost
  - 1db Loss @ 6 GHz
  - Solderless or SMT
  - Configured for 10K to 100K insertion count
  - Low-Medium Normal Force – Oxide Pierce

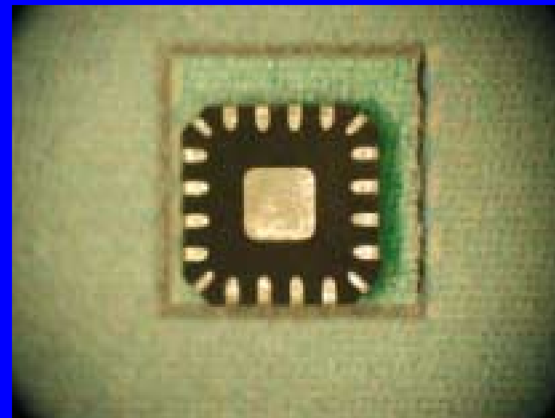
Gryphics / Molex Development Program

- Photos show a variation configured for Gullwing Leads
  - Low Cost
  - 1db Loss @ 3-4 GHz
  - Solderless
  - Configured for 100K insertion count
  - Low-Medium Normal Force – Oxide Pierce
  - Footprint Compatible



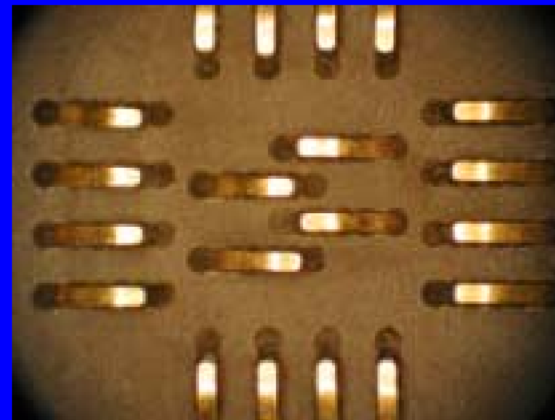
Gryphics / Molex Development Program

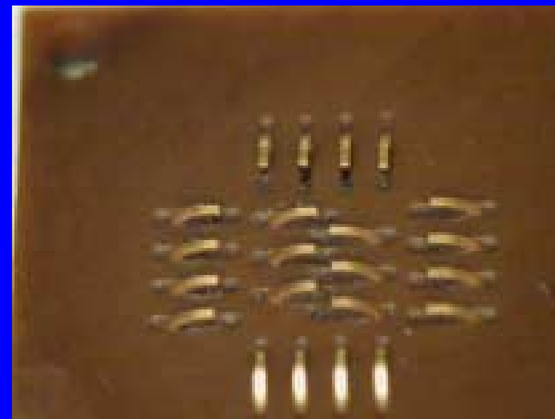
- Photo shows another type of Production LGA contact configured for MLP / LGA Test and Burn-in



Gryphics / Molex Development Program

- Independent contact sets replaced to change from one device to the next
- Maintenance done by discarding low cost contact set
- Hybrid Molding process cuts cost





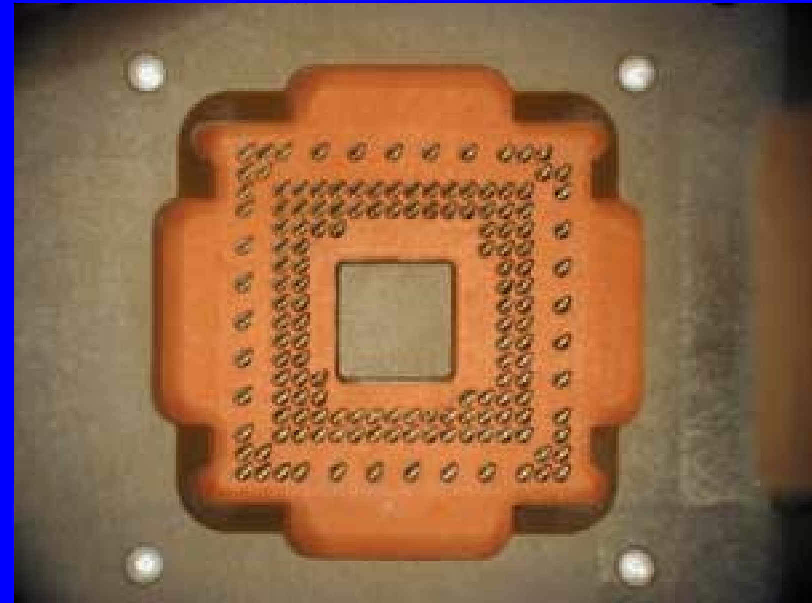
Gryphics / Molex Development Program

- Alterations in configuration apply to
  - Pin Grid Array
  - uPGA
  - Column Grid Array

Self Actuating ZIF or Zero Insertion Force adds to Life and lowers cost of use

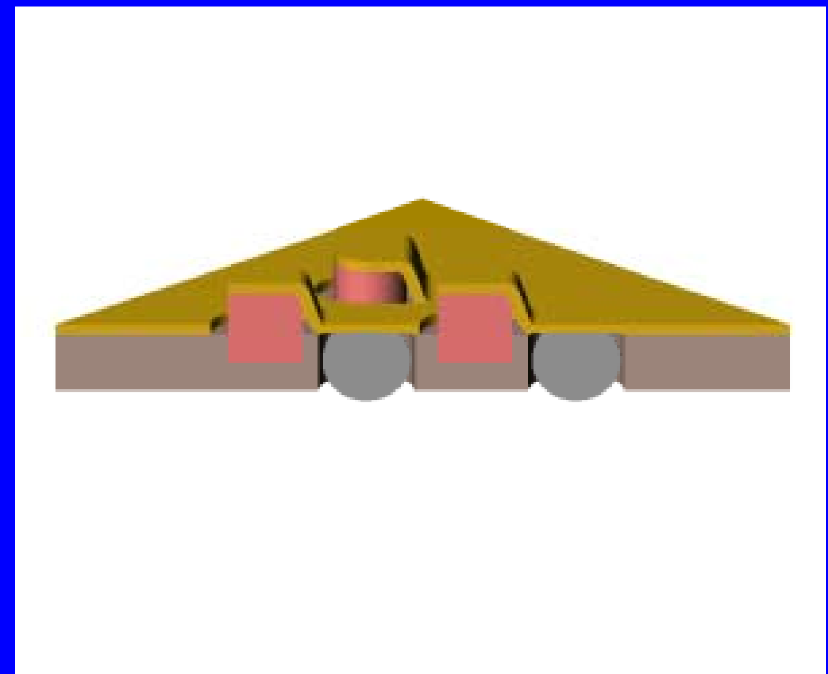
Gryphics / Molex Development Program

- Photo shows fine pitch capability of core technology for Burn In and Test Sockets
- Fine Pitch extension
  - CSP
  - FPLGA
  - Flip Chip



Gryphics / Molex Development Program

- Illustration shows section of low profile Production LGA connector based on Substrate Technology
  - Higher performance
  - Packaging Technology
  - High Volume Process
    - Variations used in low volume



Gryphics / Molex Development Program

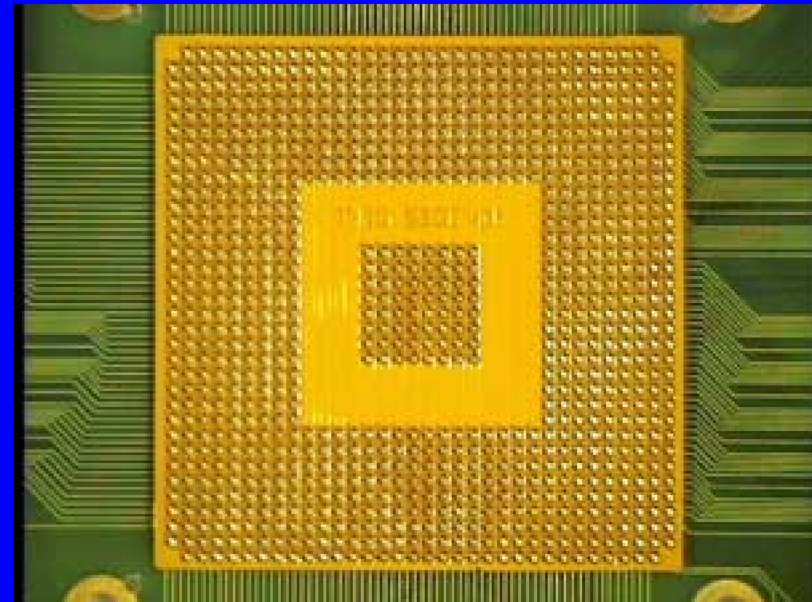
- Photo shows bottom side of connector
  - Solder Ball attach to PCB
  - High Pin Count
    - 1000 I/O Plus
    - 0.5 mm Tall
    - 10 GHz Performance

Gryphics / Molex Development Program

- Photos show variety of patterns and pitches
  - Each contact site flexes independently from its neighbor
  - Configurations for Test, Burn-In, and PES based on Production structure
  - SMT or Solderless

Gryphics / Molex Development Program

- Photo of 1100 I/O plus ASIC device connector
  - Mounted to system PCB to allow for ASIC removal

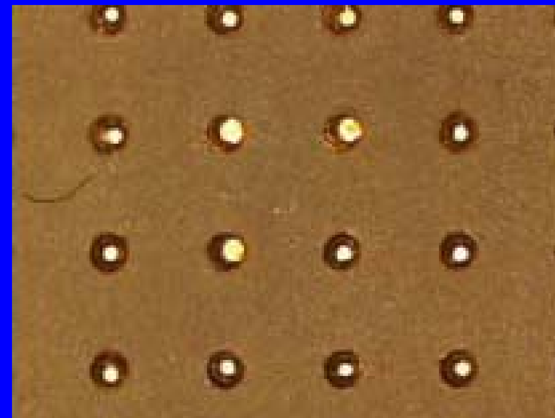


Gryphics / Molex Development Program

- ISO view of one type of independent contact arms

Gryphics / Molex Development Program

- Photos show still another variation of a Production LGA connector
  - Height Variation
    - 0.7 mm
    - 2.0 mm
    - 3.0 to 5.0mm
      - Board to Board Connectors



Conclusion

- **Why Does Molex Care about Test and BI**
  - High Performance now needed in Systems.
  - Development Refinement prior to production
  - Earlier involvement in IC or System development
  - Better serve the overall needs of customer
  - Packaging and Connectors are merging
- **How Does the Industry Benefit ?**
  - One core technology serves needs across all platforms
  - Correlation from development, test, and burn-in into production use
  - Pre-qualification of various sockets at once to the OEM
  - Dramatic overall cost reduction