Burn-in & Test Socket Workshop

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Technical Program

Session 1
Monday 3/05/01 8:30AM

Burn-in: Product Trends And Manufacturing Challenges

"Facing The Power Of The Future - High End Burn-in Directions And Trends"
Marc Knox - IBM Microelectronics

"Burn-in Of Memory Devices - A Look At The Past, Present And Future Of Memory Packaging And Interconnect Systems"
Daniel Cram – Micron Technology

"Areas Of Conflict And Bottlenecks"
Joseph J. Riggs - Lucent-Bell Labs - Agere Systems

FACING THE POWER OF THE FUTURE
HIGH END BURN-IN DIRECTIONS AND TRENDS

Marc Knox

IBM Microelectronics

Burlington VT

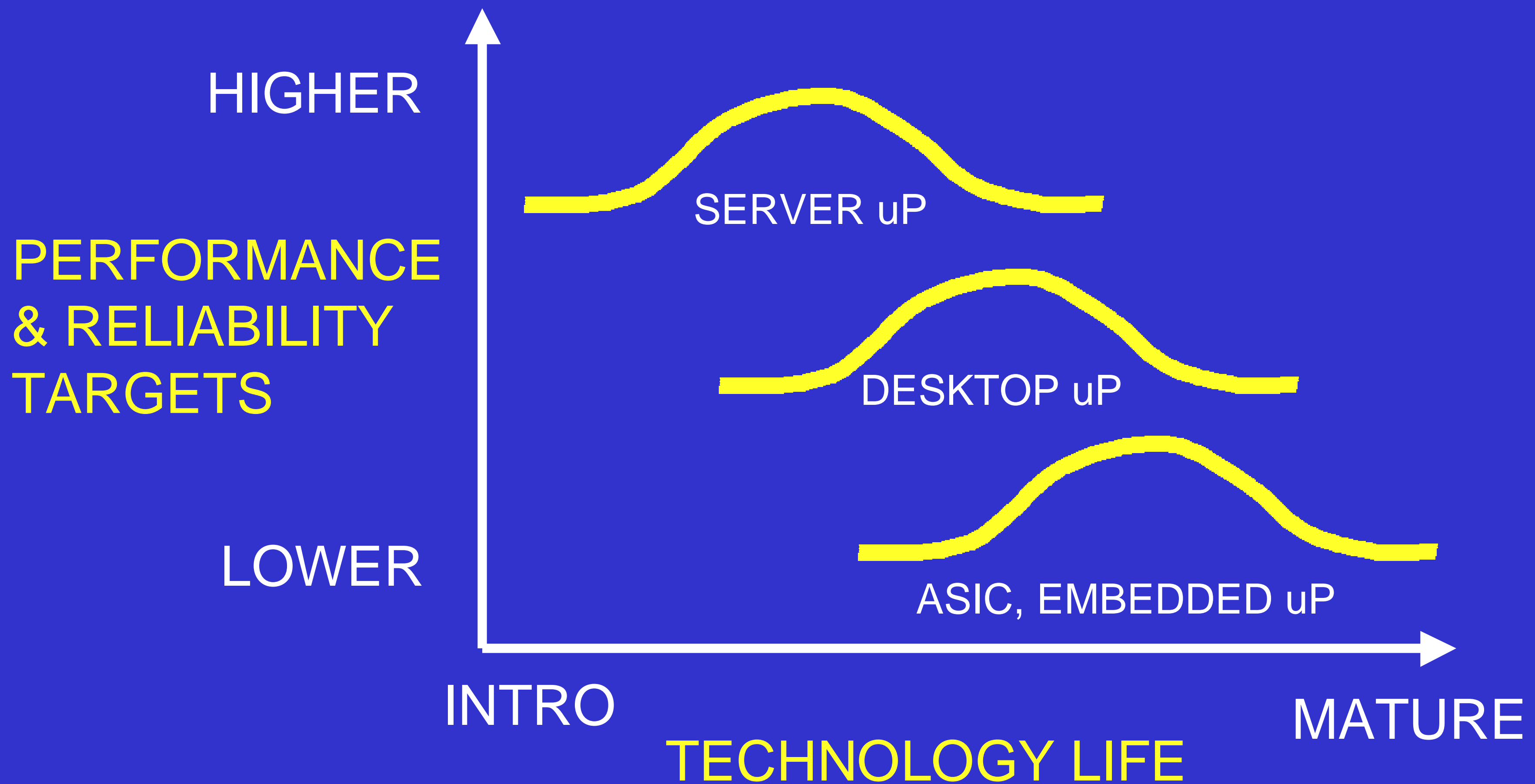
INTRODUCTION

- High end burn-in is the harbinger of general semiconductor technology trends
- Power at burn-in and test is a first order challenge for high end products today
- Power at burn-in and test will become a challenge across the board in the future
- Innovation, invention and advancement in socket power/thermal performance is critical

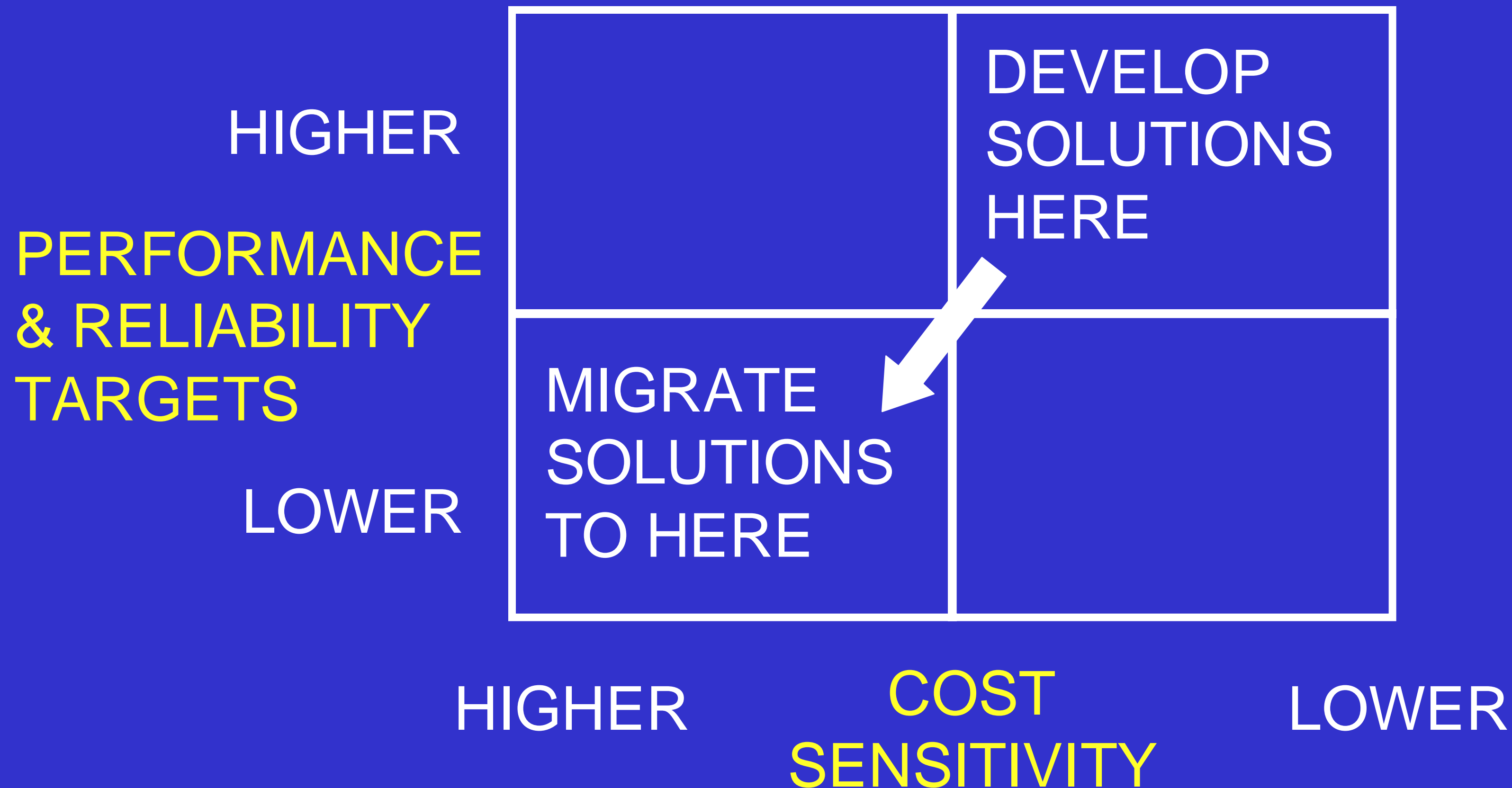
HIGH END BURN-IN DEFINED

- High transistor count, large die size
- Server and mainframe microprocessors
- Advanced technologies
- High reliability
- High performance
- Ceramic substrate, BGA packages
- Solder ball chip attach

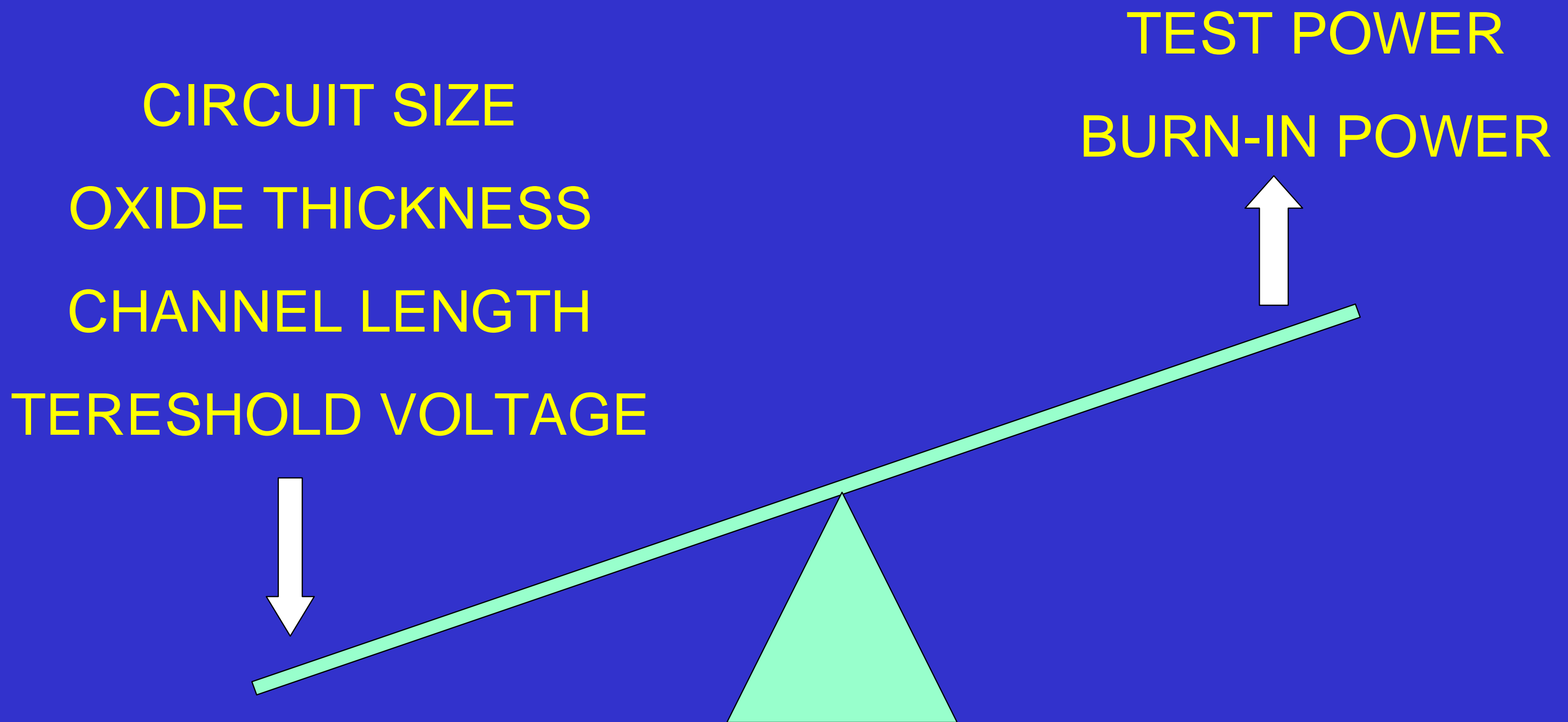
TECHNOLOGY ROLLOUT (LOGIC)



HIGH END DEVELOPMENT HAS FUTURE LOW END BENEFITS



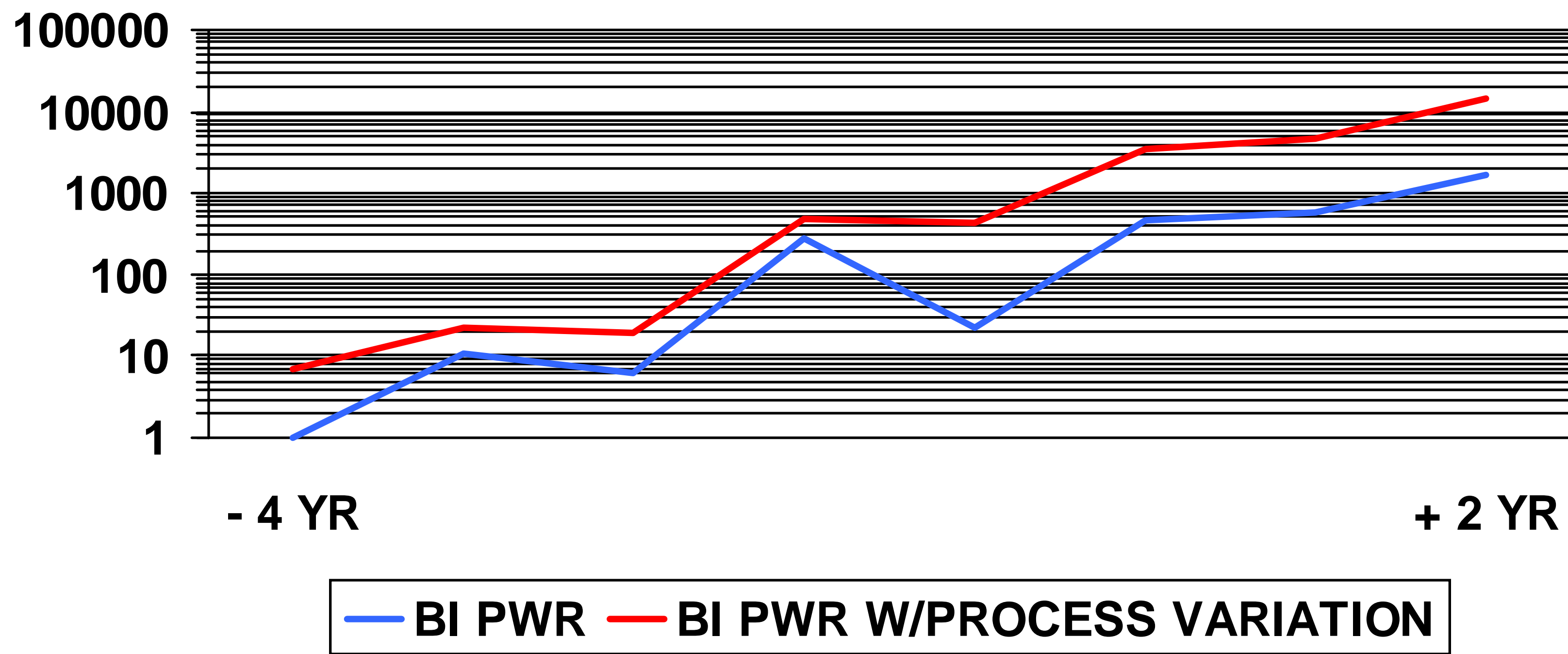
PERFORMANCE VS POWER
A MARKET DRIVEN CONTEST



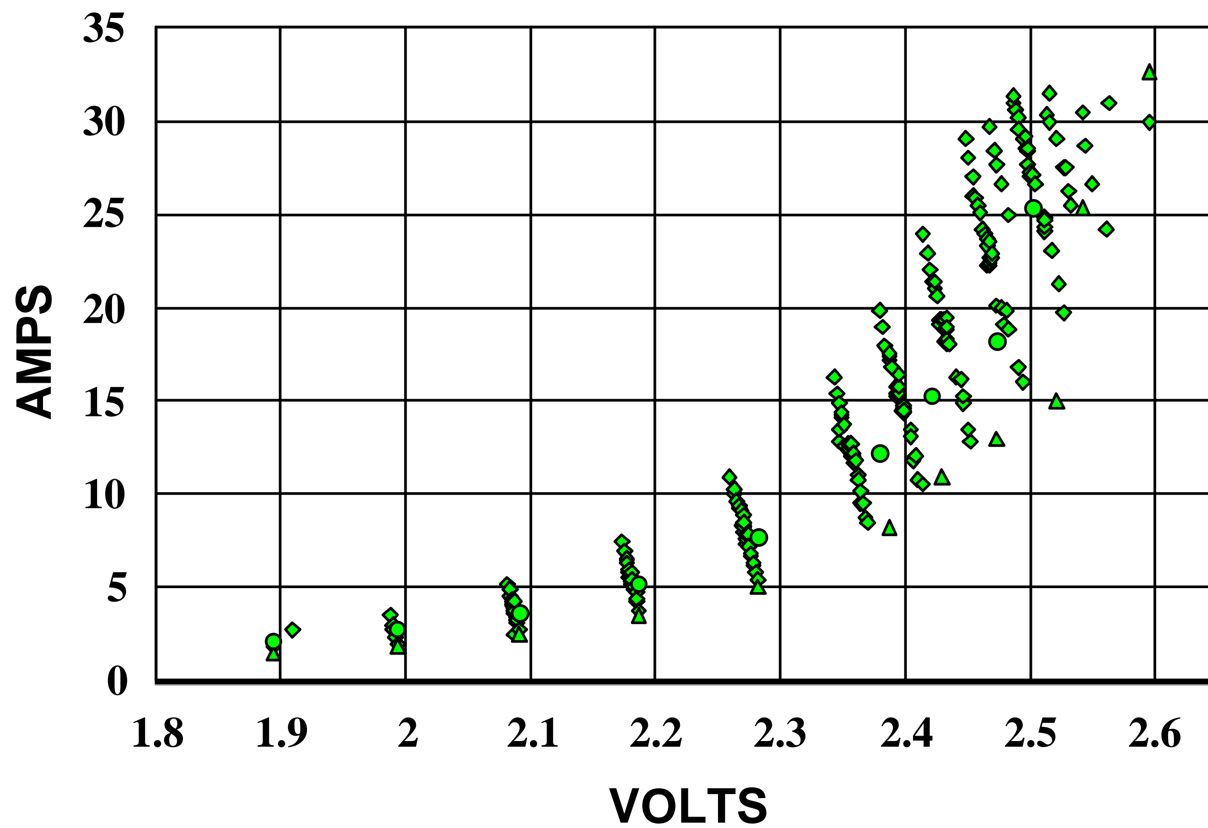
POWER AT BURN-IN CONDITIONS

- Power is not the same as in the application
- Primary power is DC
- Primary power is sub-threshold leakage (Ioff)
- AC power is typically a small portion of BI pwr
- AC power can be modulated by clock speed
- Accelerated temperature of BI increases Ioff
- Accelerated voltage of BI increases Ioff

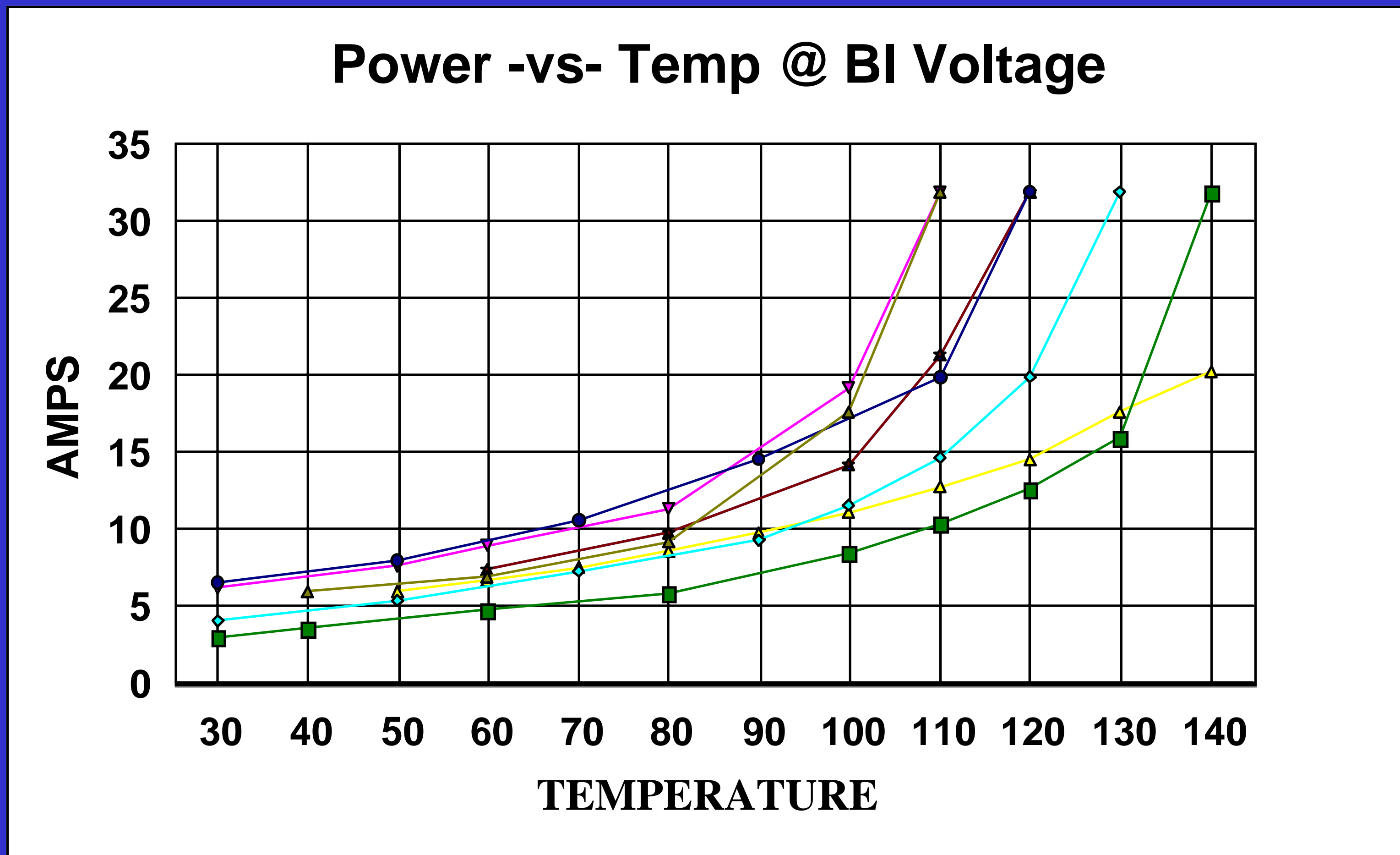
BURN-IN POWER & TECHNOLOGY PROGRESSION



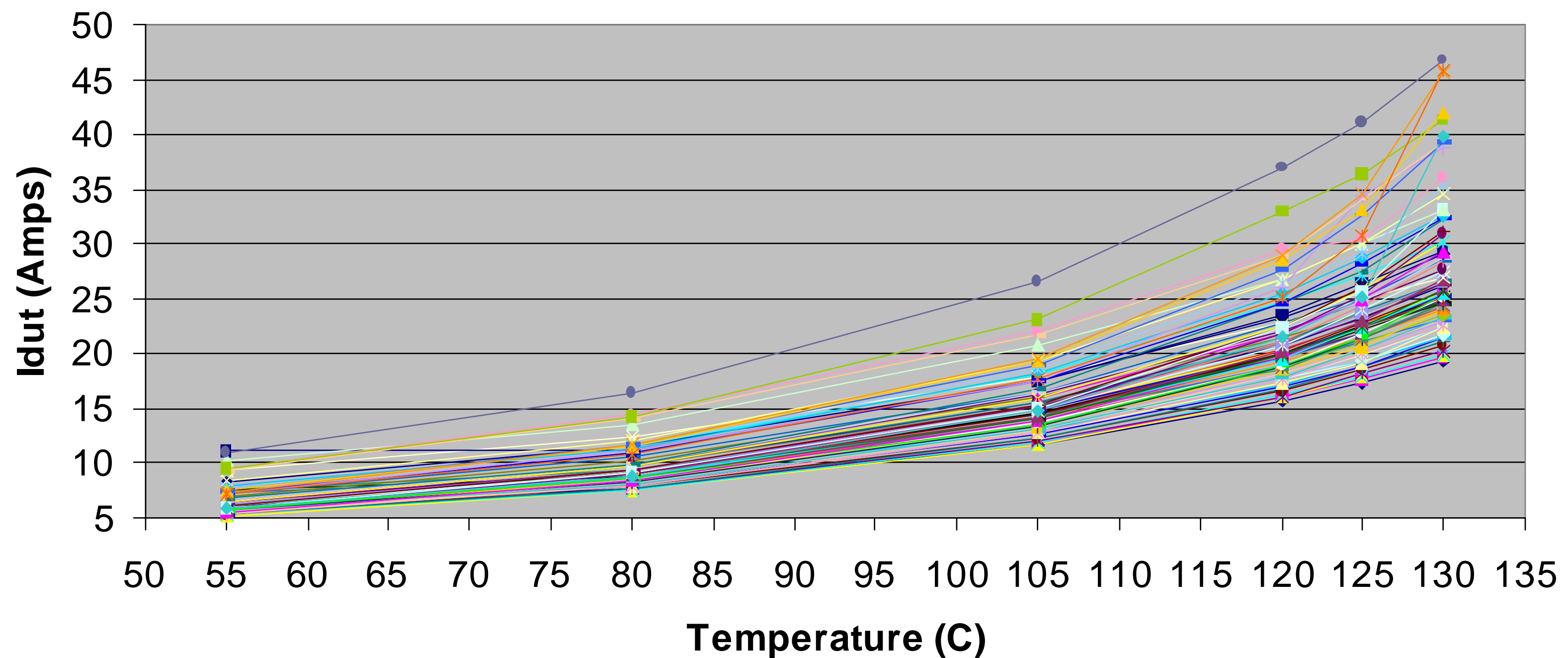
VOLTAGE VS. POWER
A TYPICAL CURVE SET



TEMPERATURE VS. POWER A TYPICAL CURVE SET



POWER VARIATION
The other half of the first order problem



DEFINITION OF TERMS

Power and power variation nomenclature

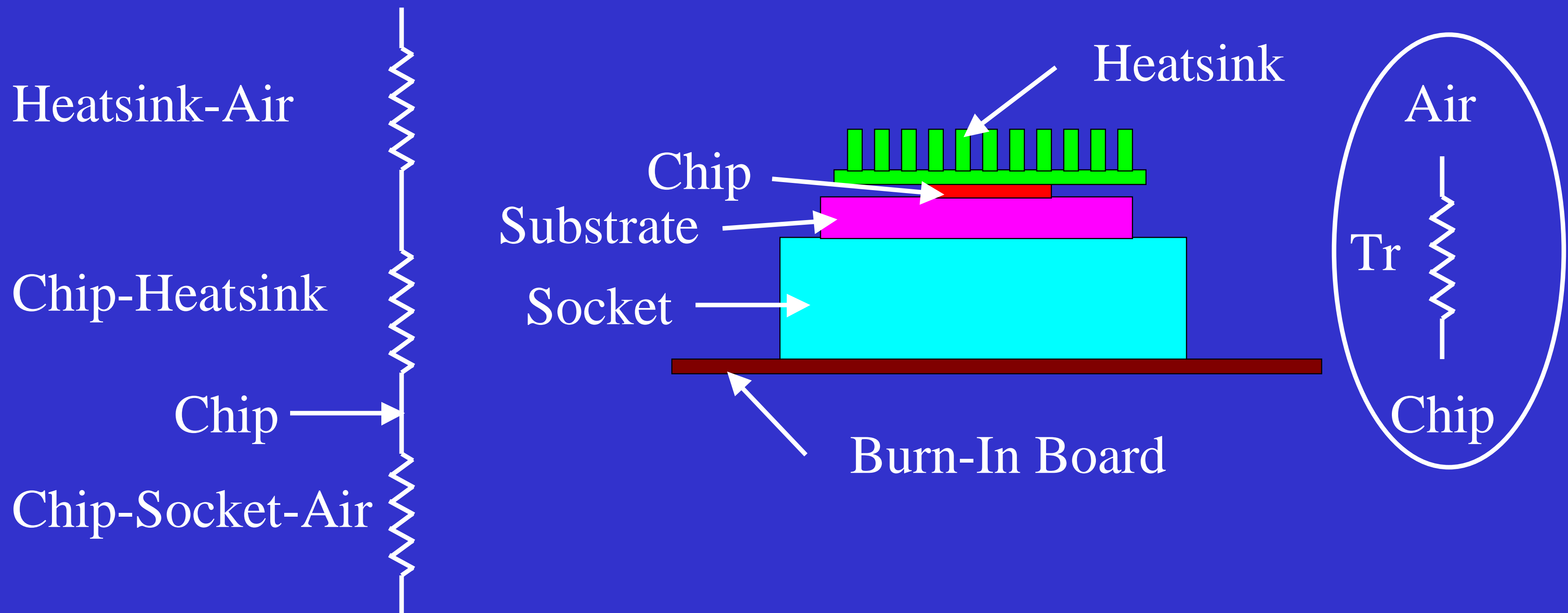
– Nominal power, +/- variation as % x nom

– 20W, 50% = 10W lowest, 30W highest

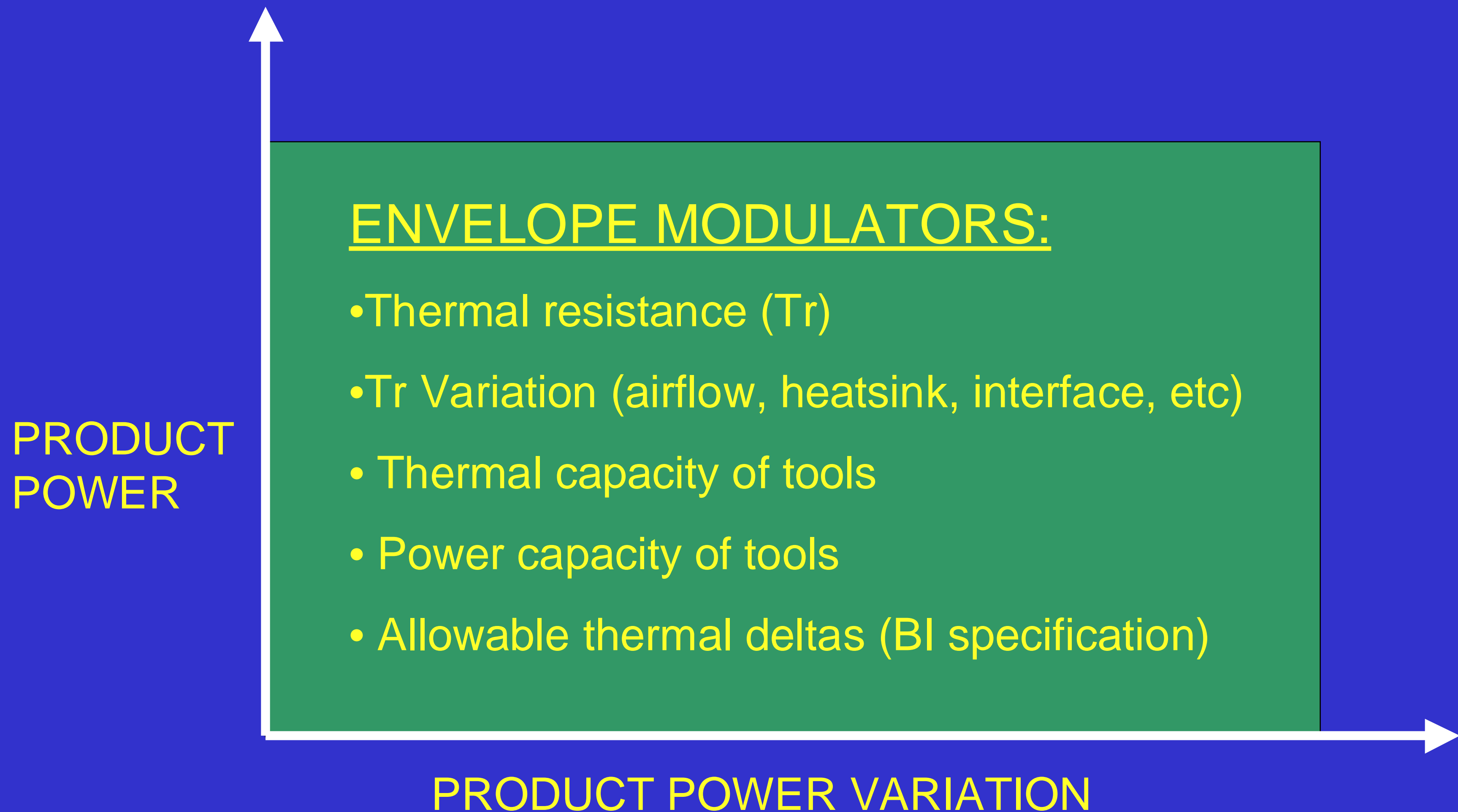
Thermal control nomenclature

- Passive – no active control, bulk cooling
- Active – control system per DUT
- Active 1 – active heating (or cooling)
- Active 2 – active heating and cooling

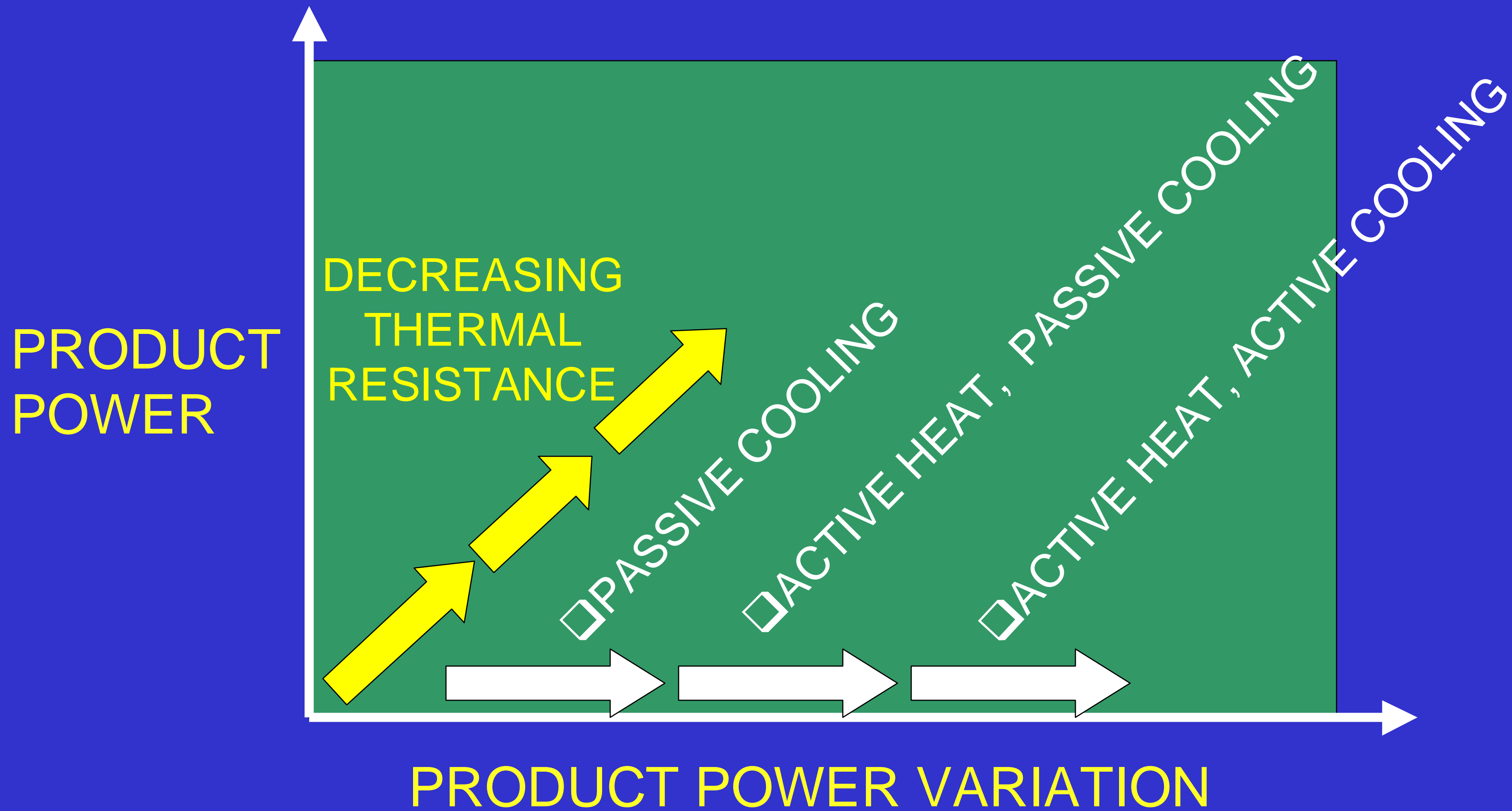
THERMAL RESISTANCE (as used in the examples)



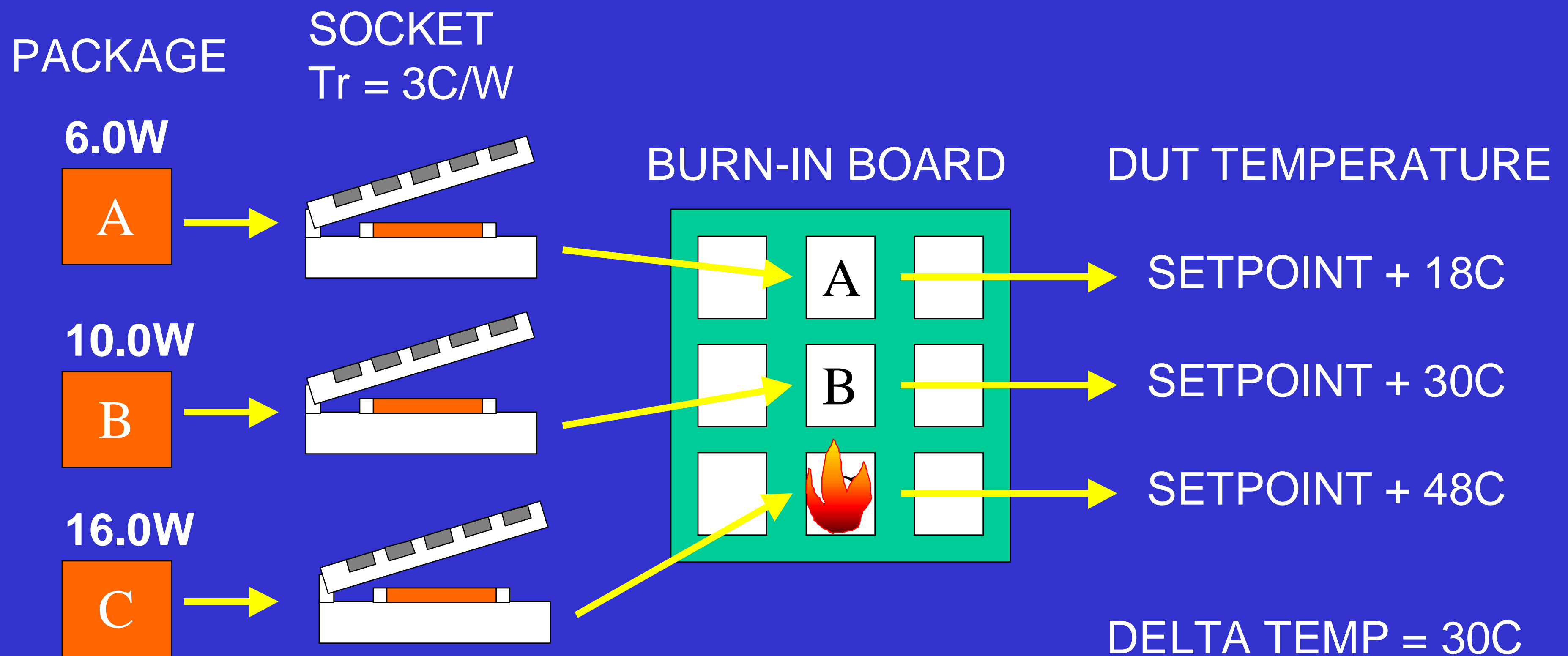
TOOLING POWER THERMAL CAPABILITY ENVELOPE



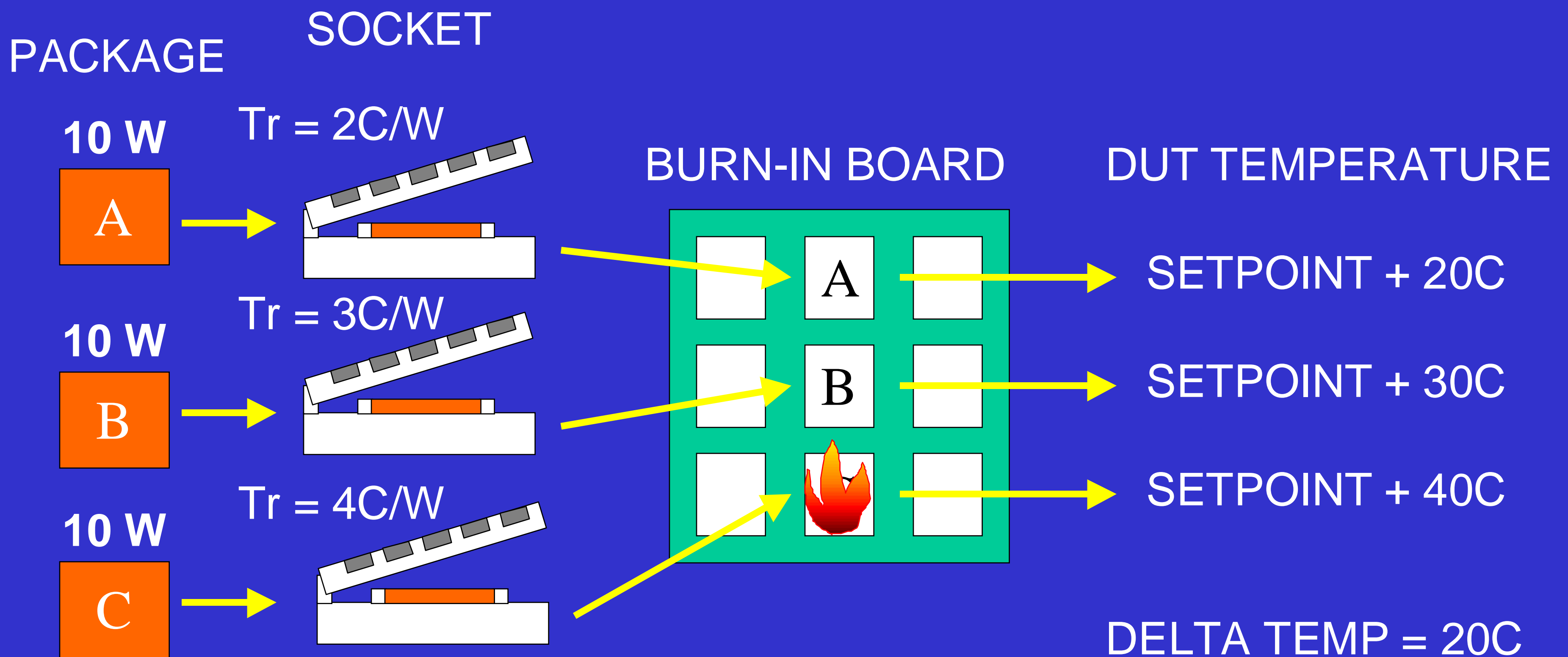
TOOLING POWER THERMAL CAPABILITY ENVELOPE



POWER VARIATION IMPACT (passive example)

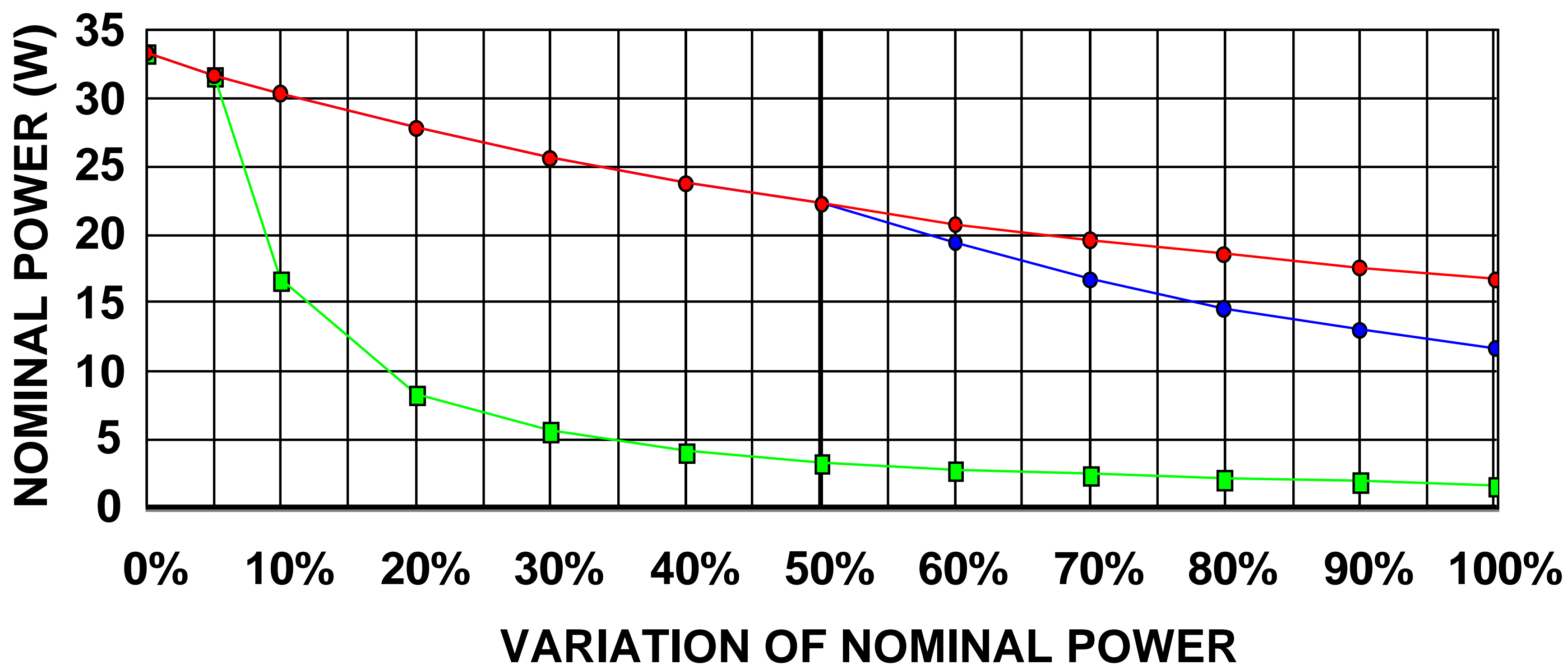


THERMAL RESISTANCE IMPACT (passive example)

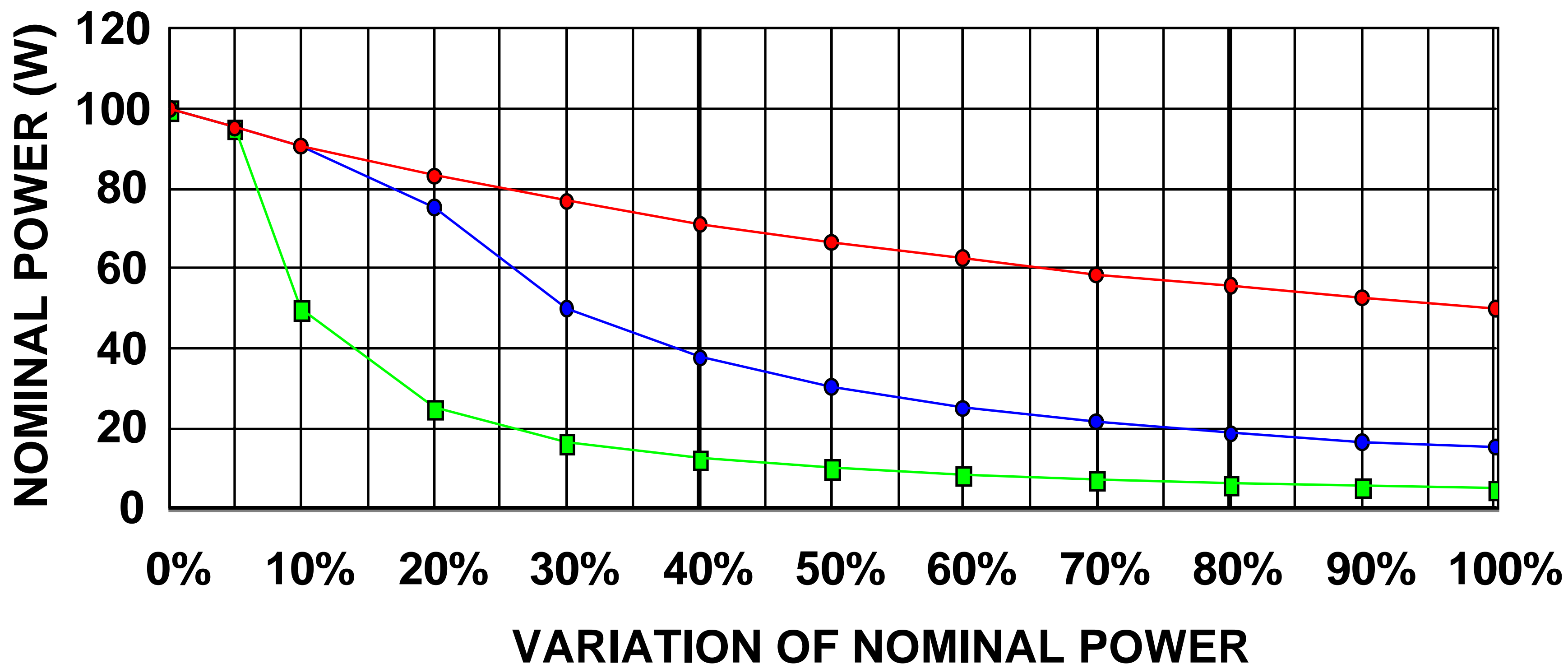


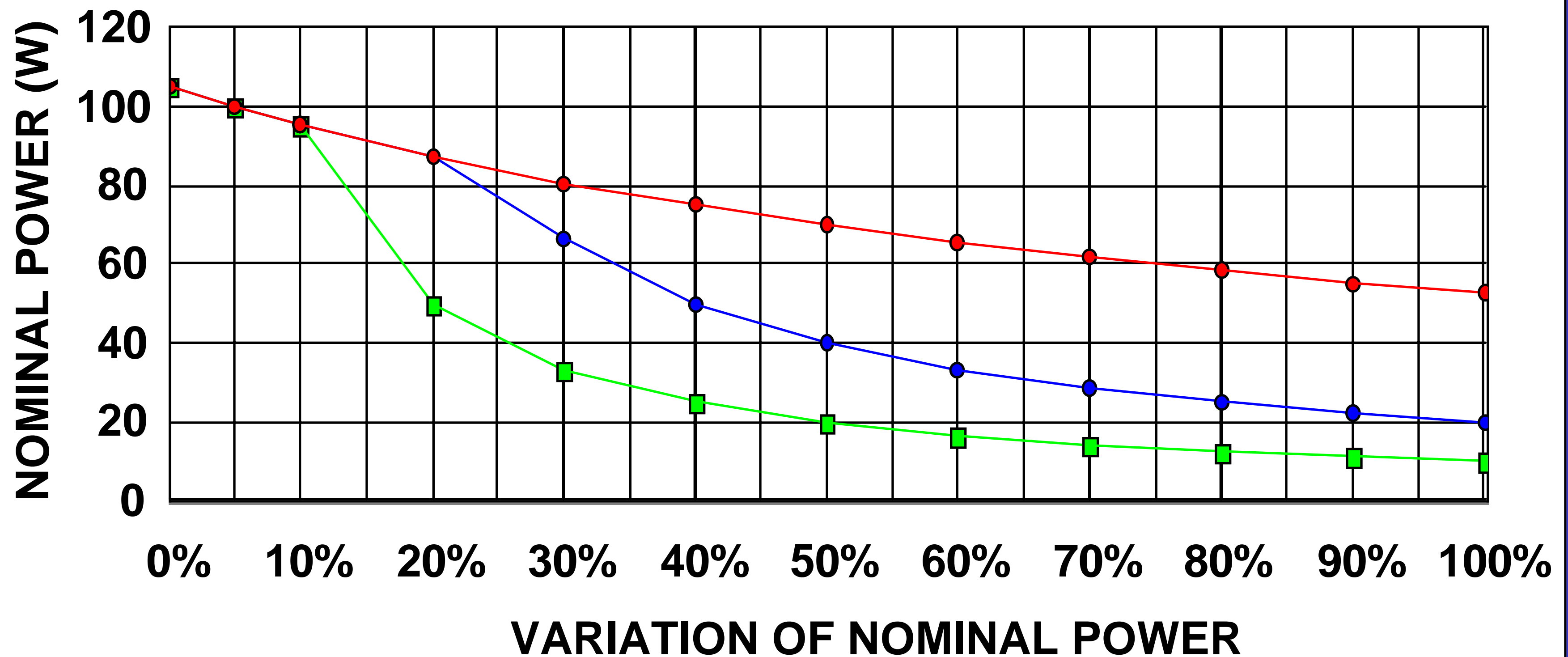
TOOLING CAPABILITY COMPARISON

3 C/W Socket (no variation), 140C +/-5C DUT Temp Spec



MIN FLUID TEMP = 45C
20W EFFECTIVE HEATER ON ACTIVE 1


TOOLING CAPABILITY COMPARISON
1 C/W Socket (no variation), 140C +/-5C DUT Temp Spec
PASSIVE
ACTIVE 1
ACTIVE 2
NOMINAL POWER (W)
120
100
80
60
40
20
0
0%
10%
20%
30%
40%
50%
60%
70%
80%
90%
100%
VARIATION OF NOMINAL POWER
MIN FLUID TEMP = 45C
20W EFFECTIVE HEATER ON ACTIVE 1


TOOLING CAPABILITY COMPARISON
1 C/W Socket (no variation), 140C +/-10C DUT Temp Spec
PASSIVE
ACTIVE 1
ACTIVE 2
NOMINAL POWER (W)
120
100
80
60
40
20
0
0%
10%
20%
30%
40%
50%
60%
70%
80%
90%
100%
VARIATION OF NOMINAL POWER
MIN FLUID TEMP = 45C
20W EFFECTIVE HEATER ON ACTIVE 1

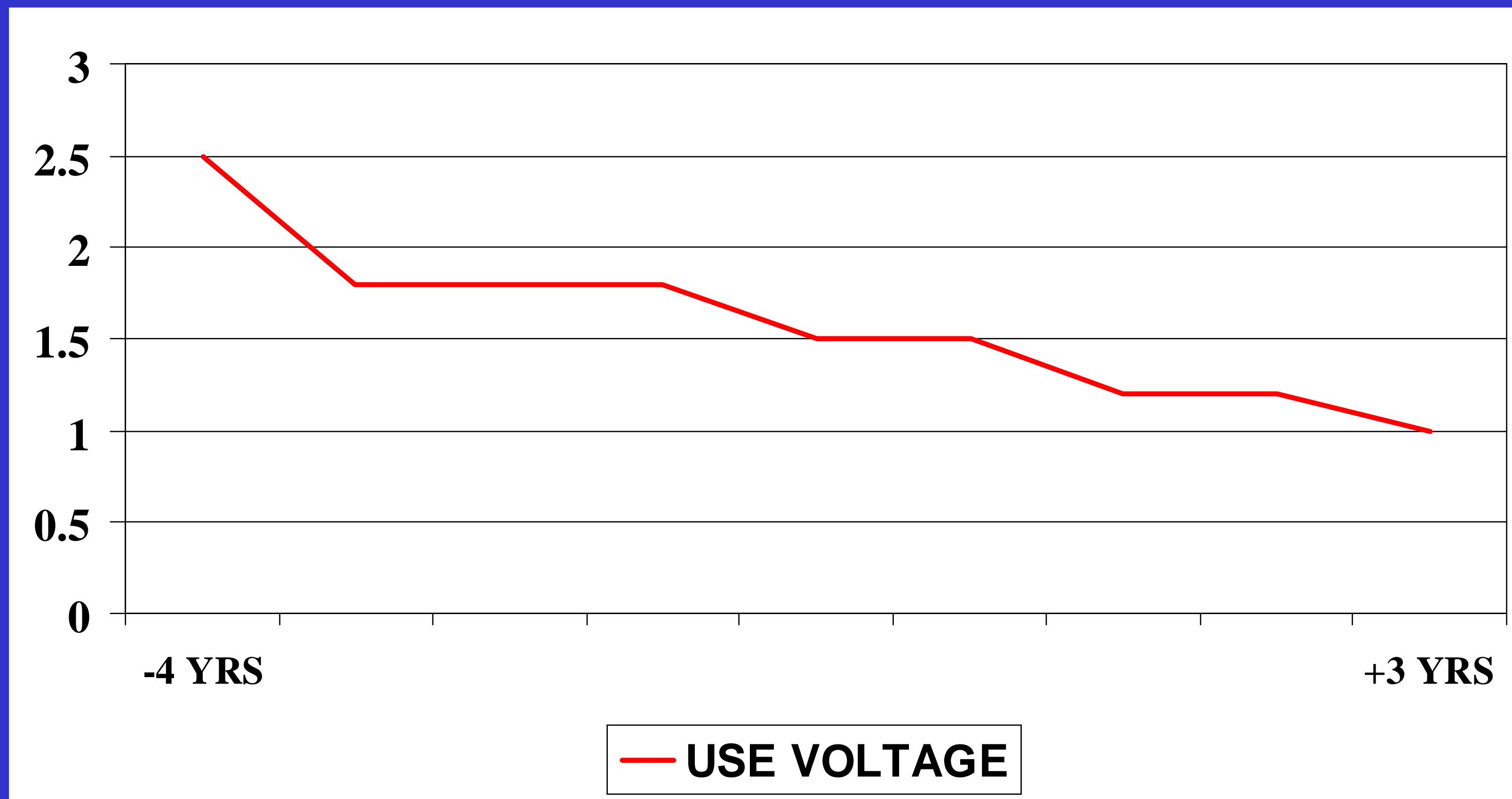
WHAT ARE THE OPTIONS WHEN TOOLING CAPABILITY IS LIMITED?

- Reduce the variation of power
  - Sort the distribution
  - Tradeoff is efficiency
  - Understanding tooling capability is critical
- Reduce the power
  - Lower the voltage
  - Lower the temperature
  - Tradeoff is effectiveness of BI (reliability)

SECOND ORDER TECHNOLOGY TRENDS ALSO IMPACT BURN-IN

- Use voltage decreasing with each technology
  - Voltage delta (use to burn-in) decreases
  - Effective BI acceleration factor decreases
- Power is increasing in the application
  - Leakage (Ioff) and AC (switching)
  - Application temperatures may grow
  - Temp delta (use to burn-in) decreases
- More burn-in required for less reliability

TECHNOLOGY APPLICATION VOLTAGE TRENDS

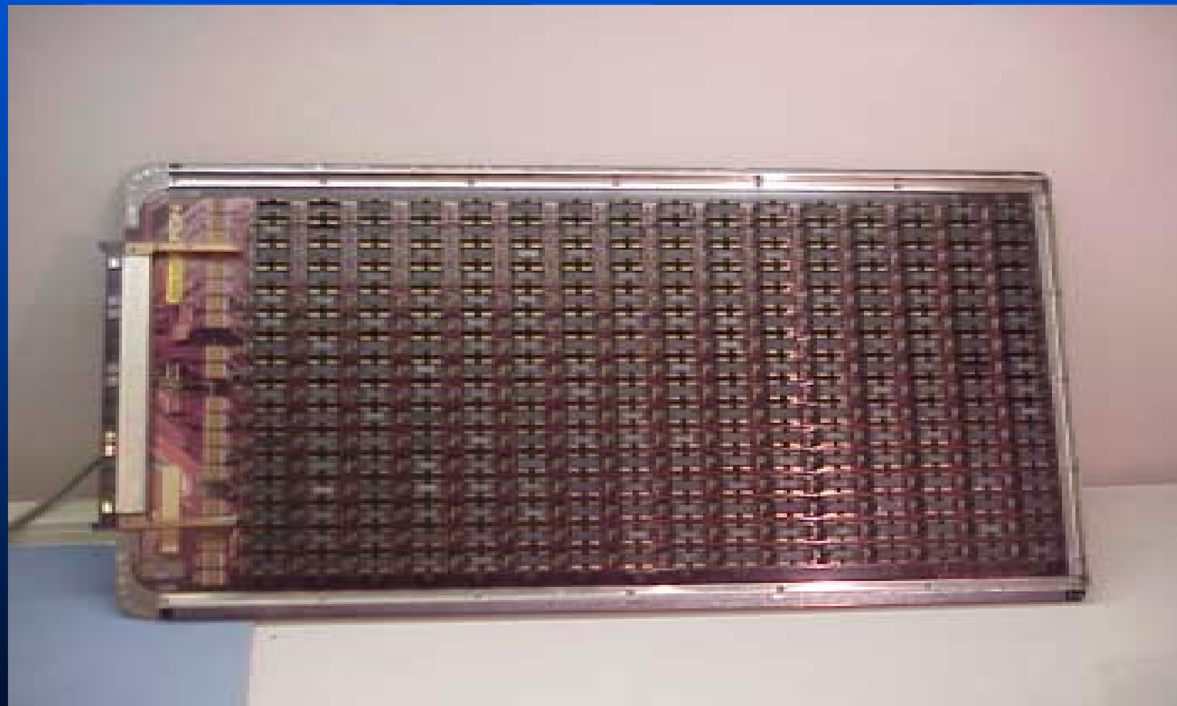


SOCKET DEVELOPMENT KEY FOCUS AREAS, A SHORT LIST

- Thermal solutions, thermal solutions, thermal solutions
- Low resistance thermal solutions
  - Chip interface, heatsinks, socket body
- Heat/cool thermal solutions
- Compliant thermal interface
- Robust temperature sensors
- Cost effective thermal solutions

BURNIN OF MEMORY DEVICES

A look at the past, present and future of memory packaging and interconnect systems.



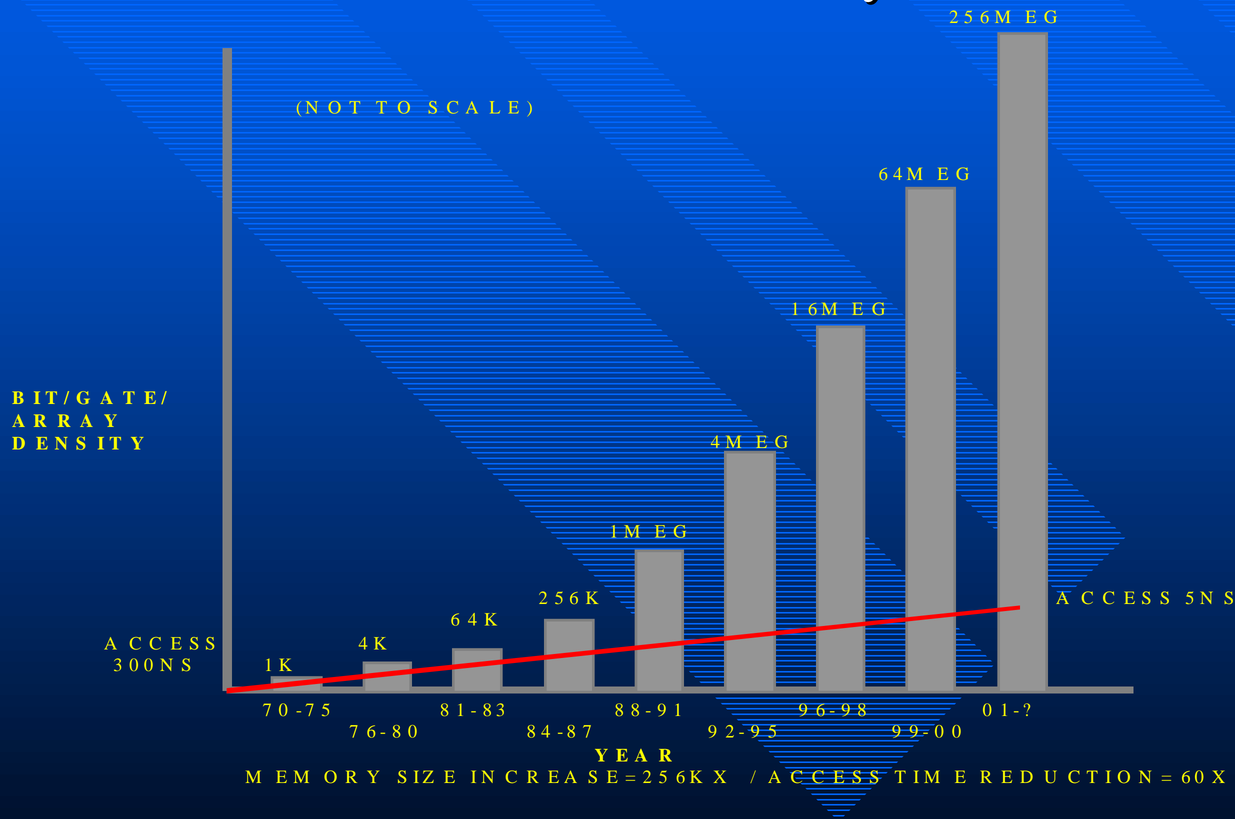
Daniel Cram

AGENDA

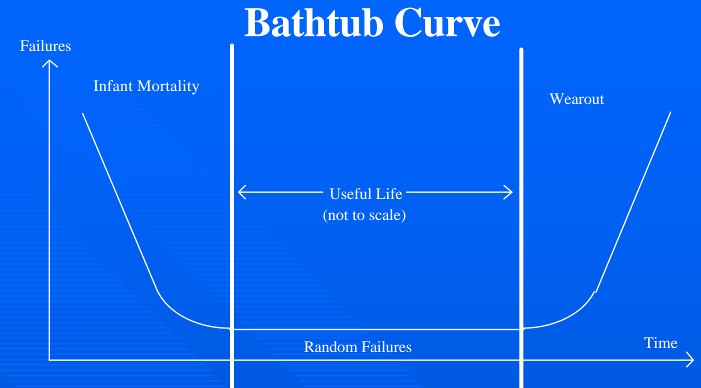
- DRAM
  - What is it?
  - What is BurnIn?
- MEMORY PACKAGING
  - Driving forces
- BURNIN SOCKET TYPES
  - Clamshell
  - LIF
  - ZIF
- SOCKET COST
  - Packaging cost
- FUTURE?

DRAM

- Dynamic Random Access Memory
- Background
- DRAMs are a commodity/Refresh



BURNIN



- MONITORED/INTELLIGENT
  - FAILURES IN TIME
  - REDUCED BURN RATES/RAPID DURATION REDUCTION
  - GANGED TEMPERATURE ENVIRONMENT
- MPT
  - BATCH PROCESS
  - DATA RETENTION/TIME INTENSIVE TESTS

- SPEED MATTERS
  - TEST SYSTEM IS INTERCONNECT SENSITIVE
  - INTEGRATED WAVEFORMS
  - NANO SECOND EVENTS/OVER-KILL/FALSE FAILURES

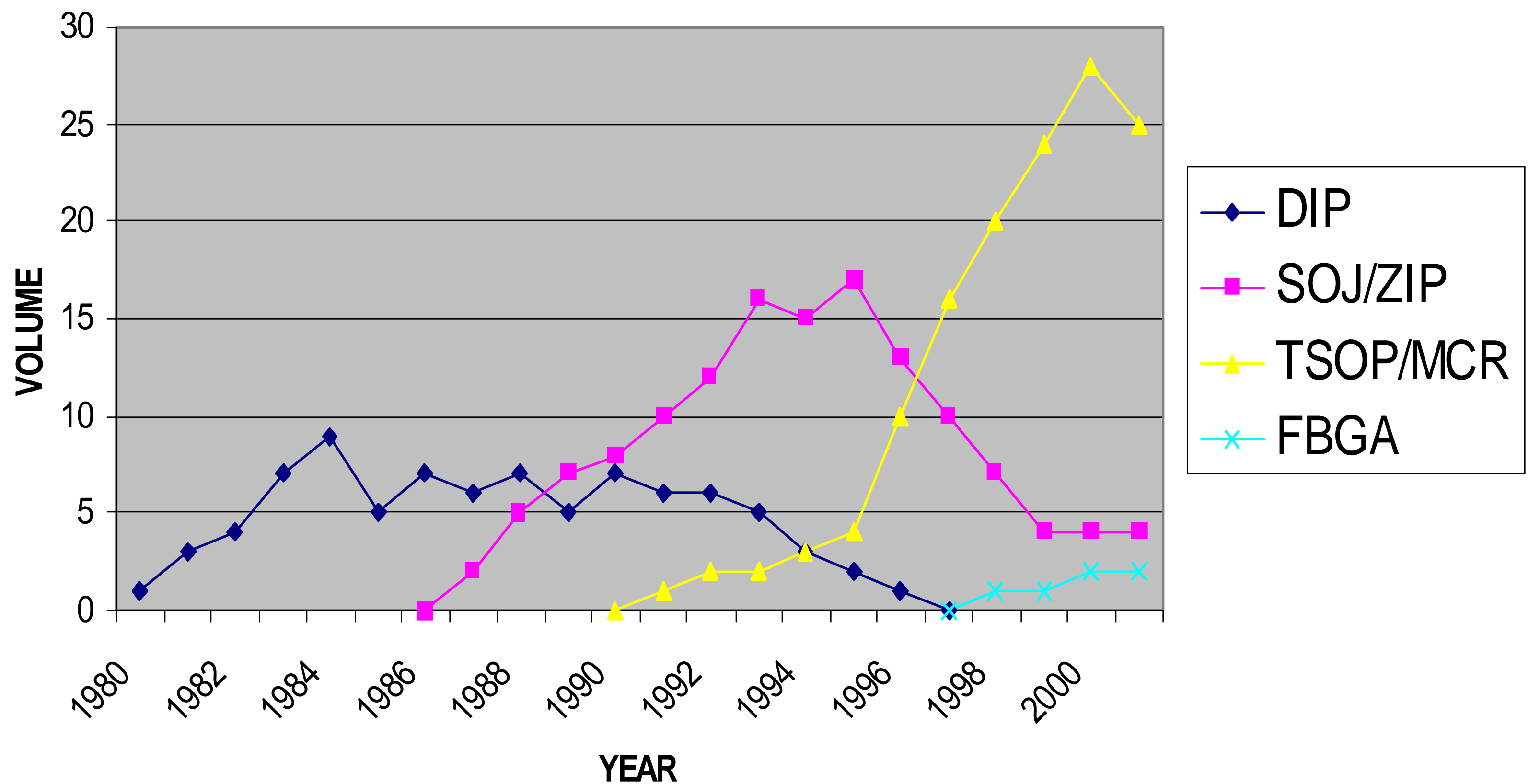
MEMORY PACKAGING

- HISTORY

  \- Memory packaging, over the last 20 years, can be divided into four primary groups; DIP, SOJ, TSOP, & FBGA.

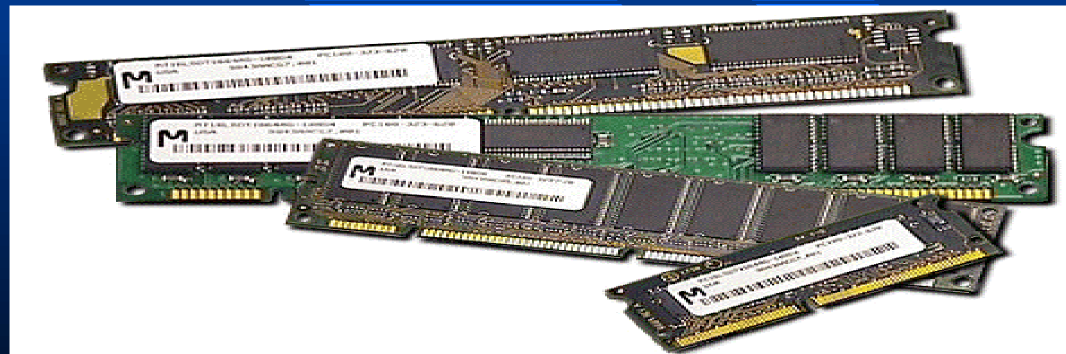
- PITCH PROGRESSION/LEAD COUNT

  \- DIP 2.54MM   <= 18 LEAD
  \- SOJ 1.27MM/.8MM <= 42 LEAD
  \- TSOP .8MM/.65MM/.5MM <= 86 LEAD
  \- FBGA .8MM/.75MM <= 90 BALL


MEMORY PACKAGING
VOLUME
30
25
20
15
10
5
0
1980
1982
1984
1986
1988
1990
1992
1994
1996
1998
2000
YEAR
DIP
SOJ/ZIP
TSOP/MCR
FBGA

DRIVING FORCES FOR PACKAGE CHANGE

- I/O COUNT - Wider buss - Increased array size
- Mother board space/module density (Surface mount)
- Die size
- Package electrical performance
- Memory modules have become one of the primary driving forces for component size and outline



BURNIN SOCKET TYPES

- Three basic types
  - Clamshell
  - LIF (Low Insertion Force)
  - ZIF (Zero Insertion Force)

- Package typically dictates designed required, however, other driving factors are;
  - Level of automation needed
  - Environment
  - Pitch
  - Level of performance
  - Cost
  - etc.

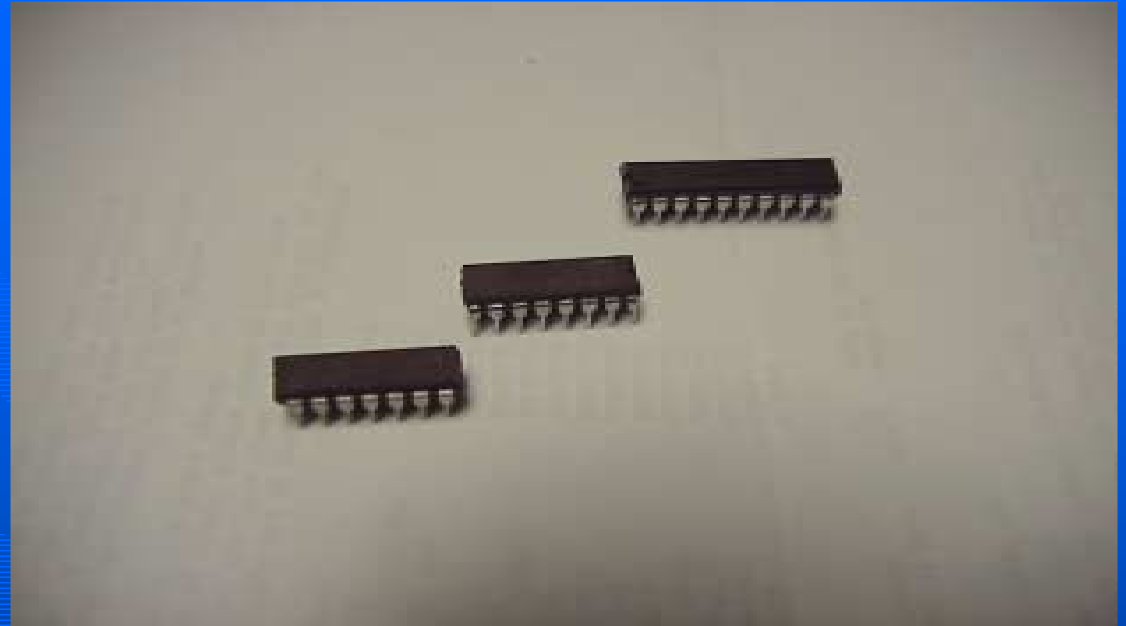
CLAMSHELL

- Advantages
  - -Reliable interconnect
  - -Standardized contact/body outline
  - -Can accommodate quad and large pin arrays
- Disadvantages
  - -High part count
  - -Two additional steps for automation
  - -High cost
- PRIMARY ROLE
  - -For TSOP/QFP early development

LIF

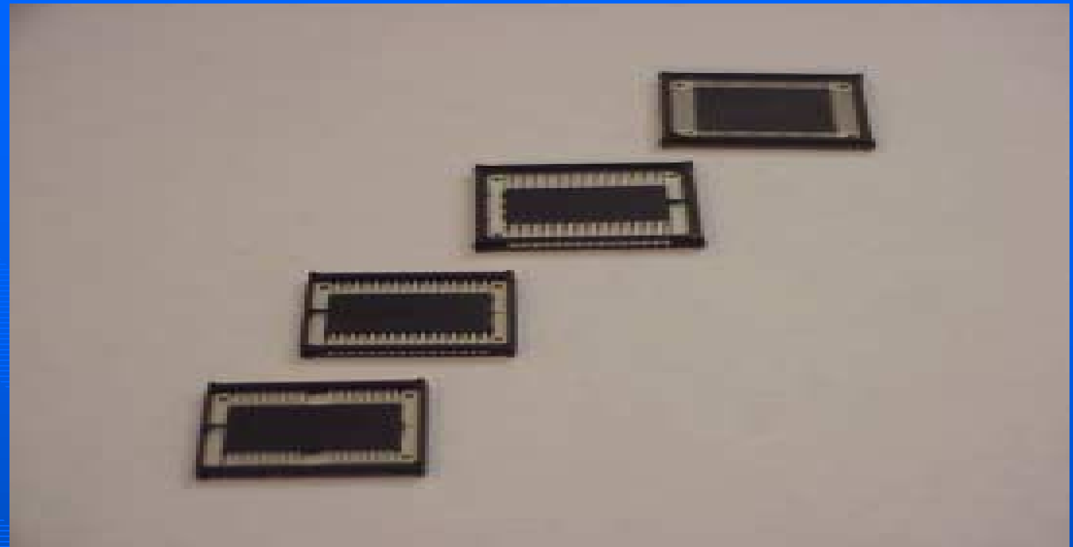
- Advantages
  - -Large surface area/scrub zone
  - -Low part count
  - -Ease of automation
  - -Low cost
- Disadvantages
  - -Practical pitch limitation is .8mm
  - -<50LD I/O count
  - -Package/lead-frame damage due to direct entry
- PRIMARY ROLE
  - -For DIP, SOJ, & MCR

DIP



SOJ

MCR



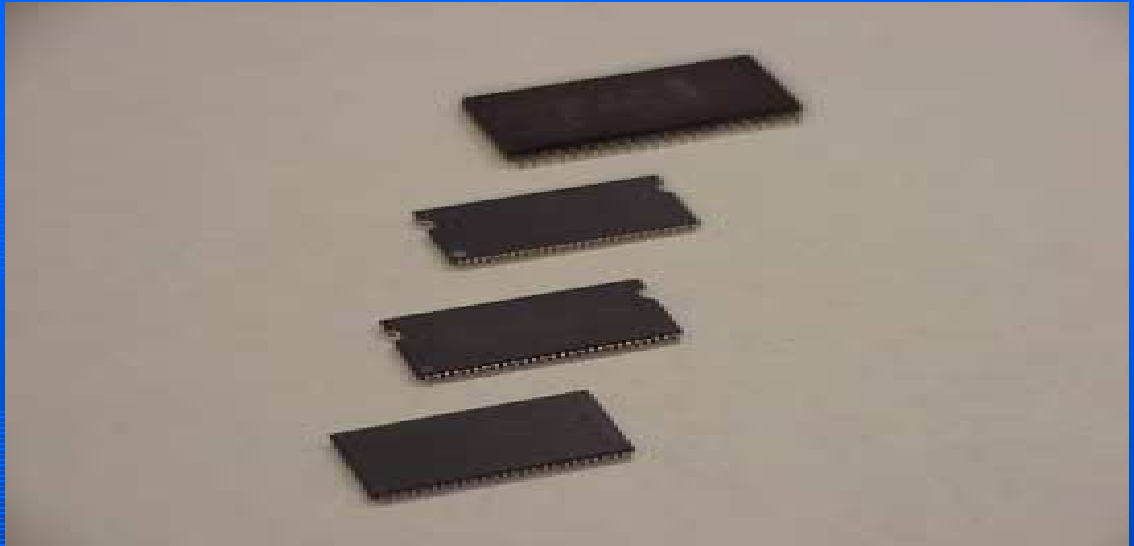
ZIF

- Advantages
  -Accommodates tight pitch with limited lead damage
  -Lower component count than clamshell
  -Pitches down to .5mm
  -Ease of automation
  -Low cost

- Disadvantages
  -Limited scrub area or wipe zone
  -Prone to long-term tin/lead transfer failure

- PRIMARY ROLE
  -For TSOP

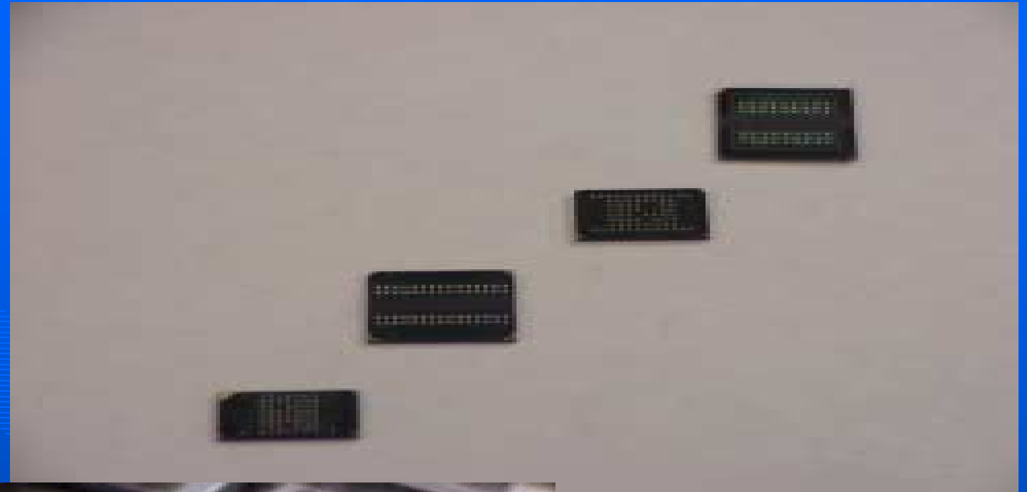
TSOP



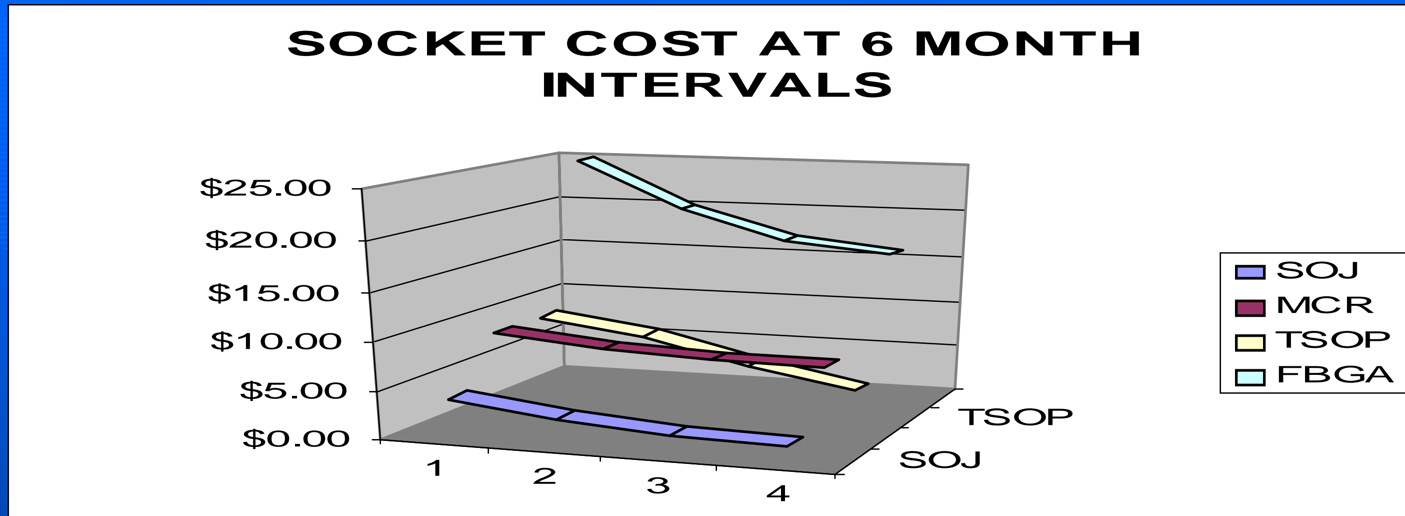
ZIF FBGA

- Advantages
  - -Accommodates tight pitch with limited ball damage
  - -Pitches down to .65mm
  - -Ease of automation
  - -Multi-point contact designs
- Disadvantages
  - - Lack of standard/long lead-time for new array
  - - Prone to tin/lead build up and reflow (Ball damage/sticking/etc.)
  - -High cost
- PRIMARY ROLE
  - - For FBGA

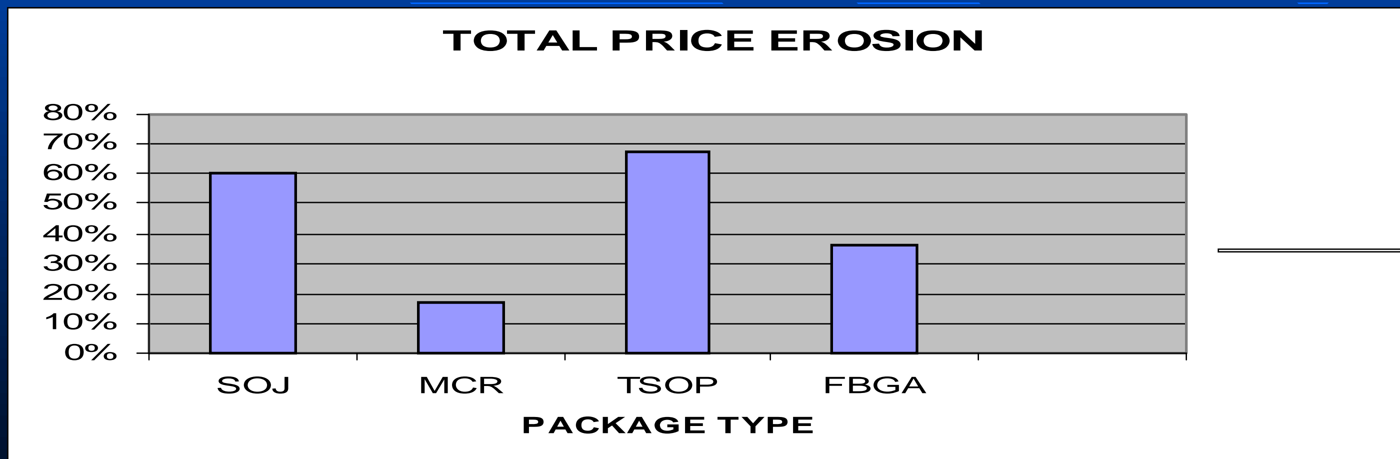
FBGA



SOCKET COST

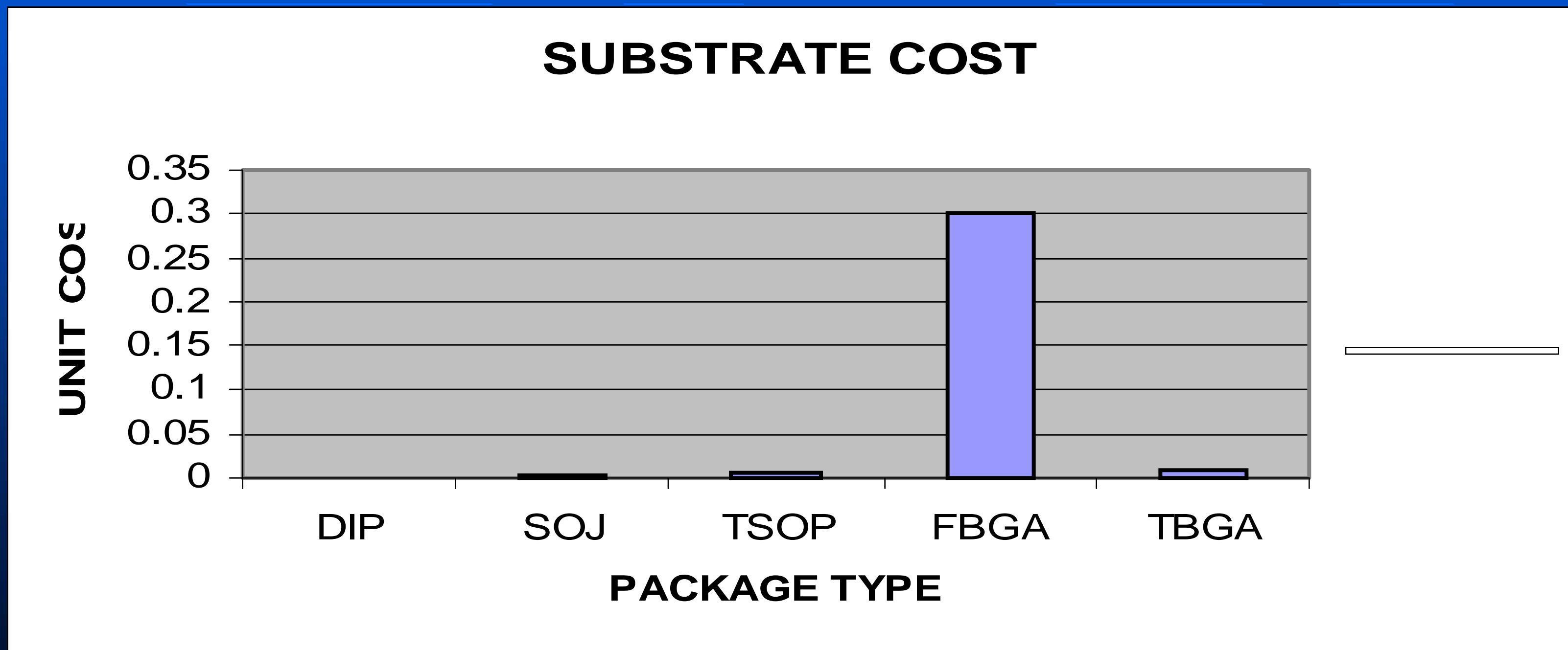


(What do sockets really cost to make anyway?)



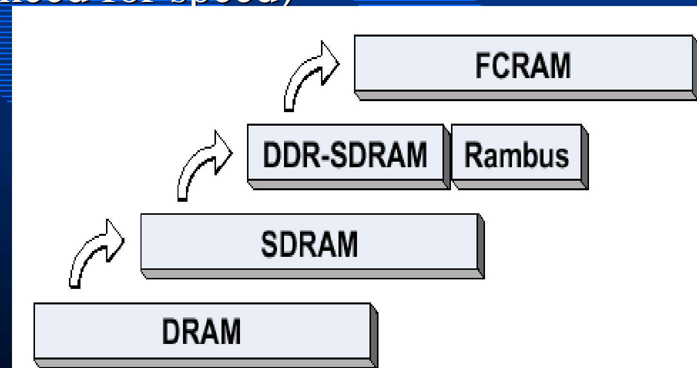
PACKAGE COST

- The primary cost in the packaging has always been the lead-frame or substrate.



FUTURE?

- Finer pitch FBGA/CSP packages
  - -<=.5mm
  - -COB, FCIP,etc.
- Flip-Chip
- Memory based MLF package?
- Due to high cost of test fixturing
  - -Test in strip (The need for speed)
  - -Module level
  - -Wafer level



FBGA/CSP

- Even if the cost of the package drops the cost of the sockets remain high.
- Solder transfer and reflow problems remain a stigma
- Package/substrate integrity?
- TBGA

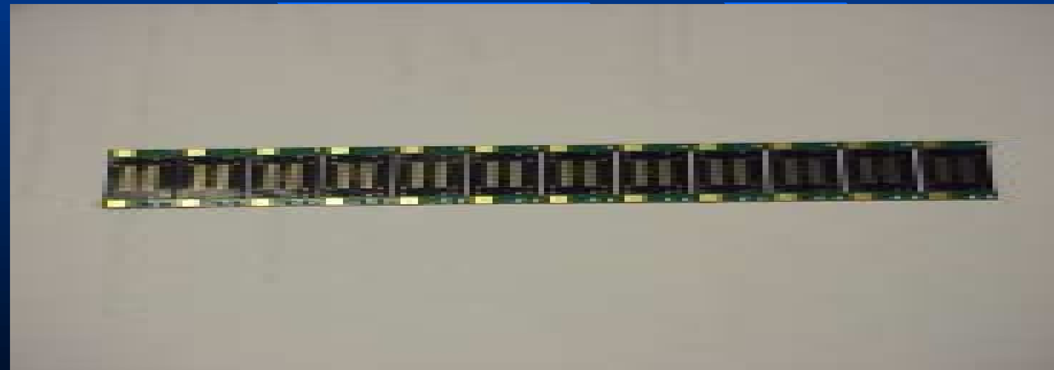
  - Tape based ball grid array appears to be a cheap alternative to rigid and semi-rigid substrates.

FLIP-CHIP

- Redistribution technology is still maturing.
- Pad array/grid is outline dependant
  -Die shrink can force retooling
- Handling bare die
  -Chipping/cracking
- If bumped
  - requires clamshell or force distribution method

STRIP TESTING

- Adjacent cell electrical connections must be isolated
- Socket/board density can be negatively impacted
- Matrix lead-frame generally do not accommodate this approach
- Failures tie-up process unless excised
- Second pass excise operation
- Etc.,Etc...

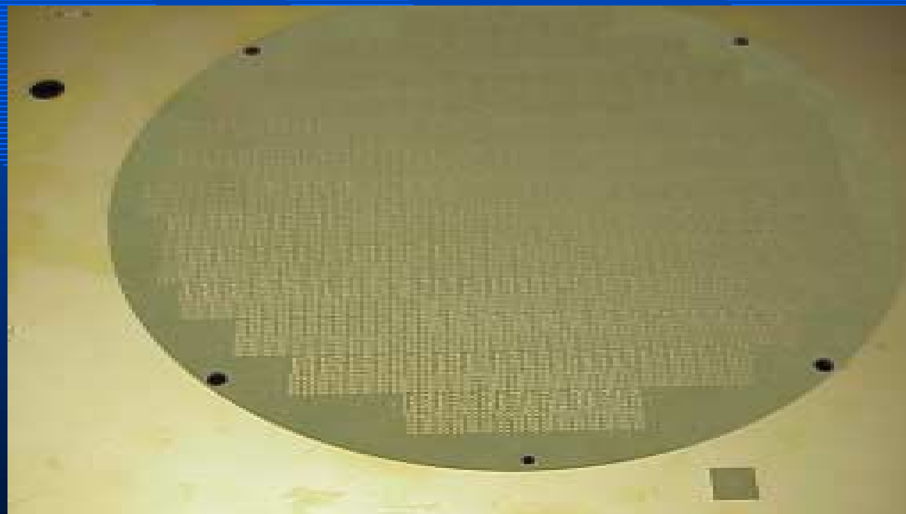


MODULE LEVEL

- Solder joint damage/cracks
- Passive component damage
- Module repair bottleneck
- Ultimate cost of scrap and recovery efforts
- Module size and power requirements could be issue for typical chambers
- Conventional/singulated component sockets may still have to be developed

WAFER LEVEL

- Die shrink requires retooling
- High risk associated with wafer handling/processing (ie: Scrap cost $$)
- Conventional socketing/tooling would still have to be developed



SUMMARY

- The single greatest challenge facing the memory producers is cost. (Margins are tight.)
- The demand for KGD is greater now than it ever was. (But the cost to process remains high.)
- The ultimate direction will likely be a variant of all the noted possibilities with production and cost factors dictating
- MODULE density, cost and performance being a primary goal/driving force

AREAS OF CONFLICT AND BOTTLENECKS

Joseph J. Riggs

Lucent-Bell Labs

Agere Systems

Allentown, Pennsylvania

Abuser of Test and Burn-In Sockets

- 1. Used at high and low temperatures
- 2. Thousands of BI cycles
- 3. Expect the sockets to work on all pins at test conditions

BI & Reliability at the Back End

- 1. Must worry about the small stuff or the job can become messy
- 2. Examples:
  - A. Titanic - 1912
  - B. Mars Lander - 1999
  - C. Company XYZ designing and packaging a device where a test and BI socket did not exist - 1995

- 1. Chip & Package Designers
- A. Not aware of testing and BI
- B. Not familiar with Reliability
- C. Do not think about job cost

Small Stuff

- 2. Cost
- A. $0.50 to $1.00 per pin
- B. $3,000-$10,000 socket cost per BI board
- C. Designers and Socket Manufactures share the blame

- 3. Reliable
- A. All pins work at test and BI conditions
- B. 100k or more device cycles required
- C.1k or more BI cycles required
- D. Socket repair and replacement easy

Small Stuff

- 4. Temperature
- A. Clam shell Vs. open top
- B. Open top Vs. no top
- C. No data available

Small Stuff

- 5. Drawings
- A. On time and accurate
- B. Able to read (Customer’s Language)
- C. Metric & English measurements
- D. Drawings reflect the socket
- E. Samples available

Small Stuff

- 6. Standard Footprints
- A. Standard footprints for device family
- B. Standard socket pin spacing
- C. Check with PCB manufactures

Small Stuff

- 7. Electrical Characteristics
- A. Low contact resistance, inductance and capacitance
- B. Maintain low values through lifetime

Small Stuff

- 8. Auto Load/Unload
- A. Desired?
- B. Difficult
- C. “Not my problem!”

Small Stuff

- 9. Socket data
- A. Difficult to obtain
- B. Inaccurate
- C. User asked to evaluate socket
- D. Data sometimes obtained from peers

Small Stuff

- 10. Cooperation
- A. Work together
- B. Share data
- C. Evaluate problems together
- D. Solve together

Conclusions

- 1. Small stuff can be killers
- 2. Without cooperation at all levels, the back end of the job can be messy

Questions?

- Contact:

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- Allentown, PA 18109
- 610-712-6433
- jjriggs@lucent.com