TEST ACCESS TO TODAY'S LEADING PACKAGES

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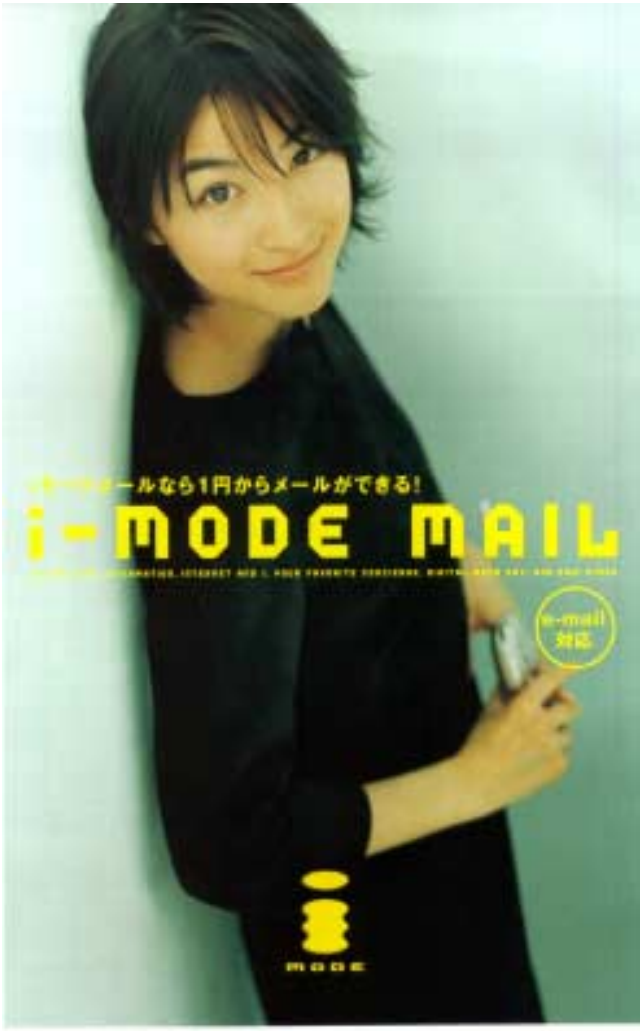
PORTABLE ELECTRONICS, THE MAJOR DRIVER FOR LEADING EDGE PACKAGES

- NTT DoCoMo's i-mode packet switching service is the most advanced mobile Internet service available.
- Five million subscribers since service started in 1999
- Uses 0.5mm pitch CSPs and wafer CSPs for RF functions such as PLL and flash memory.



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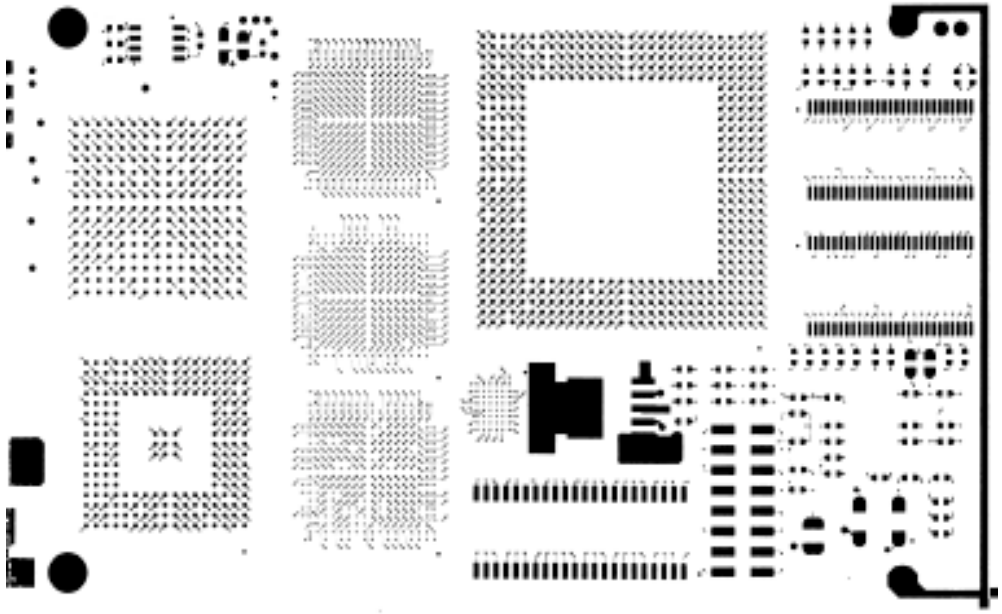
FINE PITCH PACKAGES MIGRATE FROM PORTABLE TO RACK EQUIPMENT IN THREE YEARS

- Large area communications boards (Cisco, Nortel) currently use ASICs in BGAs with 0.8mm pitch.
- Printed circuit technology is available from about 35 fabricators worldwide to economically interconnect packages at these pitches.
- Package test access lags, and is still largely based on single package sockets with stamped and formed metal contacts.



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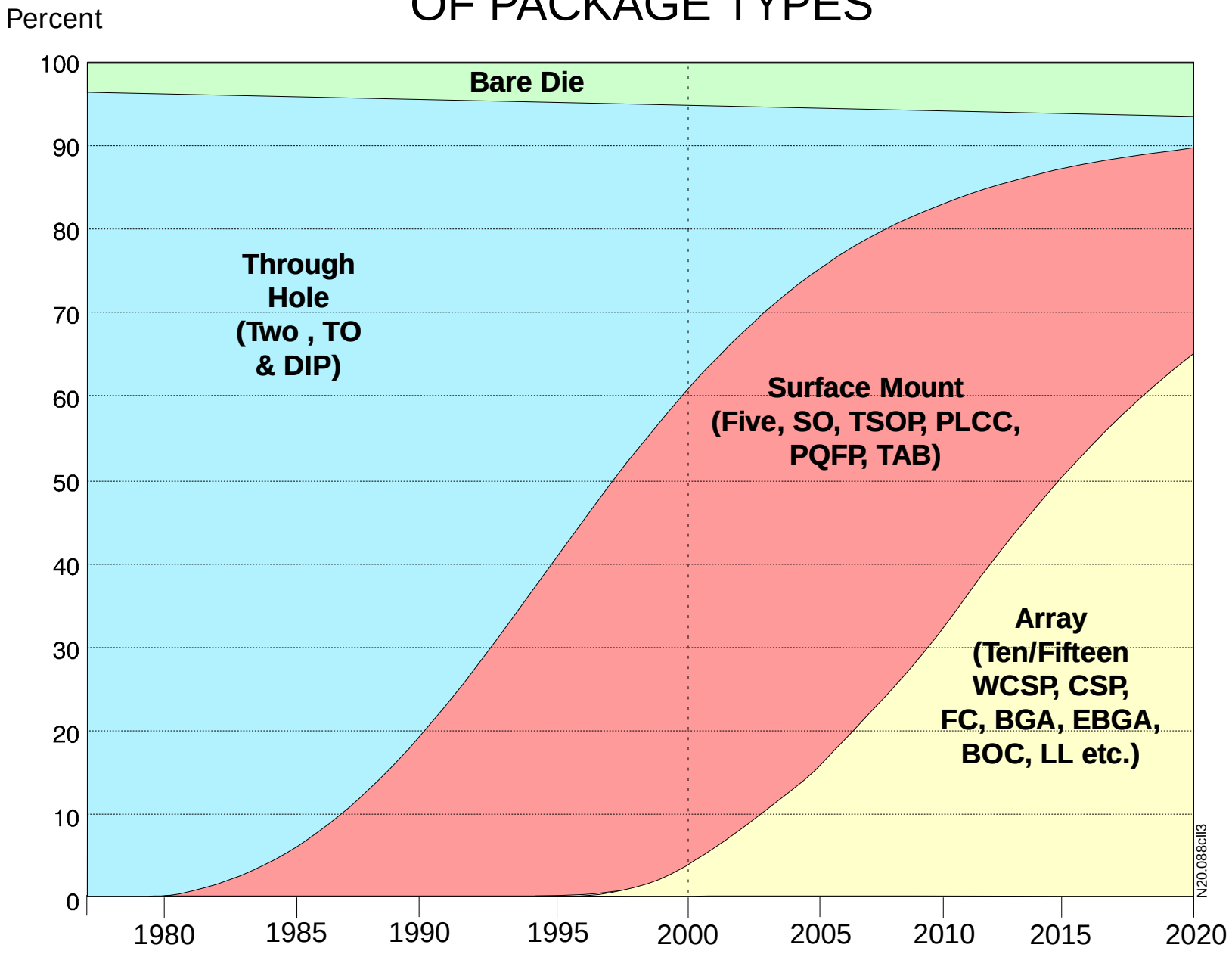
EACH WAVE OF PACKAGING BRINGS A PROLIFERATION OF PACKAGE TYPES



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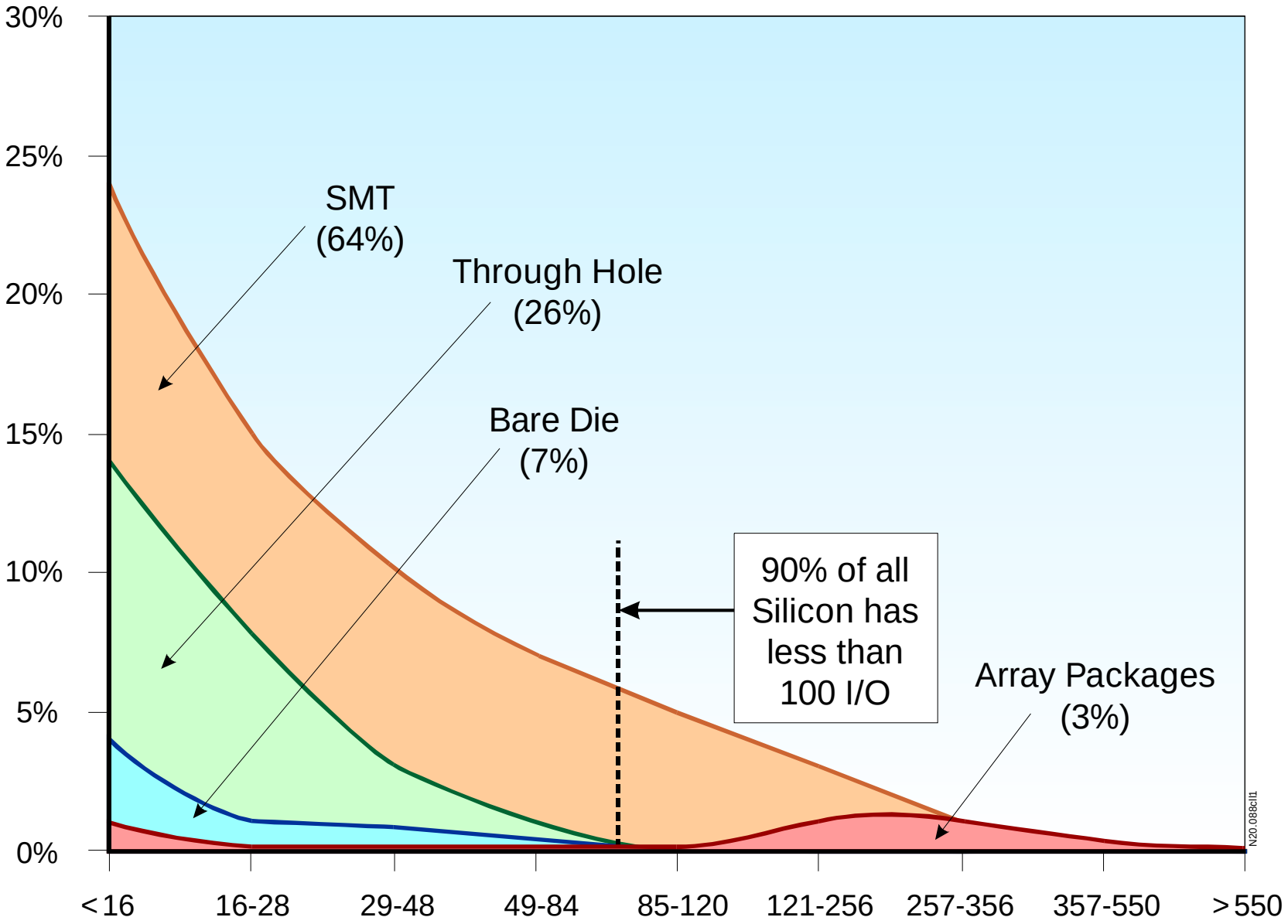
LOW LEADCOUNT STILL DOMINATES SILICON
“Market Share” by Leadcount and Package Type 1999



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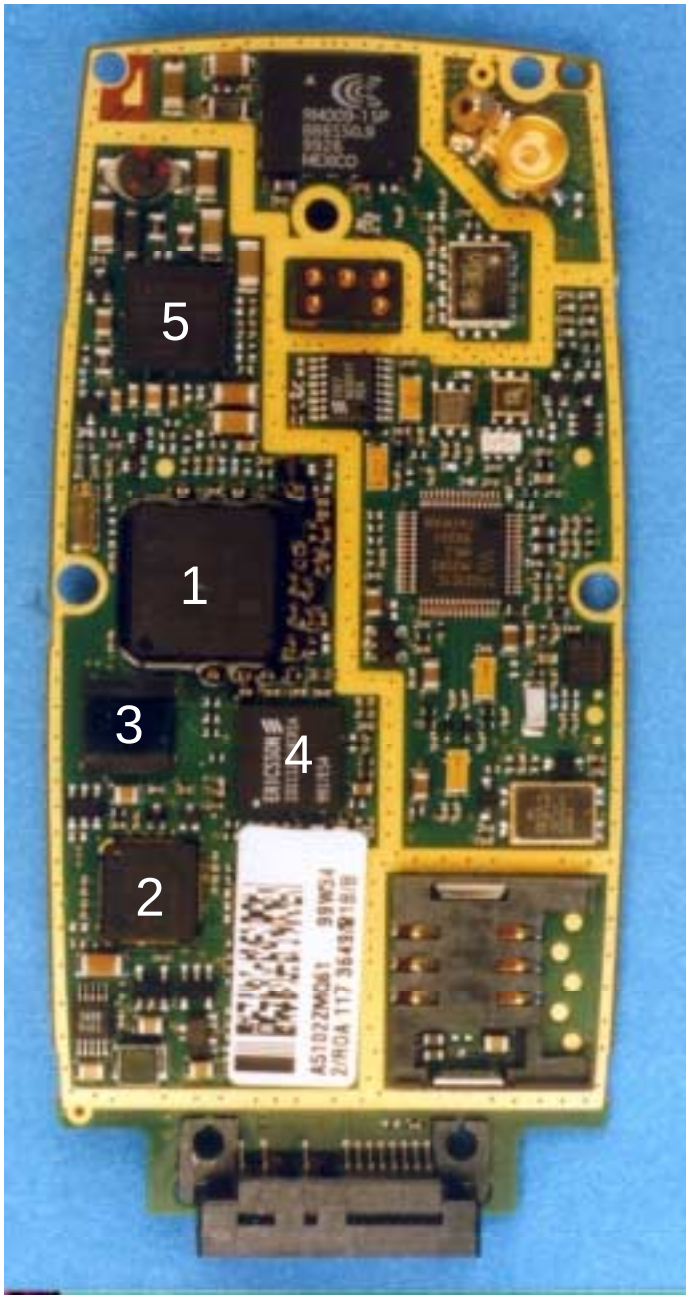
CHIP SCALE PACKAGES IN THE T28 BASEBAND SECTION

- Only one PCB assembly
  - 6 layer microvia from Suzuki
  - 125 µm laser vias, 110 µm lines
  - 30 attachment pads per cm^2
- Five CSP in baseband section
  1. Wirebond-on-flex CSP (Signal Processor)
     - 12 x 12 mm, 1.2 mm total height
     - 132 balls, 0.8 mm pitch
     - Underfilled
  2. Wirebond-on-Flex CSP (SRAM)
     - 8 x 8 mm, 1.3 mm total height
     - 64 balls, 0.8 mm pitch
  3. Tessera-type µBGA CSP (Flash)
     - 7 x 7 mm, 1.0 mm total height
     - 48 balls, 0.8 mm pitch
     - Underfilled
  4. Wirebond-on Rigid CSP (ASIC)
     - 8 x 8 mm, 1.5 mm total height
     - 64 balls, 0.8 mm pitch
  5. Wirebond-on-Rigid CSP (ASIC)
     - 8 x 8 mm, 1.5 mm total height
     - 64 balls, 0.8 mm pitch



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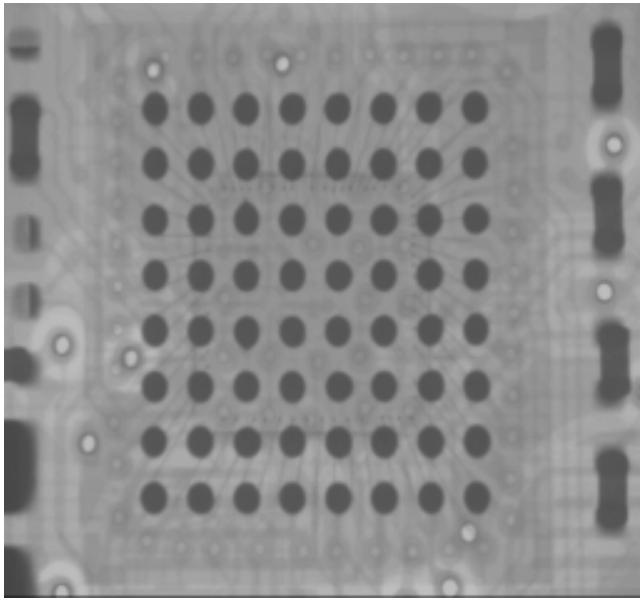
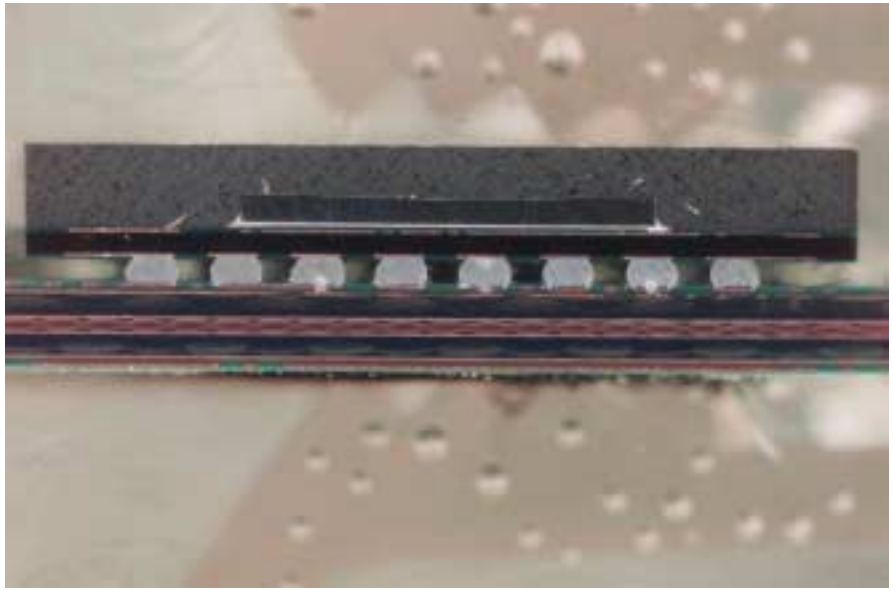
ERICSSON ASIC IN T28 PHONE

Wirebond-on-rigid CSP
Gang mold & dice

- 8 x 8 mm
- 1.5 mm total height
- 64 balls, 0.8 mm pitch
- No underfill





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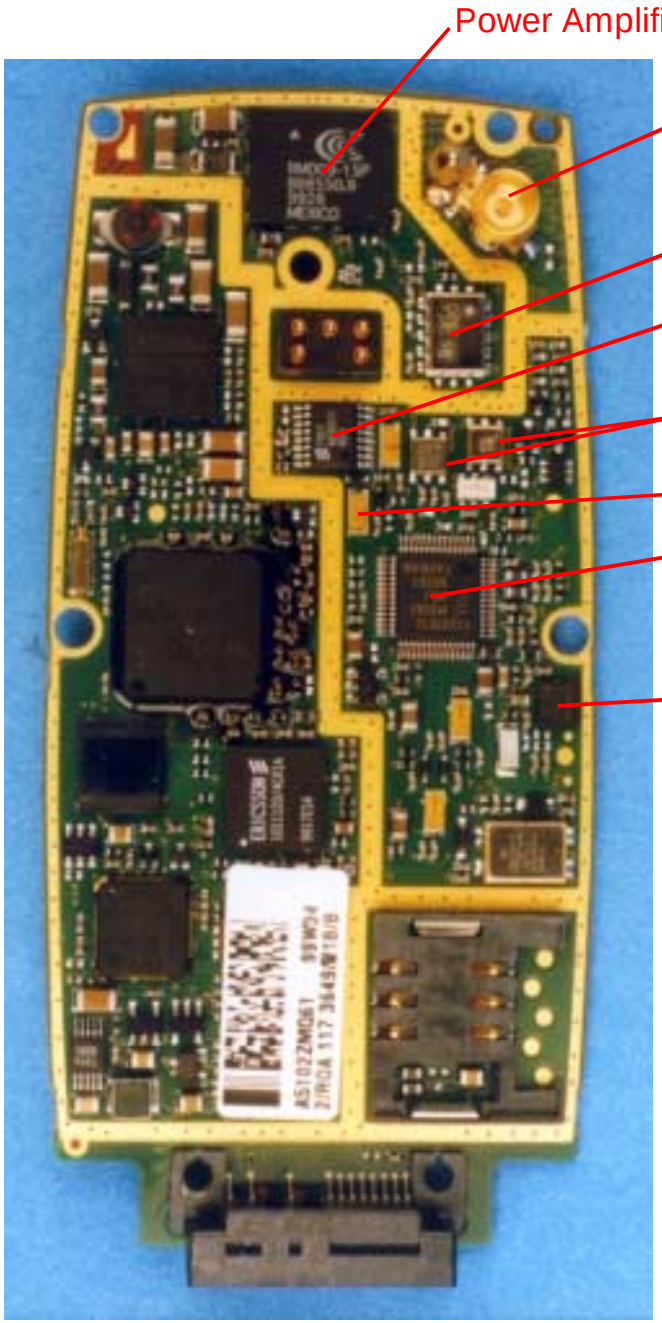
RF MODULE INTEGRATION IN THE T28 PHONE

- Ericsson Receiver
  - 64 lead QFP, 0.4 mm pitch
- Conexant Power Amplifier
  - 9.1 x 11.6 x 1.6 mm
  - 4 layer BT PCB carrier
  - Wirebonded die and SMT passives
- Murata Switchplexer
  - 6.7 x 5.0 x 2.0 mm
  - LTCC with integrated passives
  - SMT passives on top
- National Semiconductor VCO IC
  - 3.5 x 3.5 x 1.3 mm
  - Wirebond-on-rigid CSP
  - 16 external pads, no balls



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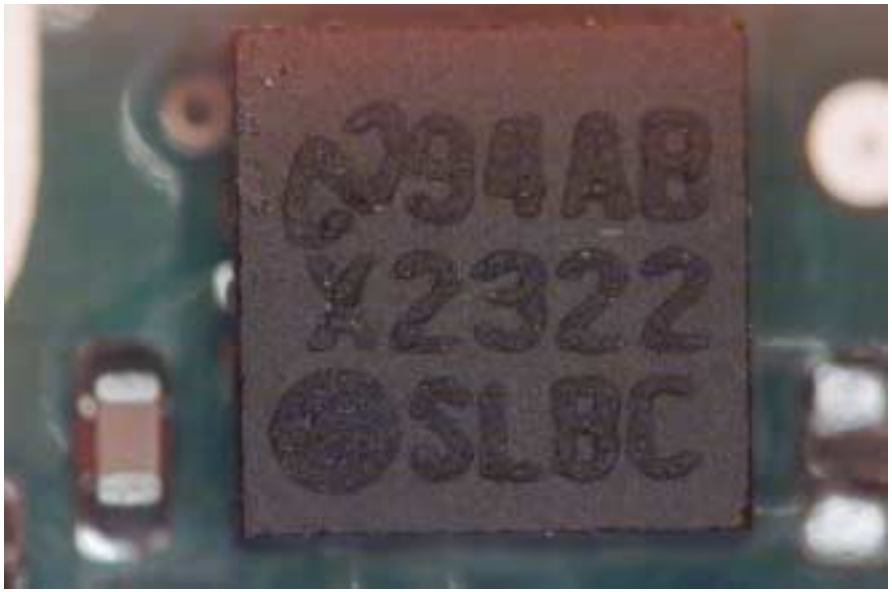
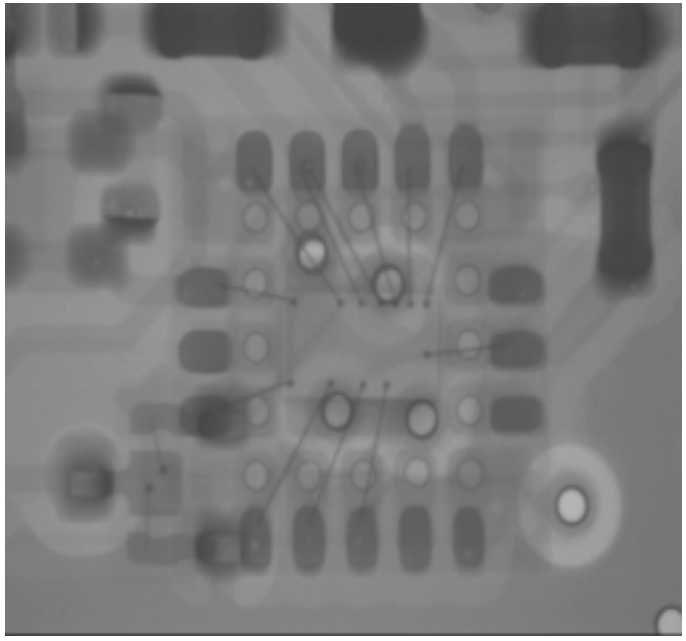
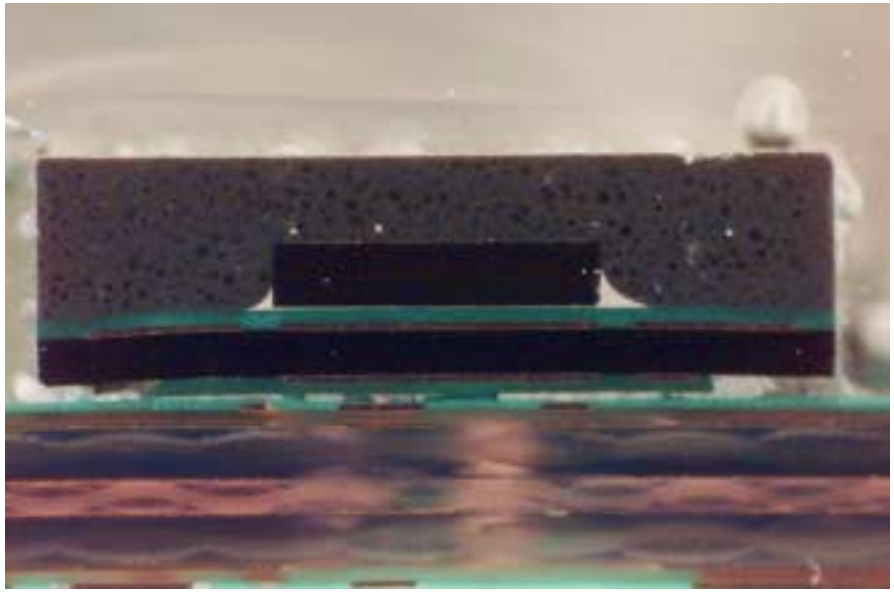
NATIONAL VCO IN THE T28 RF SECTION

- Wirebond-on-rigid CSP
  Gang mold & dice

  – 3.5 x 3.5 mm
  – 16 pads, no balls
  – No underfill







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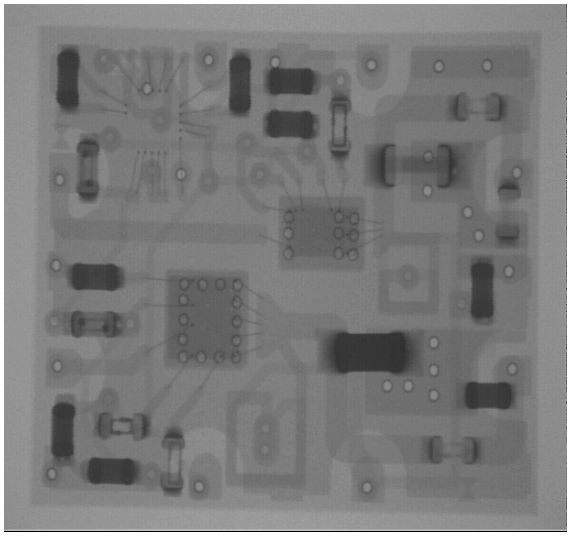
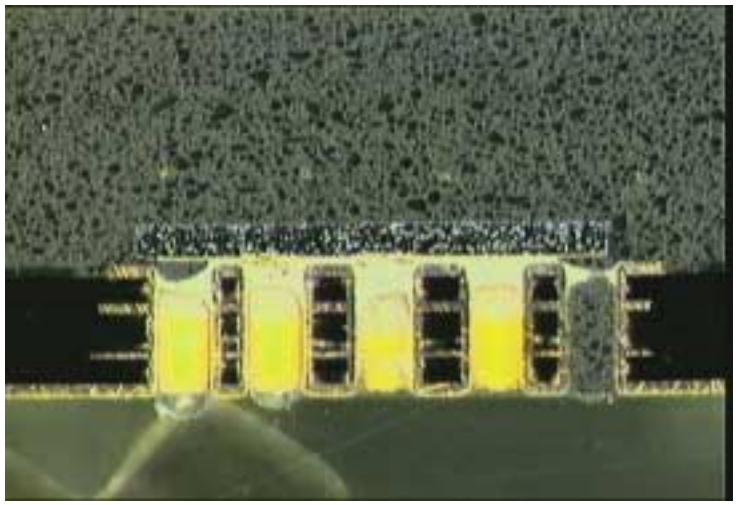
CONEXANT

- Components
  - GaAs PA with integrated resistors
  - CMOS interface die
  - 9-16 wirebonds each
  - 19 discrete passives, 0402 size (one 0603)

- Integrated Passives
  - All resistors on GaAs die (cost, design flexibility)
  - Low value inductors (<10 nH) integrated on carrier
  - High Q passives for output match better as discretes
  - Multilayer carrier provides free layers for passive integration
  - Microvia may allow further integration

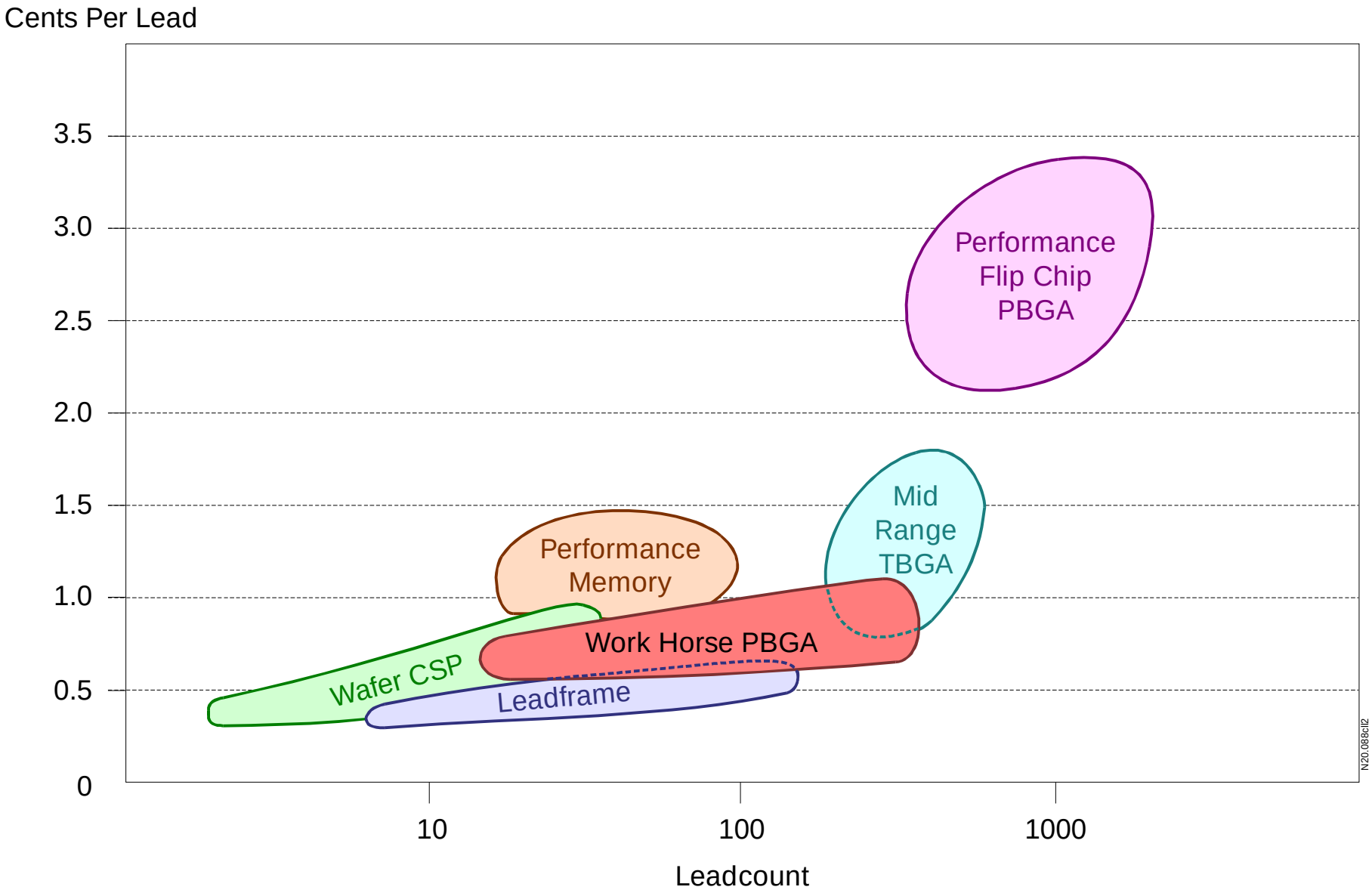
- Just started shipping in Ericsson T28 dual-band GSM phone.





PACKAGE COST DOMAINS

One Million Pieces per Month - September 1999



Source: Prismark's Quarterly Packaging Report and Survey.
Note: All packaging costs, excluding silicon.

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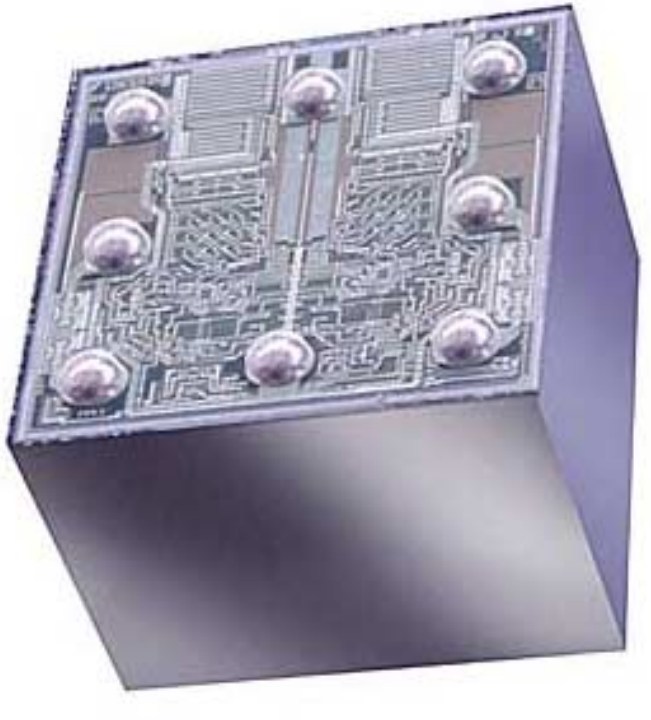
WAFER LEVEL CSPs

Company	Technology	Production Start Date	Est. Production 2000 (M units)
Dallas Semiconductors	1-Wire CSP	‘98	70M
National Semi	µSMD – Redistribution	Q4 ‘98	55M
Fujitsu/Shinko	Super CSP – Copper Post	Q3 ‘99	50M
IEP Technologies Casio/Oki JV	Wafer Level CSP – Plated Copper Post	Q1 ‘00	35M
Flip Chip Technologies	Ultra CSP – Redistribution with BCB	Q1 ‘00	10M
Apack	Redistribution	‘00	10M
ShellCase	Silicon on Glass	Q4 ‘98	6M
FormFactor /Shinko	MOST (MicroSpring on Silicon Technology)	‘00	5M
Hitachi	Redistribution with Polyimide Dielectric	‘00	2-3M
Toshiba	Redistribution with Polyimide Dielectric	‘00	2-3M
Amkor	wsCSP Wirebond onto Polyimide	‘00	1M
Others	TI, Seiko Epson, Sanyo, Rohm & Haas	—	18M
TOTAL			265M

Dallas Semiconductors



National Semiconductor

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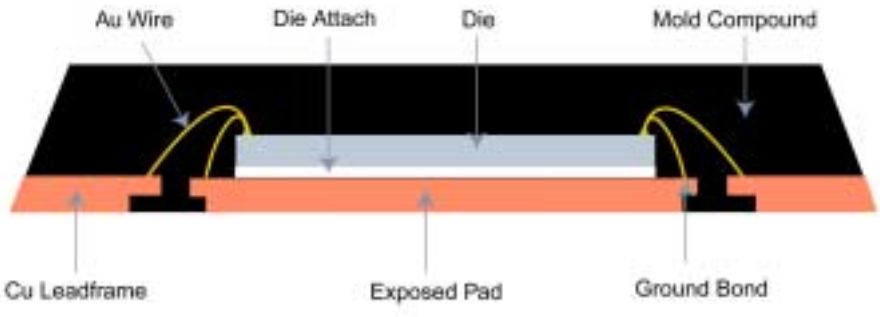
AMKOR MICRO LEADFRAME™ PACKAGE (MLF)

- Low leadcount (typically 16 to 32) leadframe type CSP package
  - Open tool 6 to 52 leads, 3 to 8 mm^2 package size.
- Volume production started 2Q 1999. Already shipping 4 million units/month
- Applications primarily RF and analog devices
  - Self inductance 1.1 nH @ (5.2nH for TSSOP)
  - Self resistance 64.4mΩ (99mΩ)
  - Bulk capacitance 0.2 pF (0.7pF)
- Similar thermal dissipation to larger TSSOP (θja 38.7°C/W)
- Reliability: JEDEC Level 1, solder joint anticipated at >5100 cycles –40C to 125C (8 mm package size, 52 lead, 0.5 mm pitch)
- Cost: competitive with TSSOP in high volume



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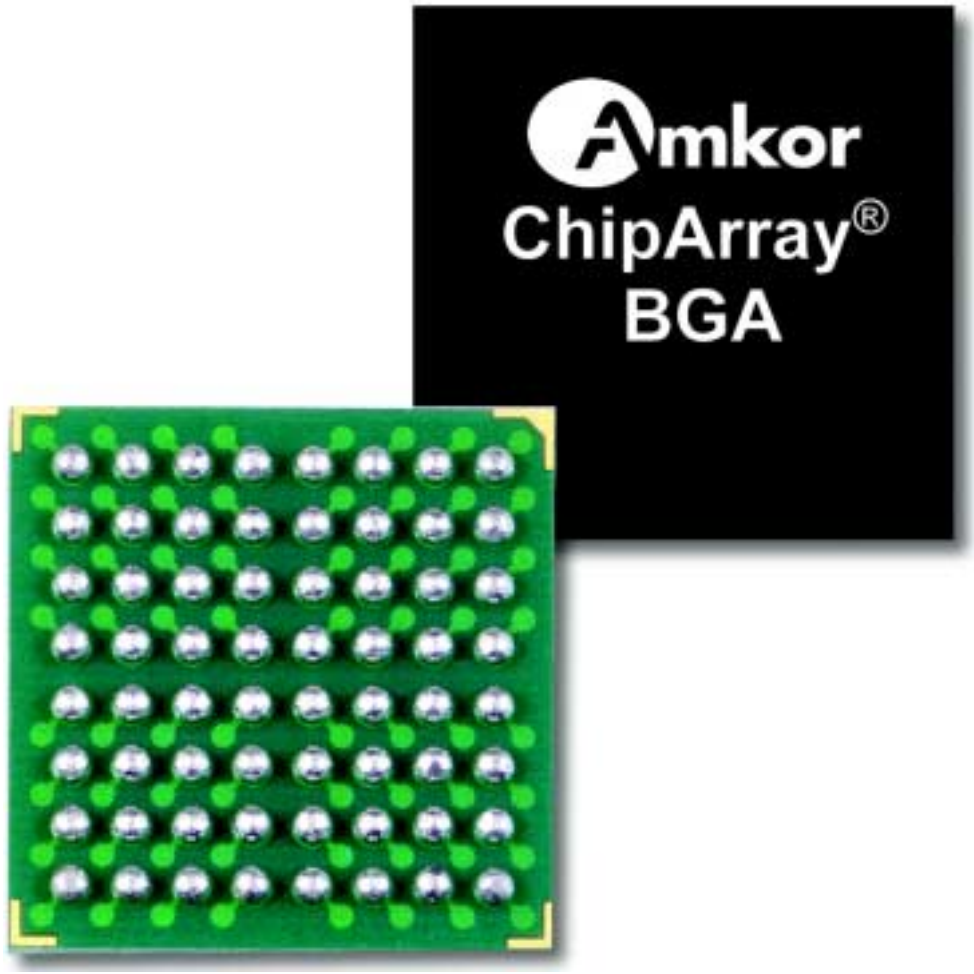
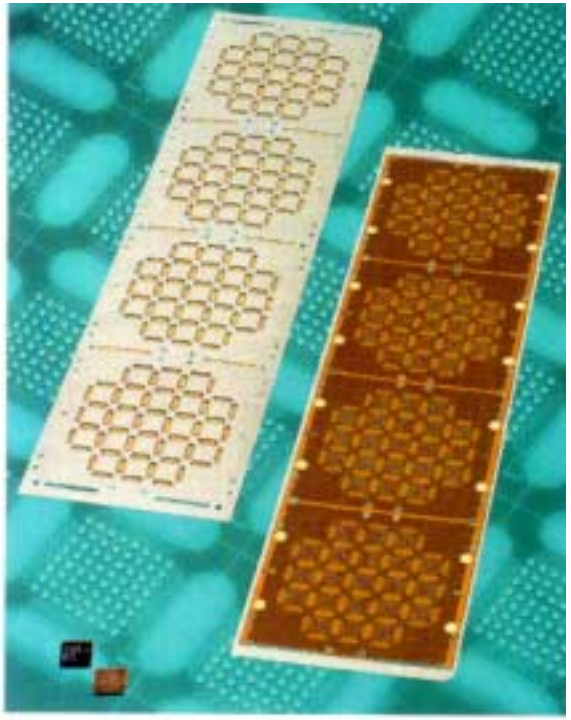
AMKOR CHIPARRAY® CSP

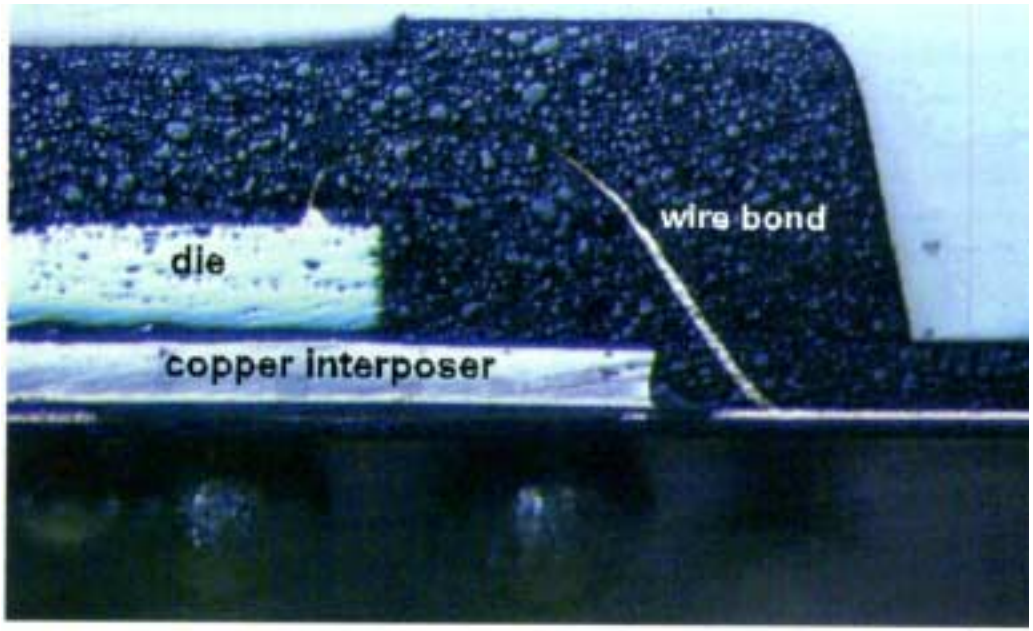
- Uses standard BGA assembly with 2 layer BT substrate
- Targets devices with pincounts from 32 to 208.
- Current applications are ASICs, PLDs, and others such as memory (flash), RF, and analog devices in portable equipment.
- Most production at 1.0 and 0.8 mm pitch, but some products now moving to 0.5 mm.



3M ENHANCED CSP CE-CSP

- Enhanced CSP constructed by laminating patterned 5-mil copper leadframe to the flex circuit.
  - IC attach to leadframe
  - IC is wirebonded through slots in leadframe
  - Overmolded and singulated
- Offers improved solder joint reliability, heat dissipation, easier handling, and improved coplanarity.
- Targeted towards devices which have high thermal dissipation (up to 6W) with leadcounts of 60 – 150+.



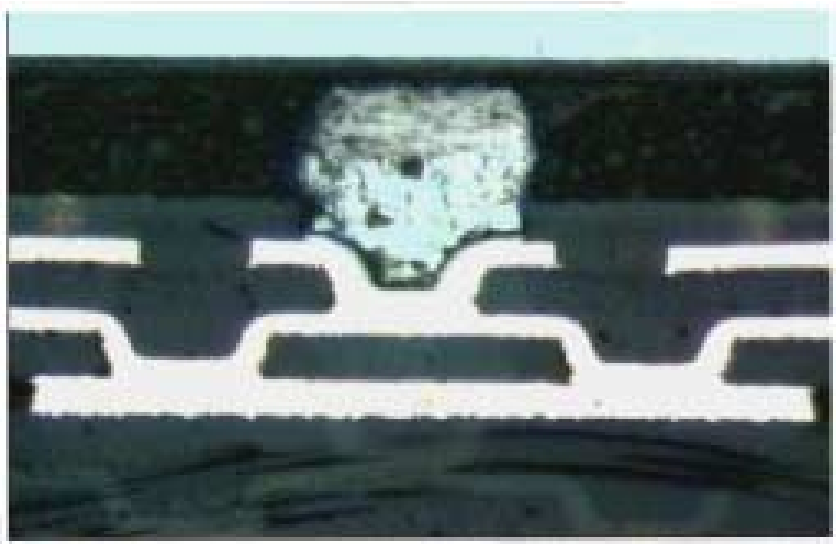


HIGH PERFORMANCE FLIP CHIP BASED PACKAGES

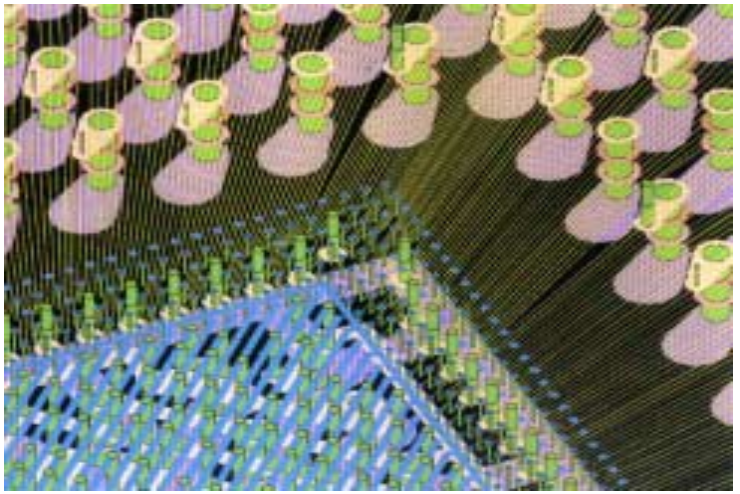
- Package parasitics are now a mainstream issue for fast memory access as well as graphics, micro, and signal processors.

- Still no agreement on preferred package configuration (Ibiden, NTK, Gore, Kyocera, Honeywell, X-Lam, Amitec, MCS, etc.

- MicroBGA™ preferred package for RAMBUS™. Other architectures and packages proliferating.



Cross section of Pentium III flip chip die to Ibiden package interface (50µm lines, 75µm vias)



Radial routing and vertical power drop in Amitec PBGA (15µm lines, 10 µm vias)

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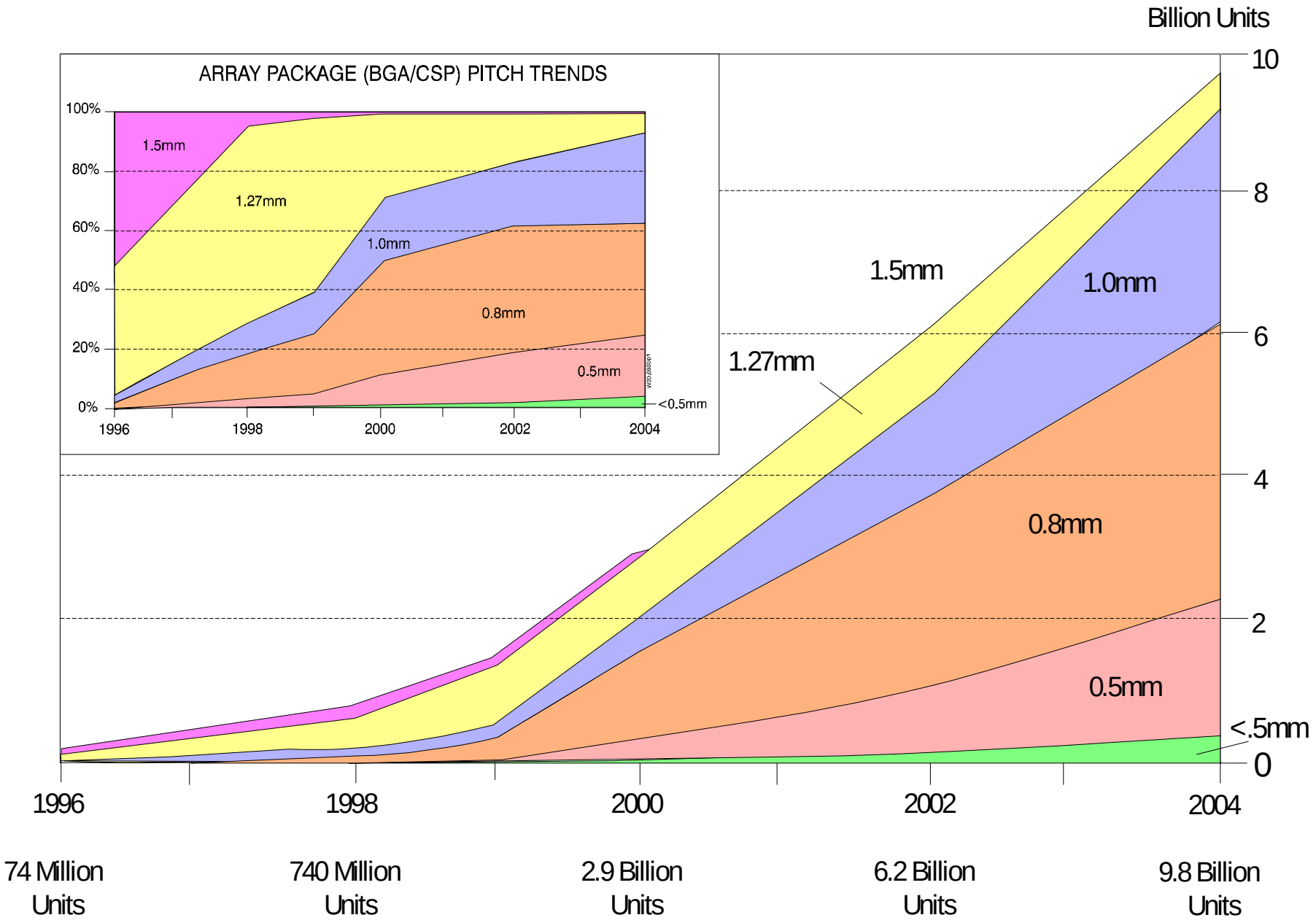
ARRAY PACKAGE (BGA/CSP) PITCH TRENDS

W20.088BP2



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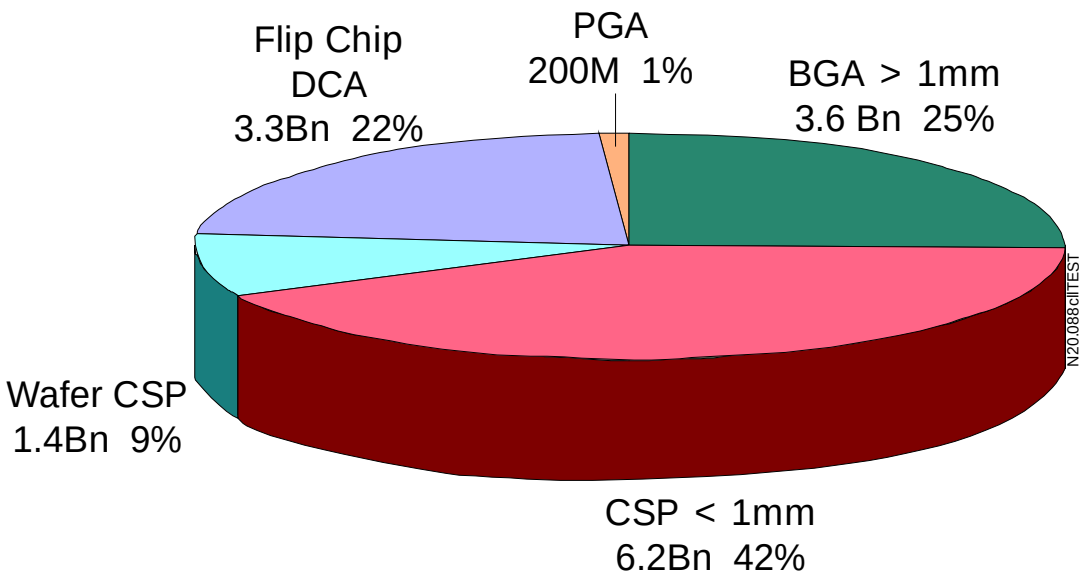
HOW BIG IS THE PROBLEM?

2004

0.6 Bn	*(4%)*	1.27 mm packages
3.2 Bn	*(22%)*	1.00 mm packages
3.9 Bn	*(26%)*	0.80 mm packages
6.9 Bn	*(47%)*	0.50 mm packages
0.2 Bn	*(1%)*	<0.50 mm packages

Note: The above excludes Flip Chip etc.

2004



14.7 Billion Packages

A VEWY BIG PLOBLEM

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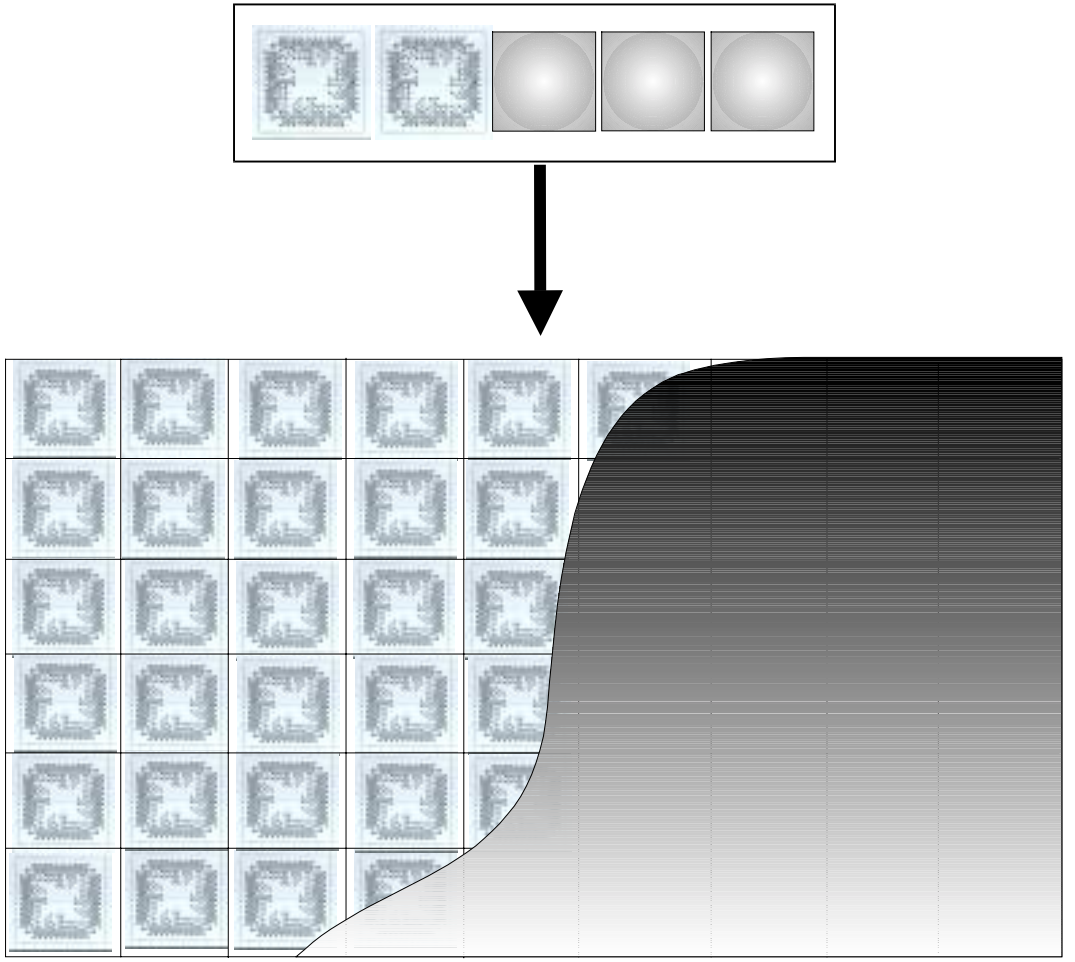
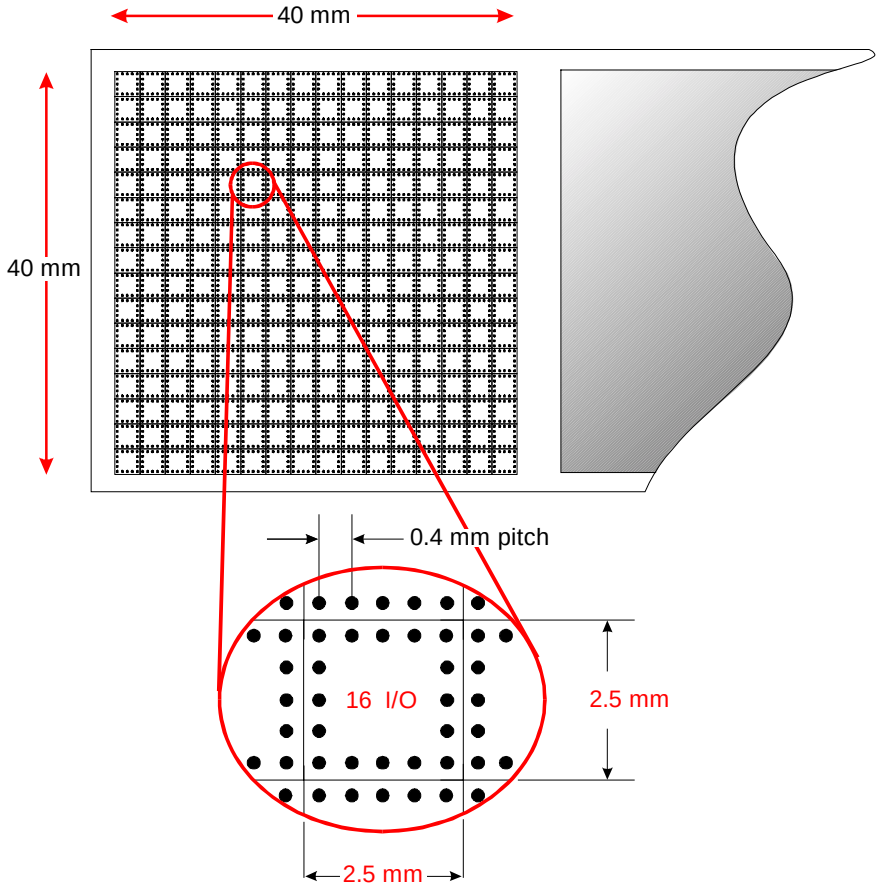
THE MOVE TO COJOINED PACKAGES

- The KGD lessons Intel (Smart Die ™), Texas Instruments, Micron.
- Established for memory, 64 die enabled by FormFactor. Matsushita claims full wafer level test.
- Emerging for packaged devices driven by compelling economics
  - Substrate is 50% of package cost. Therefore, maximize utilization of expensive real estate
  - Mass mold and gang dice provides for package proliferation without multiple molds
  - Multiplexing test improves utilization of high capital cost test equipment.



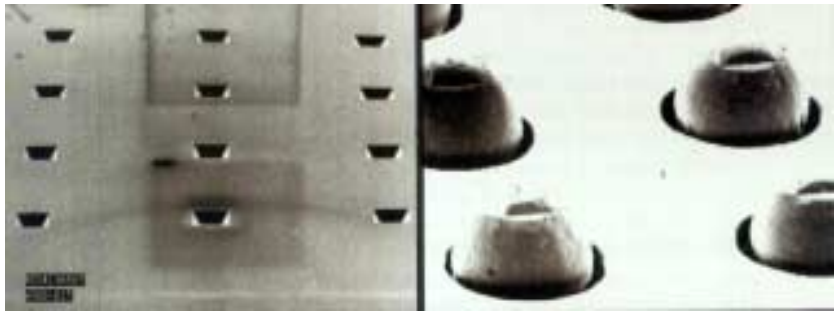
LEADING EDGE CSP TEST IN JAPAN

- 256 packages in 40mm square single molding
- Over 3000 short pogo pins to high density, multilayer test head
- RF device operating frequency 1.8 GHz
- 31 Kg (70 lbs.) contact force

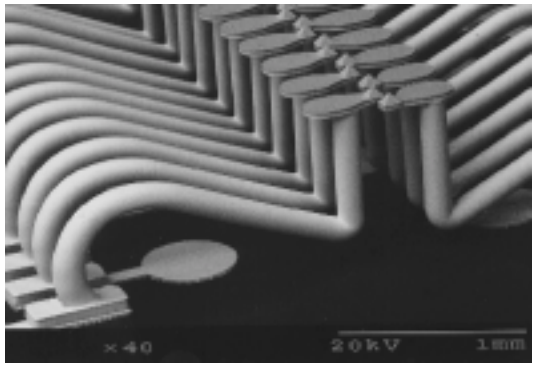


VEWY BIG PLOBLEM

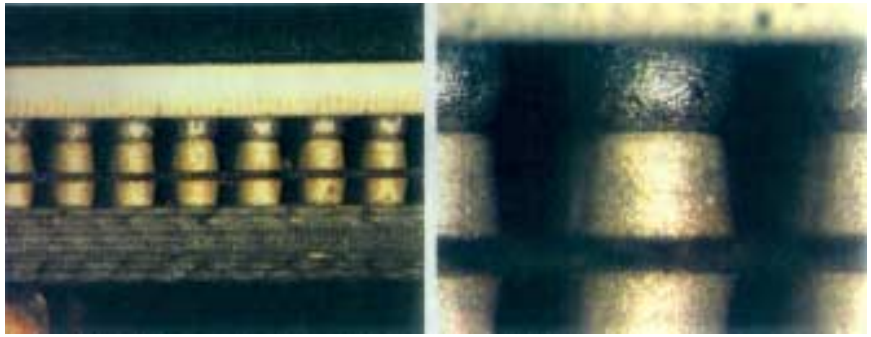
- Contiguous package manufacturing
- Electrically isolated packages before singulation
- 3000 contact pads per square inch
- Comparable complexity of test head
- Increasingly high frequencies and shrinking electrical budgets
- Less than perfect planarity
- An industry-wide problem, not just small form factor electronics



Silicon wafer based systems.



Source: FormFactor.



Source: Thomas & Betts.

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