Burn-in & Test Socket Workshop 2000

Session 4a

Burn-in Board Design

IEEE COMPUTER SOCIETY

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BURN-IN & TEST
SOCKET WORKSHOP

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Presentations

“Burn-in Board Design For Manufacturing”
Aamir Jamil
Pycon, Inc.

“Burn-in Board Design Consideration For High Speed & High Power Devices”
Aamir Jamil
Pycon, Inc.

“Burn-in Board Design Considerations”
Tony Valente
Unisys – Unigen

PYCON INCORPORATED

Burn-In Board Design For Manufacturing

2000 Burn-in and Test Sockets Workshop

BiTS
BURN-IN & TEST SOCKET WORKSHOP

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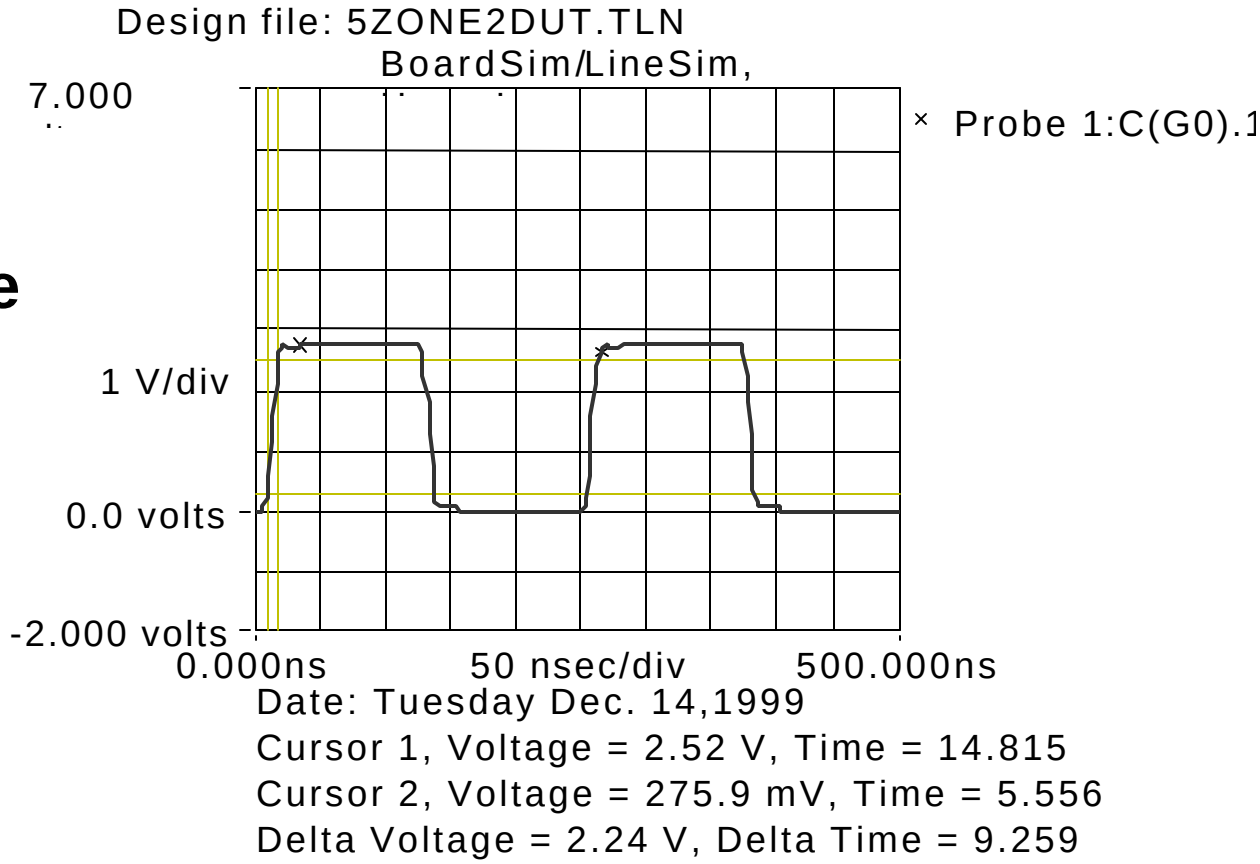
Agenda

- **Transition in Design**
- **Constraints**
- **SMT (S**urface **M**ount **T**echnology**) contact: Case study**
- **Step board: Case Study**

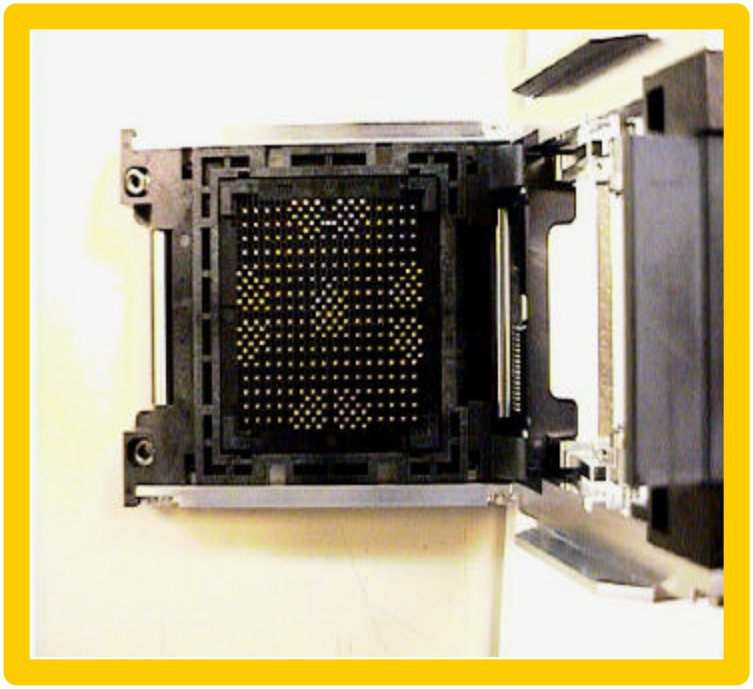
Transition in Design

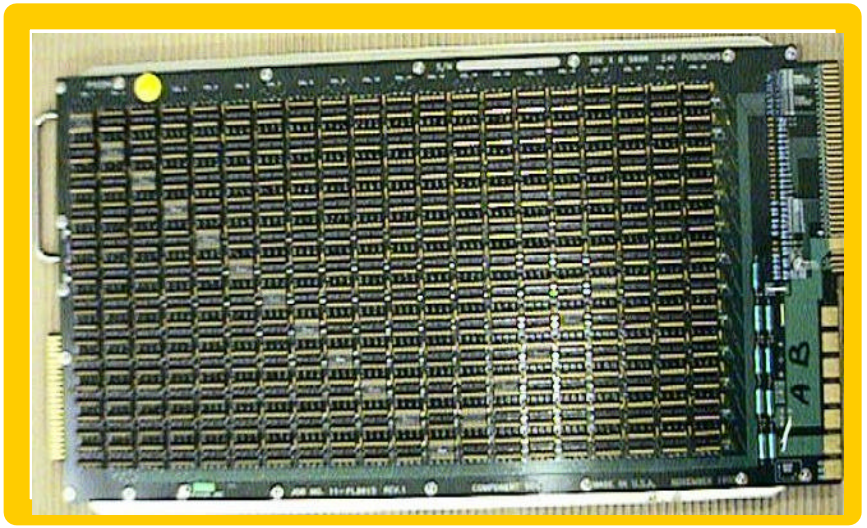
- **BIB(Burn-in Board) Devices require**
  - **Higher speed**
  - **Lower voltage**



Transition in Design Cont'

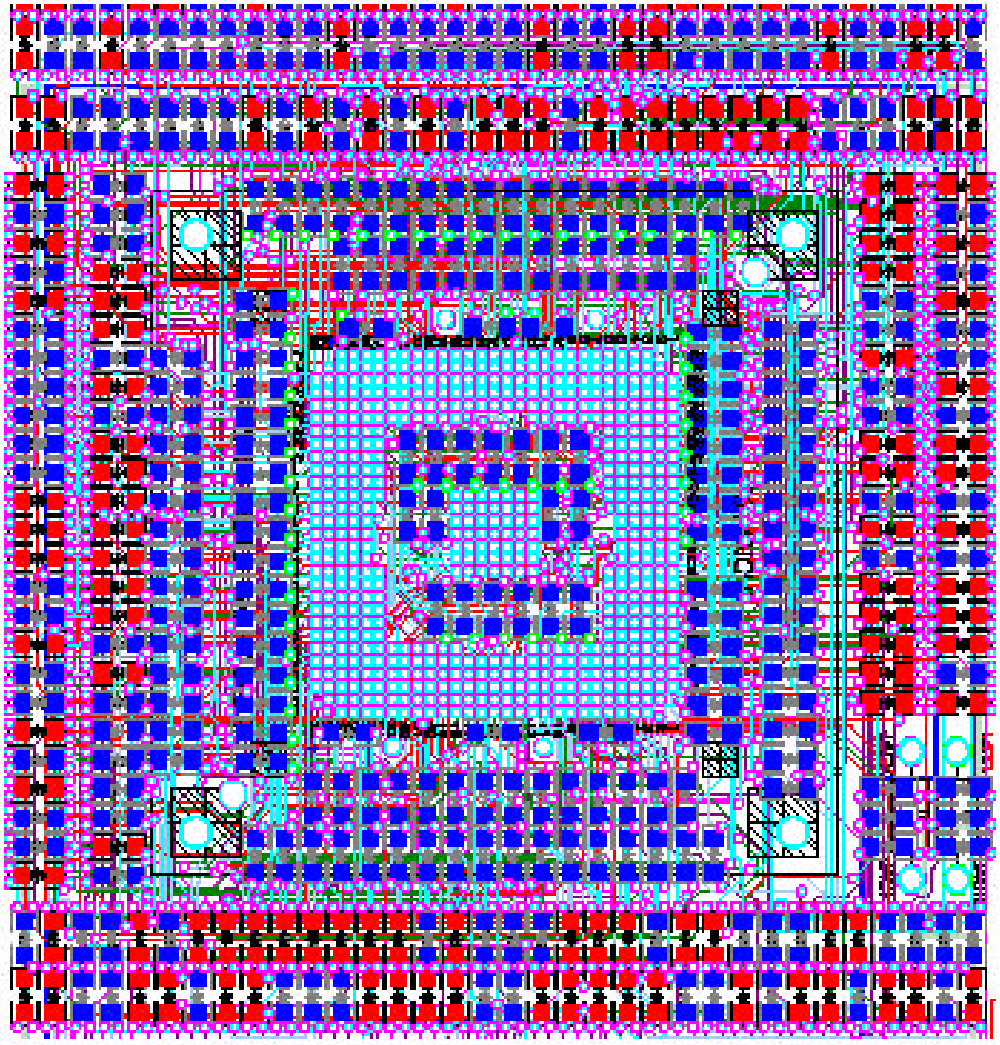
- **BIB(Burn-in Board) Devices require**
  - **Sockets with Higher pin count**
  - **BIB design with higher density**





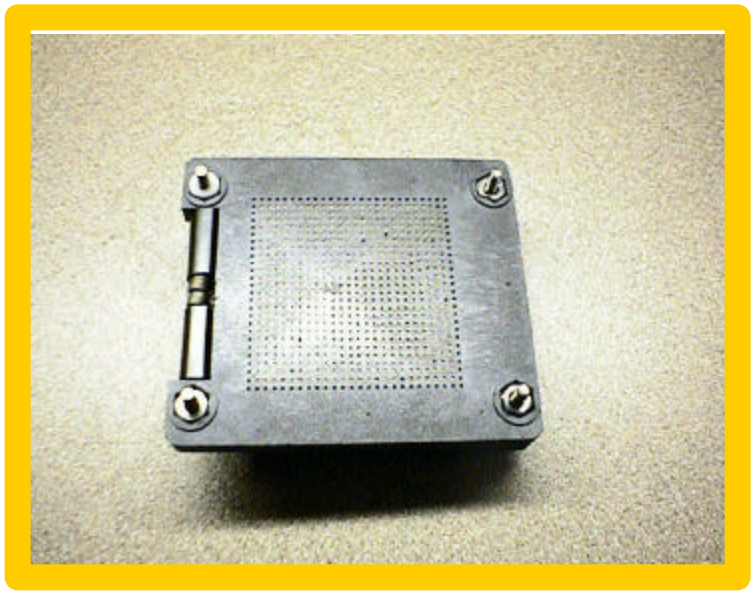
Transition in Design Cont'

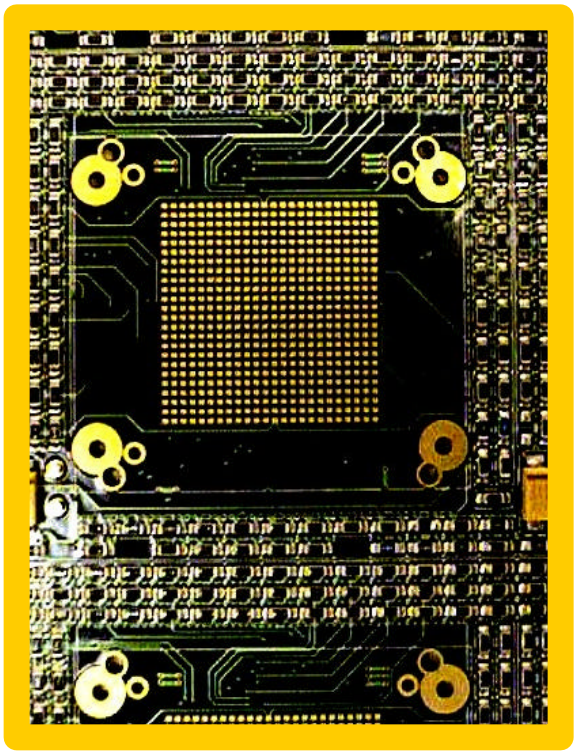
- **BIB(Burn-in Board) Devices require**
  - **More Layers**
  - **Matched impedance**
  - **Shorter cycle time**
  - **Higher efficiencies = better reliability**



Transition in Design Cont'

- **BIB(Burn-in Board) Devices require**
  - **SMT(Surface Mount Technology)**
  - **BGA (Ball Grid array)**





Constraints

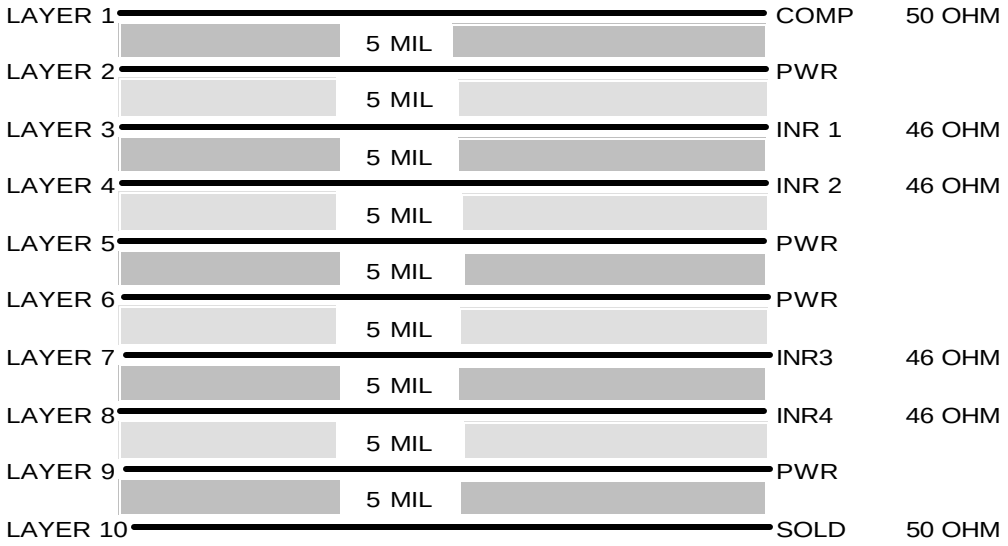
- **Board size & thickness**
  - **Dedicated to 62 mils(10Layer MAX with 50≮ Imped.)**

BURN-IN BOARD

MECHANICAL SPEC. OF THE CIRCUIT BOARD

STANDARD 10 LAYER CONSTRUCTION

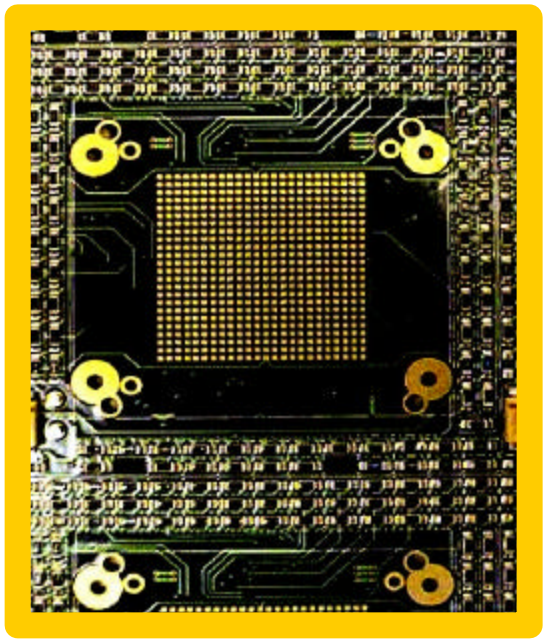
FOR RELIABILITY STYLE OVEN

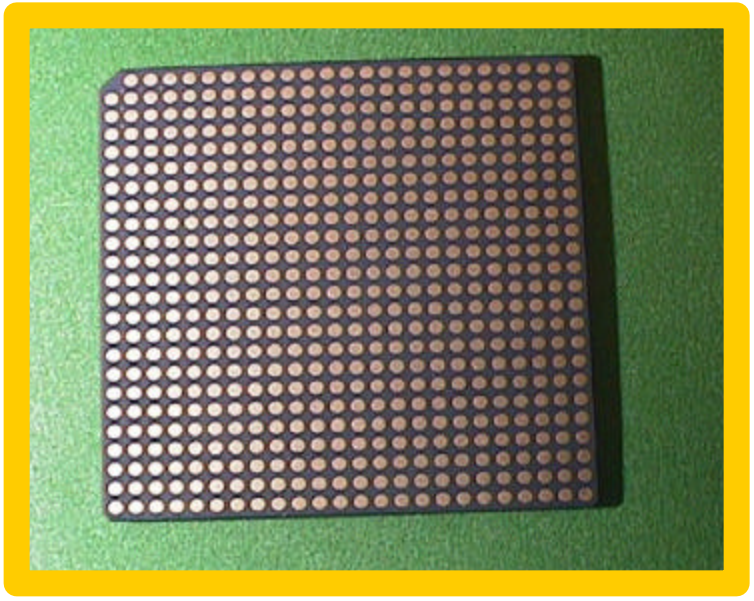


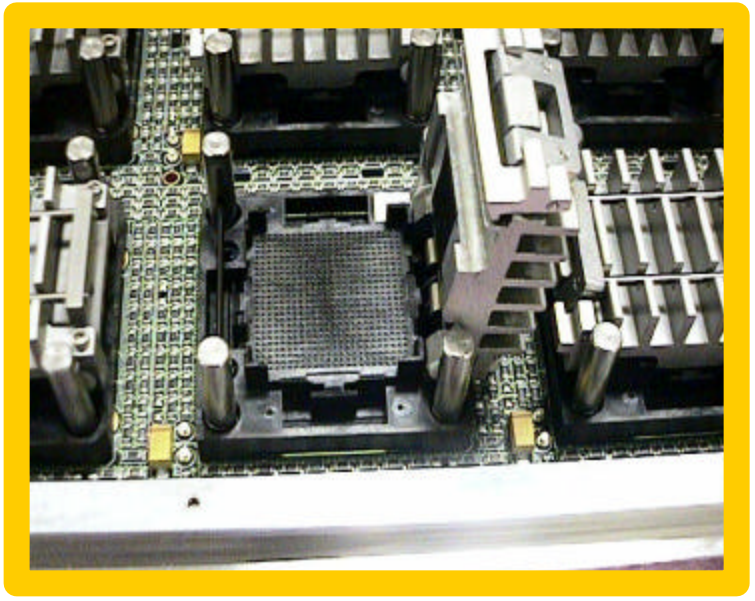
1. All Cores are of **1oz Cu**
2. Trace Width = **8 Mils**
3. Over all board thicknes **62 MILS +/- 10%**
4. Impedance is **50 OHMS**
5. Material is **POLYIMIDE**
6. Traces must be running **Perpendicular to the adjacent layers in the Dual Stripline only.**

Constraints Cont'

- **SMT Sockets**
  - **Device contact reliability**
  - **Socket contact reliability**
  - **Top probe for testing**

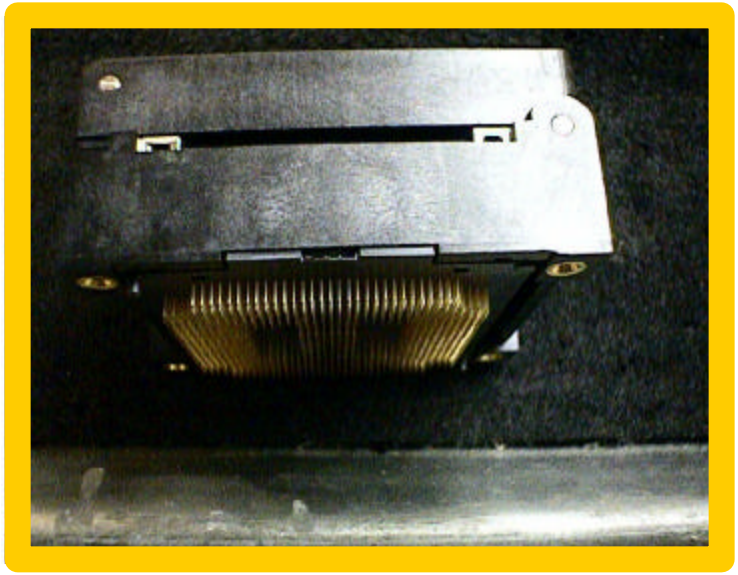


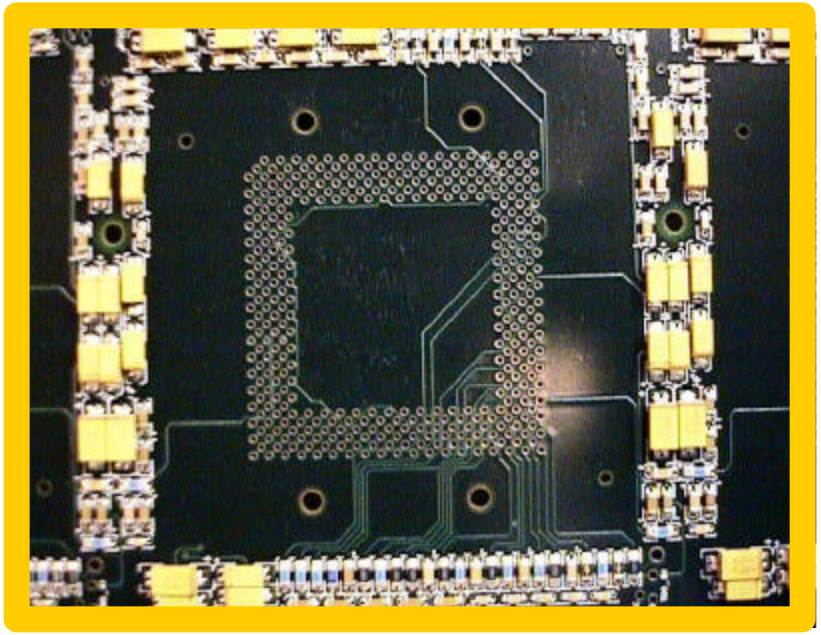


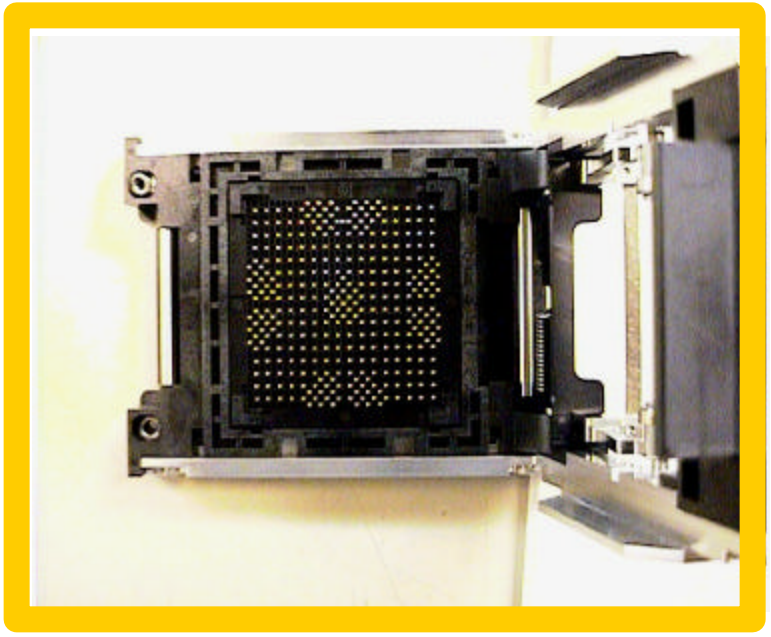


Constraints Cont’

- **Thru-hole sockets**
  - **Higher drill count**
  - **Increases layer count**
  - **Higher aspect ratio required**

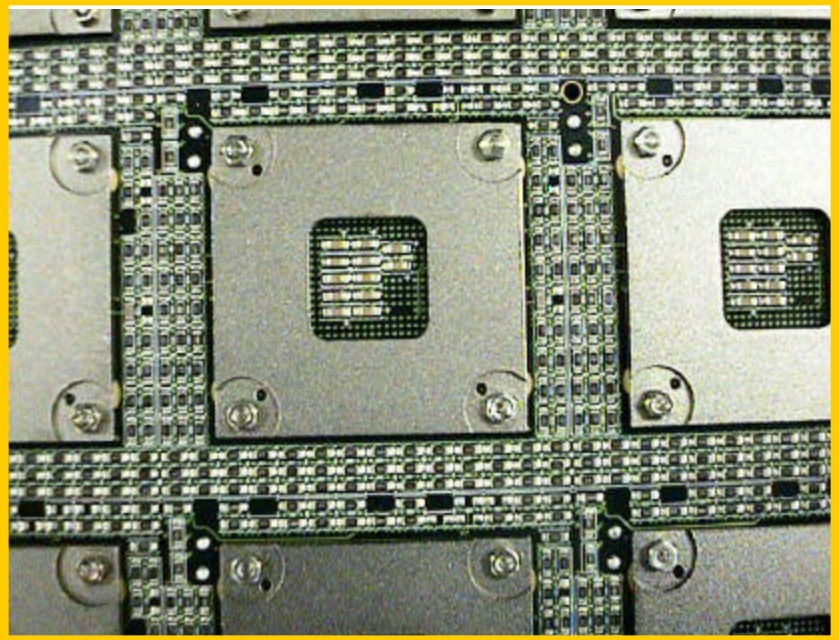


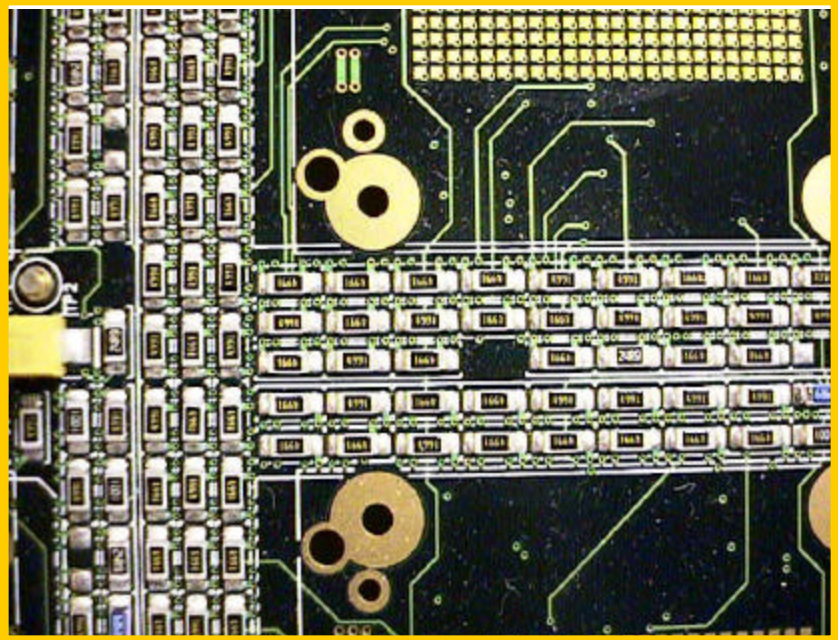




Constraints Cont’

- **SMT Components**
  - **Vias too close to Pads, causes solder bridge and Solder Escape**

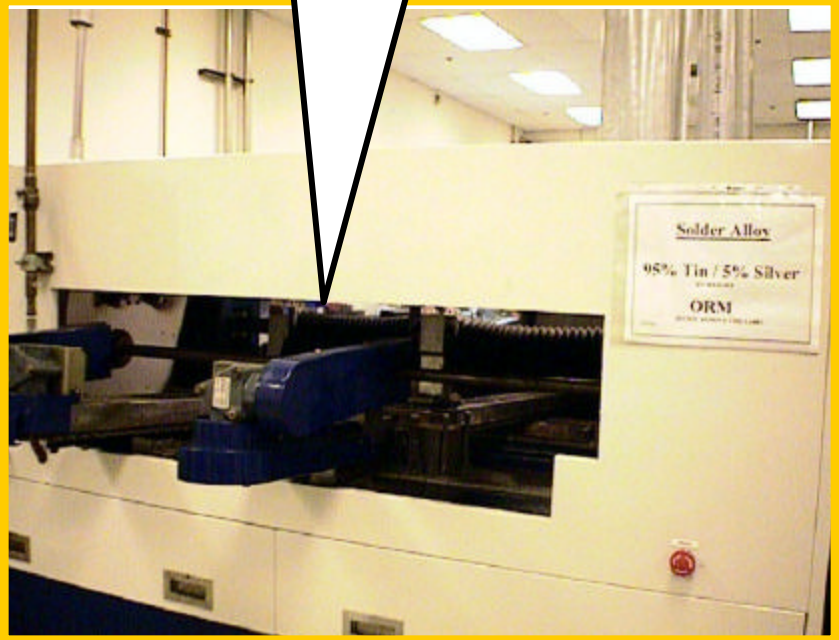




Constraints Cont’

- **SMT Components**
  - **Assembly to use Re-Flow for SMT and Wave solder for Through Hole components.**

Wave Solder



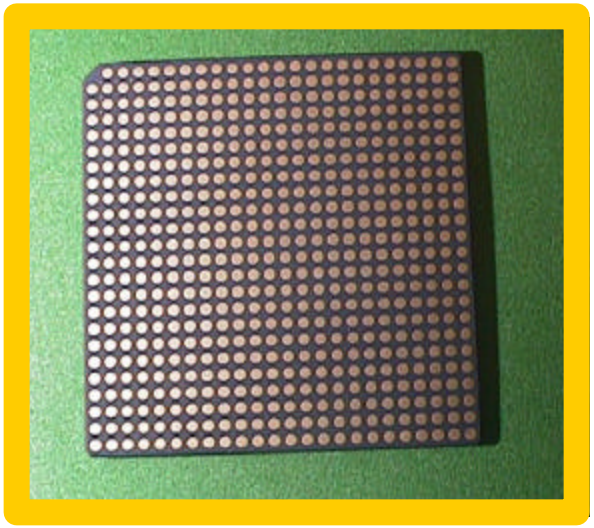
Re-flow Chamber

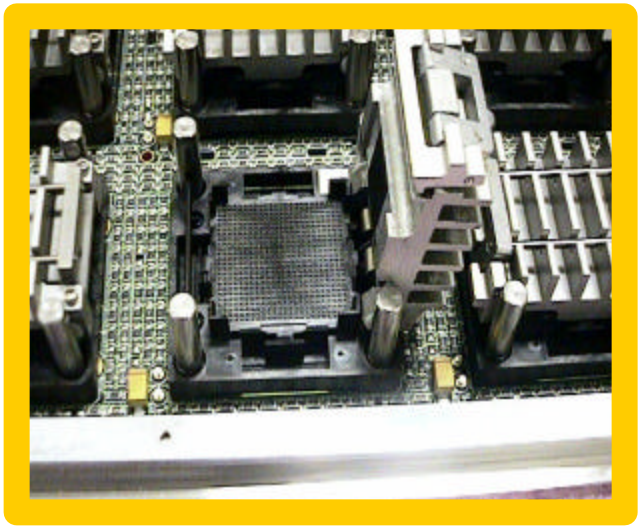
Constraints Cont’

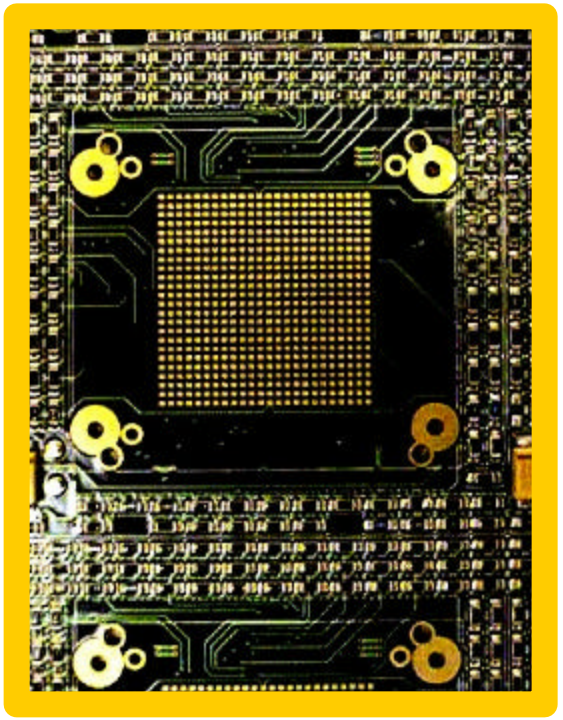
- **Power planes**
  - **Require higher CU count**
  - **Additional Power planes**
- **Signal Layer**
  - **Require higher number of signal layers**
  - **Require smaller trace width and line spacing**

SMT contact: Case study

- **Problem**
  - **Devices fail randomly in SMT sockets.**
- **Diagnosis**
  - **Contact issues b/w BIB Pads and socket pins**
  - **Contact issues b/w socket pins and DUT contacts**
  - **Oxidation on BIB SMT pads**





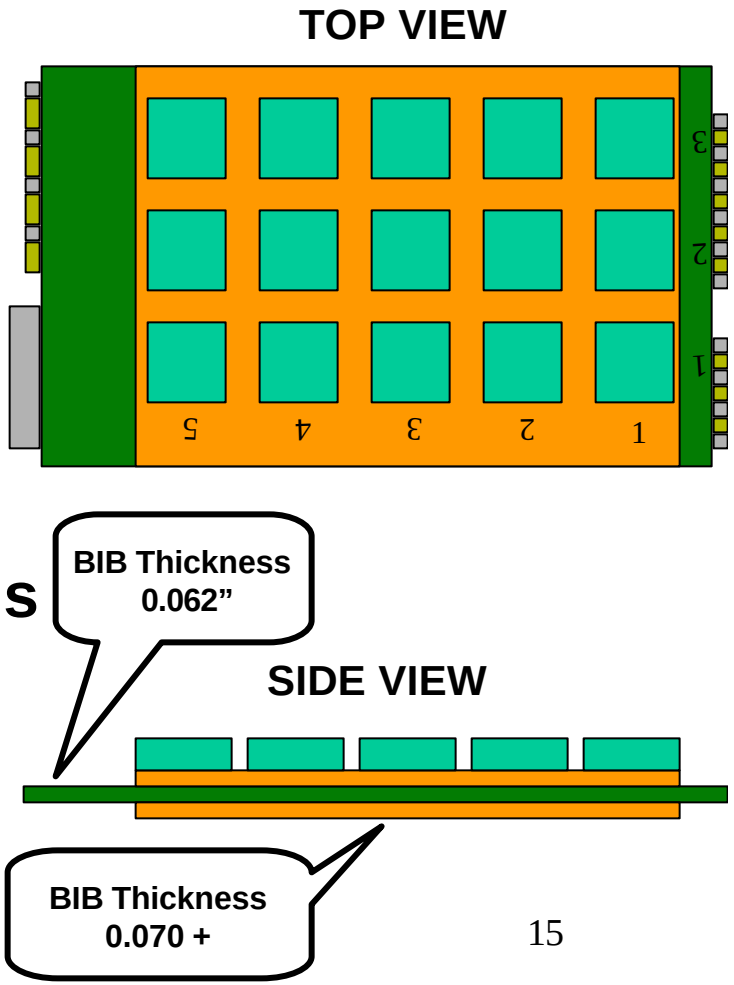


SMT contact: Case study

- **Solution**
  - **High pressure wash and bake BIB**
  - **BIB Pad cleaning using Alcohol before installing sockets**

Step Board: Case Study

- **Problem**
  - **Need 70+ Mils of layers on a 62 Mil BIB**
- **Non-Solutions**
  - **Squeezing design creates crosstalk issue**
  - **Squeezing layers creates impedance issue**
- **Step-board Solution**
  - **70+ Mils in socket area, 62 Mils connector area**
  - **Add signal layers only under the socket area**



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Burn-In Board Design consideration for High Speed & High Power Devices

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Agenda

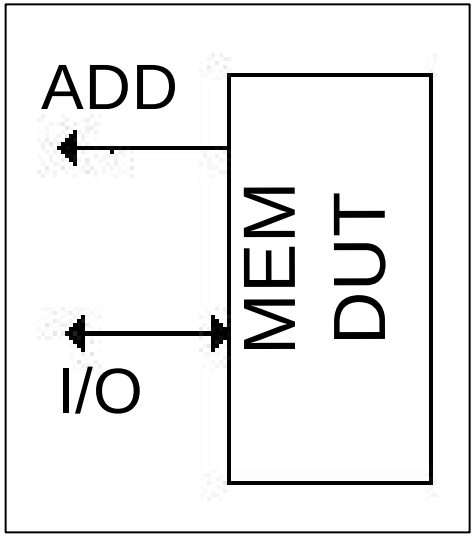
- **Introduction to Design**
- **Memory Board Design**
- **Logic Board Design**
- **Simulation**
- **Fabrication & Assembly**

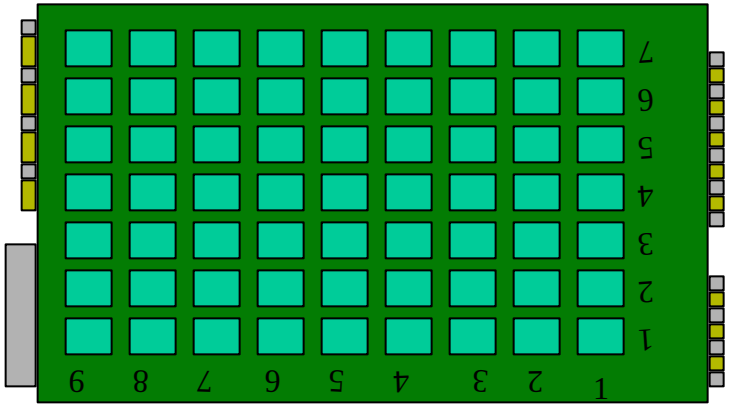
Introduction to Design

- **Static/Dynamic**
  - **Static: Constant power to device**
  - **Dynamic: Signals toggling**
- **TDBI (T**est **D**uring **B**urn-**I**n**)**
  - **Monitor sign of life from device**
  - **Compare actual vs. expected**
- **Memory/Logic**
  - **Memory: Read & Write on the same channel**
  - **Logic: Dedicated output**

Memory Board Design

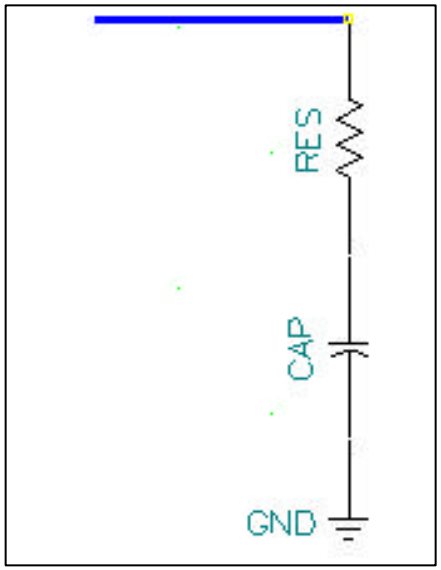
- **Device**
  - **Address inputs**
  - **I/O Bi-Directional**
  - **Small Foot Print - High Density**
- **Design**
  - **150+ devices per bib**
  - **Load per channel is higher**
  - **Isolation recommended**
  - **Rise time controlled by routing techniques**



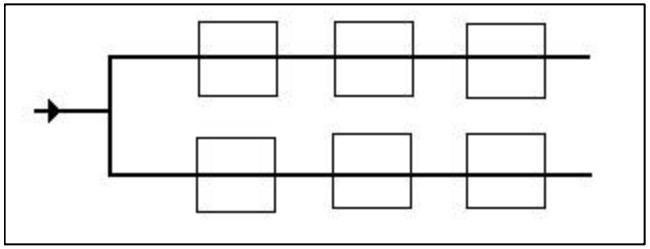


Memory cont'

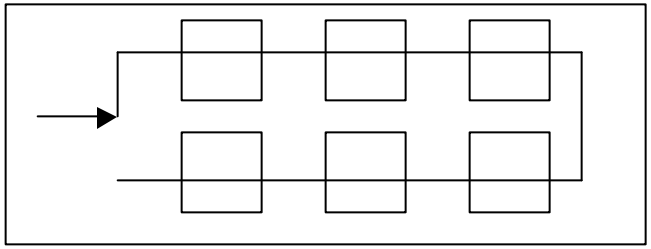
- **Routing & Termination**
  - **Parallel routing yields equal delay**
  - **AC termination yields low signal loss**
  - **Yields 10Mhz frequencies**
  - **Isolation protects from interference**



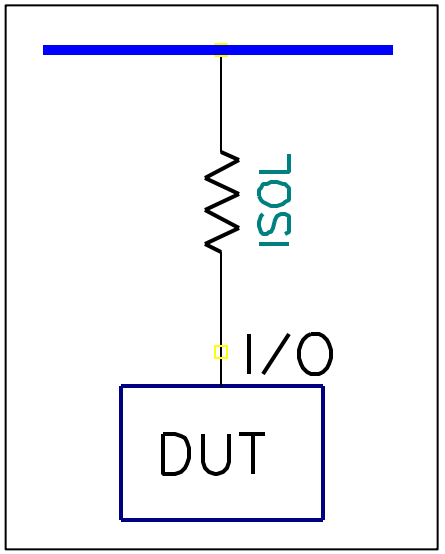
AC Term.



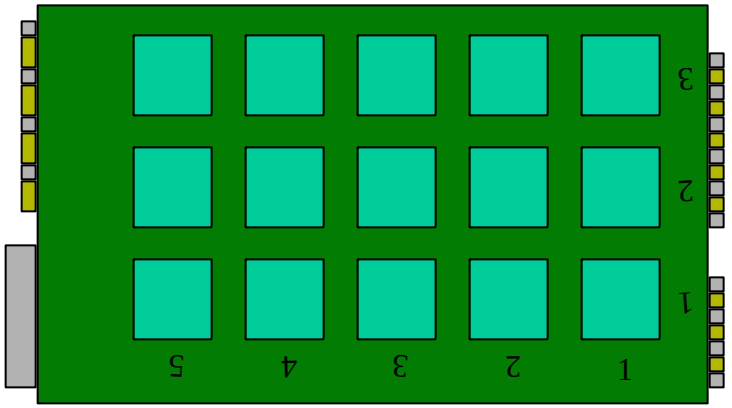
Parallel Routing



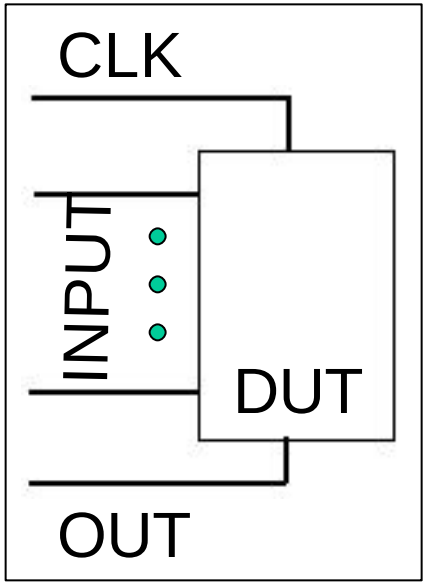
Serial Routing



Logic Board Design

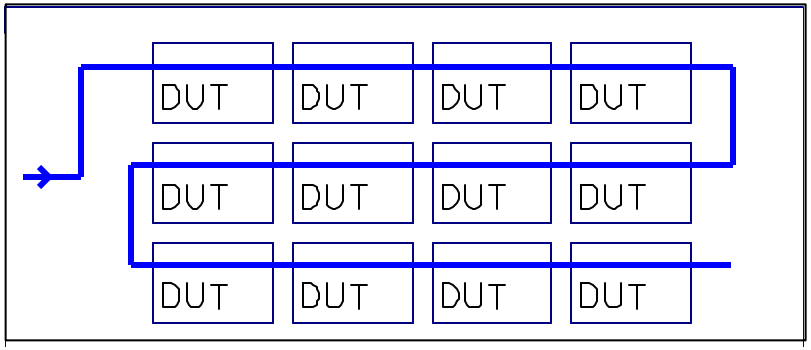


- **Device**
  - **BIST (Built-In Self Test)**
  - **Unidirectional channels**
  - **CLK parameters critical**
  - **PLL: Noise, Tr, Tf, Jitter**
- **Design**
  - **Large device - Low density**
  - **Density = Channels dedicated for output**
  - **Skew: Clocks synchronized with inputs for expected output**



Logic Board Design Cont'

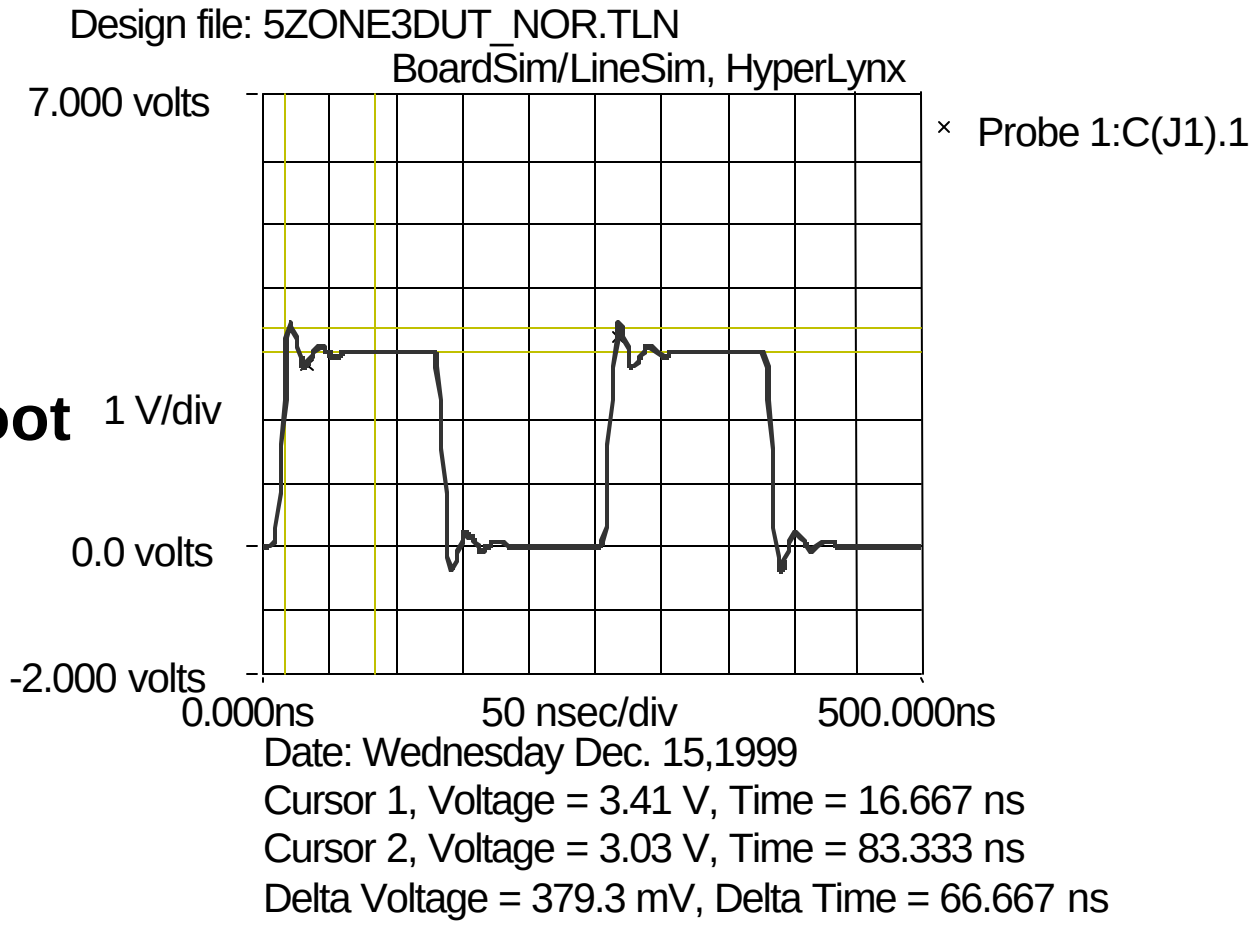
- **Routing & Termination**
  - **Pre design simulation for routing technique**
  - **CLK routing point to point for Tr**
  - **Serpentine routing for limited channels**
  - **DC termination for better Tr**
  - **AC termination avoids signal attenuation**
  - **Impedance matched for device load**



Serpentine Routing

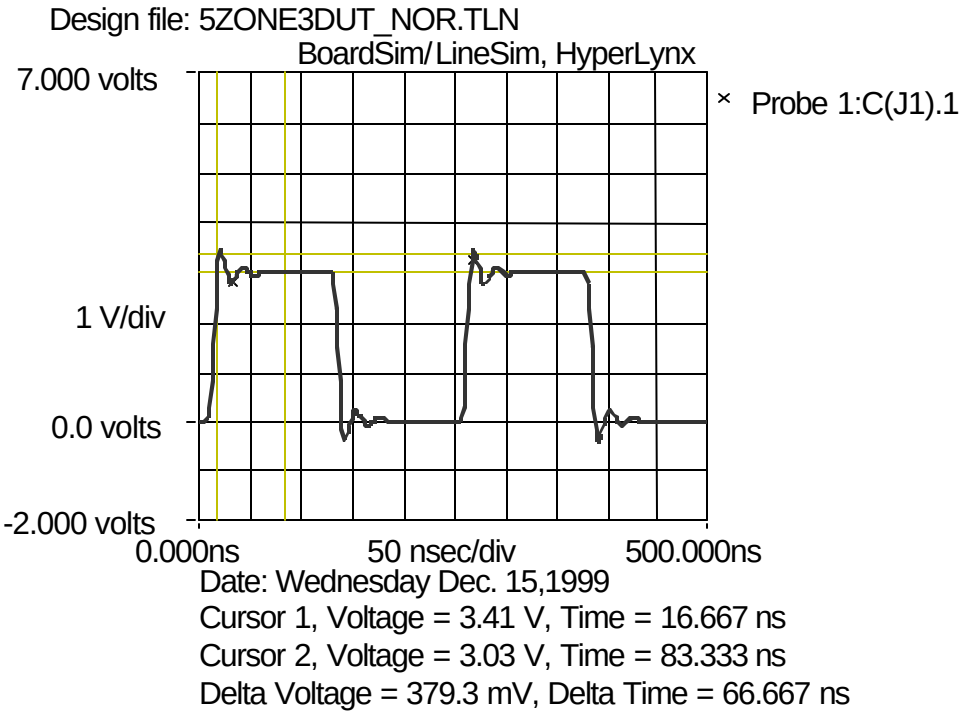
Simulation

- **Specification**
  - **Rise/Fall time**
  - **Over/Under shoot**
  - **Signal Losses**

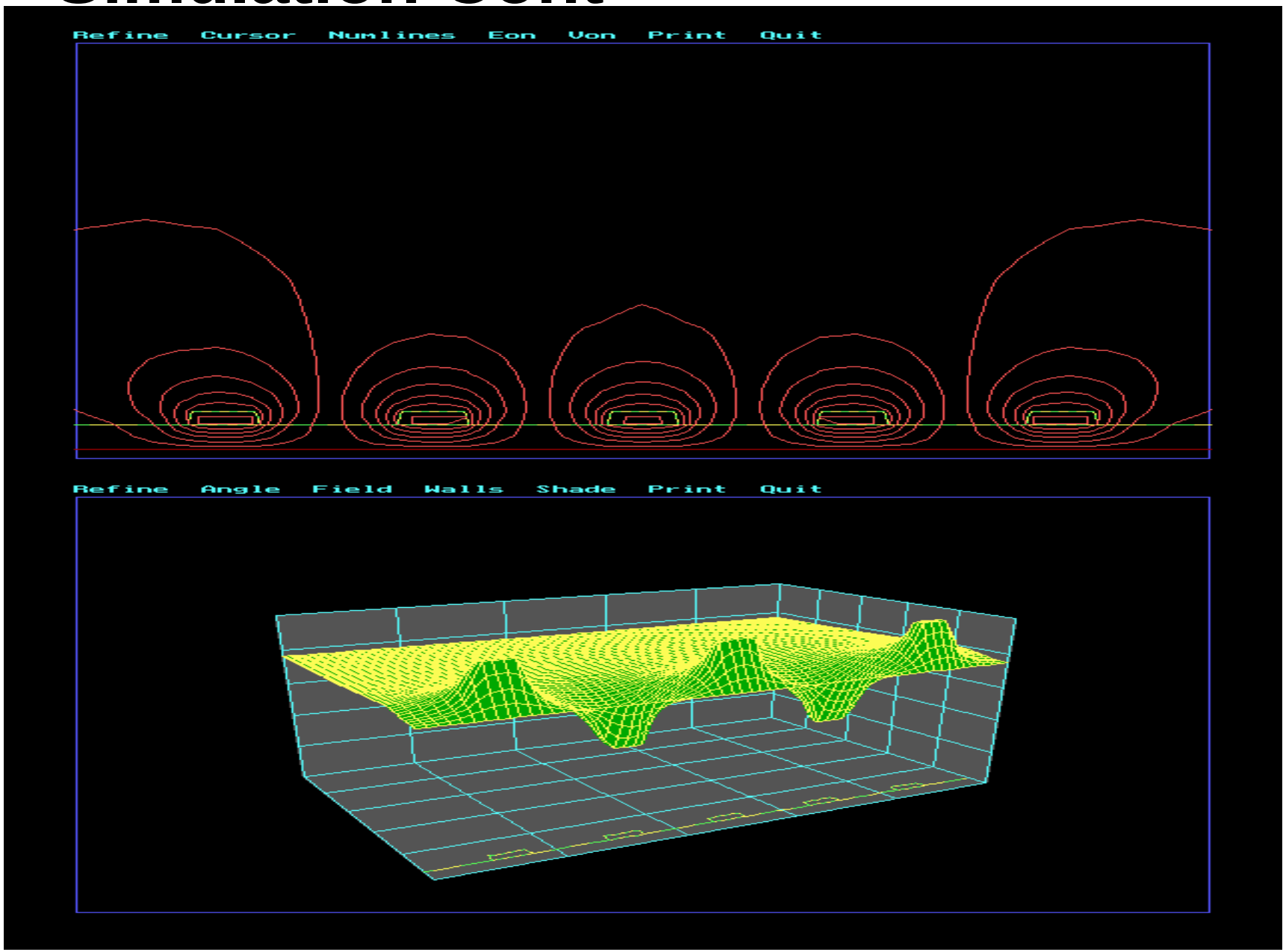


Simulation Cont'

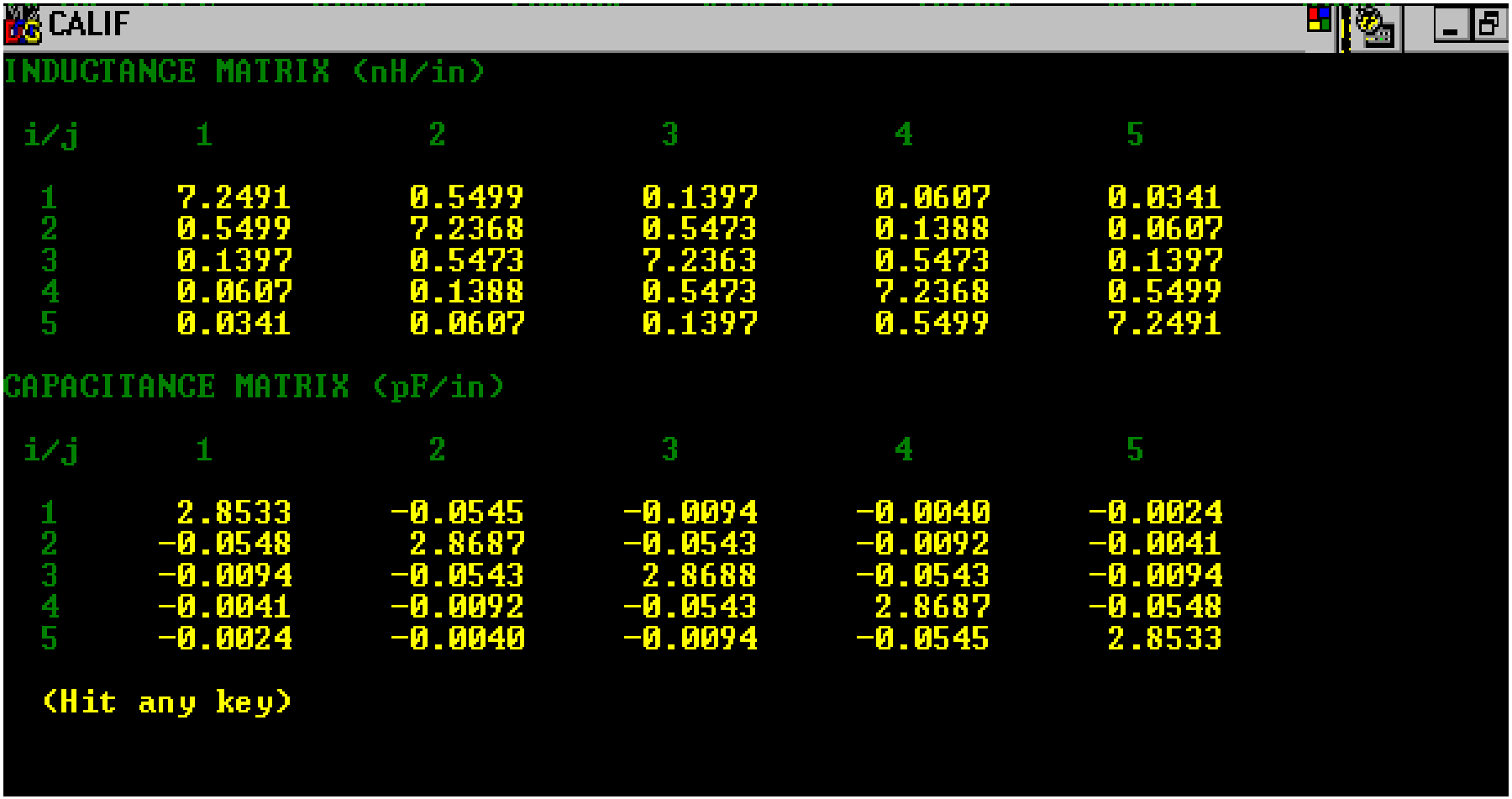
- **Pre-Fabrication Simulation**
  - **V/T graphs for all critical pins**
  - **Adjust termination values**
  - **Measure skew between signals**
  - **Calculate Signal Integrity crosstalk**
  - **5% Accuracy between simulated and actual design**



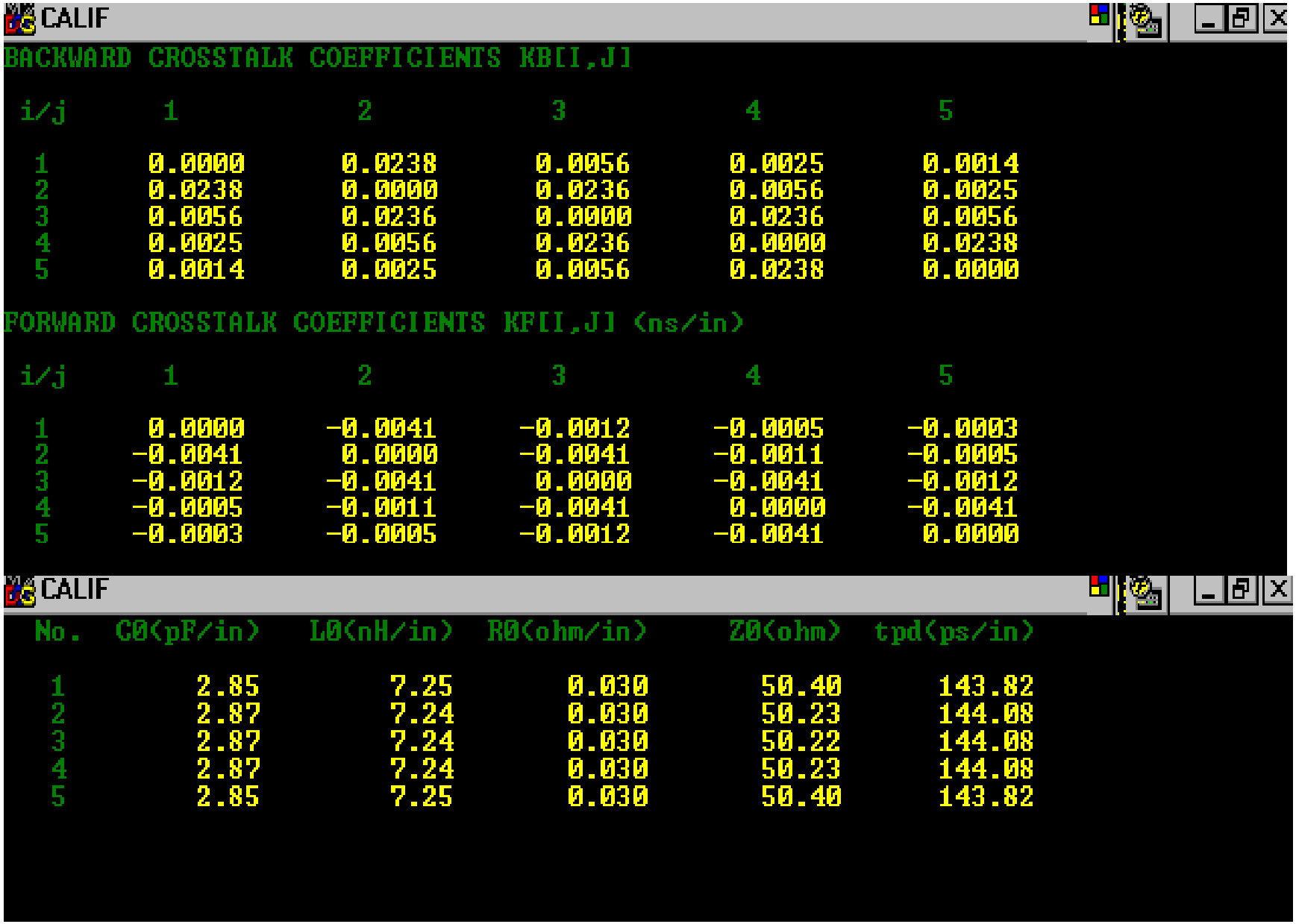
Simulation Cont’



Simulation Cont’



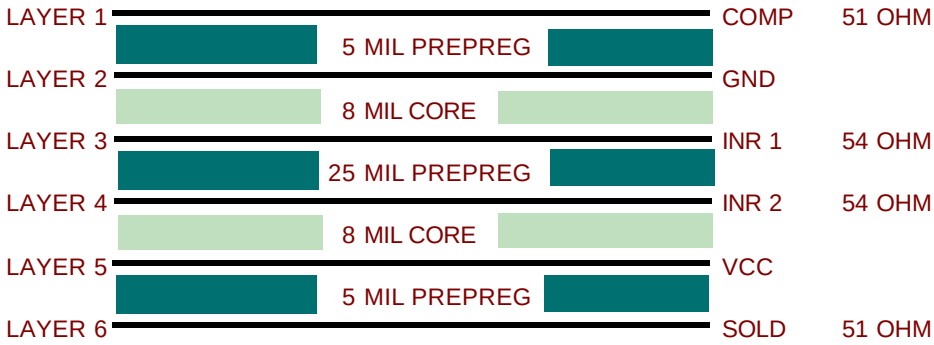
Simulation Cont'



Simulation Cont’

BURN-IN BOARD

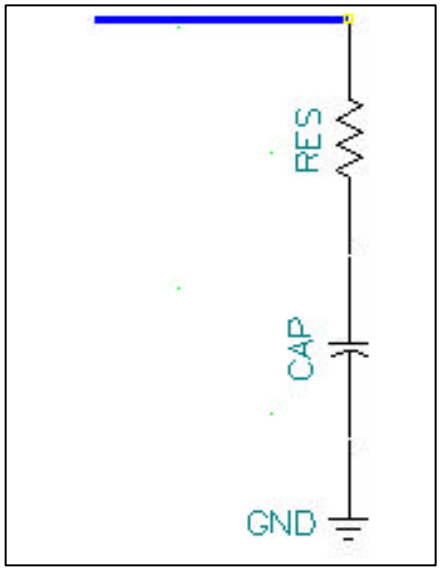
MECHANICAL SPEC. OF THE CIRCUIT BOARD
LAYER CONSTRUCTION



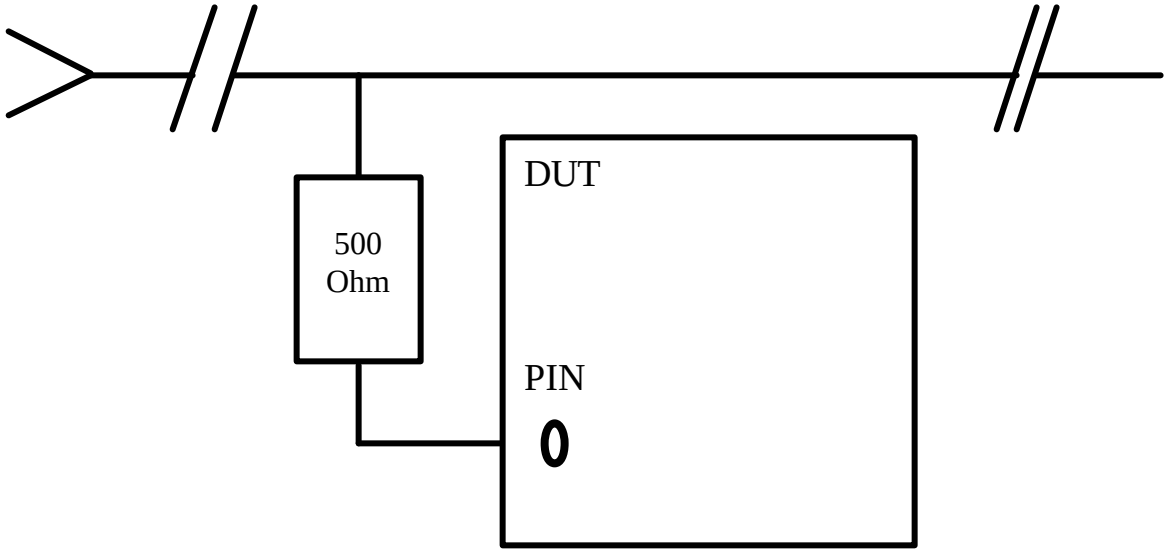
1. All Cores are of **1oz Cu**
2. Trace Width = **8 MILS**
4. Over all board thickness **62 MILS +/-10%**
5. Impedance is **50 Ohms +/-10%**
6. Material is **POLYIMIDE**
7. Minimum distance b/w the Traces on COMP is **15 MILS**
8. Minimum distance b/w the Traces on INR 1 & INR 2 is **25 MILS**
9. Direction of Traces on INR 1 & INR 2 must be **Perpendicular**

Simulation Cont'

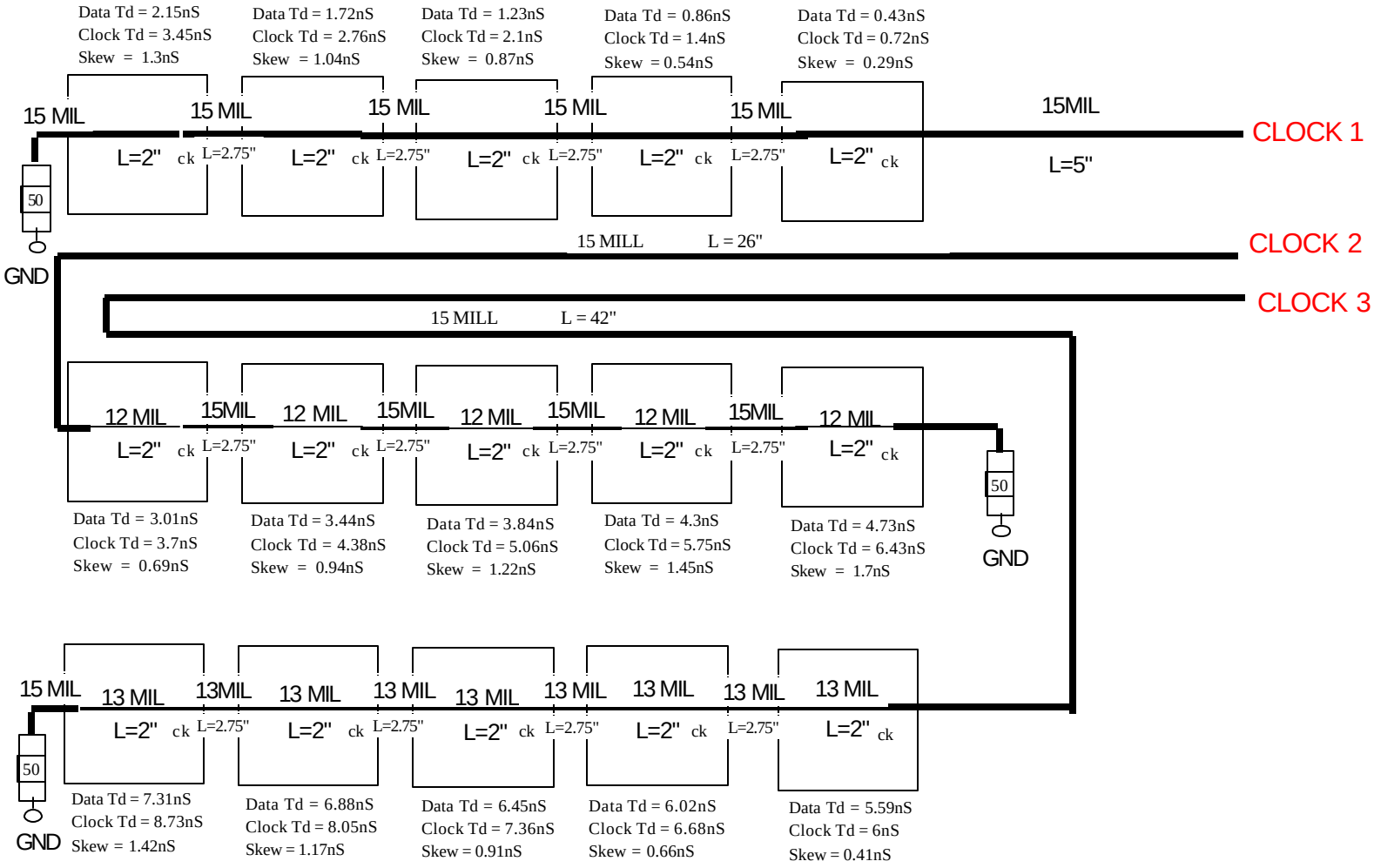
- **Pre-layout simulation**
  - **What-if scenario**
  - **Routing methodology for critical parameters**
  - **Termination selection**
  - **Component value estimation**



AC Term.



Simulation Cont'



FAT

- **Fabrication**
  - **Number of layers, drill count/size and impedance requirement add to complexity**
- **Assembly**
  - **Pin count, pin length and mounting affect assembly**
- **Test**
  - **Design probe**
  - **Verify actual board with schematic**

Burn-In Board Design Considerations

2000 Burn-in and Test Sockets Workshop

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PCB Design Manager
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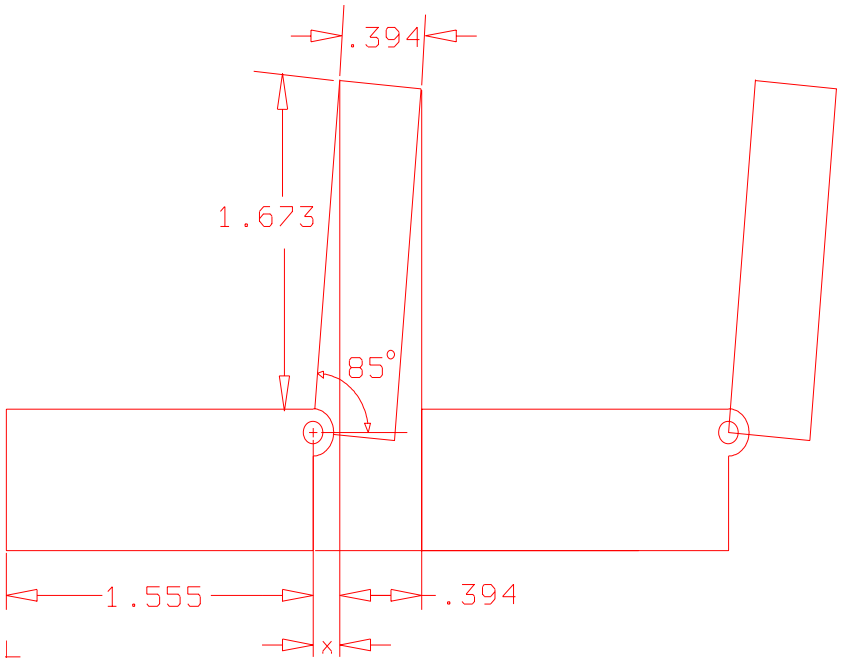
Agenda

- Mechanical Structures
  - Clam shell (“shadow spacing”)
  - Mounting hardware
- Electrical impact
  - Pitch of pins
  - Routing layers
- Through Hole
  - Clam shell (“shadow spacing”)
  - More stable mounting structure
- Surface Mount
  - Buried vias
    - Open routing paths
    - Testability

Mechanical Structures

- Clam Shell
  - Shadow spacing
- Open Top
  - Ability to move sockets closer than Clam Shell
  - Creates access to heat removal
- Mounting Hardware
  - Especially needed for SMT devices.
- Pin pitch
  - Reduces manufacturability

Calculating Shadow Spacing



- X = COS 85º * 1.673
- X = .087 * 1.673
- X = .146

- Shadow Spacing = .394 + .146
- Shadow Spacing = .540

- Total distance between sockets would the length of the socket (1.555) plus the shadow spacing (.540). In this example the distance is 2.095 minimum between sockets.

Electrical Impact

- **Pin pitch**
  - **Tighter pitch decreases trace width (signal and power)**
  - **Spacing between rows of pins (in QFPs) decreases routing space**
  - **Hole diameter for pins (and pad size needed) decrease routing space**
- **Routing Layers**
  - **Decreased trace width may mean using multiple routing layers for Power and Ground.**
  - **With increased layer counts, overall board thickness will be effected.**

Through Hole vs. Surface Mount

- **PROs**
  - More stable structure (pin vs vias)
  - Access for all pins for testing.
- **CONs**
  - Pin lead length
  - Holes for all pins through board.

- **PROs**
  - Blind vias would increase routing paths
  - Easier to drill tolerance for vias vs pin diameter.
  - Not limited by board thickness
- **CONs**
  - Blind vias limit accessibility for test.
  - More handling needed in assembly.