Burn-in & Test Socket Workshop 2000

Session 3

Evaluation and Characterization

IEEE COMPUTER SOCIETY

IEEE

IEEE COMPUTER SOCIETY

BiTS

IEEE

BURN-IN & TEST
SOCKET WORKSHOP

Presentations

“A Method For Measuring And Evaluating Contact Resistance In Burn-in And Test Sockets”

Angelo Giaimo
IBM Microelectronics

“Methodology For Characterizing RF Response Of Sockets And Test Contactors”

Valts Treibergs
PrimeYield Systems, Inc.

“Test And Burn-in Socket Evaluation For PBGA Devices”

Zenon Podpora
IBM Microelectronics

“Characterization Of High Performance Contactors For Production RDRAM Chip-scale Package Test”

Ken Karklin	Francois Billaut	Gary L. Chew
Agilent Technologies	Hewlett Packard	Hewlett Packard

A Method for Measuring and Evaluating Contact Resistance in Burn-in and Test Sockets

2000 Burn-in and Test Sockets Workshop

Angelo Giaimo

IBM Corporation

AGENDA

PROBLEM

- CHALLENGES IN CONTACT EVALUATION

MEASUREMENT THEORY REVIEW

- 2 POINT MEASUREMENTS
- 4 POINT MEASUREMENTS

SOLUTION

- INTRODUCTION OF P4PM SYSTEM
- HW/SW IMPLEMENTATION
- SAMPLE DATA: OPENS/DELTAR

CONCLUSION

- REVIEW

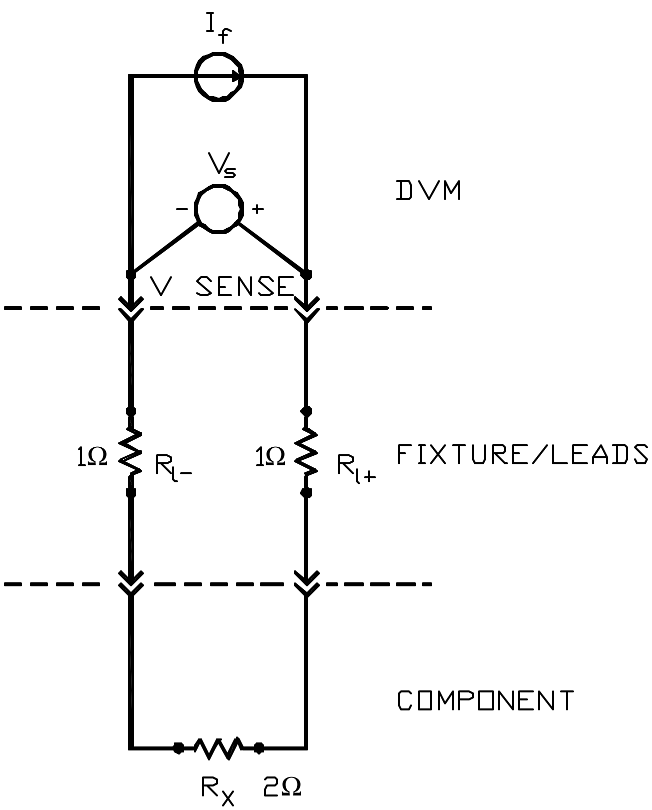
CHALLENGES IN CONTACT EVALUATION

- TIGHTER PITCH / LOWER CONTACT FORCE
- SHORTER CONTACTS / LOW COMPLIANCE
- INCREASED PIN COUNT / HIGH RELIABILITY CONTACT
- TAKE MORE SAMPLE DATA PER TOUCHDOWN

2 POINT MEASUREMENTS

- LEAST ACCURATE METHOD OF MAKING CONTACT RESISTANCE MEASUREMENTS.
- FIXTURE RESISTANCE CANNOT BE NULLED OUT.
- EASIEST METHOD TO MAKE MEASUREMENTS

2 POINT EXAMPLE

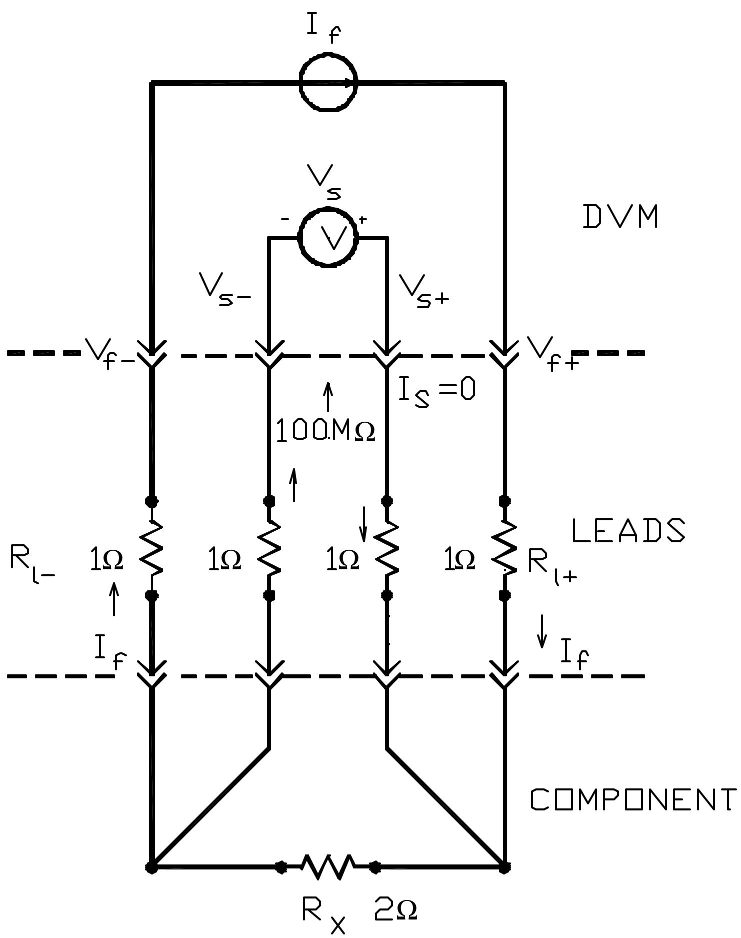


- Force Current I(f)
- Measure Voltage V(s)
- R(m) = V(s) / I(f)
- R(m) = R(x) + R(L+) + R(L-)
- Sense Point Location
- Measurement Error

4 POINT MEASUREMENTS

- Used when R(L) approaches R(x)
- More-accurate method of making contact resistance measurements.
- Lead and Fixture bulk resistance can be nulled out.
- Wiring for multiple measurements can get complex (4 points/contact measurement)

4 POINT EXAMPLE

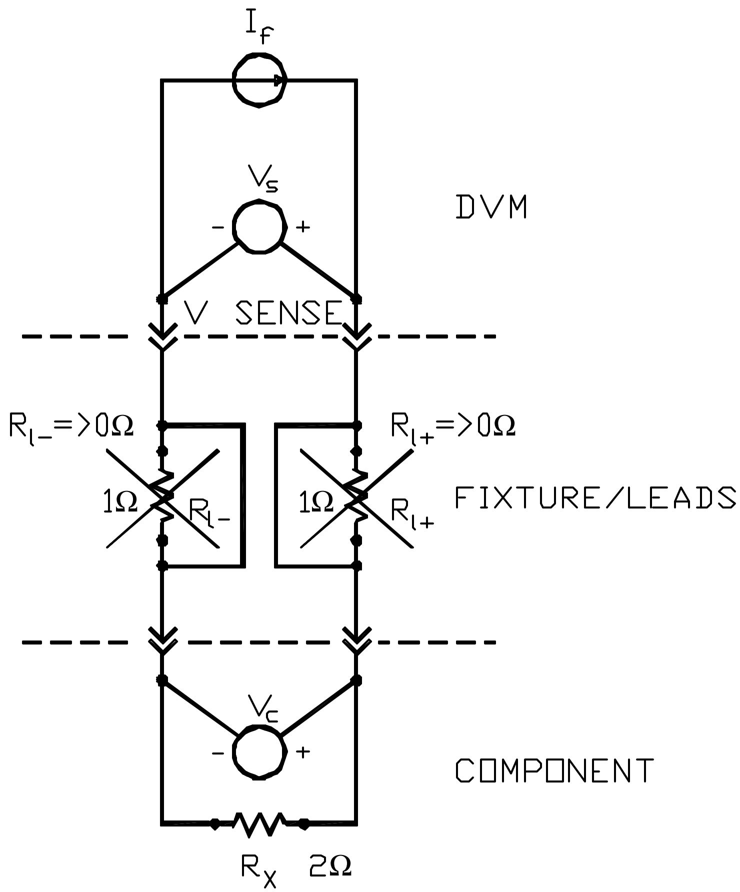


- Force I(f)
- Measure V(s)
- R(m) = V(s) / I(f)
- R(m) = R(x)
- Sense Point Location gives accuracy
- What if we relocate sense points?

PSEUDO 4 POINT MEASUREMENTS

- USES 2 POINT MEASUREMENT HWRE TO ACHIEVE 4 POINT MEASUREMENT ACCURACY.
- ACHIEVED BY “MOVING” THE SENSE POINTS TO THE CONTACT, OR,
- REDUCING THE EFFECTIVE R(L+) AND R(L-) => ZERO

P4PM SYSTEM THEORY

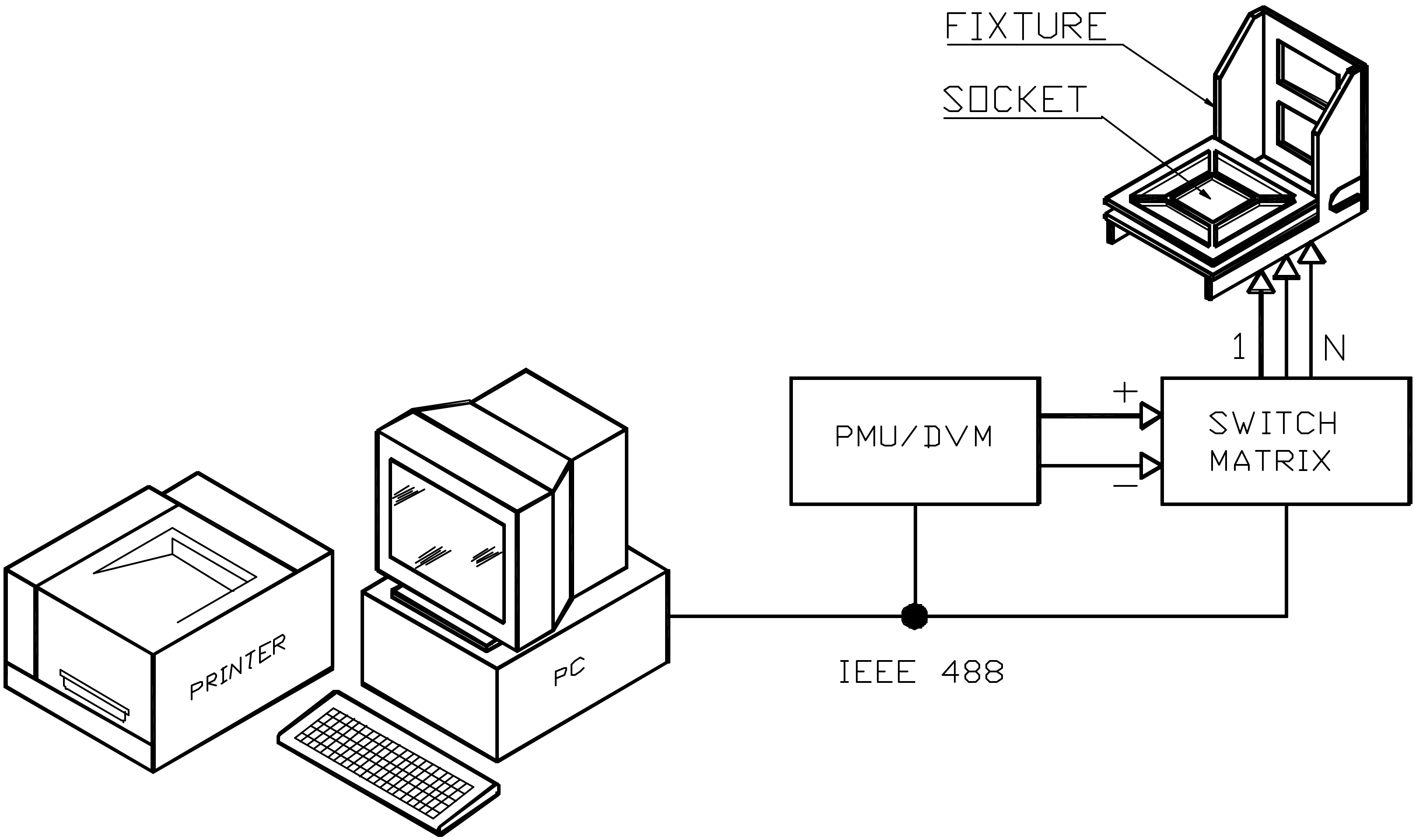


- Reduces R(L-) to 0 by creating multiple return paths. (Hardware)
- Reduces R(L+) to 0 by subtracting minimum values on a per-channel basis. (Software)

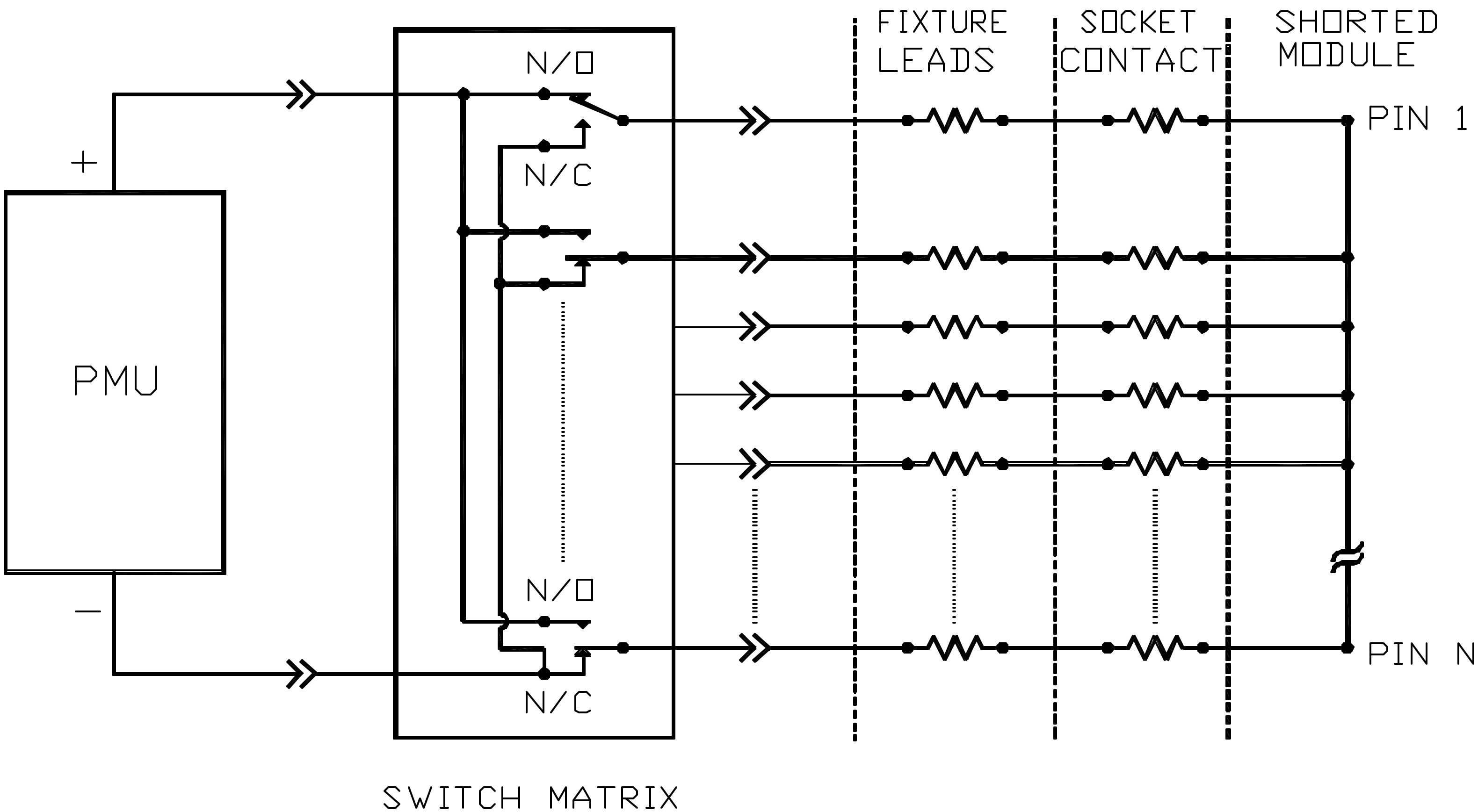
P4PM SYSTEM HARDWARE

- PC – FOR DATA STORAGE AND SYSTEM CONTROL (IEEE 488 BUSS)
- PMU – FOR CONTACT RESISTANCE MEASUREMENT
- SWITCHING MATRIX – FOR DUT I/O PIN SELECTION
- CONTACTOR FIXTURE – CONNECTS SWITCHING MATRIX TO SOCKET

P4PM SYSTEM

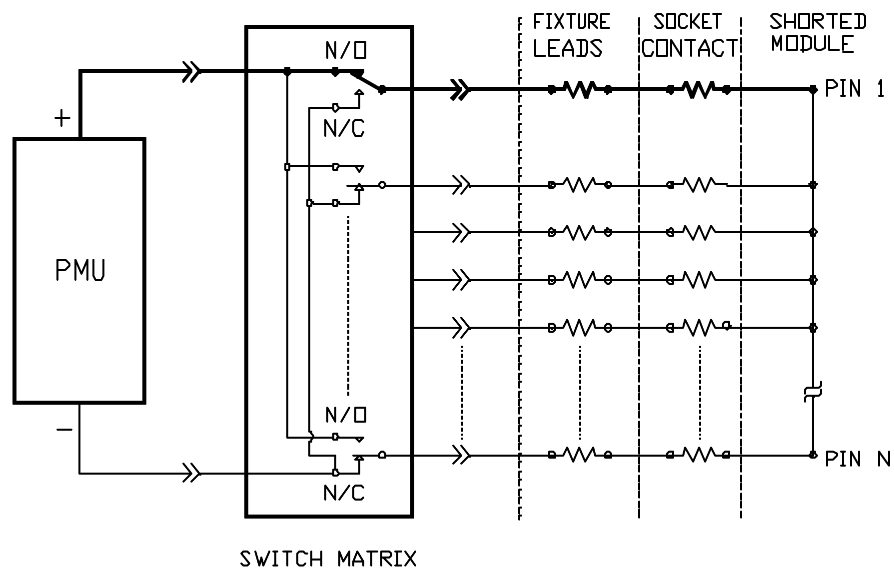


P4PM SYSTEM IMPLEMENTATION



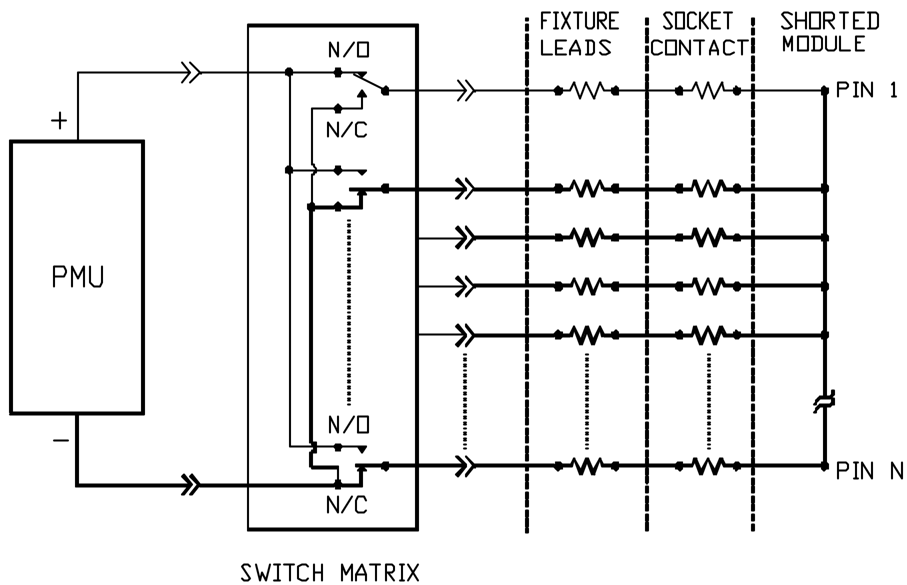
P4PM OPERATION (+)

- SELECT RELAY.
- +PATH IS THRU 1 PIN ONLY TO SHORTING DEVICE.
- R(+) = R(F) + R(C)
- STATISTICALLY REMOVE R(F), LEAVING R(C).



P4PM OPERATION (-)

- -PATH IS THRU N-1 UNSELECTED RELAYS
- IF N IS LARGE, R(-) => ZERO
- V(-) => ZERO



SYSTEM SOFTWARE I

- DATA COLLECTION:
  - SAVED BY CHANNEL, READING, JOB, TESTER AND FIXTURE; DATE & TIME.
- CALCULATIONS:
  - MINVALUE PER CHANNEL PER JOB
  - UPDATE MINVALUE FILE. (MULTIPLE MINVALUE FILES FOR DIFFERENT TESTERS AND FIXTURES)
  - R(C)=(READING-MINVALUE)/I(F)

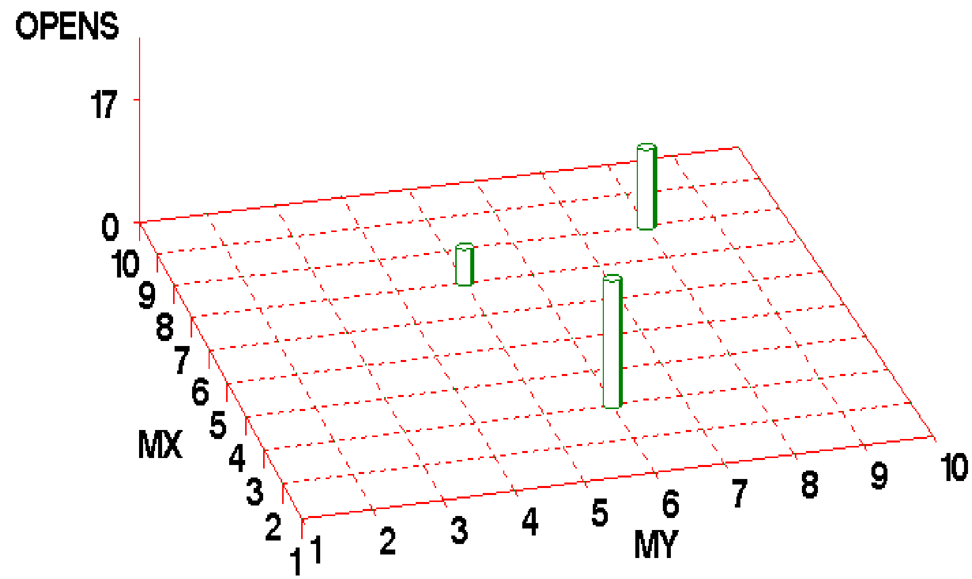
SYSTEM SOFTWARE II

- R(C)
- AVERAGE R(C)
- OPEN PINS
- THRESHOLD VALUES

- TABLE / GRAPH
- BY PIN LOCATION
- BY MODULE
- BY JOB
- BY SOCKET

OPENS EXAMPLE

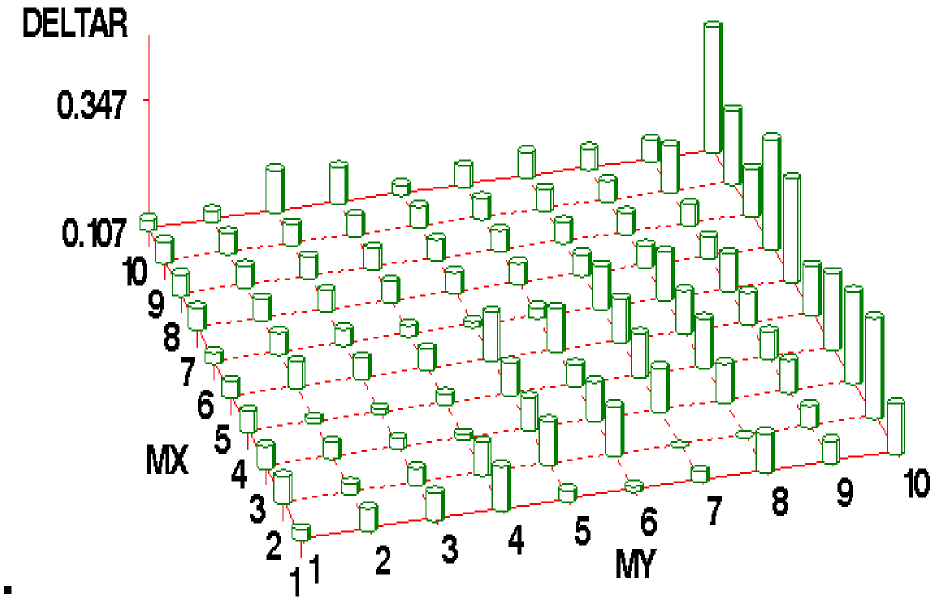
- LOW YIELD – INTERMITTENT SOCKET
- 50 CYCLE TEST
- GRAPH SHOWS FREQUENCY OF FAILED PINS



SOCKET PIN OPENS DISTRIBUTION

R(C) EXAMPLE

- TO SHOW R(C) VARIATIONS ACROSS SOCKET
- SINGLE READING OR STATISTICAL READINGS ACROSS SOCKET. (MIN/MAX/AV)



SOCKET PIN DELTAR DISTRIBUTION

MEASUREMENT ERROR

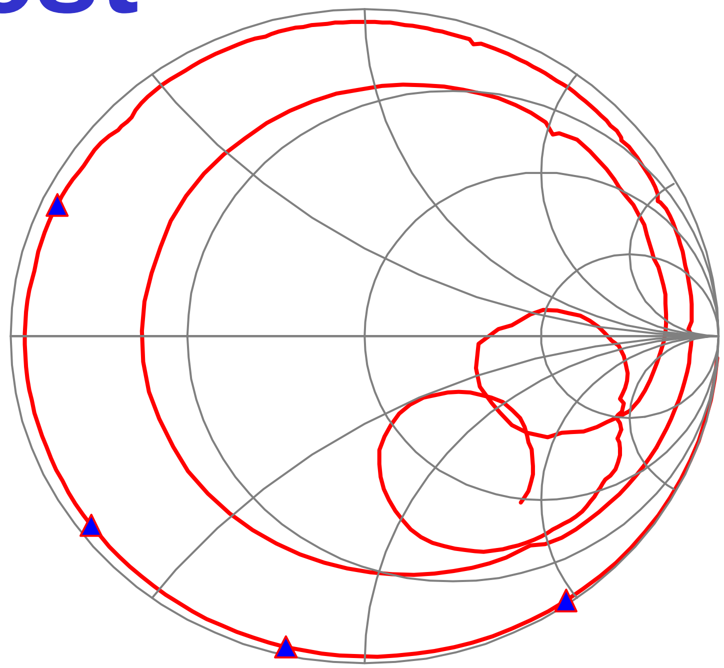
- NOTE: ALL MEASUREMENTS ARE BASED ON MINVALUE = 0 R(C)
- TRY TO INSURE THAT R(-) x I(F) IS LESS THAN LSB OF PMU OR DESIRED RESOLUTION.
- LOW I/O SOCKETS PRONE TO ERROR DUE TO FEWER RETURN PINS.

CONCLUSION

- DESCRIBED CHALLENGES
- REVIEWED 2 AND 4 POINT MEASUREMENTS
- INTRODUCED P4PM SYSTEM
- SHOWED IMPLEMENTATION HW/SW
- EXAMPLE WITH SAMPLE DATA
- MEASUREMENT ERROR

Methodology for Characterizing RF Response of Sockets and Test Contactors

Theory & Basic Techniques Using Readily Available Tools



BURN-IN & TEST SOCKET WORKSHOP

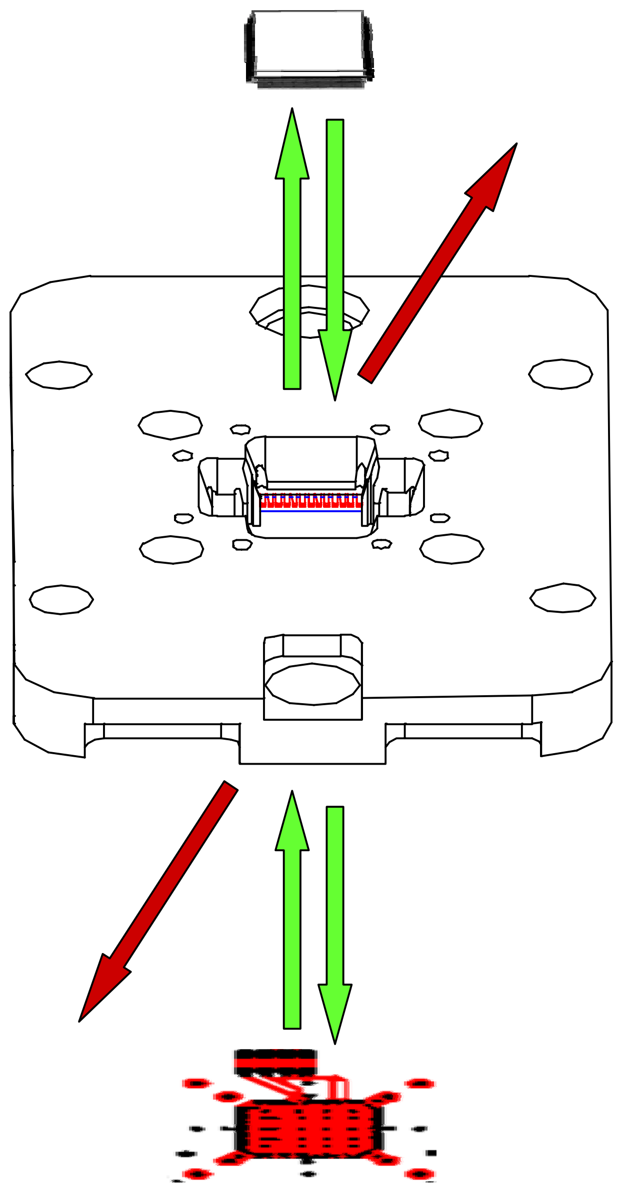
Valts Treibergs

PrimeYield Systems, Inc.

PrimeYield Systems, Inc.

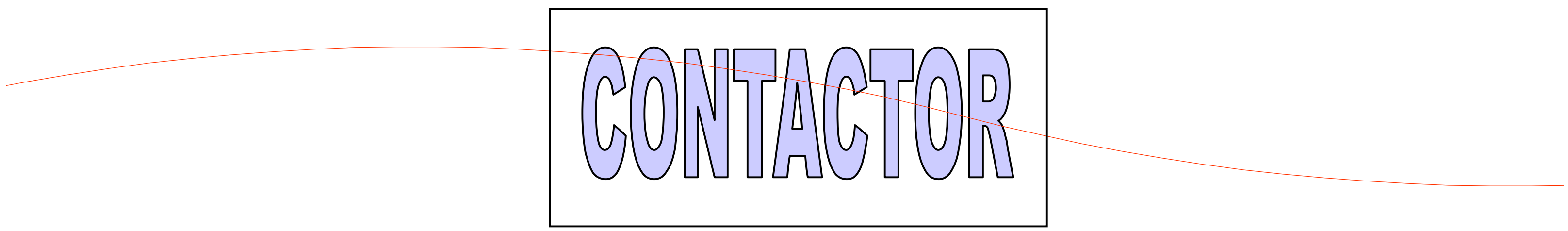
Topics

- **Transmission Line Basics**
  - **Impedance**
  - **Inductance and Capacitance**
  - **Frequency Domain Response**
    - **Reflection**
    - **Transmission**
- **Tools and Fixturing**
  - **Vector Network Analyzer**
  - **Air Coplanar Probes**
  - **Printed Circuit Board Considerations**
- **Measurement Techniques**
- **Results**

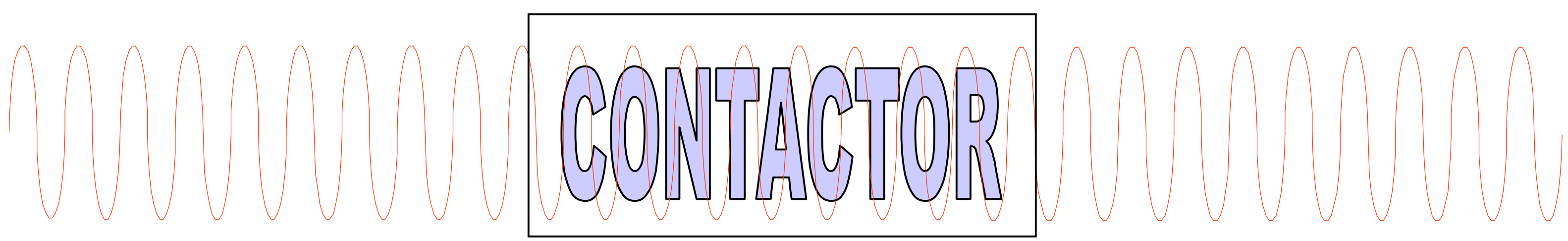


Transmission Line Basics

- A transmission line is used to transfer AC signals with minimum power loss efficiently from one device to another
  - At low frequencies (wavelengths >> structure size), voltage and current are not dependent on time



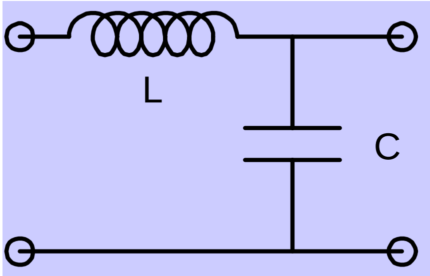
  - At high frequencies (wavelengths ≈ or << structure size), characteristic impedance (Z_0) must be matched, voltage is dependent on time



Transmission Line Basics

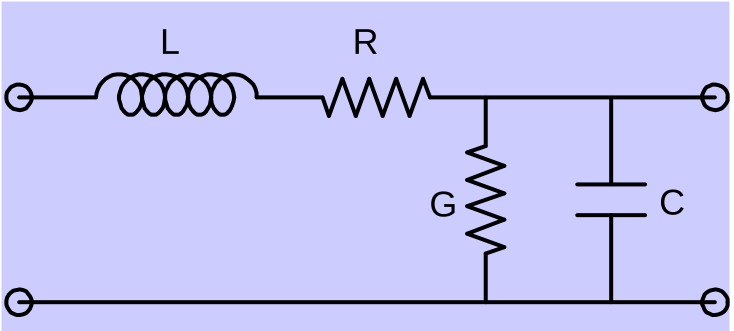
Characteristic Impedance Z_0

- In a lossless transmission line, the physical geometry alone defines a constant quantity: the Characteristic Impedance (Z_0)
- Z_0 is a function of geometry of the conductors and the dielectric properties of the structure
- The unit of impedance is the ohm (Ω)
- The time delay or electrical length of the transmission line is t_d (seconds)
- The lossy transmission line includes series inductance and shunt capacitance with resistances



$$Z_0 = \sqrt{\frac{L}{C}}$$

$$t_d = \sqrt{LC}$$

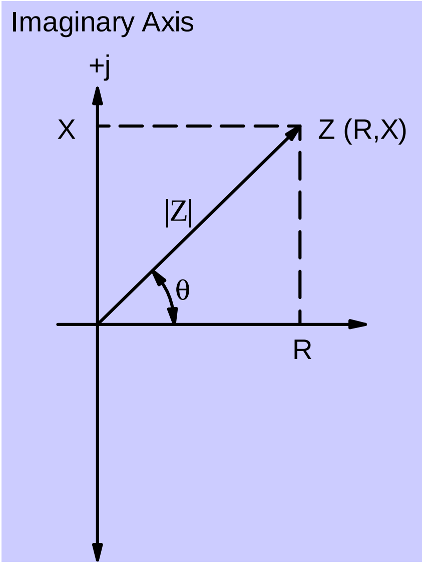


Transmission Line Basics

Impedance Z as a Vector Quantity

- Since a transmission line carries an AC signal, impedance inherently is a vector quantity - it has magnitude and phase
- The real part of the vector is resistance (R) and is ≥ 0
- The imaginary part of the vector is reactance (X)
  - Reactance takes two forms - Inductive(X_L) and Capacitive (X_C)
- f = frequency (Hz), ω = angular frequency (rad/s)

$$Z = R + jX = |Z| \angle \theta$$



INDUCTIVE: $jX>0$

CAPACITIVE: $jX<0$

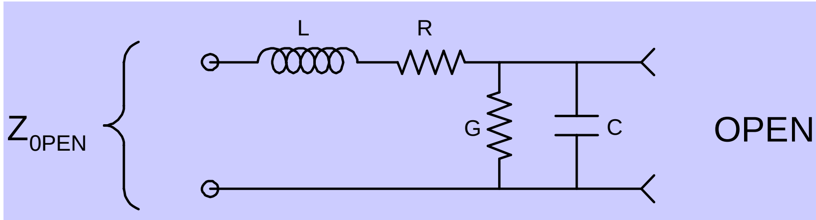
$$X_C = \frac{1}{2\pi f C} = \frac{1}{\omega C}$$

$$X_L = 2\pi f L = \omega L$$

Transmission Line Basics

Extracting L and C

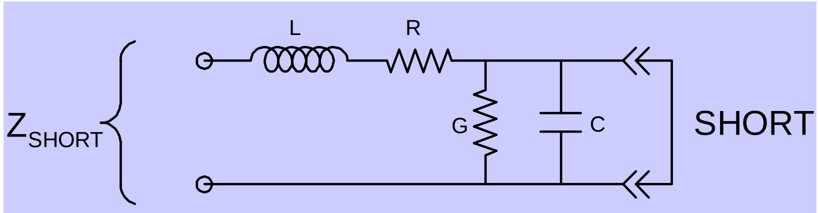
- **OPEN CIRCUIT**
  - Essentially zero current is flowing through L and R
  - **Capacitive reactance** is dominant
  - Capacitance is expressed in Farads (F)



$$Z_{OPEN} = \frac{1}{G_{OPEN} + j\omega C_{OPEN}}$$

$$\left(R_{OPEN} + j\omega L_{OPEN} << \frac{1}{G_{OPEN} + j\omega C_{OPEN}} \right)$$

- **SHORT CIRCUIT**
  - Essentially all current bypasses C and G
  - **Inductive reactance** is dominant
  - Inductance is expressed in Henrys (H)



$$Z_{SHORT} = R_{SHORT} + j\omega L_{SHORT}$$

Transmission Line Basics

Sockets and Contactors as Transmission Lines

<u>REFLECTION (A/R)</u>

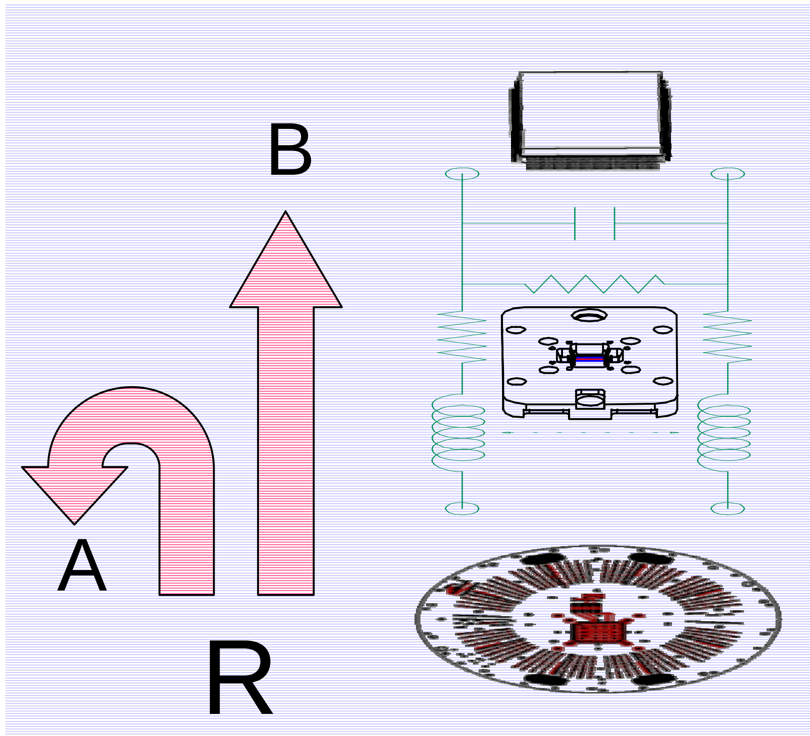
•Reflection Coefficient (Γ,ρ)

•Impedance (R+jX)

•Return Loss

•SWR

•S_{11}, S_{22}



<u>TRANSMISSION (B/R)</u>

•Transmission Coefficient (T,τ)

•Insertion Phase

•Insertion Loss

•Group Delay

•S_{21}, S_{12}

- Sockets and contactors do not have a single characteristic impedance because of the mechanical requirements and different materials
- Transitions in impedance result in signals passing through the contactor to be partially reflected back to the source of the signal

Reflection

Reflection Coefficient

- Γ is a complex quantity, and ρ is the magnitude portion, Φ is the phase angle
- Z_0 is system impedance
- Z_L is device impedance
- Γ is a function of frequency
- The Smith Chart maps rectilinear impedance onto the polar reflection plane
  - Circles are constant resistance
  - Arcs are constant reactance
  - $Z_L=Z_0$ is chart center - perfect load
  - $Z_L= \infty$ is at 0° - OPEN
  - $Z_L= 0$ is at 180° - SHORT

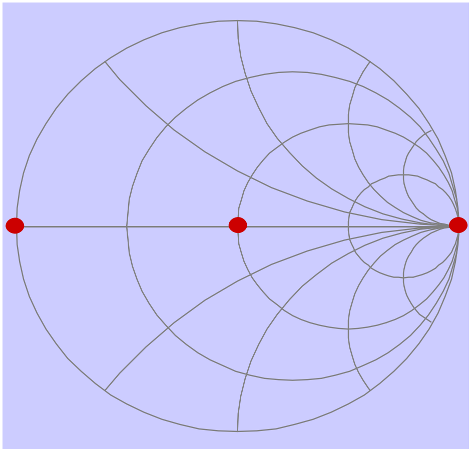
$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \rho\angle\Phi = \frac{Z_L - Z_0}{Z_L + Z_0}$$

$$0 \geq \rho \geq 1$$

$$\text{Return loss} = -20\log(\rho)\ \text{dB}$$

$$\text{Return loss} \leq 0$$

$$\text{SWR} = \frac{1+\rho}{1-\rho} \qquad \text{SWR} \geq 1$$



$$Z_L = Z_0 \frac{(1+\Gamma)}{(1-\Gamma)}$$

Transmission

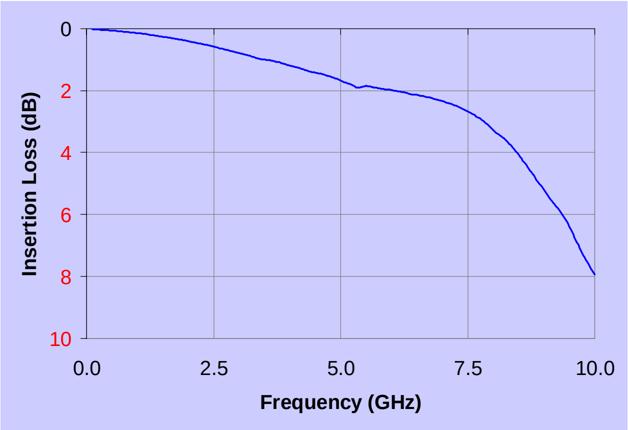
Transmission Coefficient

- T is a complex quantity, and τ is the magnitude portion, ϕ is the insertion phase angle
- T is a function of frequency
- If $|V_{\text{transmitted}}|<|V_{\text{incident}}|$, you have attenuation or insertion loss
- Insertion loss is a measure of the frequency bandpass characteristics of the transmission line
- Device bandwidth is commonly defined as the frequency where the insertion loss attains 1dB or 3dB
- Differentiating the phase response gives group delay, or electrical length, t_d in seconds over frequency

$$\mathrm{T} = \frac{V_{transmitted}}{V_{incident}} = \tau \angle \phi$$

$$\text{Insertion loss} = -20 \log \tau$$

$$\text{Insertion loss } (dB) \leq 0$$



Tools and Fixturing Required for RF Measurements

- **Vector Network Analyzer**
  - HP 8510C and HP 8720D VNA families are common
  - Must be capable of full 2-port error correction and calibration
- **Air Coplanar Probes**
  - Available in many different configurations from different manufacturers ‘off the shelf’
- **Calibration Substrate**
  - Must have calibration data for VNA to be used
- **PC Boards Designed to Simulate Contactor in Use**
- **Probing Station**
- **Data Analysis Software**
- **Patience**

The Vector Network Analyzer

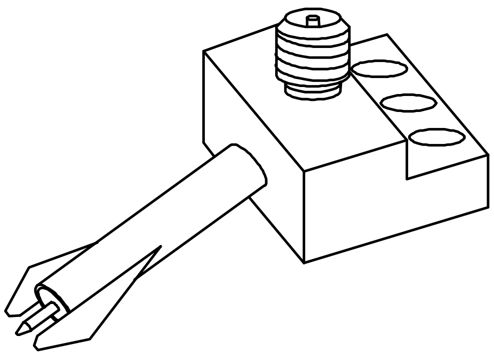
Capabilities Needed for Contactor Characterization

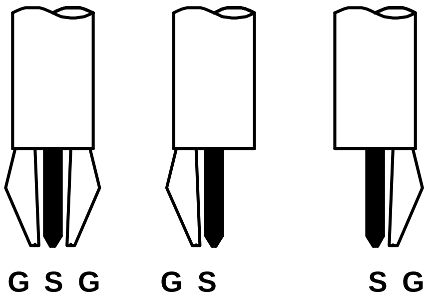
- **Full 2-Port S-parameter measurements**
  - S_{21} or S_{12} needed for bandwidth measurements
  - S_{11} or S_{22} needed for reflection, capacitance and inductance measurements
- **Be Capable of SOLT Vector Calibration and Error Correction**
- **Frequency of VNA Must Be Greater Than That of Desired Measured Values**
- **Time Domain Capability**
  - Can be very useful in troubleshooting set-ups

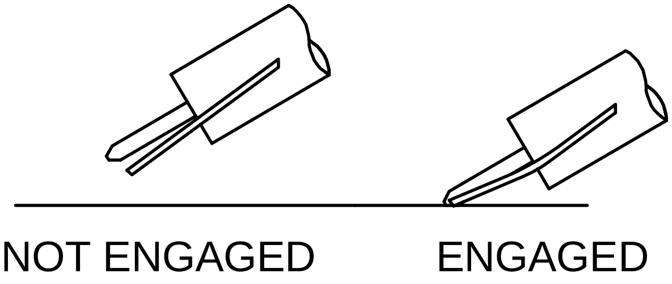
HP 8510C Vector Network Analyzer

Air Coplanar Probes

- Probes available with different coaxial connectors (SMA, K, 3.5mm, 2.4mm, etc.)
- Match connector with extension cable of VNA
- Probes available to 1250 micron pitch
- Probe mounts must be matched to probing station manipulator
- PROBES ARE VERY DELICATE!!!

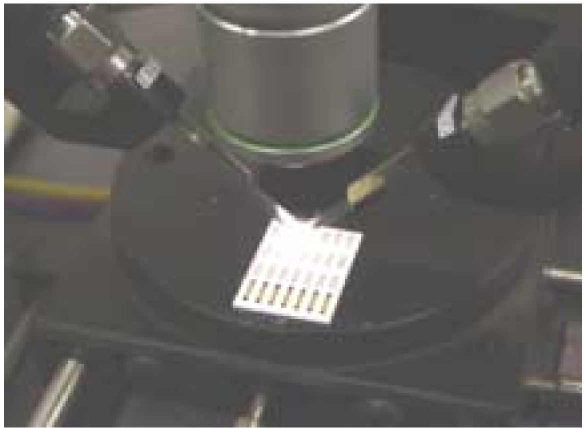


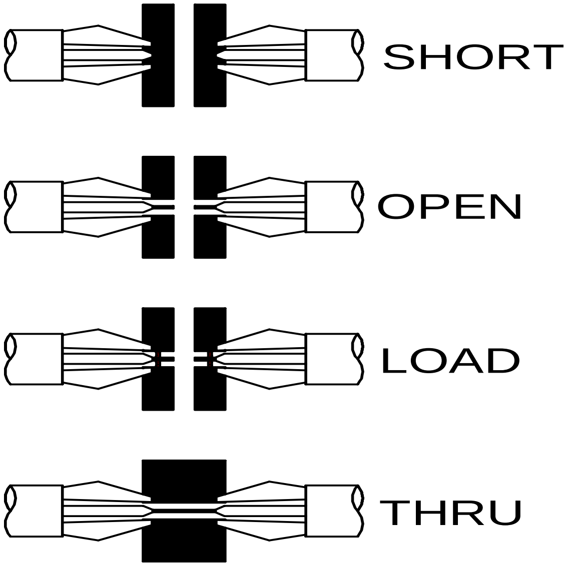




ACP Calibration Standard Substrate

- **Precision alumina substrate with calibration structures for ACP probing**
  - **SOLT (Short, Open, Load, Through) structures**
- **Calibration constants for VNA**
  - **Floppy disk, tape, or hardcopy constants**
- **Calibration standard should match probes used**
- **Substrate may also have additional structures to be used for calibration verification**

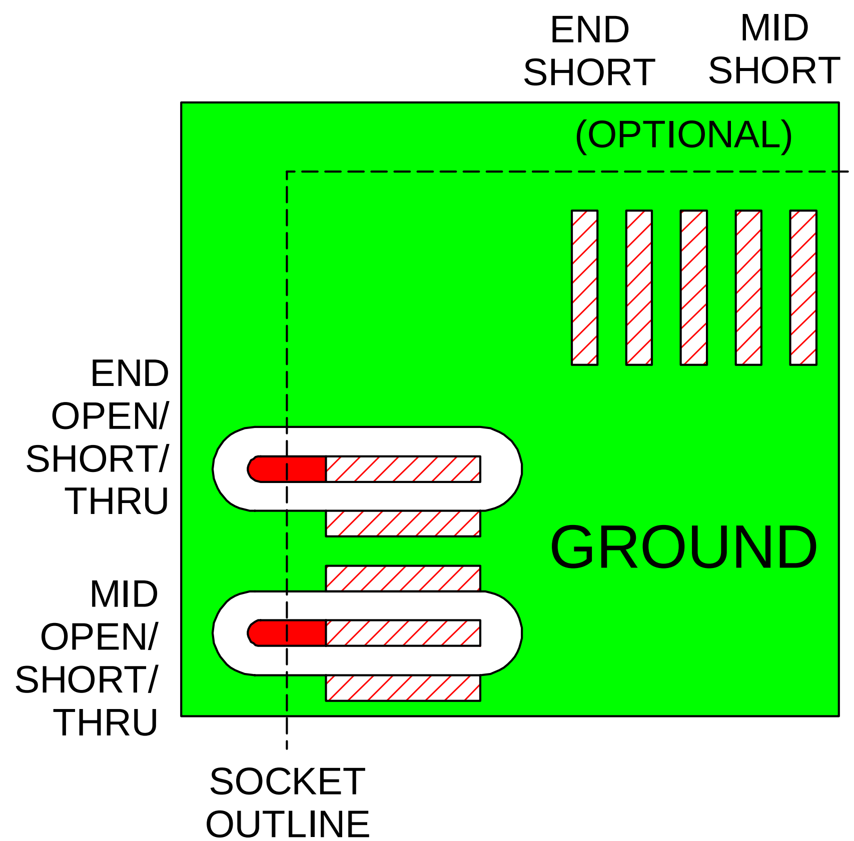




Printed Circuit Boards

Peripherally Leaded Contactors

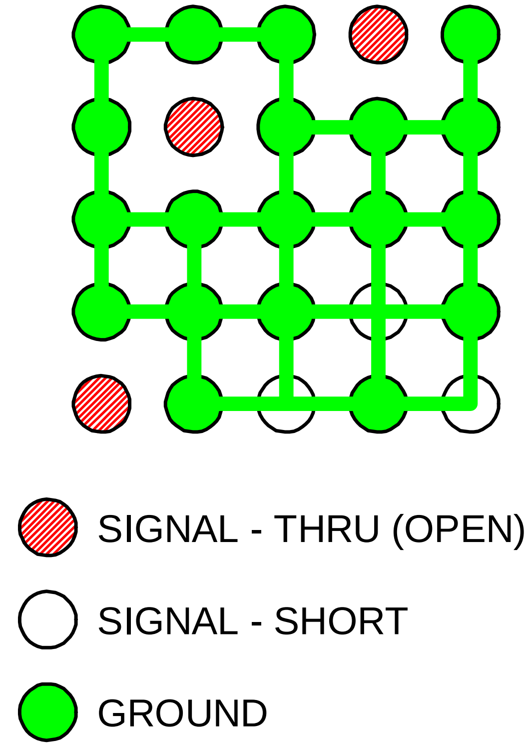
- Contactor footprint pattern must adhere to manufacturer's recommended layout
- Keep additional signal traces to a minimum length (.010") [.25mm] max beyond contactor
- PCB can be 1-sided
- Consider end contacts as well as mid-array contacts
- 1 Required structure:
  - Thru /OPEN / SHORT
- Optional SHORT structure for S_{22} SHORT
- Place ground wherever possible
- Gold plating is best, no soldermask

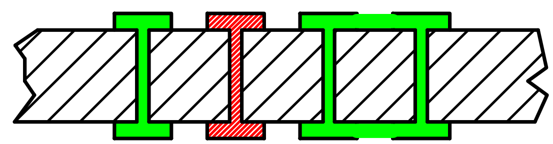


Printed Circuit Boards

Area Array Sockets

- Socket footprint pattern must adhere to manufacturers recommended layout
- Signal traces are plated through vias
- Use thinnest PCB possible to keep signal length short
- PCB must be 2-sided
- Consider corner, edge, and mid-array contacts
- 2 Required structures for each:
  - Short
  - Through
- Open measurements made on bare PCB or dummy pads
- Gold plating recmmended, no soldermask





Probing Station

- Choose or build a probing station with generous X, Y, Z travel of both the manipulators and the optical microscope
- Probing stations designed for wafer probe may not be suitable
  - often not enough Z travel
- Manipulators should be compatible with probe mounting holes
- Area array ‘THRU’ measurements need some custom fixturing so that one probe can be mounted beneath the PCB, or so that both probes can be mounted horizontally
- Both wide and narrow field microscopes are useful
- Cables to VNA must be long enough to easily reach the probes

MP-10

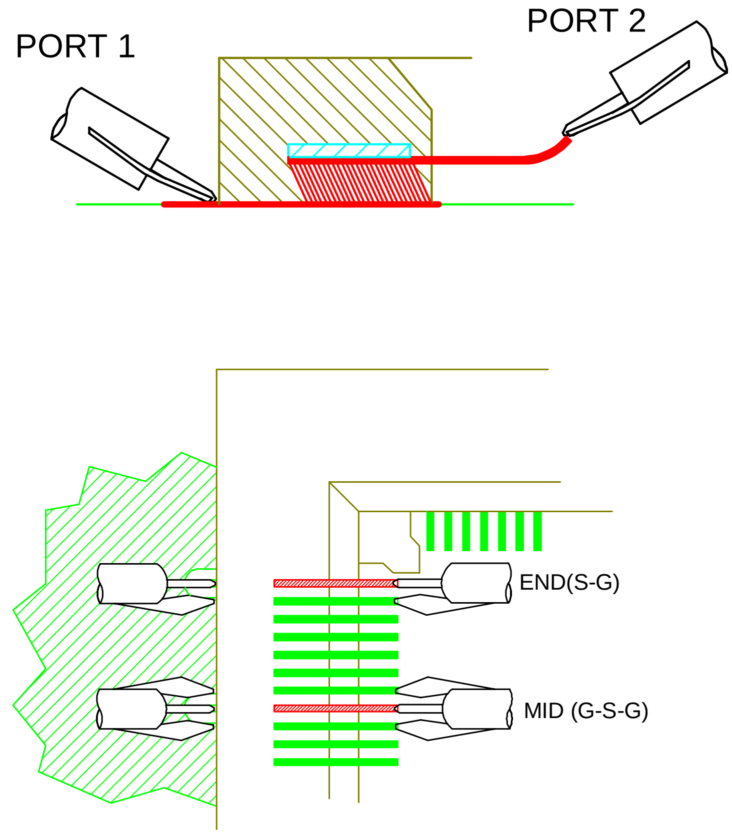
Measurement Techniques

- Perform full 2-Port VNA calibration using ACP substrate to desired frequency
- Transmission Measurements (2 Port)
- Reflection Measurements (1 Port)
  - Both OPEN and SHORT circuit measurements needed
- Measurement Configurations:
  - Peripherally leaded contactors
  - Area array contactors
- Save each measurement electronically as raw data
- Analyze the data in a spreadsheet or on the VNA

Transmission Measurements

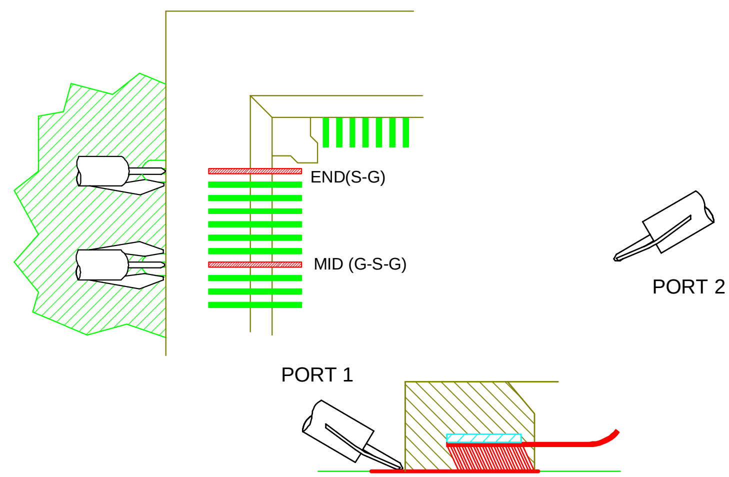
Peripherally Leaded Sockets

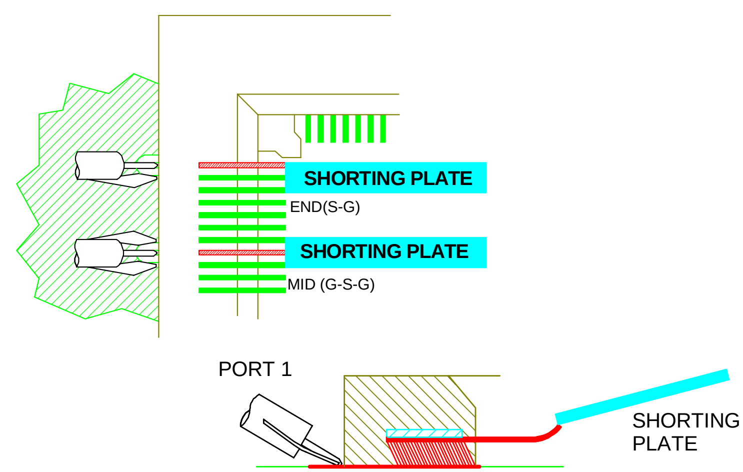
- Place Port 1 probe at outside contactor as close as possible on THRU structure (.010” max from contactor)
- Place Port 2 probe on corresponding contact where actual DUT would engage
- Measure end- and mid-array contacts
- Save S_{21} and S_{12} data



Reflection Measurements
Peripherally Leaded Sockets

- **OPEN MEASUREMENTS**
  – Place Port 1 probe at outside contactor as close as possible on THRU structure (.010 “ max from contactor)
  – Remove or raise Port 2 probe a minimum of 3X contact tip height
  – Measure end- and mid-array contacts
  – Save S_{11} data
- **SHORT MEASUREMENTS**
  – Port 2 probe is removed
  – Place shorting plate on contact tips where actual DUT would engage
  – Place Port 1 probe at outside contactor as close as possible on THRU structure (.010” max from contactor)
  – Measure end- and mid-array contacts
  – Save S_{11} data

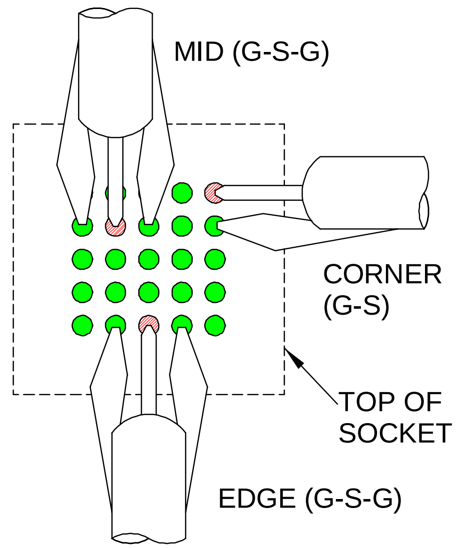


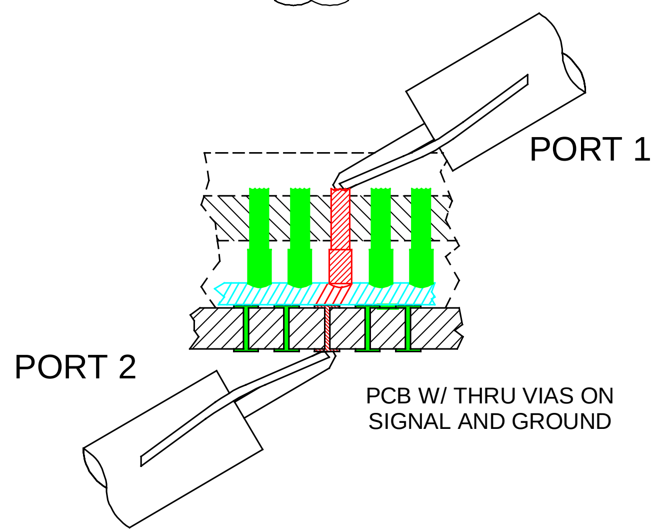


Transmission Measurements

Area Array Contactors

- Fixture contactor and PCB on its side in probing station
- Precompress contacts if necessary
- Place Port 2 probe at opposite side of PCB via on THRU structure
- Place Port 1 probe on corresponding contact where actual DUT would engage
- Measure corner, edge, and mid array contacts
- Save S_{21} and S_{12} data
- **THIS IS THE MOST DIFFICULT FIXTURING. PROBES MUST BE MOUNTED FIRMLY AND ACCURATELY. USE AN EXTERNAL MICROSCOPE FOR MANEUVERING.**

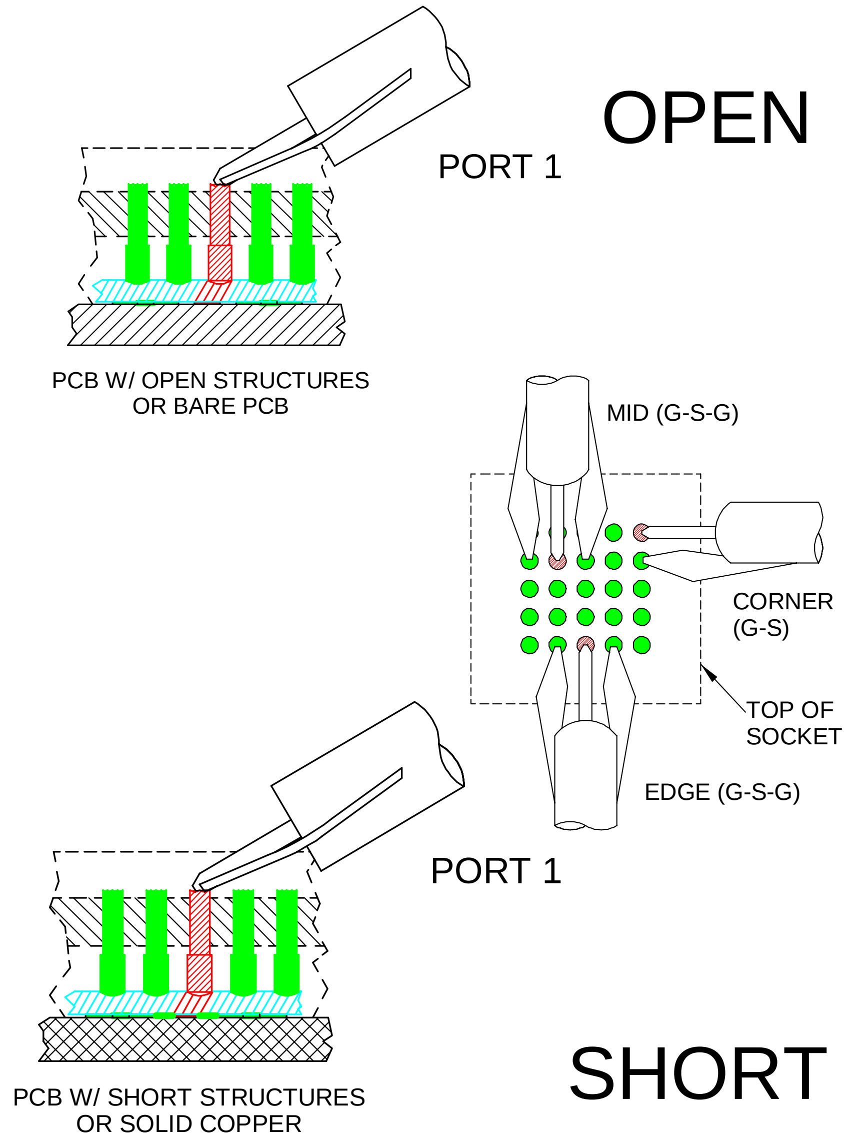




Reflection Measurements

Area Array Sockets

- For **OPEN** measurements, use a bare PCB or PCB with dummy pads
- For **SHORT** measurements, use a solid copper plate or shorting structures on the PCB
- Fixture contactor and PCB normally or on its side in probing station
- Precompress contacts if necessary
- Port 2 probe is not needed
- Place Port 1 probe on corresponding contact where actual DUT would engage
- Measure corner, edge, and mid array contacts
- Save S_{11} data



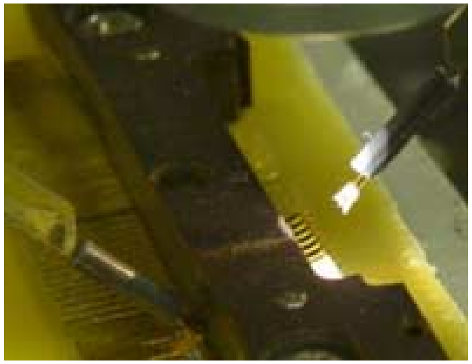
Results (Crunching the Numbers)

- VNA data files contain real and imaginary reflection and transmission coefficients of all frequency points (or time domain increments) tested for S_{11}, S_{21}, S_{12}, and S_{22}
- Data files generated by the VNA can be imported into a spreadsheet program such as Microsoft® Excel
- The following can be automatically calculated: Insertion loss, phase, deviation from linear phase, electrical delay, impedance, capacitance, inductance, return loss, VSWR, etc.
- Standard log-mag, real and polar plots of all of the above can be generated, including Smith Charts with full marker capability

Results

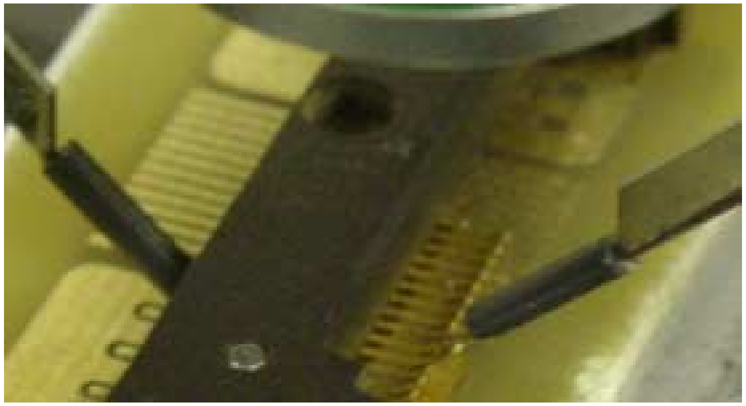
Example - PrimeYield Systems .8mm QFP Contactor

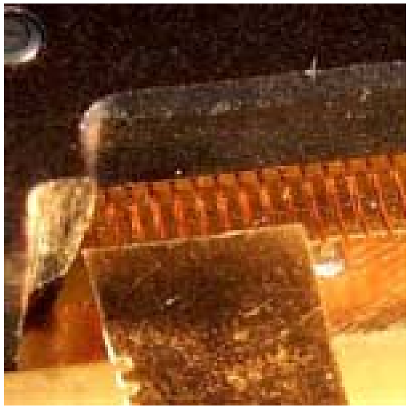
- Contactor was cut away for fixture development
- A PCB was constructed as described earlier
- 800µm air coplanar probes were chosen (G-S-G)
- THRU, OPEN, and SHORT configuration frequency and time domain data was recorded to 15 GHz on a HP 8510C VNA.
- All data analyzed and displayed in Excel



OPEN measurement

THRU measurement





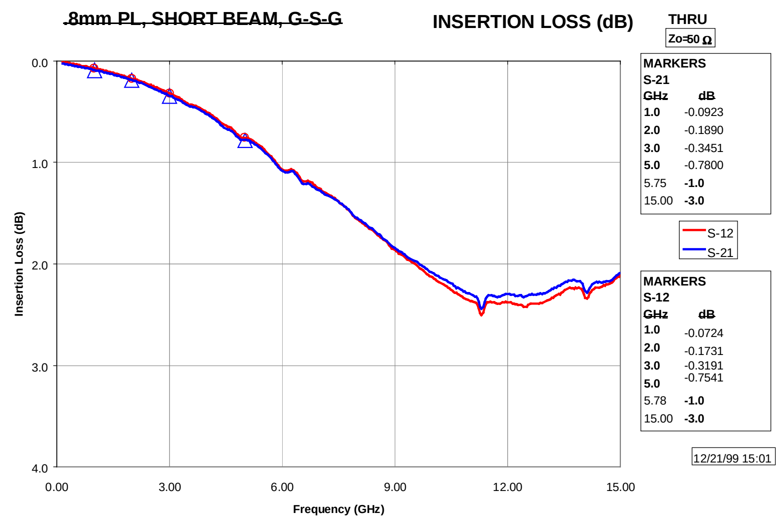
SHORT measurement

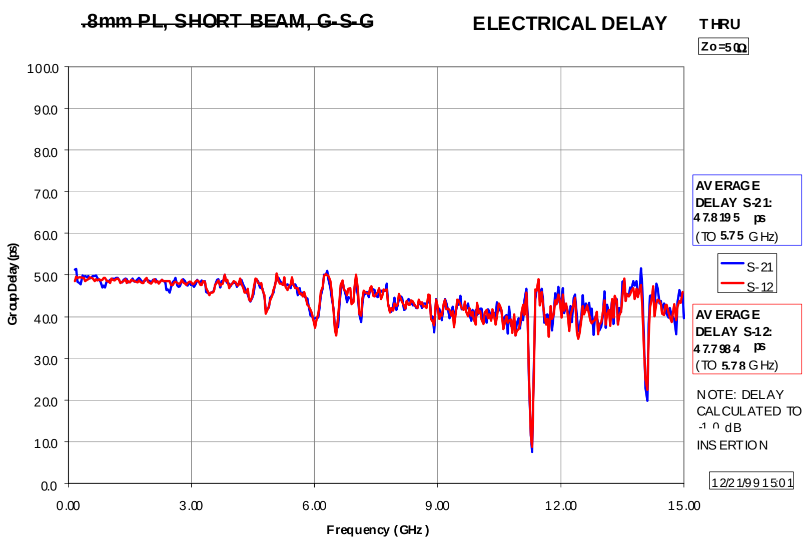
Results

Example - PrimeYield Systems .8mm QFP Contactor

Bandwidth - Insertion Loss

- Calculated from S_{21} and S_{12} THRU measurements
- -1 dB at 5.75 GHz
- -3 dB at > 15 GHz
- Data contains PCB parasitics





Electrical Delay

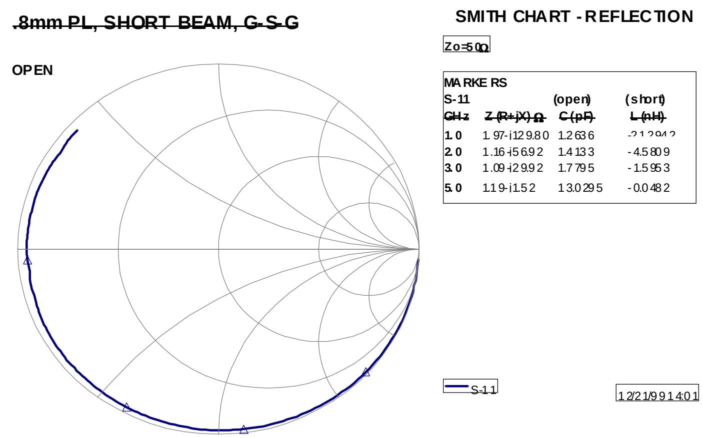
- Calculated from S_{21} and S_{11} THRU measurements
- 47.81 ps delay
- Stable, linear behavior to 6.00 GHz
- Data contains PCB parasitics

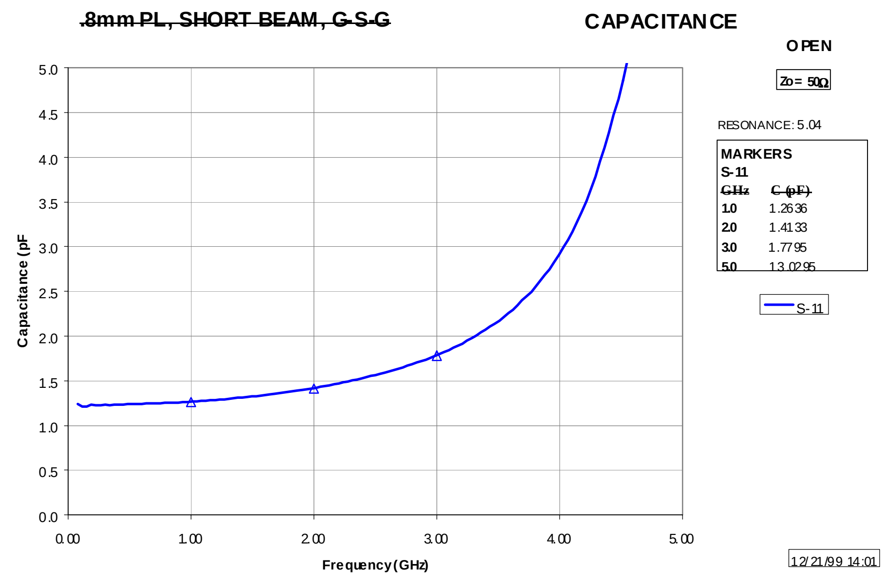
Results

Example - PrimeYield Systems .8mm QFP Contactor

Capacitive Reactance

- Calculated from S_{11} OPEN measurement
- 1.26 pF at 1.0 GHz
- 1.41 pF at 2.0 GHz
- 1.78 pF at 3.0 GHz
- Resonance seen at approximately 5 GHz
- Data contains PCB parasitics



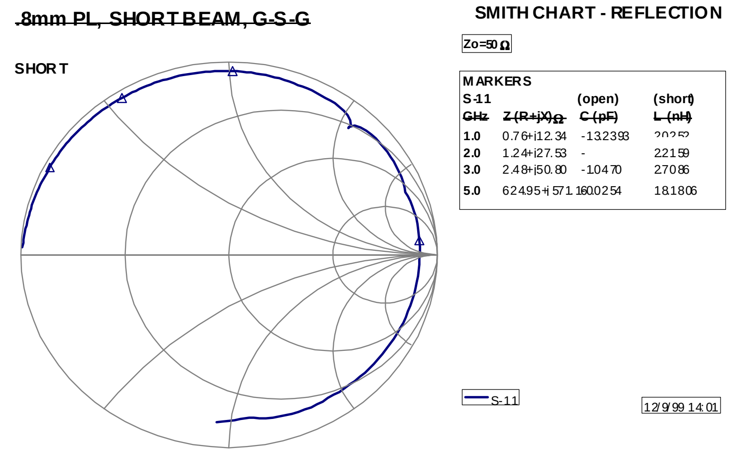


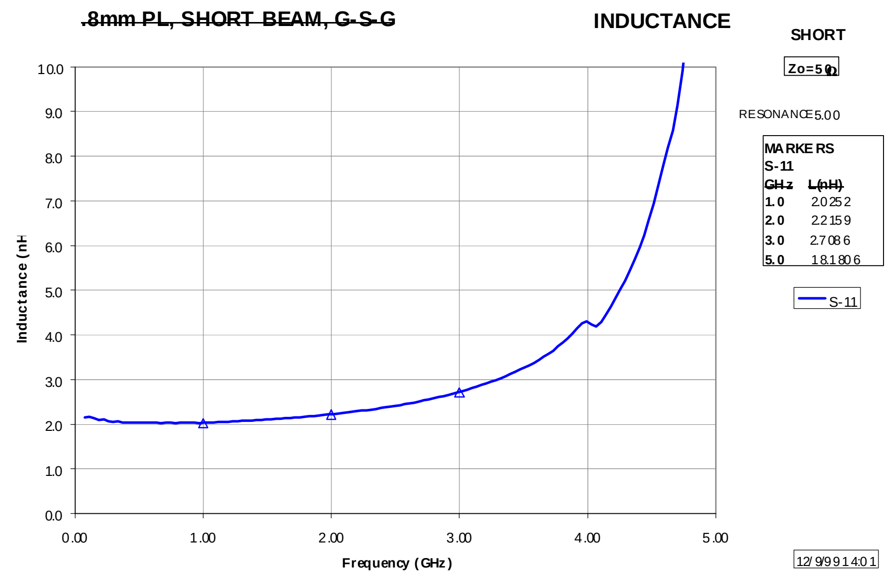
Results

Example - PrimeYield Systems .8mm QFP Contactor

Inductive Reactance

- Calculated from S_{11} SHORT measurement
- 2.03 nH at 1.0 GHz
- 2.22 nH at 2.0 GHz
- 2.71 nH at 3.0 GHz
- Resonance seen at approximately 5 GHz
- Data contains PCB parasitics - probably most influential





References / Bibliography

- M. Honda: *The Impedance Measurement Handbook*, Hewlett-Packard 1989
- Fabrio Zanella and Mark Galius: *Optimizing Signal Integrity in High Speed PCB Connectors*, Electronic Packaging and Production, April 1993
- *Understanding the Fundamental Principles of Vector Network Analysis*, Hewlett-Packard, Application Note 1287-1
- William Hayt, Jr.: *Engineering Electromagnetics*, Mcgraw-Hill 1958,1967, 1974
- Donald Dearholt: *Electromagnetic Wave Propoagation*, McGraw-Hill 1973
- Howard Johnson, Martin Graham: *High-Speed Digital Design*, Prentice Hall, 1993
- *Obtain S-Parameter Data from Probe*, MicroSim design Source Newsletter, April 1994
- *S-Parameter Techniques for Faster, More Accurate Network Design*, Hewlett-Packard, Application Note 95-1
- *8 Hints for Making Better Network Analyzer Measurements*, Hewlett-Packard Application Note 1291-1
- David Ballo: *Network Analyzer Basics*, from *'Back to Basics Seminar'*, Hewlett-Packard 1998
- David Dascher: *Measuring Parasitic Capacitance and Inductance Using TDR*, Hewlett-Packard Journal, 1996

Test and Burn-in Socket Evaluation for PBGA Devices

2000 Burn-in and Test Socket Workshop

Zen Podpora
IBM Microelectronics
Contacting Systems Engineering

02/27/2000

Objectives

- Socket selection / evaluation parameters
- Socket design considerations for socket developers
- Possible consequences of poor socket selection

Agenda

Intro to sockets

- Basic functions of test and burn-in sockets
- Typical socket structure

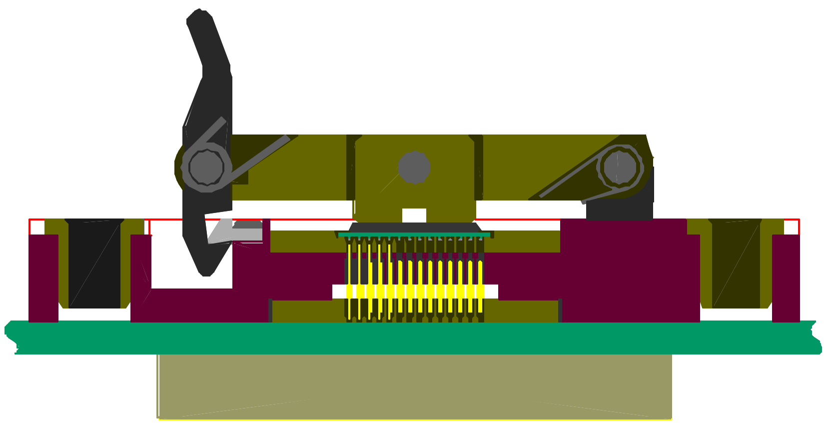
Selection process

- Defining operating conditions and restrictions
- PBGA device - socket interface considerations
- Socket lead - DUT board interface considerations
- Electrical parameters evaluation

Conclusion

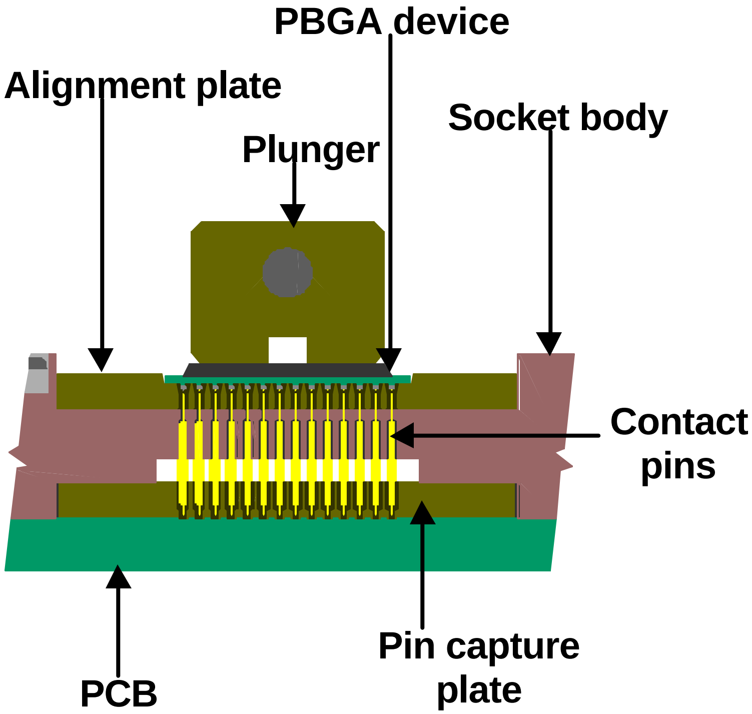
- Significance of device - socket match

Basic functions of test and burn-in sockets



- Device housing and alignment
- Electrical connection from DUT to device
- Heating / cooling of the device

Typical socket structure



- Body
- Contact capture plates
- Alignment plate
- Device clamping mechanism
- Thermal management components

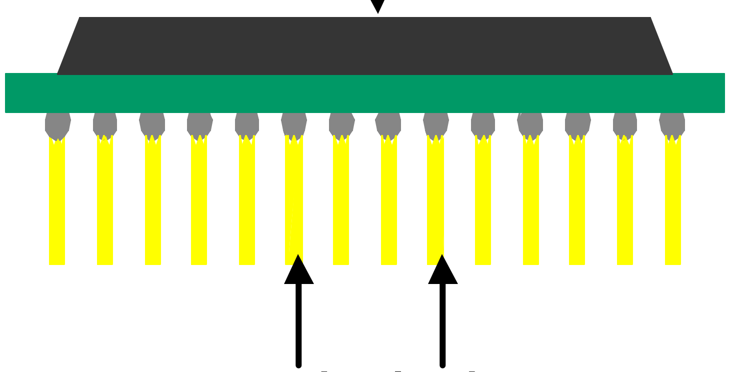
Defining operating conditions and restrictions

- Environment
  - Temperature, humidity, vibration, pressure
- Socket size restrictions
  - Number of sockets per board, height restrictions
- Handling
  - Auto / manual, actuation force, ease of automation

Defining operating conditions and restrictions

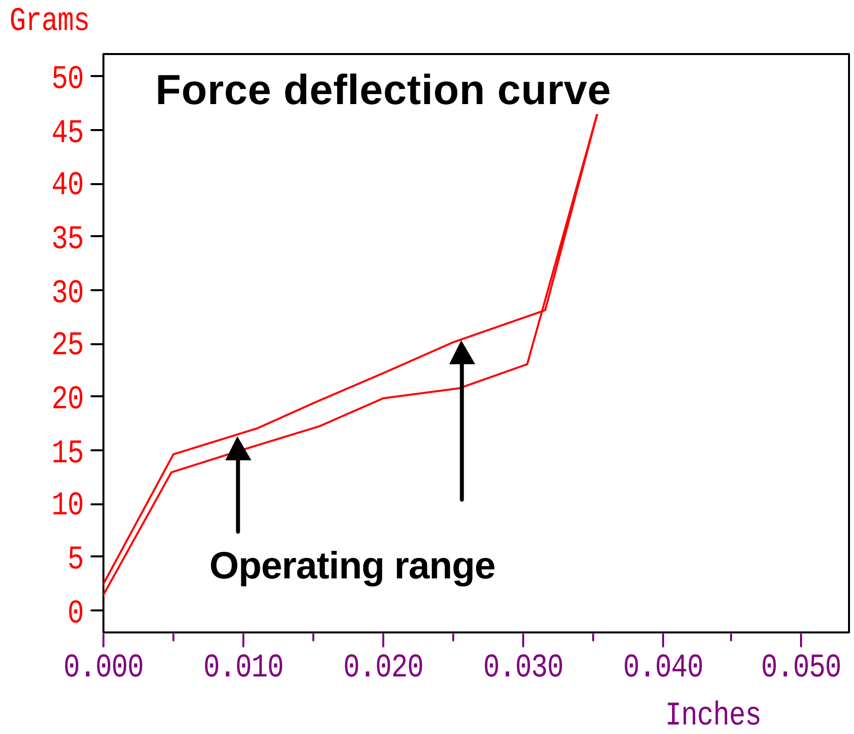
- Electrical requirements
  - Current, voltage, electrostatic discharge, test signals speed
- Socket life expectancy
  - Load / unload cycles, hours of burn-in, number of compressions
- IC device lead damage
  - Tolerable damage to package lead inflicted by socket contact

PBGA device – socket interface



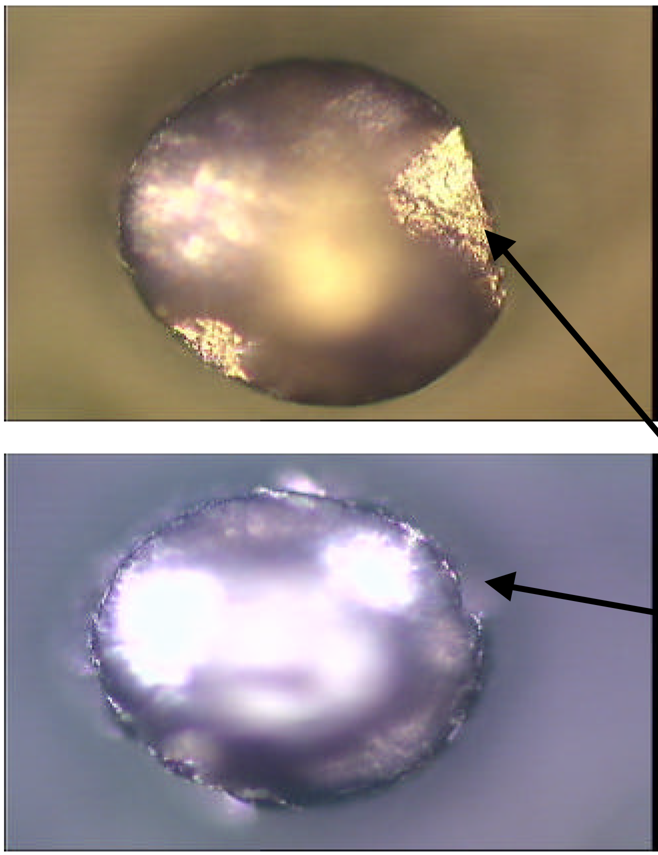
- Geometric compatibility
  - Solder sphere ⇔crown, cup, pinch
- Alignment
  - Utilize solder sphere to align product to socket contact

PBGA device – socket interface



- Contact force
  - Sufficient to penetrate metal oxides and maintain solid electrical connection
  - Depends on ; contact shape, base and surface materials, wiping action

PBGA device – socket interface

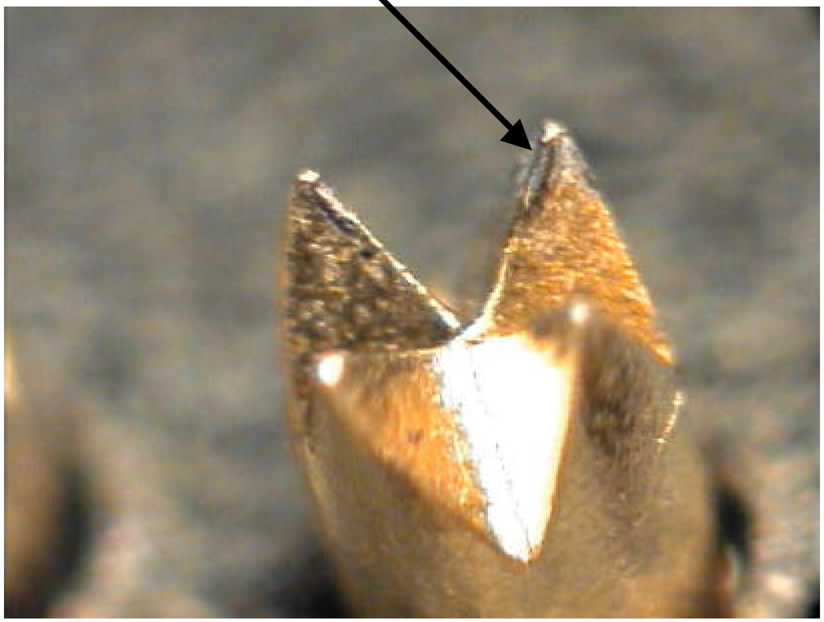


- Ball damage
  - **Usually generous amount of damage allowed if solder balls are reflow prior to further processing**

Ball damage area

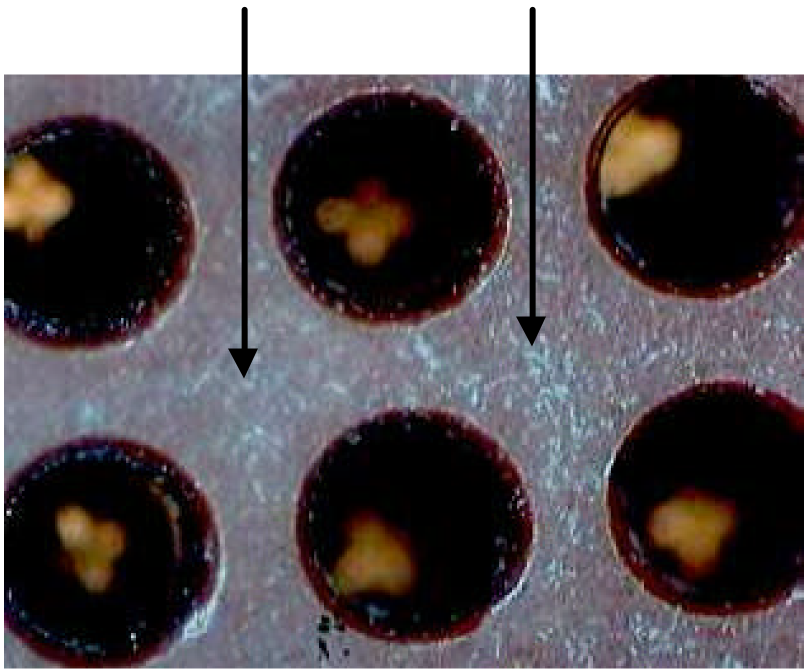
PBGA device – socket interface

Solder contamination



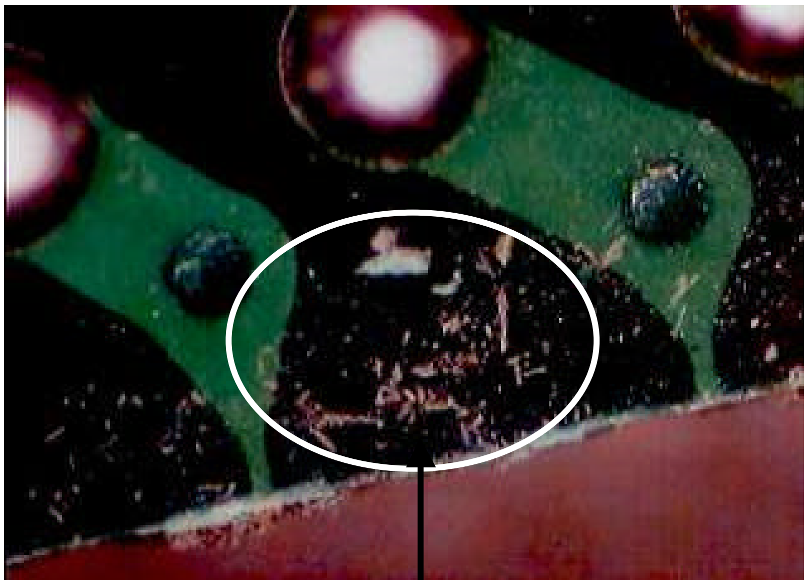
- Solder transfer onto socket leads
  - Wiping less effective
  - Higher contact resistance

PBGA device – socket interface



- Socket wear and maintenance considerations
  - Can contacts be cleaned easily and effectively
  - How often cleaning is need
  - Can single contact be replaced

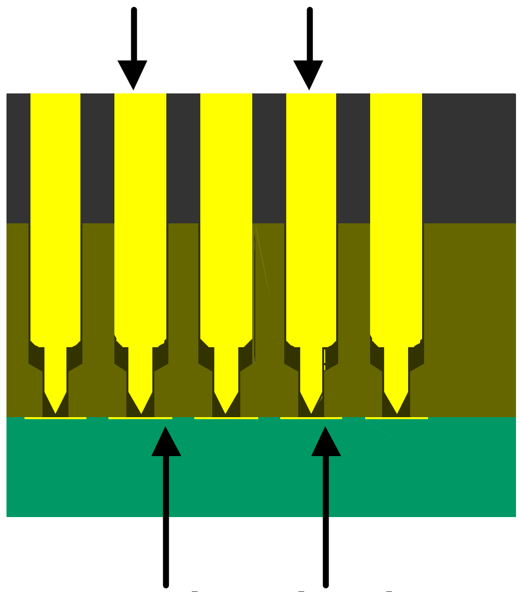
PBGA device – socket interface



Contamination from prior process

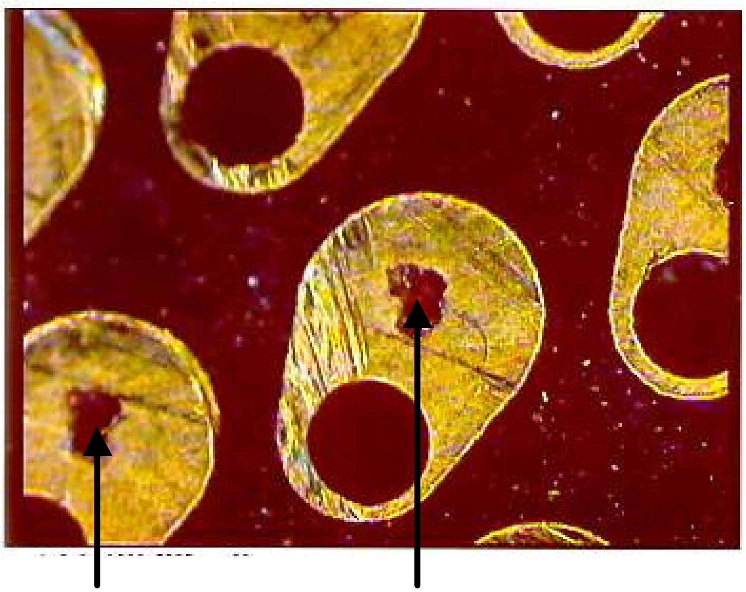
- Product contamination
  - From prior processing
  - From handling

Socket lead – DUT board pad interface



- Mounting
  - Surface mount
  - Pin-thru-hole (PTH) (soldered**)**
- Geometric compatibility
  - Board pad ⇔ spear, crown, dome, cup
  - PTH ⇔ solder tail length, diameter

Socket lead – DUT board interface



Pad damage from socket leads

- Board pad damage
  - Excessive wiping
  - Excessive force
  - Aggressive contact shape
  - Insufficient / inferior pad metallurgy

Electrical parameters

- Contact resistance
  - Contactor pin + device lead and pin connection + pin and DUT board connection
- Inductance
  - Single contactor pin from end to end
- Capacitance
  - Between two adjacent pins

Electrical parameters

- Impedance
  - Single pin over frequency range
- Attenuation
  - 1dB signal loss through contactor pin
- Propagation delay
  - Time delay through single contactor pin

Significance of device – socket match

- Product damage
- Yield loss
- Loss of production capacity
- Increased cost of ownership
  - Maintenance / pin replacement
  - Additional test / burn-in hardware

Significance of device – socket match

- Higher product cost
- Production / delivery delays
- Customer dissatisfaction
- Loss of business

Characterization of high performance contactors for production RDRAM chip-scale package test.

2000 Burn-in and Test Sockets Workshop

Francois Billaut
Hewlett Packard

Geary Chew
Hewlett Packard

Ken Karklin
Agilent Technologies

Agenda / Outline

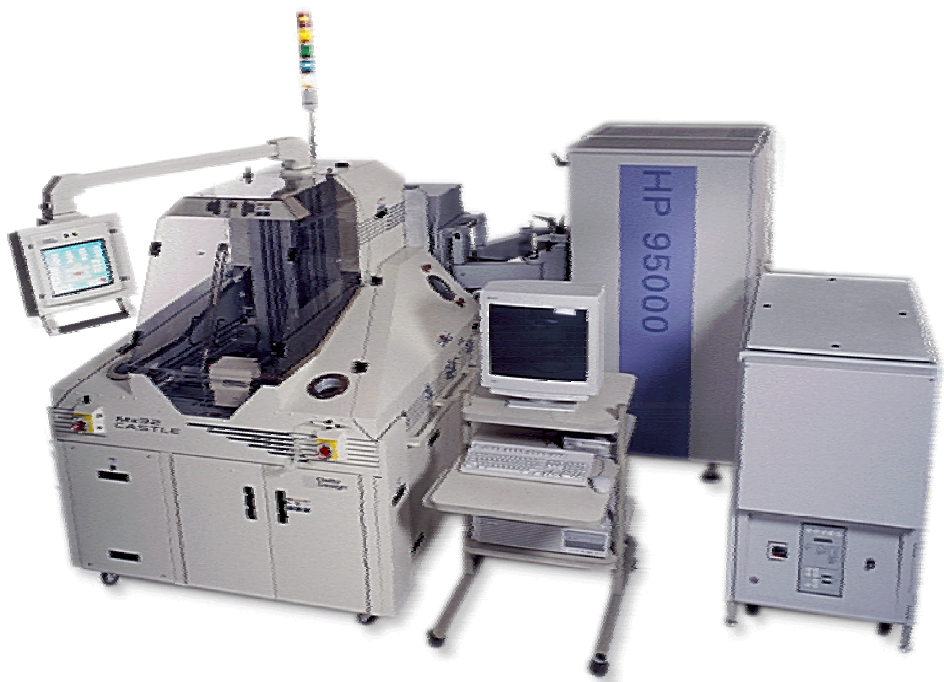
- Background of need driven by RDRAM
- Overall evaluation methodology
- High frequency evaluation
- Mechanical evaluation
- Impact to CSP assembly and reliability
- Applications testing
- Key Learnings
- Conclusions

New Requirements of High Speed Memory Final Test

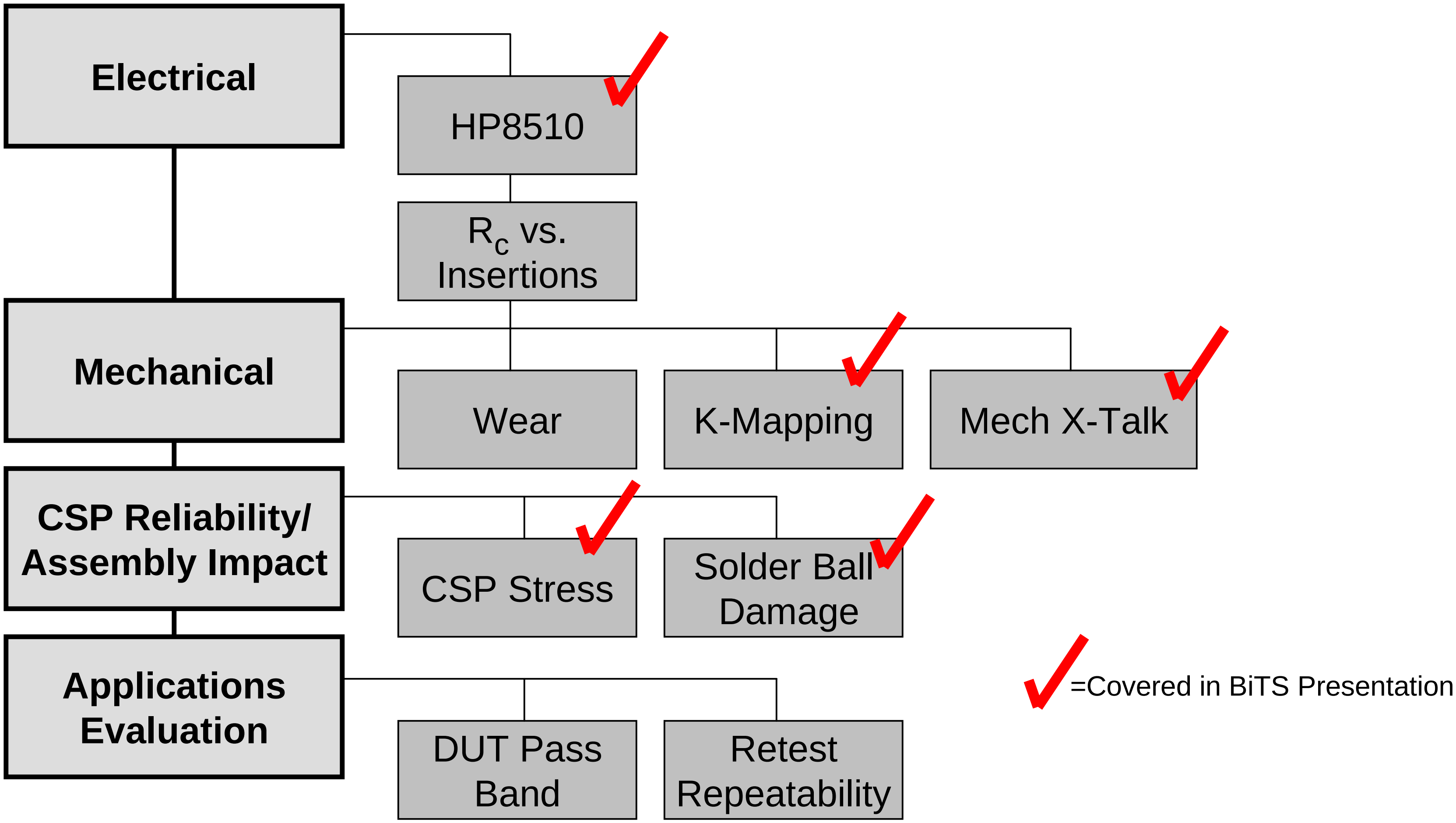
- Much Higher Data Rates
  - RDRAM data rates to1Gbs+
- New Package Technology
  - CSP
  - DRAM Mfg specific variations
- Support Lowest Cost of Test
  - Device Yield, Device Assembly
  - Overall Contact reliability
  - parallelism, contactor cost

Application Environment

- Rambus direct memories from all major DRAM manufacturers world wide
  - Multiple CSP variations
- Agilent 95000 High Speed Memory Series Tester
- Delta Castle Mx32 Handler
  - x16 and x32 DUTs
  - -30C to 120C

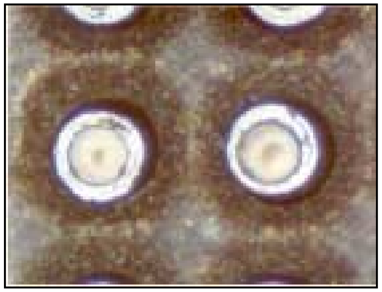


Highlights of Evaluation Methodology
(Technical Portions)



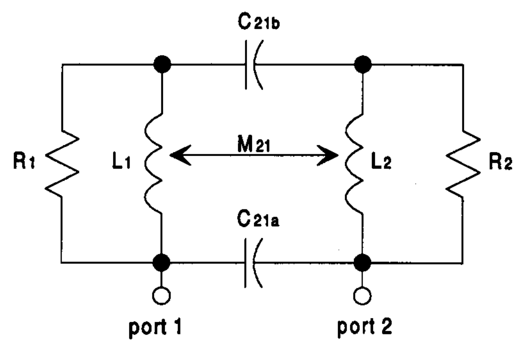
Contactors Evaluated

Contactor	Characteristics
Type I	- Technology: pogo pins with floating plate - Stiffness of contact pins: spring loaded pogo pins - Shape of top of pogo pin: crown (not axisymmetric) - Ball/pin type of contact: indentation
Type II	- Technology: S-shape pins floating in elastormer - Stiffness of contact pins: friction + elastomeric layer - Shape of top of contact: inclined plane - Ball/pin type of contact: 45 degree friction
Type III	- Technology: rigid contact pins with no floating plate - Stiffness of contact pins: SMM constrained - Shape of top of contact pin: tube (axisymmetric) - Ball/pin type of contact: indentation



RF Evaluation

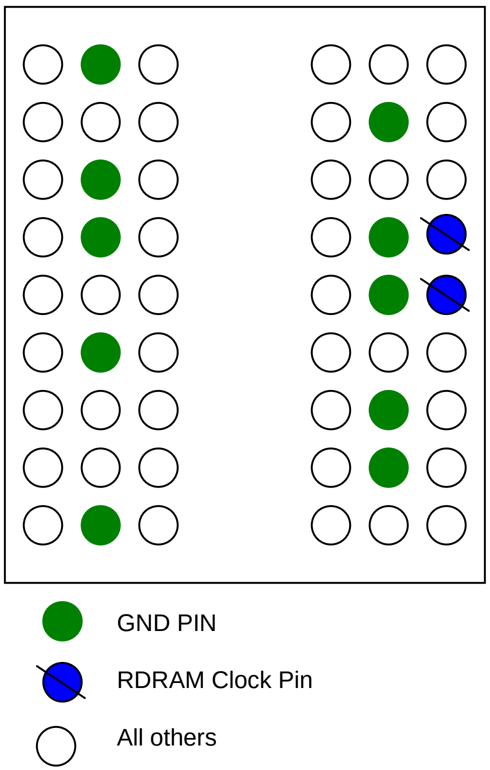
- HP 8510C: parameter measurement
- MDS simulation
  - First pass results:
    - All technologies >5GHz -3dB bandwidth (BW)
    - Basic circuit model developed for all technologies
  - First pass BW did not correlate with application results



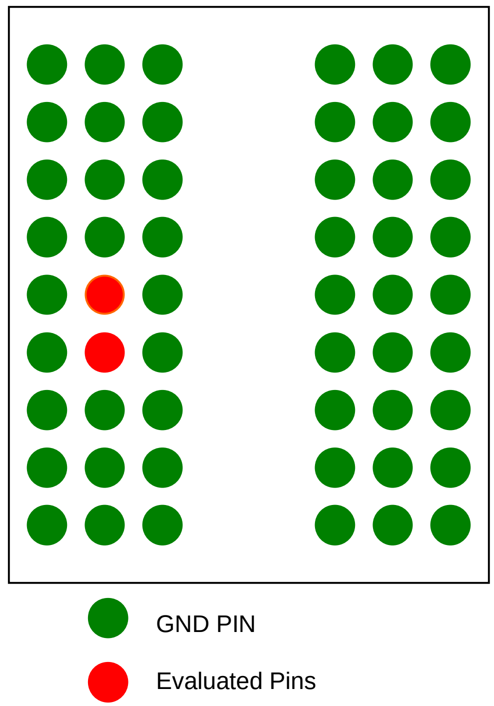
RDRAM Ball-out vs. surrogate DUT

(for bandwidth testing to -3dB)

Typical DRDRAM 144mb CB Pin Out



First Pass Surrogate DUT *effective* Pin out

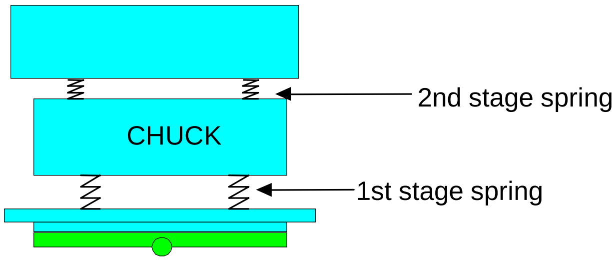


- Measurable difference in bandwidth depending on ground pin proximity and population

Mechanical Evaluation

- Simulation of mechanical environment:
  - Delta Castle Chuck
  - Thermal
- Critical Tools:
  - Instron
  - Custom Tooling

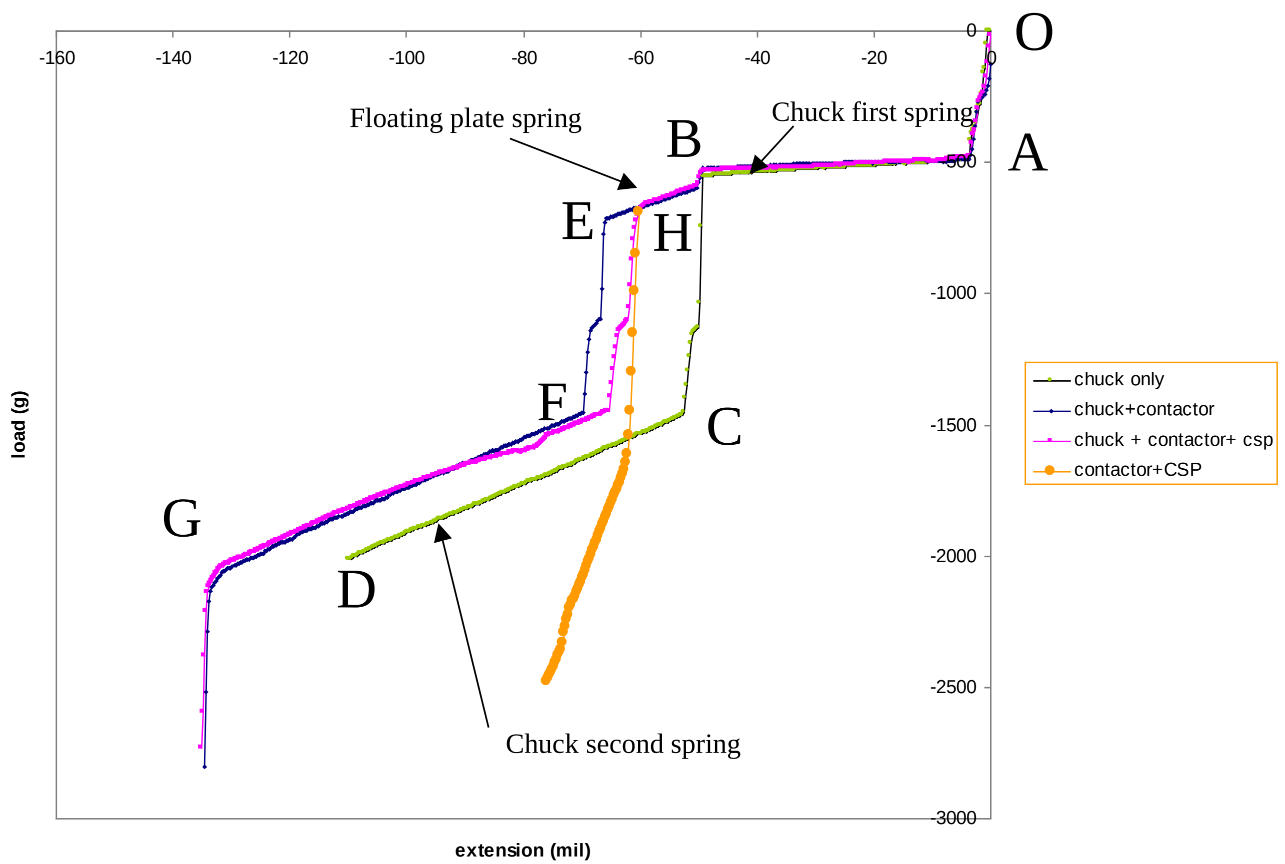
Delta Castle Mx 32 Chuck



Wear, K-Mapping, Mechanical X-Talk Test Setup

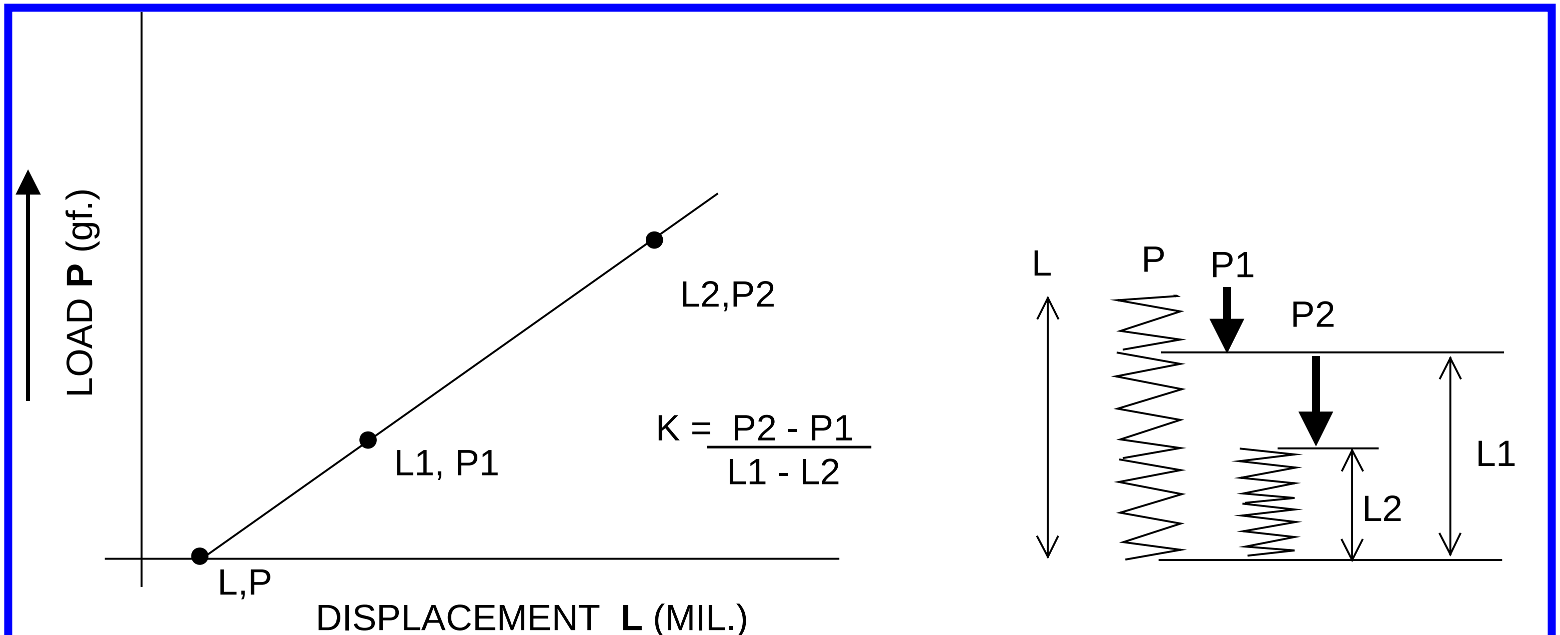
What a CSP sees: Load v. displacement

- Type I Contactors + Handler Chuck



K-Mapping: Understanding the Load on individual Balls

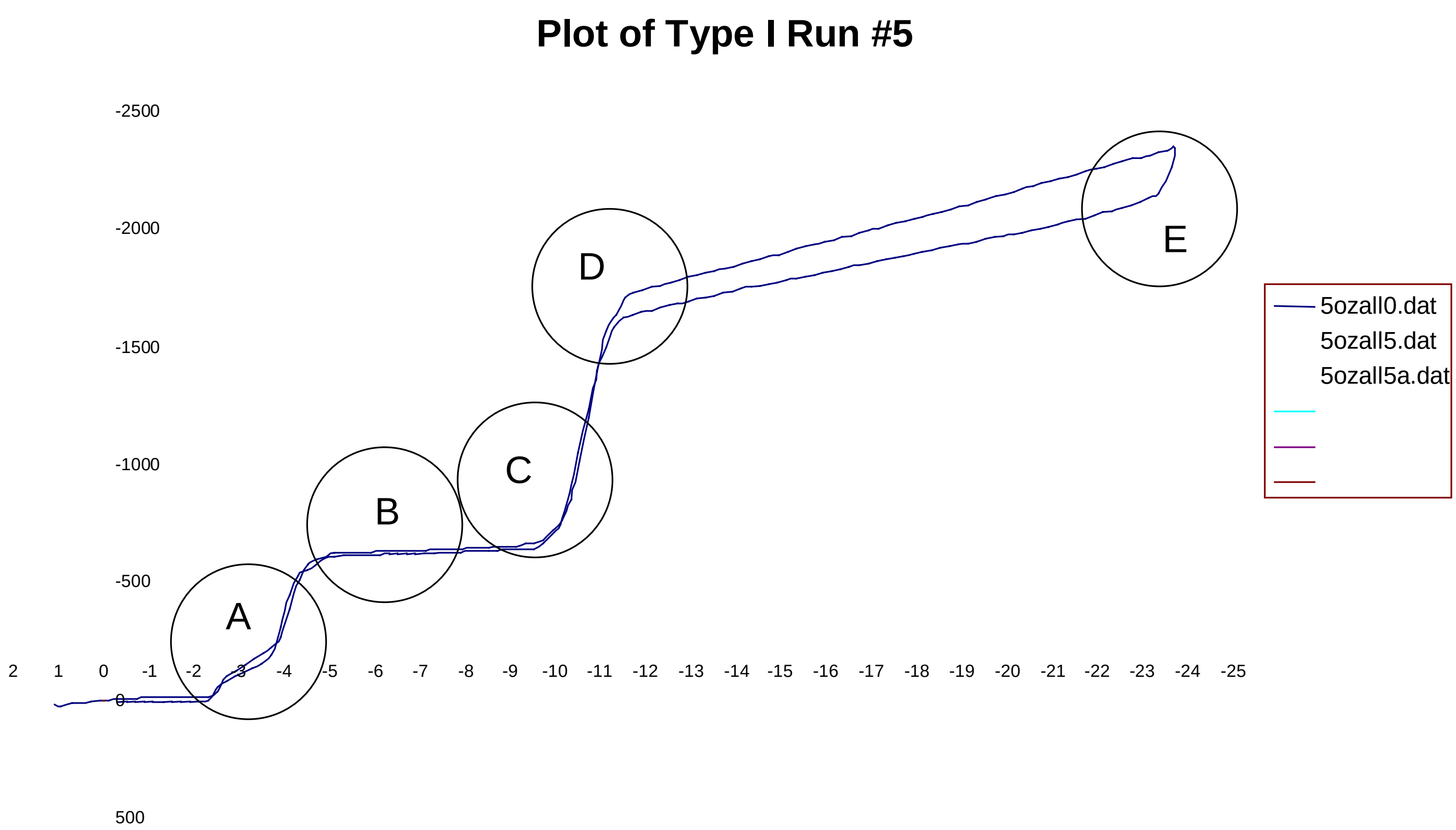
- Instron + Contactor + Surrogate DUT



Spring length: long ---------------------------short (compressed)

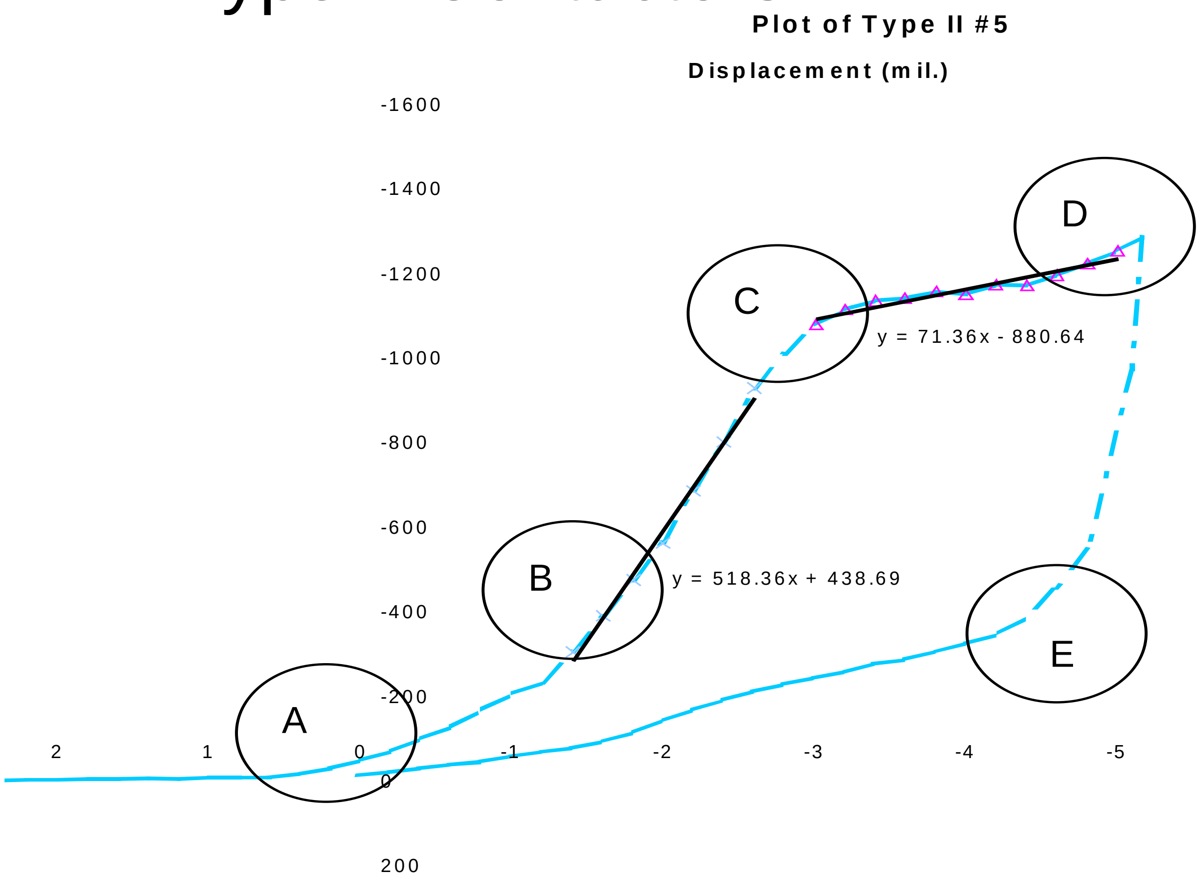
K-mapping Results

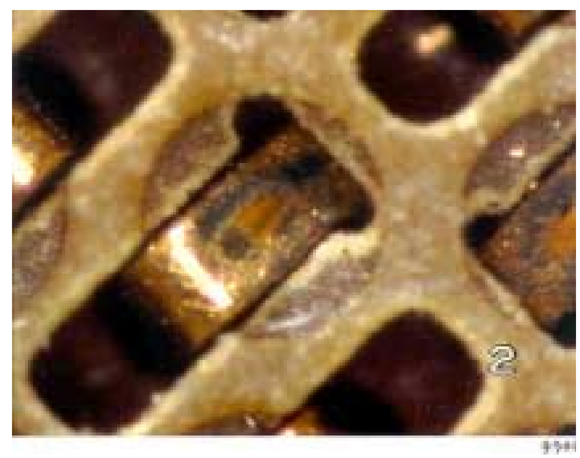
- Type I Contactors



K-mapping Results (Continued)

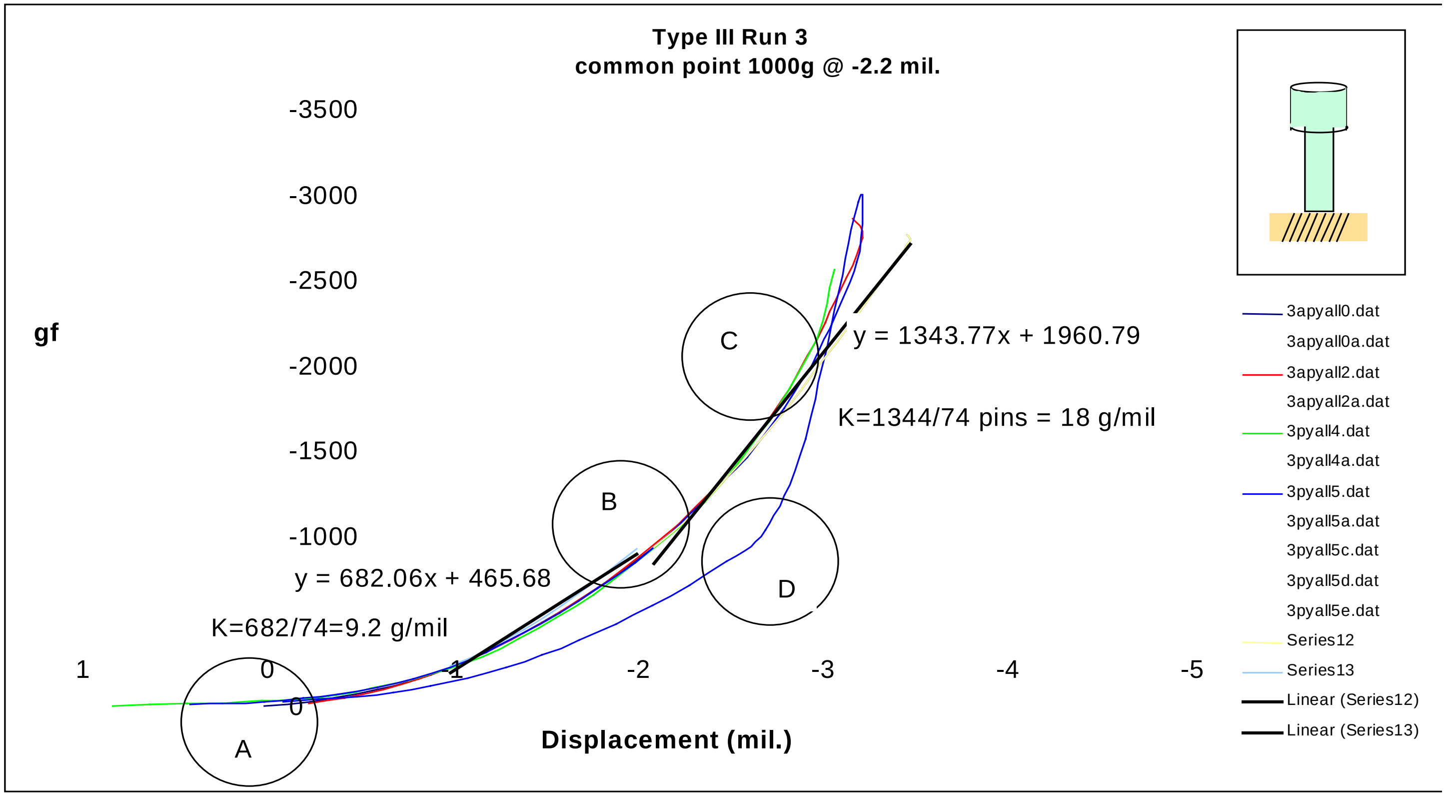
- Type II Contactors





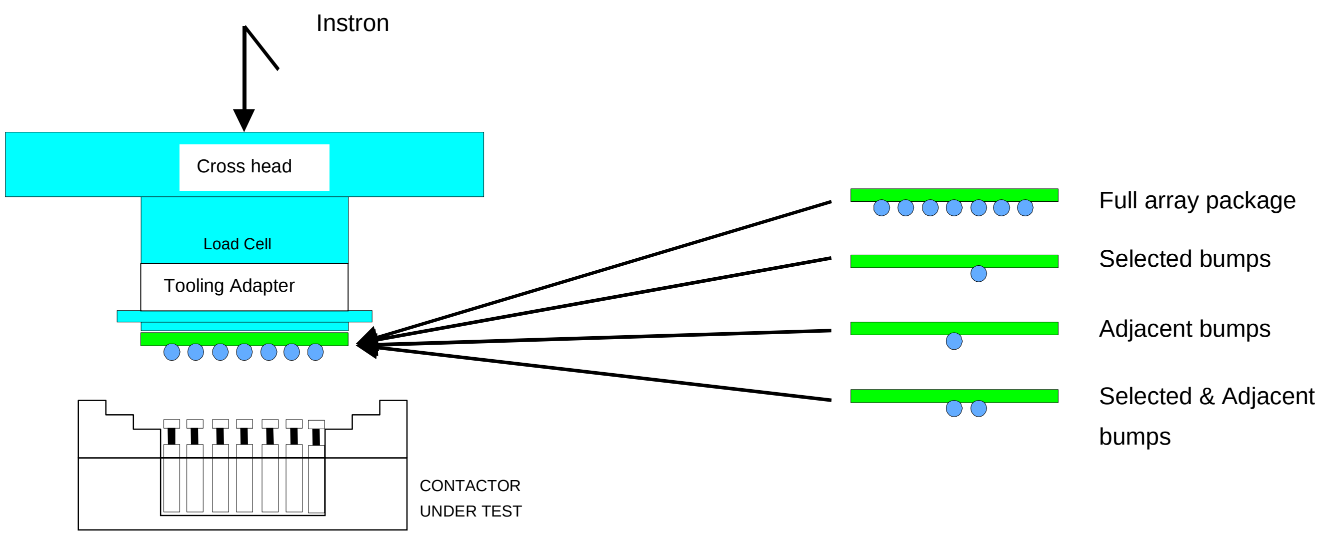
K-mapping Results (Continued)

- Type III Contactors



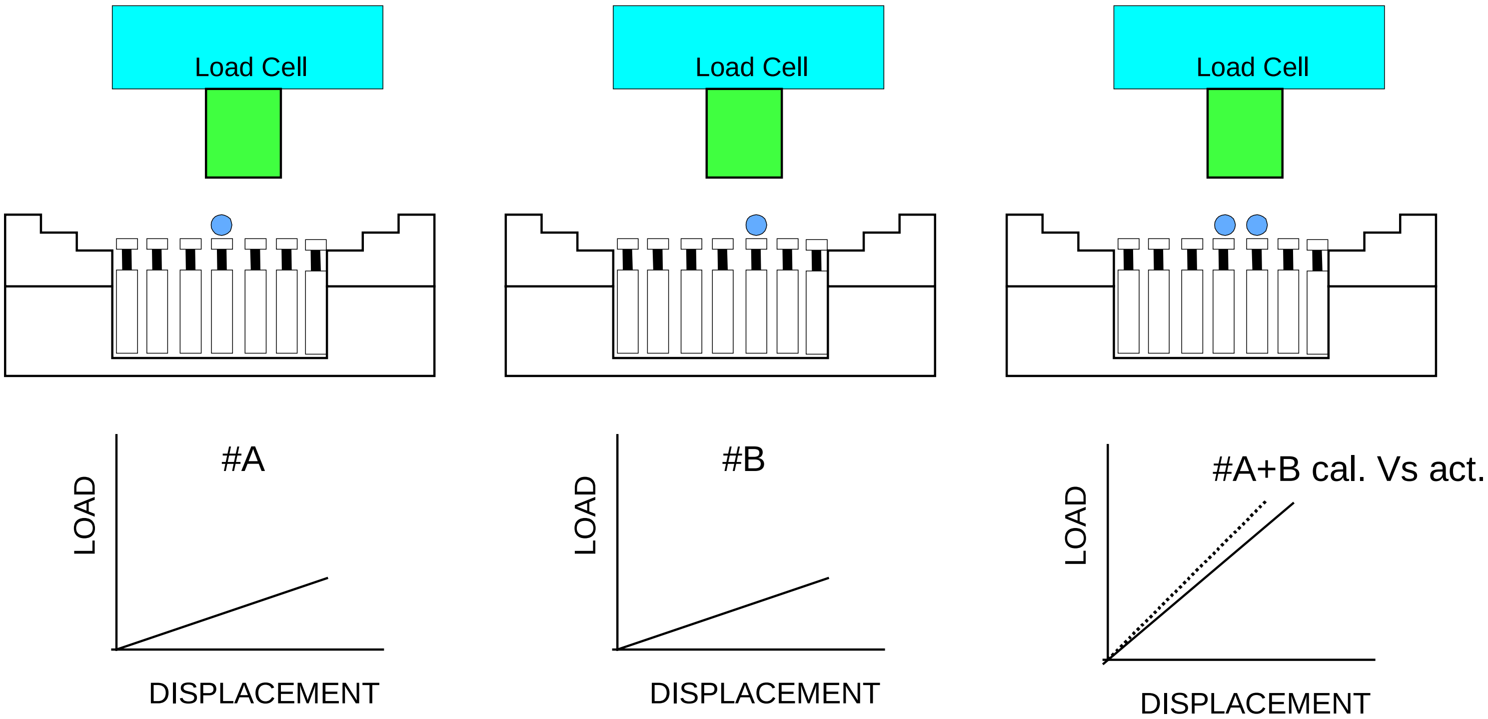
Mechanical X-Talk

- Determine movement of contact based on depression of adjacent contact
  - Metric of sensitivity to ball size/placement variation
  - Data is first step towards interconnect Cpk Model

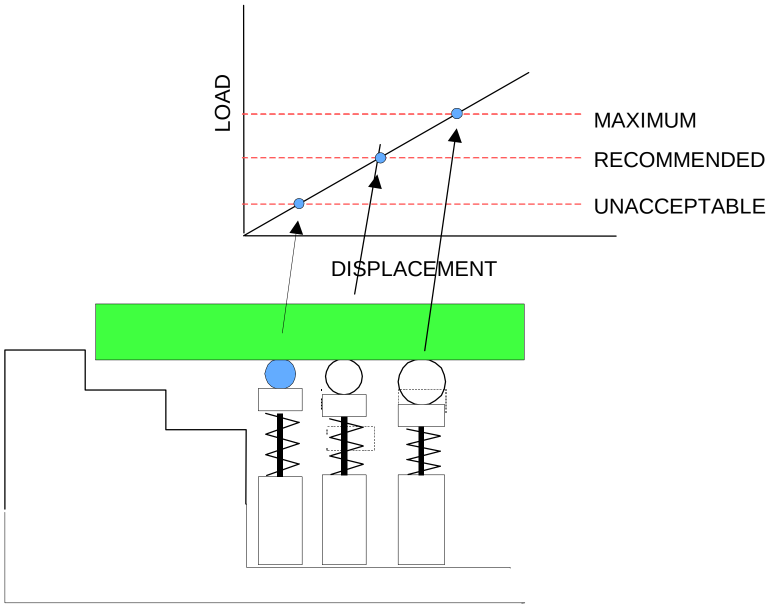


Mechanical X-Talk

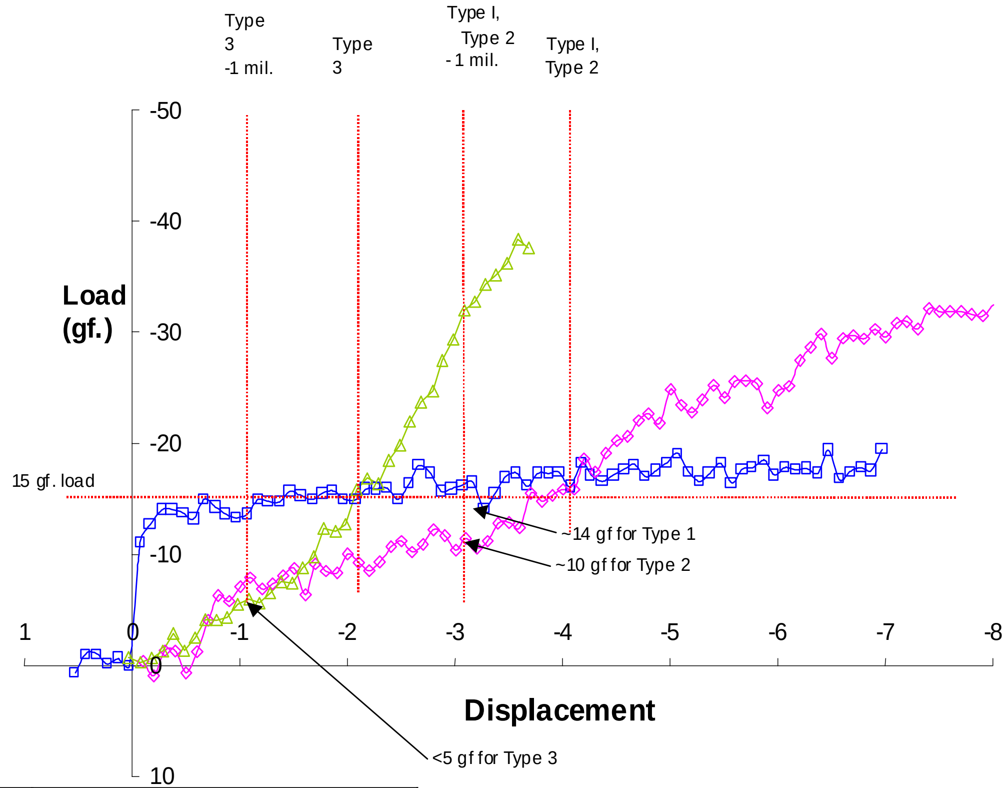
- Basic Methodology



Mechanical X-Talk -- Results



Comparing Type I, II, III

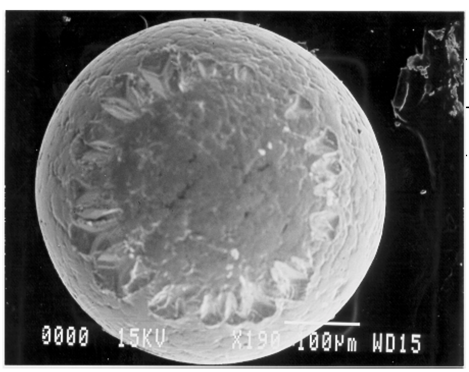


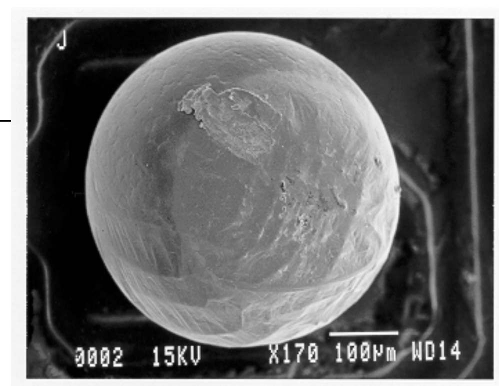
Contactor	Relative Mech X Talk Results
Type I	Linear
Type II	Some
Type III	Most

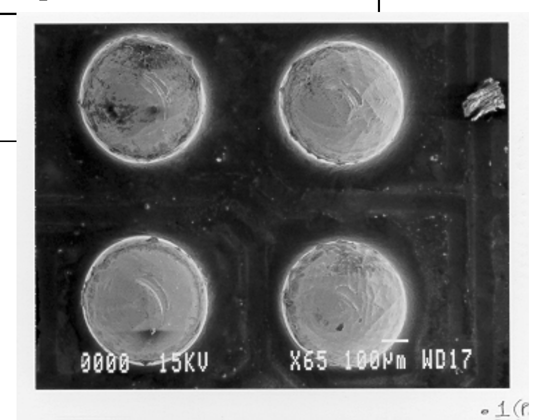
Solder Ball Damage

- Methodology:
  - Start w/ re-flowed part, weigh the part
  - Multiple (10) Insertions @ 90C
  - Weigh the part + SEM observations

Contactor	Mark on the solder ball	Location
Type I	4 triangular indentations	Between the side and the top
Type II	Flat Scrub	On the side
Type III	Portion of circle	Sometimes at the top of the ball

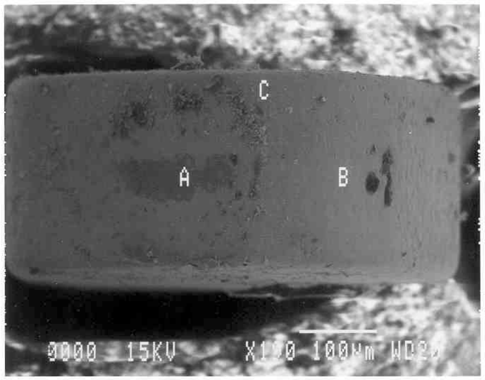






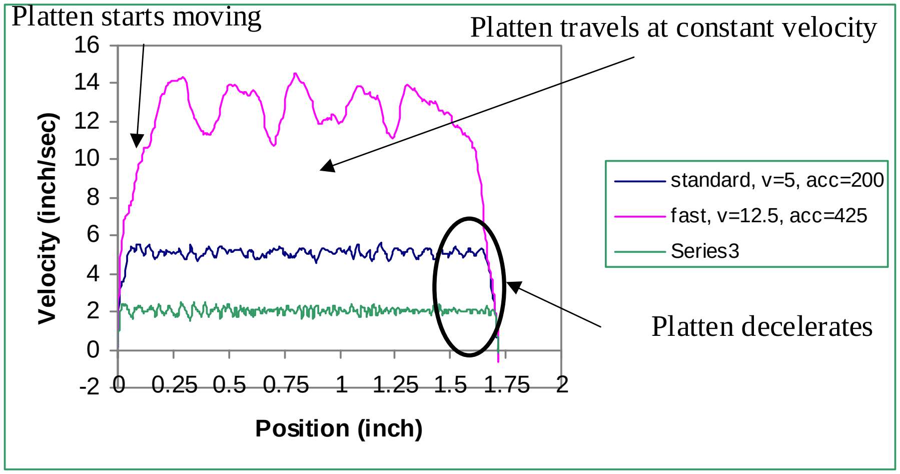
Solder Ball Damage (continued)

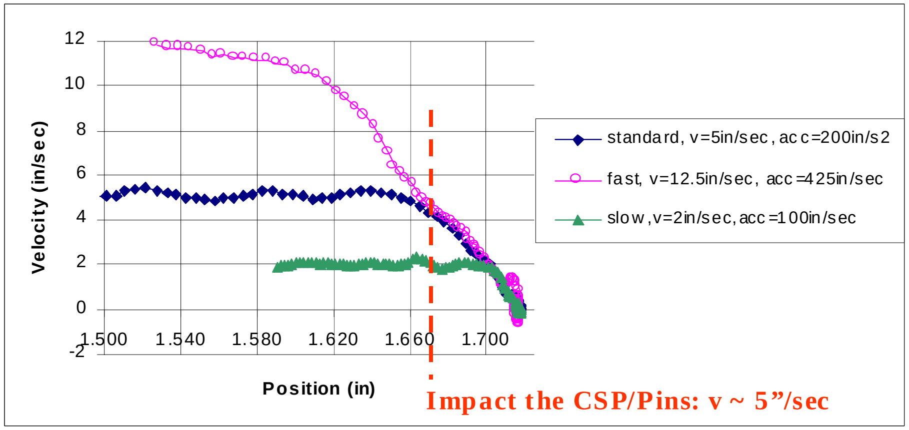
- Ball Damage Conclusions Results :
  - Missing Solder had quantity had to be estimated / calculated geometrically from SEM results
    - In all cases, <1% solder loss after 10 insertions
  - NO impact to CSP assembly -- from ANY technology
    - Marks in “no damage zone” inconsequential
  - Cosmetic/placement differences in marks
  - After 10 insertions, only Type II contactor had measurable quantities of solder



CSP Reliability Impact

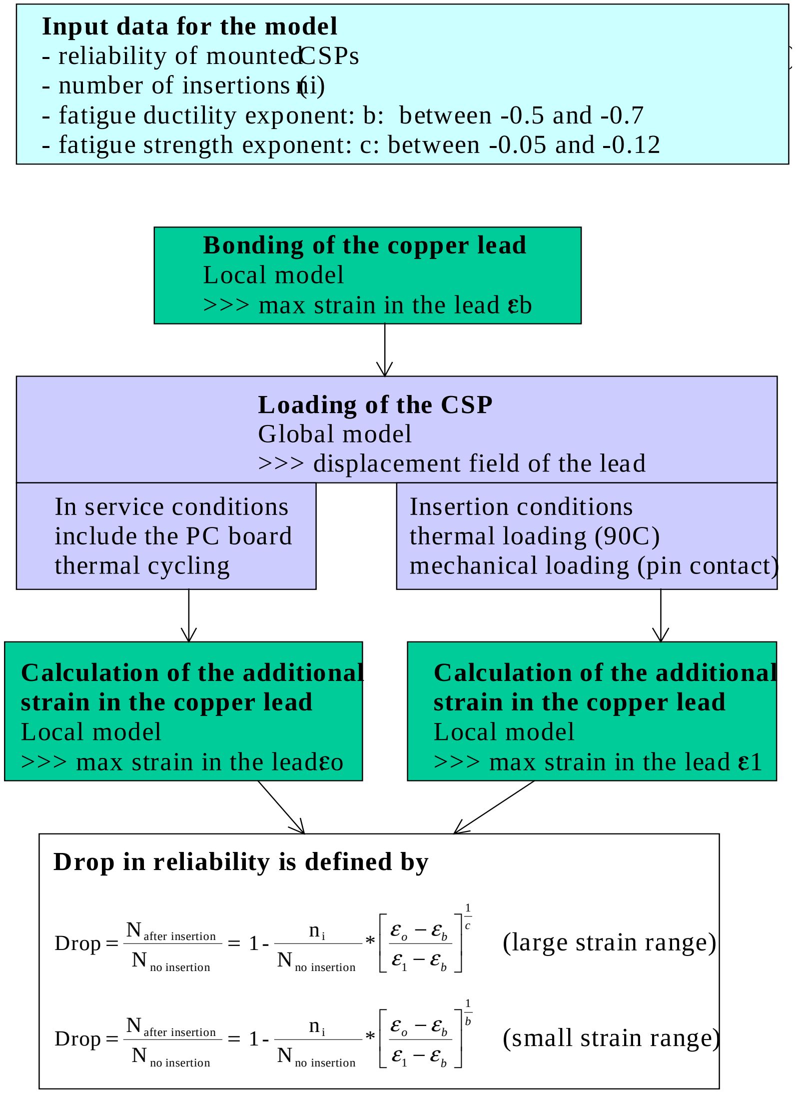
- Concern:
  - Depending on the spring characteristics of the contactor, there may be an impact to the long term lifetime of the CSP device due to the stress impact of test insertions





CSP Reliability Impact (continued)

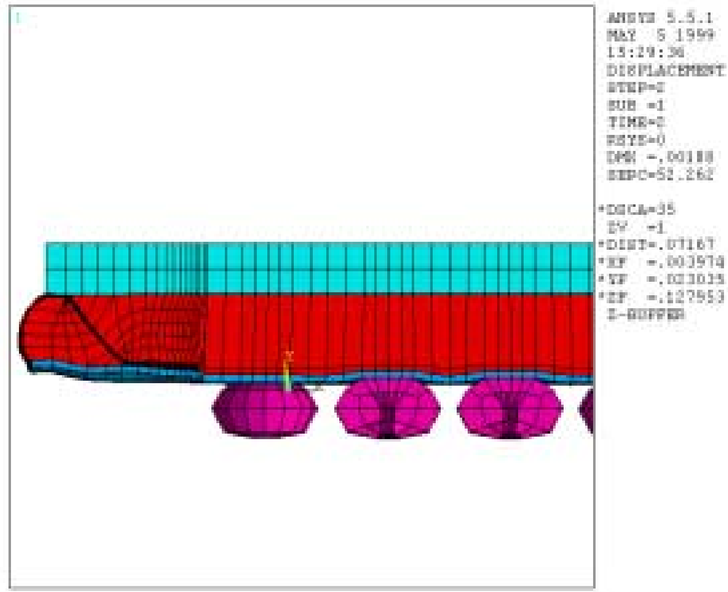
- Methodology:
  - FEA
  - Determine difference in in-service conditions vs. insertion conditions
  - Tessera CSP type modeled (though there were variations in customer applications
  - Entire CSP considered, focus on strain of copper lead



CSP Reliability Impact (continued)

FEA Local Model
Principal Stress I
Cu Lead:
Tessera Type CSP
Thermal Load + Insertion Load

Deformed Shape, Global Model,
Themal & Mechanical Loads.
Note Local deformation above
bumps due to loading



CSP Reliability Impact (continued)

- Critical Assumptions
  - Failure mode is in the copper lead
  - Coffin-Mason approach, relating plastic strain range to the fatigue life of the part
  - Add to this: Modeled insertion strain
- Conclusions:
  - 18% strain level during insertion
  - 18.1% strain level during in-service conditions
  - None of the technologies are detrimental to fatigue life of the part

Significant Learnings and Conclusions

- Bandwidth test setup should simulate application
- K-mapping instructive on loads on CSP vs. Contactor Technology in application environment
- Mechanical X-talk potentially a significant contributor to false failures due to opens
  - Applies where high ball diameter variation is significant
- Solder ball damage:
  - What's your *real* requirement for assembly?
- CSP reliability:
  - Insertion less traumatic than typical thermal cycle
- Mechanical Capability:
  - CSP contacting capable across multiple Contactor technologies

Acknowledgements

Steve Chaikin, Agilent Technologies, California Semiconductor Test Division, Santa Clara, California

Jian Miremadi, Hewlett Packard Company, Product Generations Solutions Technology Center, Palo Alto, California

Cecil Dowdy, Agilent Technologies, EPS Timing Division, Santa Clara, California

Judy Glazer, Hewlett Packard Company, Product Generations Solutions Technology Center, Palo Alto, California

Rob Lawson, Hewlett Packard Company, Product Generations Solutions Technology Center, Palo Alto, California

Jeff Davis, Agilent Technologies, California Semiconductor Test Division, Santa Clara, California